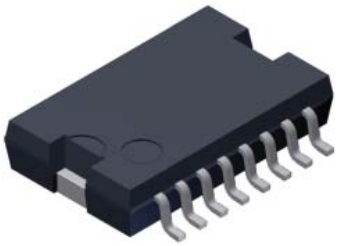
Full Bridge DC Motor Driver

Features and Benefits

- Supply voltage, V_{BB}, 36 V maximum
- Maximum DC current 3 A continuous, 6 A pulsed (1 kHz, duty cycle < 1%, pulse width < 10 µs)
- $R_{DS(on)}$ = 300 mΩ maximum, at T_J = 125ºC
- Operation modes: forward, reverse, brake (high- or low-side freewheeling current circulation)
- Output disable pin (DI pin)
- Protections:
  - Overvoltage protection (OVP), 36 V minimum
  - Overcurrent protection (OCP), 3 A typical
  - Overcurrent limitation (OCL), 6 A typical
  - Externally adjustable delay timer to halt OCL
  - Thermal shutdown protection (TSD), 151°C minimum
  - Undervoltage lockout on V_{BB} (UVLO), 4.2 V minimum
  - Open load detection at startup
- Diagnosis output linked to OVP, OCP, TSD, UVLO, and open load detection, at startup and in operation

Package: 16 pin HSOP with exposed thermal pad and tabs



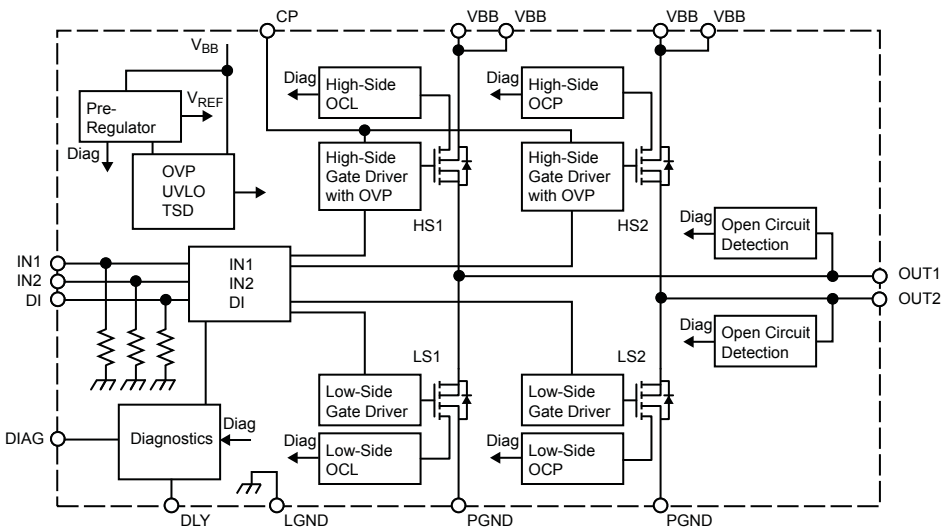
Not to scale

Description

The SPF7302 is a fully protected, single chip full-bridge driver IC for DC brush motor applications. The various protection circuits integrated are: overvoltage protection (OVP); overcurrent protection (OCP) with latch, which is adapted to the DMOSFETs in each full bridge; undervoltage lockout (UVLO); open load detection; and overcurrent limitation.

The package is a thermally enhanced 16-pin HSOP power package with an exposed thermal pad on the bottom side of the package.

Functional Block Diagram



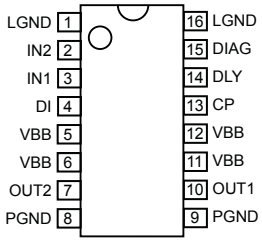
Selection Guide

Part Number	Package	Packing
SPF7302	Thermally enhanced surface mount (HSOP), 16-pin	Minimum quantity 1400 pieces

Absolute Maximum Ratings at T_A = 25°C

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		–0.3 to 36	V
IN1, IN2, DI, and DLY Pin Input Voltage	V_x		–0.3 to 6	V
Output Current	I_O		±3	A
	I_{Opeak}	Continuous: 1 kHz, duty cycle <1%; pulse: < 10 µs	±6	A
DIAG Pin Output Voltage	V_{DIAG}		–0.3 to 6	V
DIAG Pin Input Current	I_{DIAG}	DIAG pin sink current	–2	mA
CP Pin Voltage	V_{CP}		–0.3 to 36	V
Power Dissipation	P_{D1}	With infinite heatsink	39	W
	P_{D2}	Mounted on glass epoxy PCB, 50 mm × 74 mm × 1.6 mm; 0.5 oz copper (18 µm thick) exposed copper area	4	W
Junction Temperature	T_J		–40 to 150	ºC
Operating Ambient Temperature	T_A		–40 to 105	ºC
Storage Temperature	T_{stg}		40 to 150	ºC
Thermal Resistance, Junction to Case	$R_{\theta JC}$	Mounted on glass epoxy PCB, 50 mm × 74 mm × 1.6 mm; 0.5 oz copper (18 µm thick) exposed copper area	3.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$		31	°C/W

Pin-out Diagram



Terminal List Table

Number	Name	Description
1	LGND	Logic GND
2	IN2	Input pin 2
3	IN1	Input pin 1
4	DI	Disable pin
5	VBB	Supply input voltage
6	VBB	Supply input voltage
7	OUT2	Output 2
8	PGND	Power GND
9	PGND	Power GND
10	OUT1	Output 1
11	VBB	Supply input voltage
12	VBB	Supply input voltage
13	CP	Charge pump capacitor pin
14	DLY	Overcurrent limitation delay setting input pin
15	DIAG	Diagnostics output pin
16	LGND	Logic GND

All performance characteristics given are typical values for circuit or system baseline design only and are at the nominal operating voltage and an ambient temperature, T_A, of 25°C, unless otherwise stated.

ELECTRICAL CHARACTERISTICS[1] valid at T_J = –30°C to 125°C, V_{BB} = 14 V, V_{DI} = 5 V, C_{CP} = 47 nF, R_{DIAG} = 5.1 kΩ, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{BB}		6	–	18	V
OUTx Pin Leakage Current	I_{leakHS}		–1	–	–	mA
	I_{leakLS}		–	–	1	mA
DMOSFET On Resistance	$R_{DS(ON\_1H}$	I_{OUT} = 1 A	–	–	300	mΩ
	$R_{DS(ON)\_2H}$	I_{OUT} = 3 A	–	–	300	mΩ
	$R_{DS(ON)\_1L}$	I_{OUT} = 1 A	–	–	300	mΩ
	$R_{DS(ON)\_2L}$	I_{OUT} = 3 A	–	–	300	mΩ
DMOSFET Body Diode Forward Voltage	V_{F_H1}	I_{OUT1} = 1 A	–	1.0	2.0	V
	V_{F_H2}	I_{OUT2} = 1 A	–	1.0	2.0	V
	V_{F_L1}	I_{OUT1} = –1 A	–	1.0	2.0	V
	V_{F_L2}	I_{OUT2} = –1 A	–	1.0	2.0	V
Quiescent Current	I_{BB}		–	7	–	mA
Overcurrent Limit (OCL)	I_{OCL_H1}	T_J = –40°C to 150°C, $I_{OCL} < I_{OCP}$; guaranteed by design	2.0	3.0	4.5	A
	I_{OCL_H2}		2.0	3.0	4.5	A
	I_{OCL_L1}		2.0	3.0	4.5	A
	I_{OCL_L2}		2.0	3.0	4.5	A
Overcurrent Protection (OCP)	I_{OCP_H1}	T_J = –40°C to 150°C, $I_{OCL} < I_{OCP}$; guaranteed by design	4.5	6.0	8.0	A
	I_{OCP_H2}		4.5	6.0	8.0	A
	I_{OCP_L1}		4.5	6.0	8.0	A
	I_{OCP_L2}		4.5	6.0	8.0	A
IN1, IN2, DI, and DLY Pin Input Voltage	V_{x_H}		3.0	–	5.3	V
	V_{x_L}		–0.3	–	1.5	V
IN1, IN2, DI, and DLY Pin Input Current	I_{x_H}	V_{DLY} = 5 V	–	100	200	µA
	I_{x_L}	V_{DLY} = 0 V	–1	–	1	µA
DIAG Pin Output Voltage	V_{DIAG_H}	V_{CC} = 5 V	4.0	–	–	V
	V_{DIAG_L}	I_{sink} = 2 mA	–	–	0.4	V
DIAG Pin Output Current	I_{DIAG_H}	V_{CC} = 5 V, DIAG pin source current	–250	–	–	µA
	I_{DIAG_L}	V_{CC} = 5 V, DIAG pin sink current, V_{DIAG} = 2 V	–	–	3	mA
IN1 and IN2 Pin Input Propagation Time	t_{INx_ON}	Delay from V_{INx} = 2 V→V_{OUTx} × 0.2	–	7	15	µs
	t_{INx_OFF}	Delay from V_{INx} = 1.5 V→V_{OUTx} × 0.8	–	7	15	µs
Output Rise Time	t_{rx}	Delay from V_{OUTx} = 20%→80% points, at I_{OUTx} = 1 A	–	0.5	2	µs
Output Fall Time	t_{fx}	Delay from V_{OUTx} = 20%→80% points, at I_{OUTx} = 1 A	–	0.5	2	µs

Continued on the next page…

ELECTRICAL CHARACTERISTICS[1] (continued) valid at T_J = –30°C to 125°C, V_{BB} = 14 V, V_{DI} = 5 V, C_{CP} = 47 nF, R_{DIAG} = 5.1 kΩ, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DLY Pin Threshold Voltage	$V_{DLY(th)}$	Overcurrent limitation (OCL) activating voltage	1.4	1.6	1.8	V
DLY Pin Sourcing Current[2]	I_{DLY}		15	30	60	µA
UVLO Releasing Voltage	V_{UVLO_OFF}		–	–	5.2	V
UVLO Activating Voltage	V_{UVLO_ON}		4.2	–	–	V
UVLO Hysteresis	$V_{UVLOhys}$		–	0.2	–	V
OVP Protection Activating Voltage	V_{OVP_ON}		36	–	42	V
OVP Protection Releasing Voltage	V_{OVP_OFF}		32	–	38	V
OVP Hysteresis	V_{OVPhys}		–	5	–	V
Thermal Shutdown Activating Temperature[3]	T_{TSD_ON}	Starts at 165°C typical; guaranteed by design	151	165	–	ºC
Thermal Shutdown Releasing Temperature[3]	T_{TSD_OFF}	Guaranteed by design	136	150	–	ºC
Thermal Shutdown Hysteresis[3]	T_{TSDhys}	Guaranteed by design	–	15	–	ºC

[1]The parameters at T_J = –40ºC to 150ºC are specified by design. The actual production tests are done at 25ºC and 125ºC.
[2]The individual overcurrent limitation of each DMOSFET is masked during the delay period. Therefore, ensure proper thermal design for dissipating transient temperature increase caused by current during this period.
[3]TSD (thermal shutdown protection starts at 165ºC typical, and it is specified by design.

Motor Control Truth Table[1]

Reference Number	Status	Input			Output			DMOSFET status			
		DI	IN1	IN2	OUT1	OUT2	DIAG	HS1	LS1	HS2	LS2
1	Forward rotation[2]	H	H	L	H	L	H	ON	OFF	OFF	ON
2	Reverse rotation[2]	H	L	H	L	H	H	OFF	ON	ON	OFF
3	Low-side freewheeling	H	L	L	L	L	H	OFF	ON	OFF	ON
4	High-side freewheeling	H	H	H	H	H	H	ON	OFF	ON	OFF
5	Output disabled	L	X	X	Z	Z	H	OFF	OFF	OFF	OFF
6	Overcurrent limitation (OCL) active (HS1)	H	H	X	H	X	H	ON	OFF	X	X
7	Overcurrent limitation (OCL) active (HS2)	H	X	H	X	H	H	X	X	ON	OFF
8	Overcurrent limitation (OCL) active (LS1)	H	L	X	L	X	H	OFF	ON	X	X
9	Overcurrent limitation (OCL) active (LS2)	H	X	L	X	L	H	X	X	OFF	ON
10	Overcurrent protection with latch (OCP) active (HS1)	H	H	X	Z	Z	L	OFF	OFF	OFF	OFF
11	Overcurrent protection with latch (OCP) active (HS2)	H	X	H	Z	Z	L	OFF	OFF	OFF	OFF
12	Overcurrent protection with latch (OCP) active (LS1)	H	L	X	Z	Z	L	OFF	OFF	OFF	OFF
13	Overcurrent protection with latch (OCP) active (LS2)	H	X	L	Z	Z	L	OFF	OFF	OFF	OFF
14	Undervoltage lockout (UVLO) protection active	X	X	X	Z	Z	L	OFF	OFF	OFF	OFF
15	Overvoltage protection (OVP) active	X	X	X	X	X	L	X	X	X	X
16	Open load detected at startup	L	X	X	X	X	L	OFF	OFF	OFF	OFF
17	Open load detected in operation	H	X	X	X	X	L	X	X	X	X
18	Thermal shutdown protection (TSD) active	X	X	X	Z	Z	L	OFF	OFF	OFF	OFF

[1]X is "don't care," Z is high impedance.
[2]"Forward" and "reverse" only indicate opposite relative direction.

Switching Operation Timing Charts

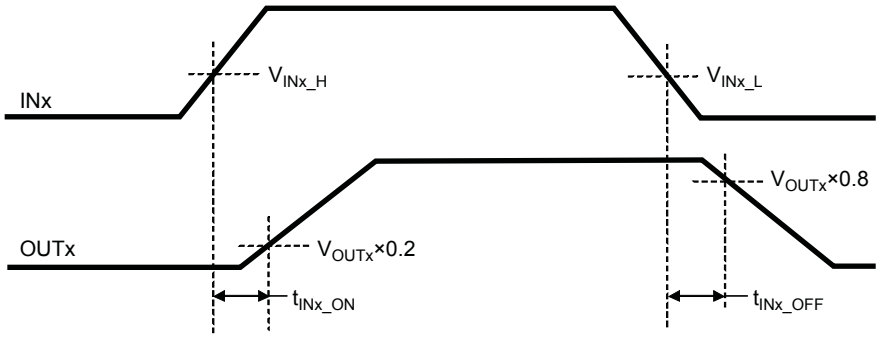


Figure 1. Output Delay Time

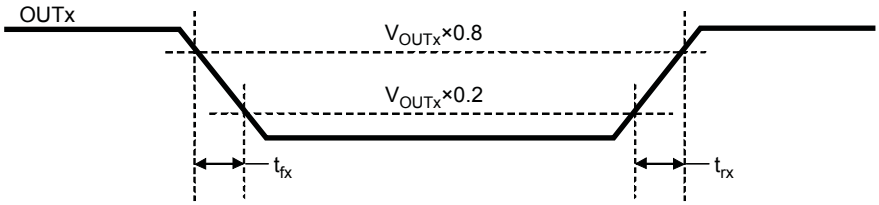
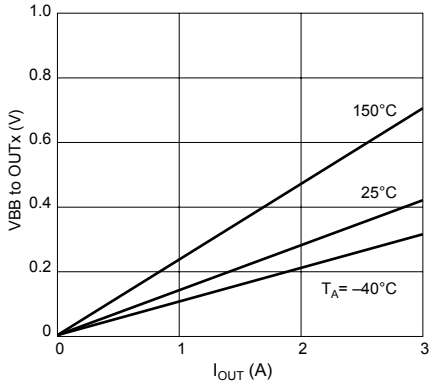


Figure 2. Output Switching Time

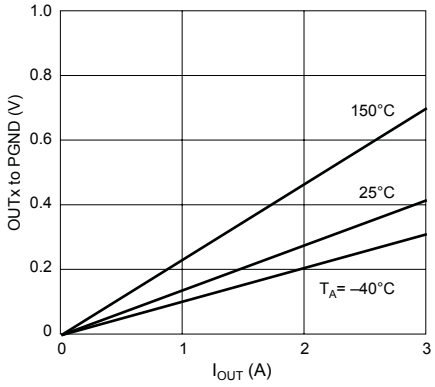
Characteristic Performance

T_A = 25°C unless otherwise specified

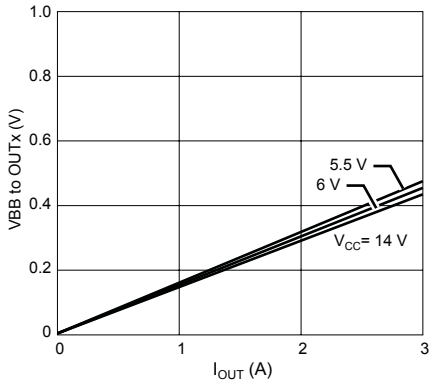
High-side DMOSFET $R_{DS(on)}$



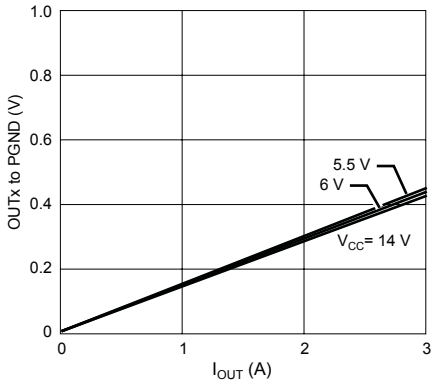
Low-side DMOSFET $R_{DS(on)}$



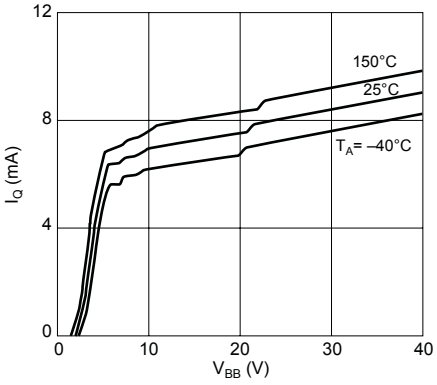
High-side DMOSFET $R_{DS(on)}$



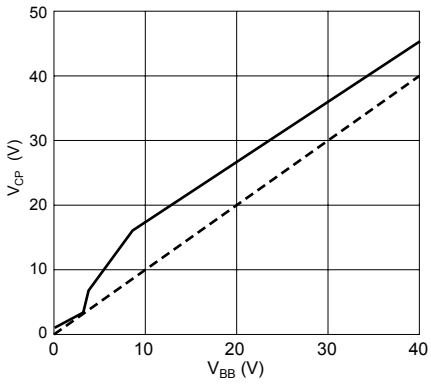
Low-side DMOSFET $R_{DS(on)}$



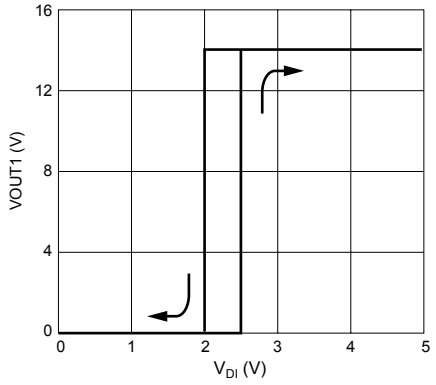
Quiescent Current versus Supply Voltage



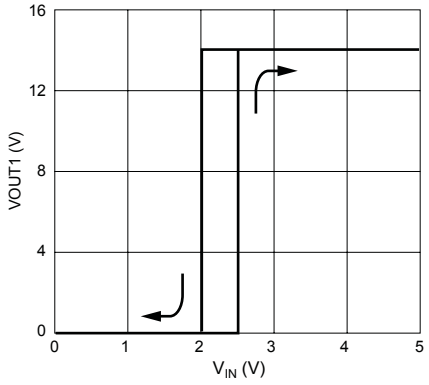
CP Pin Voltage versus Supply Voltage



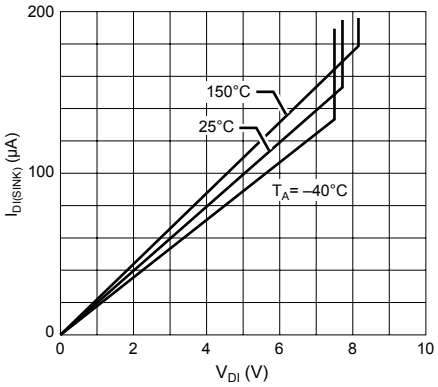
DI Pin Threshold Characteristics



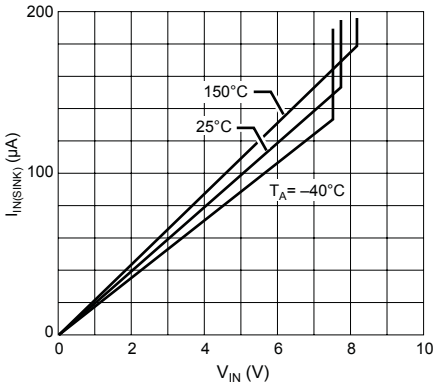
INx Pin Threshold Characteristics



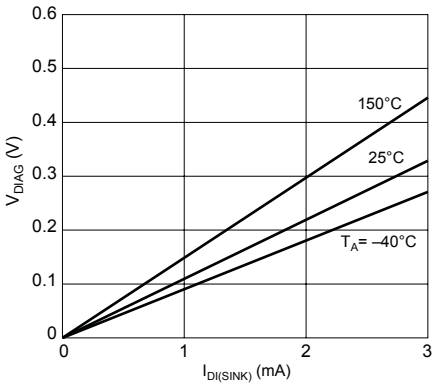
DI Pin Current Characteristics



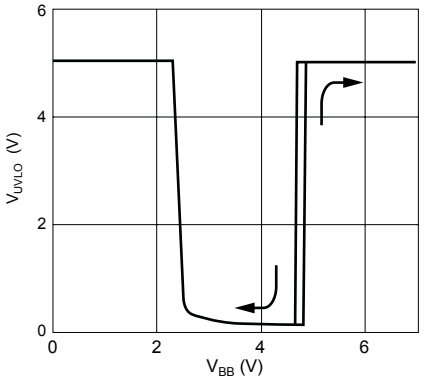
INx Pin Current Characteristics



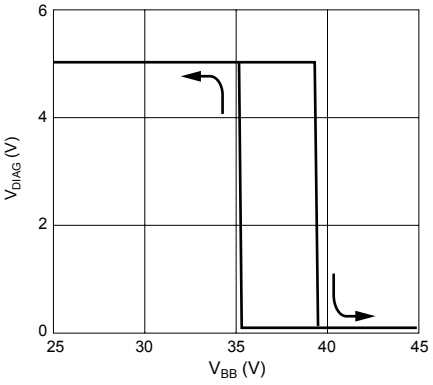
DIAG Output versus DI SInk Current



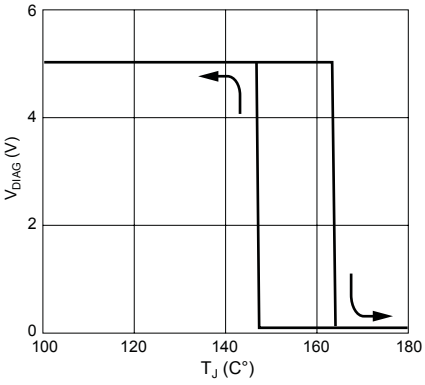
UVLO Voltage versus Supply Voltage



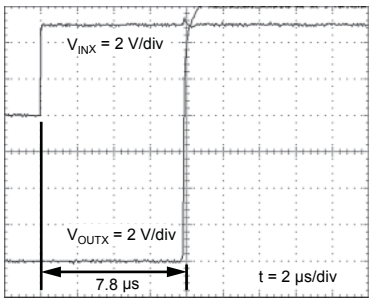
DIAG Output Voltage with OVP Activated (IC continues operation)



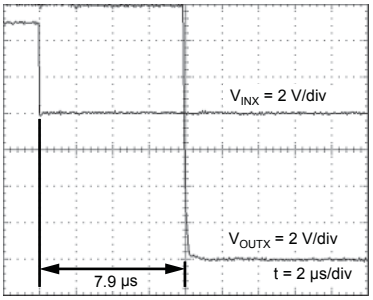
DIAG Output Voltage with TSD Activated (IC stops operation)



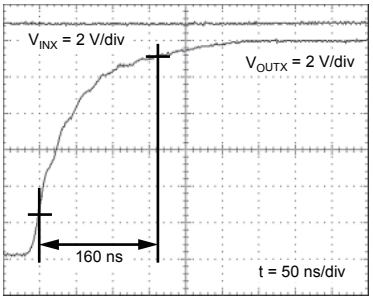
Input to Output On Propagation Delay, t_{INx_ON}



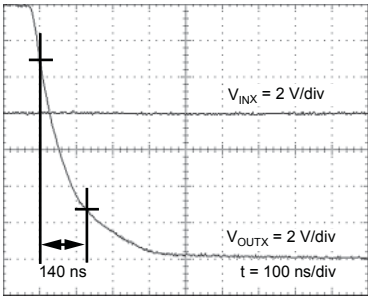
Input to Output Off Propagation Delay, t_{INx_OFF}



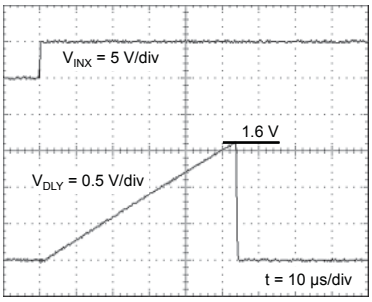
Output Rise Time, t_{RX}



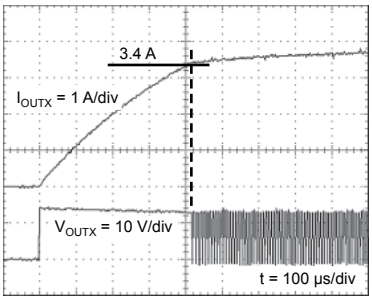
Output Fall Time, t_{FX}



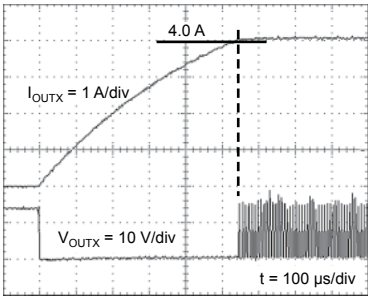
DLY Voltage
versus
INx Pin Voltage



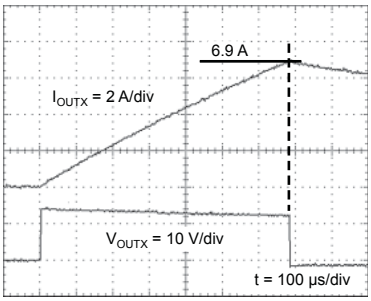
High-side DMOSFET
OCL Operation Example



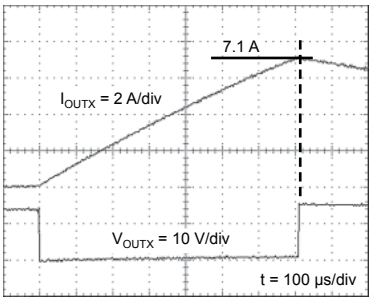
Low-side DMOSFET
OCL Operation Example



High-side DMOSFET
OCP Operation Example



Low-side DMOSFET
OCP Operation Example



Protection Function Operation

Current Limitation and Overcurrent Protection

The overcurrent limit is adapted to each DMOSFET, and is activated when the drain current reaches 3 A typical. After that, it is followed by a 3 µs typical off-time, and then it restarts automatically.

Overcurrent protection is activated when the drain current reaches 6 A typical within 3 µs, as shown in figure 3. It shuts down the IC in a latch mode. Setting the DI pin to logic low level resets the internal logic circuit and releases the latch.

DIAG Pin and Open Load Detection Behavior

Open load detection does not operate until after the output voltage of OUT1 (V_{OUT1}) reaches about $V_{BB} - 2$ V. If an open load is detected, the DIAG signal goes high. The process of open load detection is shown in figure 4:

A. During this period, UVLO is activated and DIAG stays low.

B. If a filtering capacitor is used at the outputs, it causes a delay of open load detection. (Refer to figure 5 for the relationship of the delay versus the filtering capacitor value.)

C. The open load detection period starts functioning. Raising DI input above V_{DI_H}(threshold), that is, by activating the IC, clears the DIAG signal. Therefore, the open load condition must be checked before the time of that event.

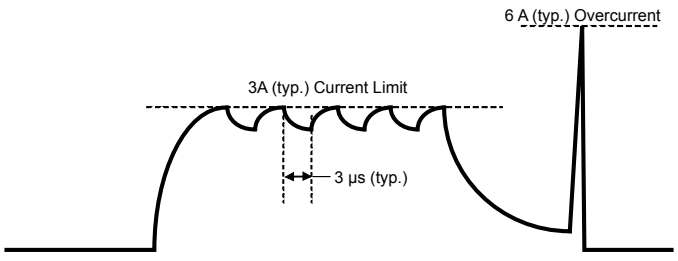


Figure 3. Behavior of Current Limitation and Overcurrent Protection function

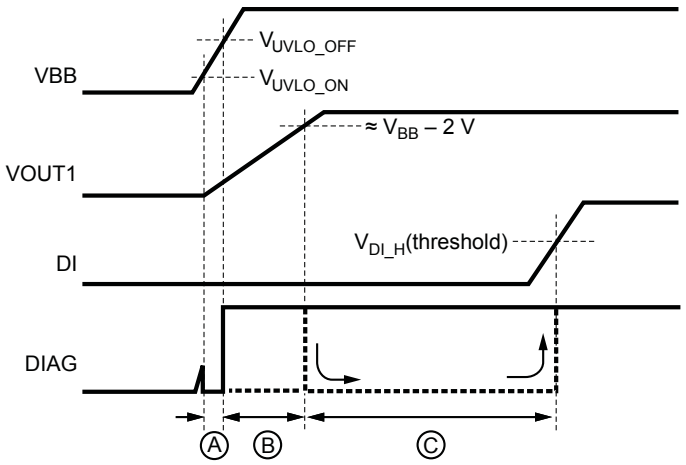


Figure 4. Open Load Detection

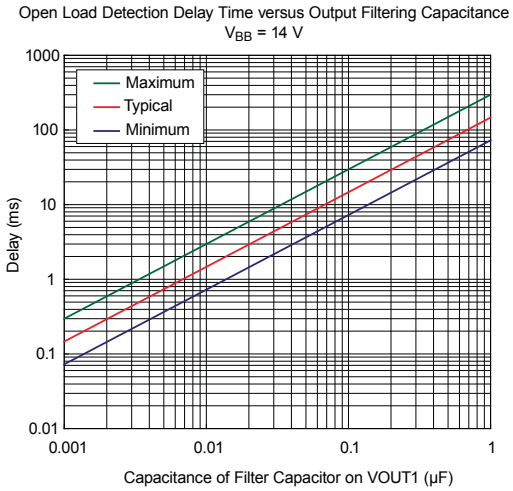


Figure 5. Delay to Open Load protection activation versus value of external capacitor on the output pins

Open load detection during normal operation of the IC is done by checking the negative potential of the output.

Referring to figure 6, during normal operation, recirculation current causes the output to be below GND. The IC checks the output voltage during 2.5 µs typical, just after the falling edge of the corresponding IN signal, and if it does not detect the negative potential, DIAG is asserted after the 2.5 µs detection period. During the 2.5 µs period, the DIAG pin is set to high because the internal circuit is reset during that period (see the arrows marked *A* in figure 6).

Open load detection operates differently during startup of the IC. The overcurrent limitation deactivated period occurs immediately after DI is asserted. Therefore, in order to repeat OCL deactivation, recycle DI.

During this period, overcurrent protection (OCP) is still active. (With regard to OCL delay, see also note 2 to the Electrical Characteristics table.)

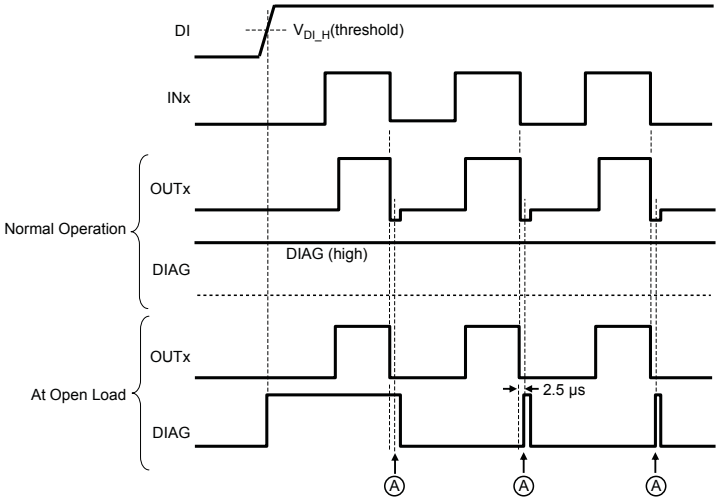


Figure 6. Open load detection in normal operation

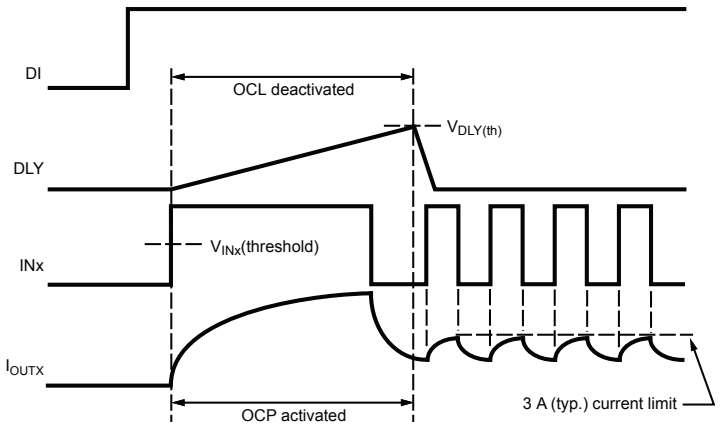


Figure 7. DLY pin effect at startup

Application Information

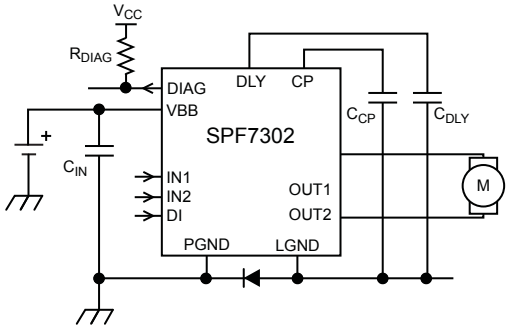


Figure 8. Typical application circuit. Recommended components are:

C_{CP}	48 nF
C_{DLY}	0.1 µF
R_{DIAG}	3.3 kΩ

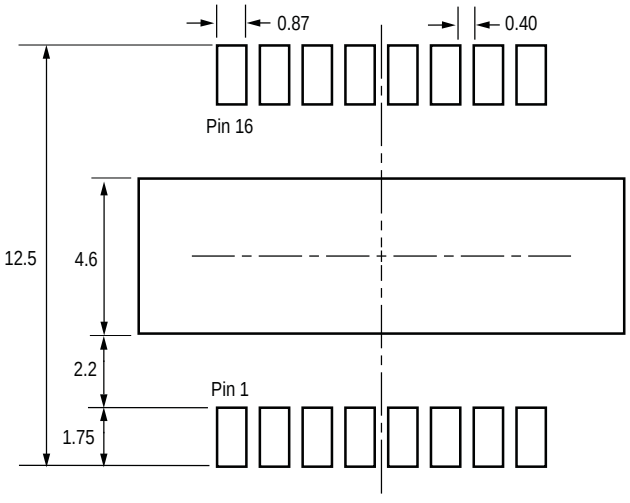


Figure 9. Recommended Solder Pad Layout, dimensions in mm

Thermal Design

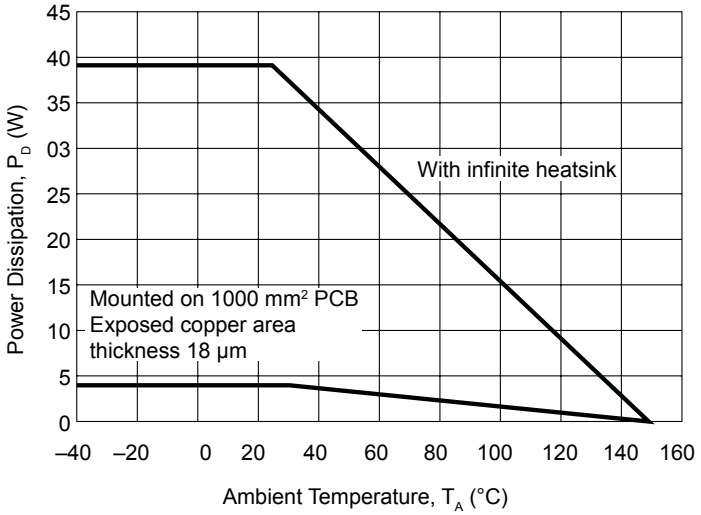


Figure 10. Power Dissipation Derating Curve

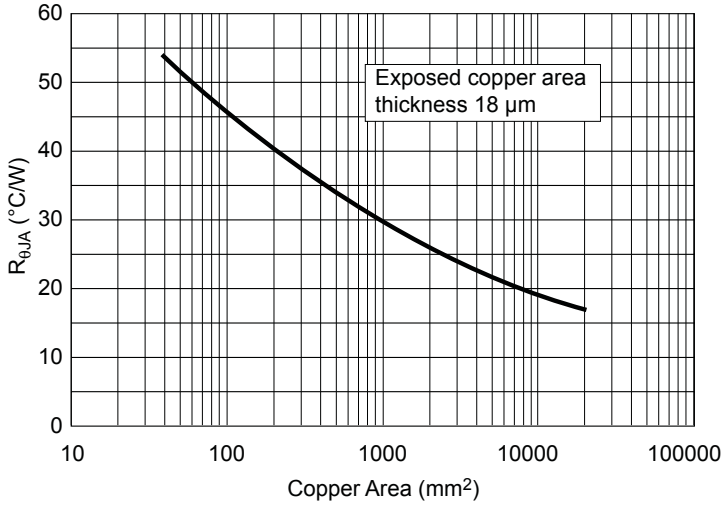


Figure 11. Thermal Resistance versus PCB Copper Area

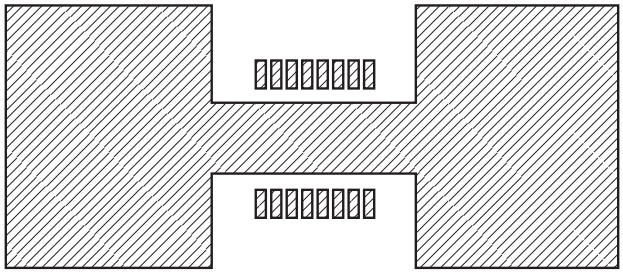


Figure 12. Test PCB Land Pattern

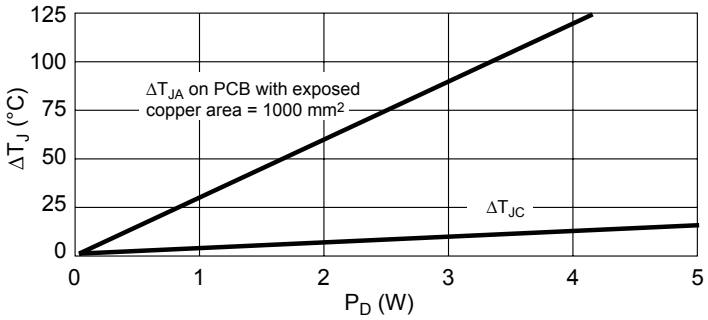


Figure 13. Thermal Performance

Approximate power dissipation, P_D, in normal operation is calculated by equation 1, and the junction temperature, T_J, is estimated by equation 2 or 3. Figure 13 shows example data of ΔT_J versus P_D. Note: a final thermal evaluation should be done under actual application conditions, taking into account actual PCB and load conditions.

$$P_D \approx V_{BB} \times I_{BB1} + (V_{satH} + V_{satL}) \times I_{OM} \times D_{ON} + (V_{satL(H)} + V_F) \times I_{OM} \times D_{OFF} \quad (1)$$

where:

V_{BB} is the supply voltage (battery voltage),

I_{BB1} is the circuit current during operation,

V_{satH} is the high-side saturation voltage,

V_{satL} is the low-side saturation voltage,

V_F is the freewheeling diode forward voltage,

I_{OM} is the motor current,

D_{ON} is the IN1 and IN2 duty cycle (proportion on), and

D_{OFF} is the IN1 and IN2 proportion off ($D_{ON} + D_{OFF} = 100\%$).

To calculate T_J:

$$T_J = R_{\theta JA} \times P_D + T_A \quad (2)$$

or

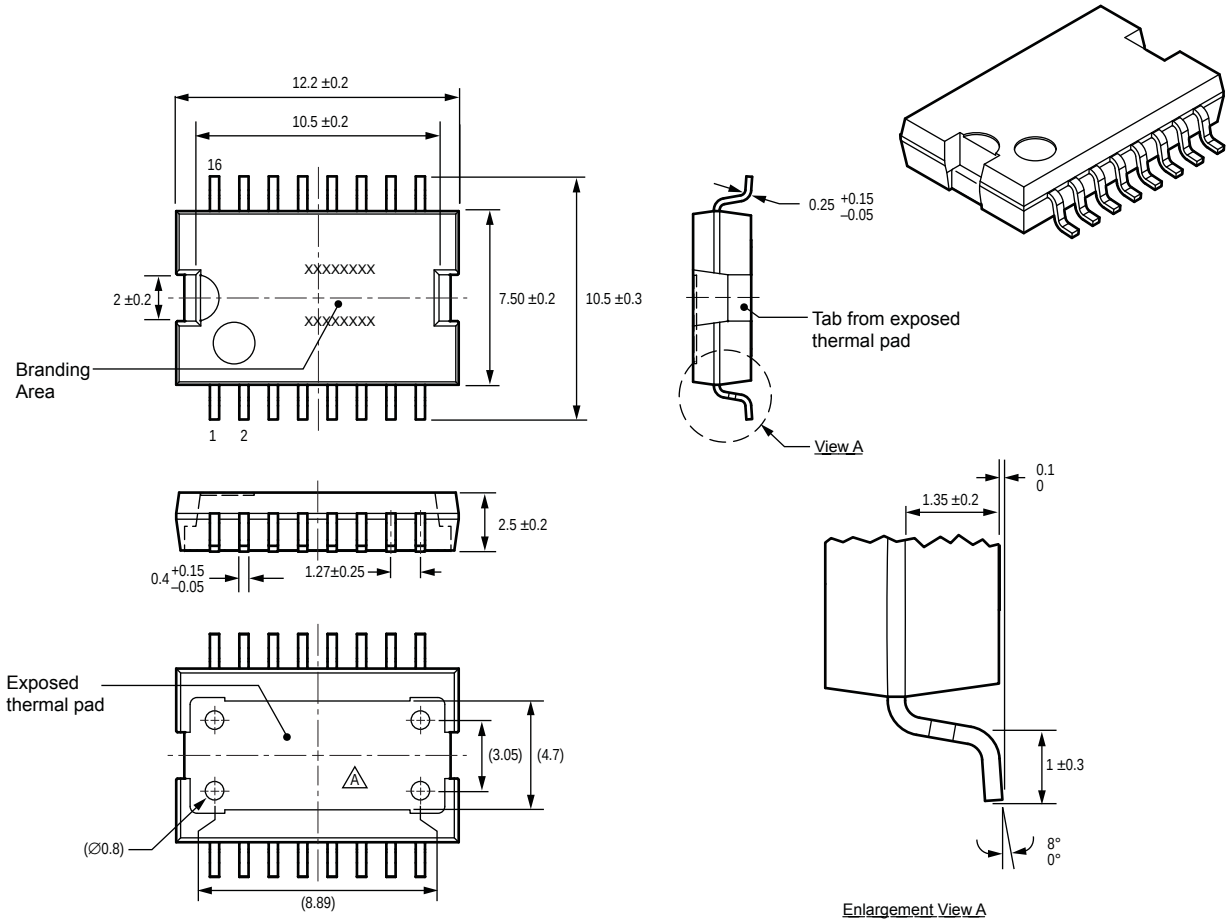
$$T_J = T_P + R_{\theta JC}\,(3.2°C/W) \times P_D \quad (3)$$

where:

$R_{\theta JA}$ can be obtained from figure 11, and

T_P is the temperature at the exposed thermal pad of the device.

Package Outline Drawing, 16 Pin HSOP



Package: HSOP-16

Dimensions in millimeters

Branding codes (exact appearance at manufacturer discretion):
1st line, type: SPF7302
2nd line, lot: *YMDD*
Where: Y is the last digit of the year of manufacture
M is the month (*1* to *9*, *O*, *N*, *D*)
DD is the date

Leadframe plating Pb-free. Device composition complies with the RoHS directive.

WARNING — These devices are designed to be operated at lethal voltages and energy levels. Circuit designs that embody these components must conform with applicable safety requirements. Precautions must be taken to prevent accidental contact with power-line potentials. Do not connect grounded test equipment.

The use of an isolation transformer is recommended during circuit development and breadboarding.

Because reliability can be affected adversely by improper storage environments and handling methods, please observe the following cautions.

Cautions for Storage

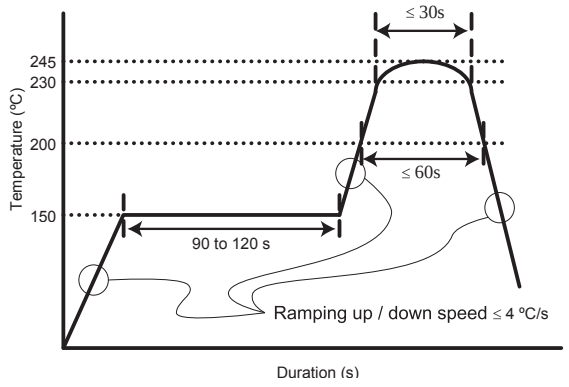
- Ensure that storage conditions comply with the standard temperature (5°C to 35°C) and the standard relative humidity (around 40 to 75%); avoid storage locations that experience extreme changes in temperature or humidity.
- Avoid locations where dust or harmful gases are present and avoid direct sunlight.
- Reinspect for rust on leads and solderability of products that have been stored for a long time.

Cautions for Testing and Handling

When tests are carried out during inspection testing and other standard test periods, protect the products from power surges from the testing device, shorts between adjacent products, and shorts to the heatsink.

Soldering

- When soldering the products, please be sure to minimize the working time, and any soldering iron should be kept at a distance from the body of the product.
- The number of reflow procedures is restricted to two only. Device reliability and appearance are guaranteed within the temperature profile below, after storage conditions of up to 168 hours at T_A = 85ºC and RH = 85%.



Solder Reflow Profile

Electrostatic Discharge

- When handling the products, operator must be grounded. Grounded wrist straps worn should have at least 1 MΩ of resistance to ground to prevent shock hazard.
- Workbenches where the products are handled should be grounded and be provided with conductive table and floor mats.
- When using measuring equipment such as a curve tracer, the equipment should be grounded.
- When soldering the products, the head of soldering irons or the solder bath must be grounded in other to prevent leak voltages generated by them from being applied to the products.
- The products should always be stored and transported in our shipping containers or conductive containers, or be wrapped in aluminum foil.

The products described herein are manufactured in Japan by Sanken Electric Co., Ltd. for sale by Allegro MicroSystems, Inc.

Sanken and Allegro reserve the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Therefore, the user is cautioned to verify that the information in this publication is current before placing any order.

When using the products described herein, the applicability and suitability of such products for the intended purpose shall be reviewed at the users responsibility.

Although Sanken undertakes to enhance the quality and reliability of its products, the occurrence of failure and defect of semiconductor products at a certain rate is inevitable.

Users of Sanken products are requested to take, at their own risk, preventative measures including safety design of the equipment or systems against any possible injury, death, fires or damages to society due to device failure or malfunction.

Sanken products listed in this publication are designed and intended for use as components in general-purpose electronic equipment or apparatus (home appliances, office equipment, telecommunication equipment, measuring equipment, etc.). Their use in any application requiring radiation hardness assurance (e.g., aerospace equipment) is not supported.

When considering the use of Sanken products in applications where higher reliability is required (transportation equipment and its control systems or equipment, fire- or burglar-alarm systems, various safety devices, etc.), contact a company sales representative to discuss and obtain written confirmation of your specifications.

The use of Sanken products without the written consent of Sanken in applications where extremely high reliability is required (aerospace equipment, nuclear power-control stations, life-support systems, etc.) is strictly prohibited.

The information included herein is believed to be accurate and reliable. Application and operation examples described in this publication are given for reference only and Sanken and Allegro assume no responsibility for any infringement of industrial property rights, intellectual property rights, or any other rights of Sanken or Allegro or any third party that may result from its use.

Anti radioactive ray design is not considered for the products listed herein.