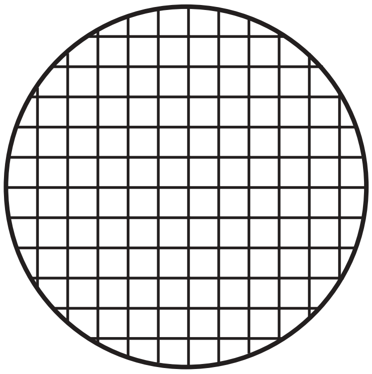
NAND01GW3A2B-KGD
NAND01GW4A2B-KGD

Known Good Die, 1 Gbit (x 8/x 16), 528 Byte/264 word page, 3 V, NAND Flash memory

Features

- High density NAND Flash memory
  - 1 Gbit memory array
  - 32 Mbit spare area
  - Cost effective solutions for mass storage applications
- NAND interface
  - x 8 or x 16 bus width
  - Multiplexed Address/ Data
  - Pinout compatibility for all densities
- Supply voltage:
  - 3.0 V device: V_{DD} = 2.7 to 3.6 V
- Page size
  - x 8 device: (512 + 16 spare) bytes
  - x 16 device: (256 + 8 spare) words
- Block size
  - x 8 device: (16 K + 512 spare) bytes
  - x 16 device: (8 K + 256 spare) words
- Page Read / Program
  - Random access: 15 µs (3 V) (max)
  - Sequential access: 50 ns (min)
  - Page program time: 200 µs (typ)
- Copy Back Program mode
  - Fast page copy without external buffering
- Fast Block Erase
  - Block erase time: 2 ms (typ)
- Status Register
- Electronic signature
- Chip Enable 'Don't care'
  - Simple interface with microcontroller



Wafer

- Serial Number option
- Hardware Data Protection
  - Program/Erase locked during Power transitions
- Data Integrity
  - 100,000 Program/Erase cycles (with ECC)
  - 10 years Data Retention

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1 Description

The NAND Flash 528 Byte/ 264 Word Page is a family of non-volatile Flash memories that uses the Single Level Cell (SLC) NAND cell technology. It is referred to as the Small Page family. The NAND01GW3A2B-KGD and NAND01GW4A2B-KGD have a density of 1 Gbits. It operates from a 3V voltage supply. The size of a Page is either 528 Bytes (512 + 16 spare) or 264 Words (256 + 8 spare) depending on whether the device has a x8 or x16 bus width.

The address lines are multiplexed with the Data Input/Output signals on a multiplexed x8 and x16 Input/Output bus on the NAND01GW3A2B-KGD and NAND01GW4A2B-KGD, respectively. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased over 100,000 cycles (with ECC). To extend the lifetime of NAND Flash devices it is strongly recommended to implement an Error Correction Code (ECC). A Write Protect pin is available to give a hardware protection against program and erase operations.

The devices feature an open-drain Ready/Busy output that can be used to identify if the Program/Erase/Read (P/E/R) Controller is currently active. The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor.

A Copy Back command is available to optimize the management of defective blocks. When a Page Program operation fails, the data can be programmed in another page without having to resend the data to be programmed.

The devices are available in unsawn wafer format for multichip package products (MCPs).

They have the Chip Enable Don't Care option, which allows the code to be directly downloaded by a microcontroller, as Chip Enable transitions during the latency time do not stop the read operation.

A Serial Number option, allows each device to be uniquely identified. The Serial Number options is subject to an NDA (Non Disclosure Agreement) and so not described in the datasheet. For more details of this option contact your nearest Numonyx Sales office.

For information on how to order these options refer to *Table 20: Ordering Information Scheme*. Devices are shipped from the factory with Block 0 always valid and the memory content bits, in valid blocks, erased to '1'.

See *Table 1: Product description*, for all the devices available.

Table 1. Product description

Part Number	Density	Bus Width	Page Size	Block Size	Memory Array	Operating Voltage	Timings				Package
							Random Access (Max)	Sequential Access (Min)	Page Program Typical	Block Erase Typical	
NAND01GW3A2B-KGD	1 Gbit	x8	256+8 Words	8K+256 Words	32 Pages x 8192 Blocks	2.7 to 3.6V	15µs	50ns	200µs	2ms	Known Good Die for MCP
NAND01GW4A2B-KGD		x16									

Figure 1. Logic diagram

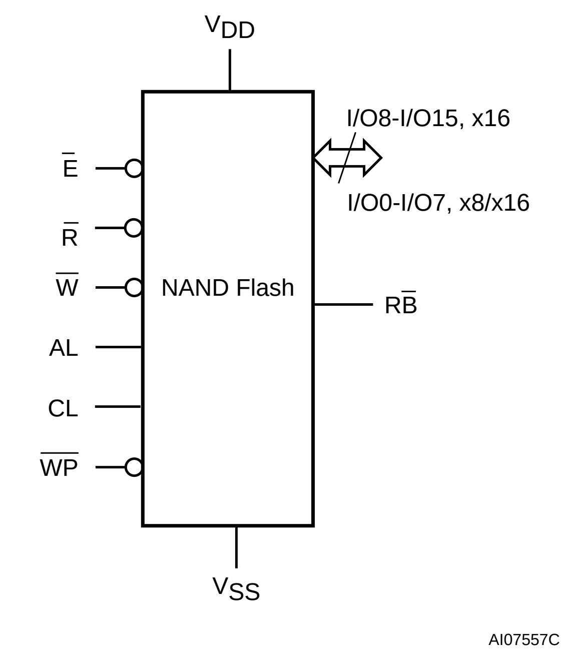
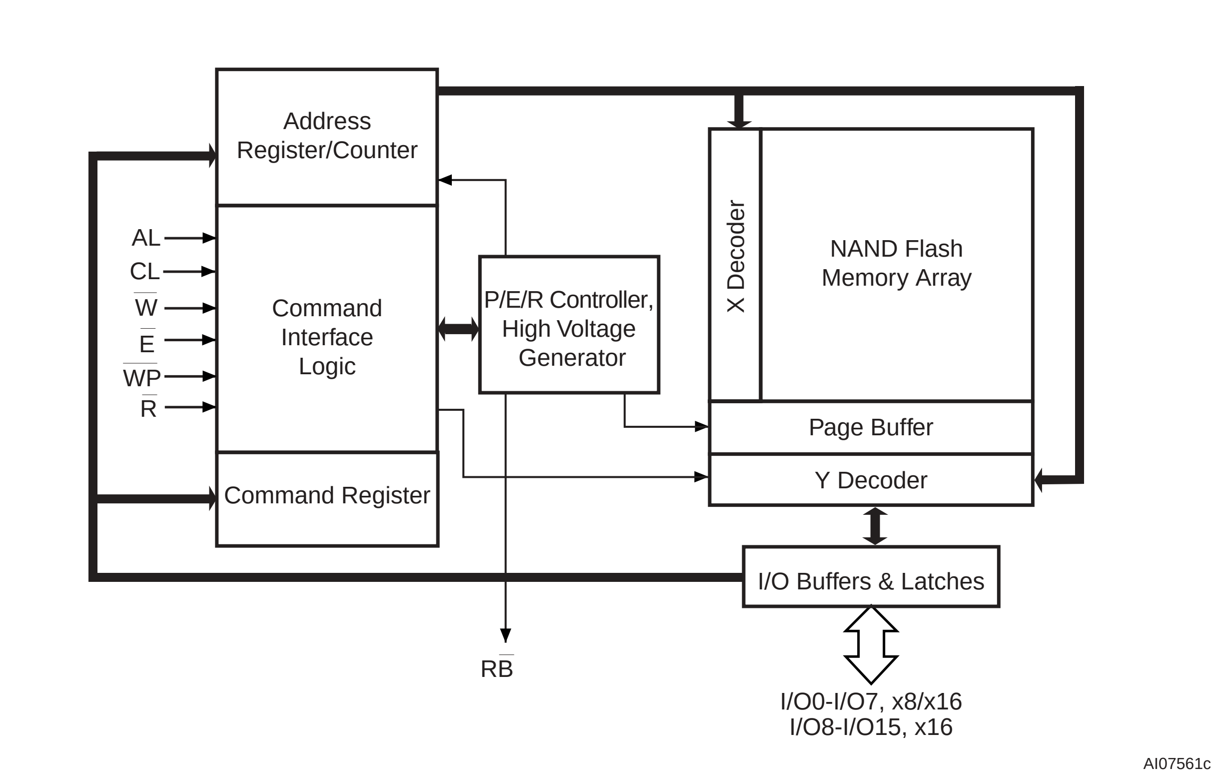


Table 2. Signal names

I/O8-15	Data Input/Outputs for x16 devices
I/O0-7	Data Input/Outputs, Address Inputs, or Command Inputs for x8 and x16 devices
AL	Address Latch Enable
CL	Command Latch Enable
E	Chip Enable
R	Read Enable
R$\overline{B}$	Ready/Busy (open-drain output)
W	Write Enable
WP	Write Protect
V_{DD}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally
DU	Do Not Use

Figure 2. Logic block diagram



2 Memory array organization

The memory array is made up of NAND structures where 16 cells are connected in series.

The memory array is organized in blocks where each block contains 32 pages. The array is split into two areas, the main area and the spare area. The main area of the array is used to store data whereas the spare area is typically used to store Error correction Codes, software flags or Bad Block identification.

In x8 devices the pages are split into a main area with two half pages of 256 Bytes each and a spare area of 16 Bytes. In the x16 devices the pages are split into a 256 Word main area and an 8 Word spare area. Refer to *Figure 3: Memory array organization*.

2.1 Bad blocks

The NAND Flash 528 byte/ 264 word page devices may contain Bad Blocks, that is blocks that contain one or more invalid bits whose reliability is not guaranteed. Additional Bad Blocks may develop during the lifetime of the device.

The Bad Block Information is written prior to shipping (refer to *Section 7.1: Bad Block Management* for more details).

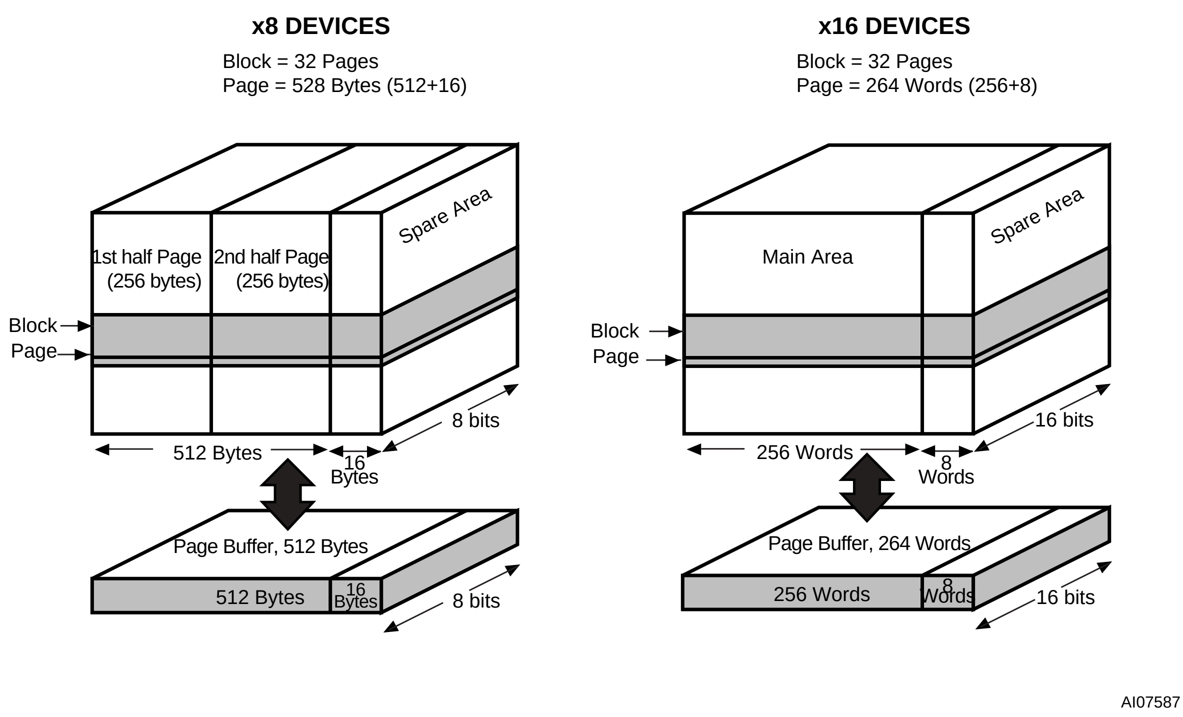
Table 3 shows the minimum number of valid blocks in each device. The values shown include both the Bad Blocks that are present when the device is shipped and the Bad Blocks that could develop later on.

These blocks need to be managed using Bad Blocks Management, Block Replacement or Error Correction Codes (refer to *Section 7: Software algorithms*).

Table 3. Valid blocks

Density of device	Min	Max
1 Gbit	8032	8192

Figure 3. Memory array organization



3 Signal descriptions

See *Figure 1: Logic diagram*, and *Table 2: Signal names*, for a brief overview of the signals connected to this device.

3.1 Inputs/Outputs (I/O0-I/O7)

Input/Outputs 0 to 7 are used to input the selected address, output the data during a Read operation or input a command or data during a Write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

3.2 Inputs/Outputs (I/O8-I/O15)

Input/Outputs 8 to 15 are only available in x16 devices. They are used to output the data during a Read operation or input data during a Write operation. Command and Address Inputs only require I/O0 to I/O7.

The inputs are latched on the rising edge of Write Enable. I/O8-I/O15 are left floating when the device is deselected or the outputs are disabled.

3.3 Address Latch Enable (AL)

The Address Latch Enable activates the latching of the Address inputs in the Command Interface. When AL is high, the inputs are latched on the rising edge of Write Enable.

3.4 Command Latch Enable (CL)

The Command Latch Enable activates the latching of the Command inputs in the Command Interface. When CL is high, the inputs are latched on the rising edge of Write Enable.

3.5 Chip Enable ($\overline{E}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and read circuitry. When Chip Enable is low, V_{IL}, the device is selected.

If Chip Enable goes High (V_{IH}) while the device is busy, the device remains selected and does not go into standby mode.

3.6 Read Enable ($\overline{R}$)

The Read Enable, $\overline{R}$, controls the sequential data output during Read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

3.7 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 10 µs (min) is required before the Command Interface is ready to accept a command. It is recommended to keep Write Enable high during the recovery time.

3.8 Write Protect ($\overline{WP}$)

The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

3.9 Ready/Busy (R$\overline{B}$)

The Ready/Busy output, R$\overline{B}$, is an open-drain output that can be used to identify if the P/E/R Controller is currently active.

When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

Refer to *Section 10.1: Ready/Busy signal electrical characteristics* for details on how to calculate the value of the pull-up resistor.

3.10 V_{DD} Supply Voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

An internal voltage detector disables all functions whenever V_{DD} is below the V_{LKO} threshold (see *Figure 30: Data protection*) to protect the device from any involuntary Program/Erase operations during power-transitions.

Each device in a system should have V_{DD} decoupled with a 0.1µF capacitor. The PCB track widths should be sufficient to carry the required program and erase currents

3.11 V_{SS} Ground

Ground, V_{SS}, is the reference for the power supply. It must be connected to the system ground.

4 Bus operations

There are six standard bus operations that control the memory. Each of these is described in this section, see *Table 4: Bus operations*, for a summary.

4.1 Command Input

Command Input bus operations are used to give commands to the memory. Command are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O0 to I/O7 are used to input commands.

See *Figure 14* and *Table 18* for details of the timings requirements.

4.2 Address Input

Address Input bus operations are used to input the memory address. Four bus cycles are required to input the addresses (refer to *Table 5* and *Table 6*, Address Insertion).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal. Only I/O0 to I/O7 are used to input addresses.

See *Figure 15* and *Table 18* for details of the timings requirements.

4.3 Data Input

Data Input bus operations are used to input the data to be programmed.

Data is accepted only when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low and Read Enable is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

See *Figure 16*, *Table 18* and *Table 20* for details of the timings requirements.

4.4 Data Output

Data Output bus operations are used to read: the data in the memory array, the Status Register, the Electronic Signature and the Serial Number.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low.

The data is output sequentially using the Read Enable signal.

See *Figure 17* and *Table 20* for details of the timings requirements.

4.5 Write Protect

Write Protect bus operations are used to protect the memory against program or erase operations. When the Write Protect signal is Low the device will not accept program or erase operations and so the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection even during power-up.

4.6 Standby

When Chip Enable is High the memory enters Standby mode, the device is deselected, outputs are disabled and power consumption is reduced.

Table 4. Bus operations

Bus operation	$\overline{E}$	AL	CL	$\overline{R}$	$\overline{W}$	$\overline{WP}$	I/O0 - I/O7	I/O8 - I/O15(1)
Command Input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X(2)	Command	X
Address Input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address	X
Data Input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	X	Data Input	Data Input
Data Output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data Output	Data Output
Write Protect	X	X	X	X	X	V_{IL}	X	X
Standby	V_{IH}	X	X	X	X	X	X	X

1. Only for x16 devices.
2. $\overline{WP}$ must be V_{IH} when issuing a program or erase command.

Table 5. Address Insertion, x 8 devices(1)(2)

Bus cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	A16	A15	A14	A13	A12	A11	A10	A9
3rd	A24	A23	A22	A21	A20	A19	A18	A17
4th	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A26	A25

1. A8 is set Low or High by the 00h or 01h Command, see *Section 6.1: Pointer operations*.
2. Any additional address input cycles will be ignored.

Table 6. Address Insertion, x 16 devices(1)(2)(3)

Bus cycle	I/O8-I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	V_{IL}	A7	A6	A5	A4	A3	A2	A1	A0
2nd		A16	A15	A14	A13	A12	A11	A10	A9
3rd		A24	A23	A22	A21	A20	A19	A18	A17
4th		V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A26	A25

1. A8 is Don't care in x 16 devices.
2. Any additional address input cycles will be ignored.
3. The 01h command is not used in x 16 devices.

Table 7. Address definitions

Address	Definition
A0 - A7	Column Address
A9 - A26	Page Address
A9 - A13	Address in Block
A14 - A26	Block Address
A8	A8 is set Low or High by the 00h or 01h Command, and is Don't care in x 16 devices

5 Command set

All bus write operations to the device are interpreted by the Command Interface. The Commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is high. Device operations are selected by writing specific commands to the Command Register. The two-step command sequences for program and erase operations are imposed to maximize data security.

The Commands are summarized in *Table 8: Commands*.

Table 8. Commands

Command	Bus Write operations(1)			Command accepted during busy
	1st cycle	2nd cycle	3rd cycle	
Read A	00h	-	-	
Read B	01h(2)	-	-	
Read C	50h	-	-	
Read Electronic Signature	90h	-	-	
Read Status Register	70h	-	-	Yes
Page Program	80h	10h	-	
Copy Back Program	00h	8Ah	10h	
Block Erase	60h	D0h	-	
Reset	FFh	-	-	Yes

1. The bus cycles are only shown for issuing the codes. The cycles required to input the addresses or input/output data are not shown.
2. Don’t Care in x 16 devices.

6 Device operations

6.1 Pointer operations

As the NAND Flash memories contain two different areas for x 16 devices and three different areas for x 8 devices (see *Figure 4*) the read command codes (00h, 01h, 50h) are used to act as pointers to the different areas of the memory array (they select the most significant column address).

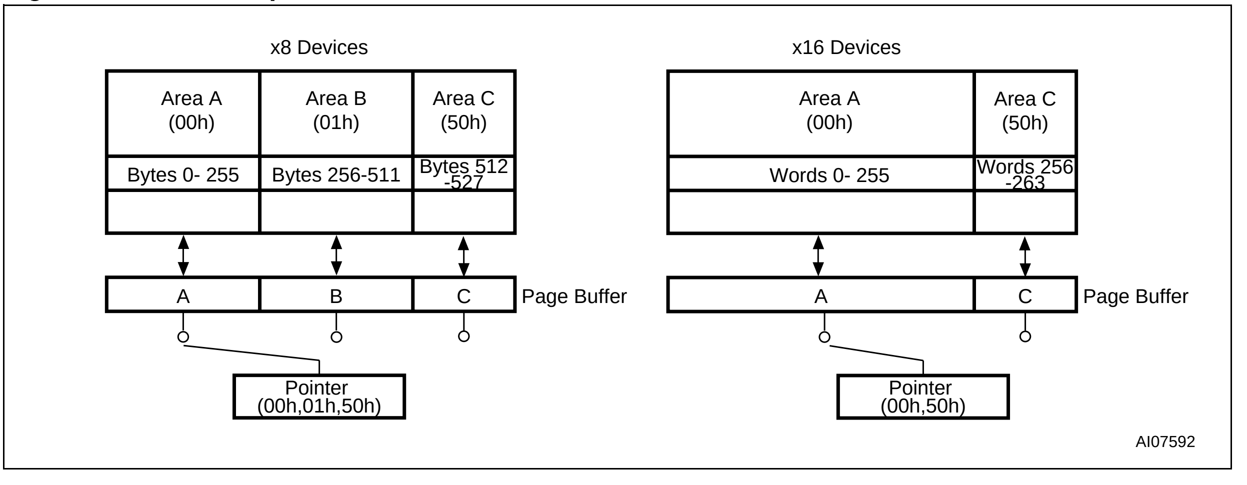
The Read A and Read B commands act as pointers to the main memory area. Their use depends on the bus width of the device.

- In x 16 devices the Read A command (00h) sets the pointer to Area A (the whole of the main area) that is words 0 to 255.
- In x 8 devices the Read A command (00h) sets the pointer to Area A (the first half of the main area) that is bytes 0 to 255, and the Read B command (01h) sets the pointer to Area B (the second half of the main area) that is bytes 256 to 511.

In both the x8 and x16 devices the Read C command (50h), acts as a pointer to Area C (the spare memory area) that is bytes 512 to 527 or words 256 to 263.

Once the Read A and Read C commands have been issued the pointer remains in the respective areas until another pointer code is issued. However, the Read B command is effective for only one operation, once an operation has been executed in Area B the pointer returns automatically to Area A.

Figure 4. Pointer operations



6.2 Read Memory Array

Each operation to read the memory area starts with a pointer operation as shown in the *Section 6.1: Pointer operations*. Once the area (main or spare) has been selected using the Read A, Read B or Read C commands, four bus cycles are required to input the address (refer to *Table 5*) of the data to be read.

The device defaults to Read A mode after power-up or a Reset operation.

When reading the spare area addresses:

- A0 to A3 (x 8 devices)
- A0 to A2 (x 16 devices)

are used to set the start address of the spare area while addresses:

- A4 to A7 (x 8 devices)
- A3 to A7 (x 16 devices)

are ignored.

Once the Read A or Read C commands have been issued they do not need to be reissued for subsequent read operations as the pointer remains in the respective area. However, the Read B command is effective for only one operation, once an operation has been executed in Area B the pointer returns automatically to Area A and so another Read B command is required to start another read operation in Area B.

Once a read command is issued two types of operations are available: Random Read and Page Read.

6.2.1 Random Read

Each time the command is issued the first read is Random Read.

6.2.2 Page Read

After the Random Read access the page data is transferred to the Page Buffer in a time of t_{WHBH} (refer to *Table 20* for value). Once the transfer is complete the Ready/Busy signal goes High. The data can then be read out sequentially (from selected column address to last column address) by pulsing the Read Enable signal.

Figure 5. Read (A,B,C) operations

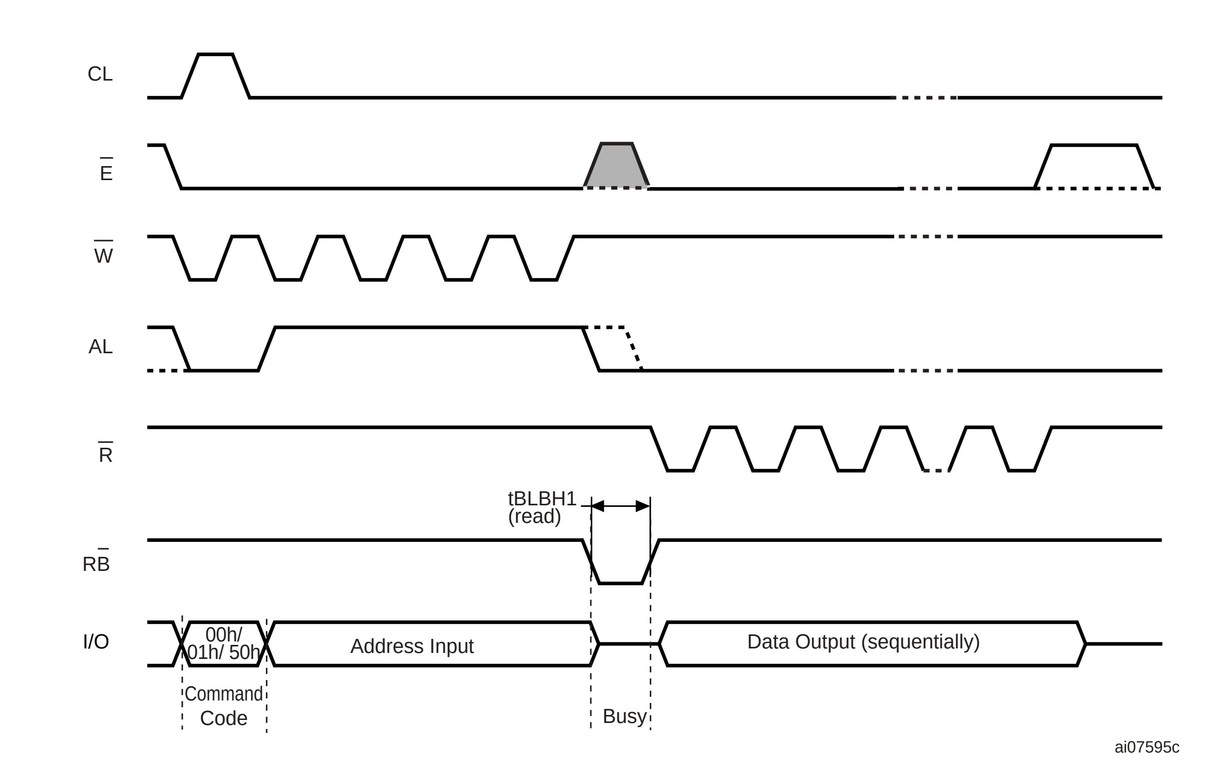
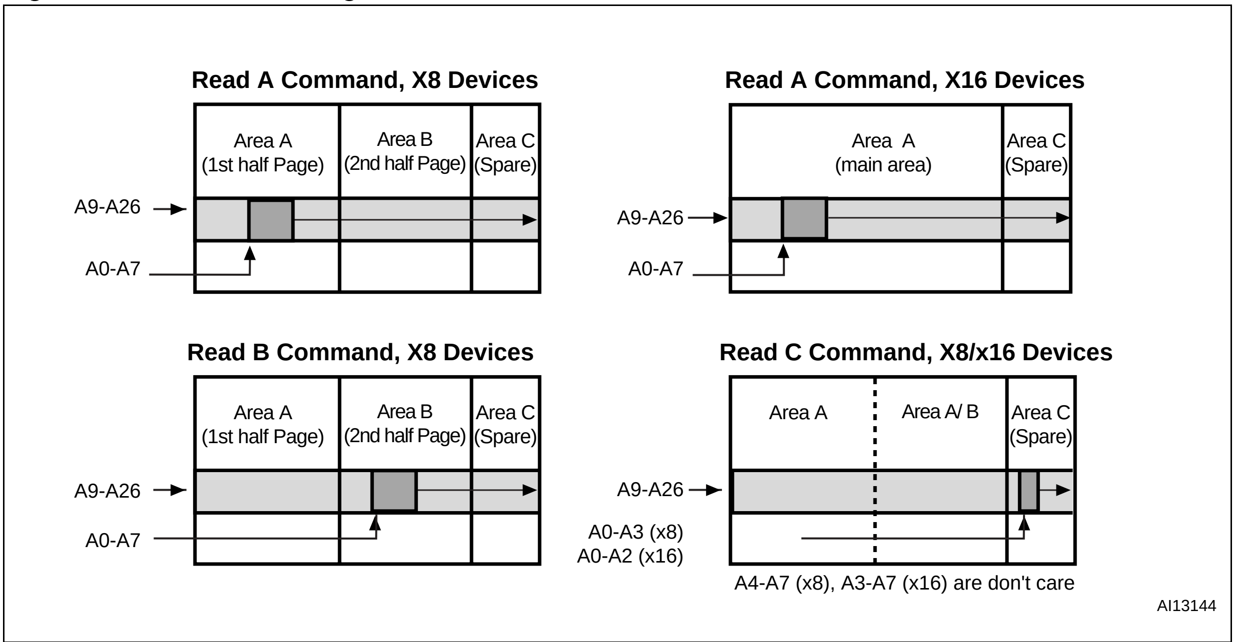


Figure 6. Read block diagrams



6.3 Page Program

The Page Program operation is the standard operation to program data to the memory array.

The main area of the memory array is programmed by page, however partial page programming is allowed where any number of bytes (1 to 528) or words (1 to 264) can be programmed.

The maximum number of consecutive partial page program operations allowed in the same page is three. After exceeding this a Block Erase command must be issued before any further program operations can take place in that page.

Before starting a Page Program operation a Pointer operation can be performed to point to the area to be programmed. Refer to the *Section 6.1: Pointer operations* and *Figure 5* for details.

Each Page Program operation consists of five steps (see *Figure 7*):

1. One bus cycle is required to setup the Page Program command
2. Four bus cycles are then required to input the program address (refer to *Table 5*)
3. The data is then input (up to 528 bytes/ 264 words) and loaded into the Page Buffer
4. One bus cycle is required to issue the confirm command to start the P/E/R Controller.
5. The P/E/R Controller then programs the data into the array.

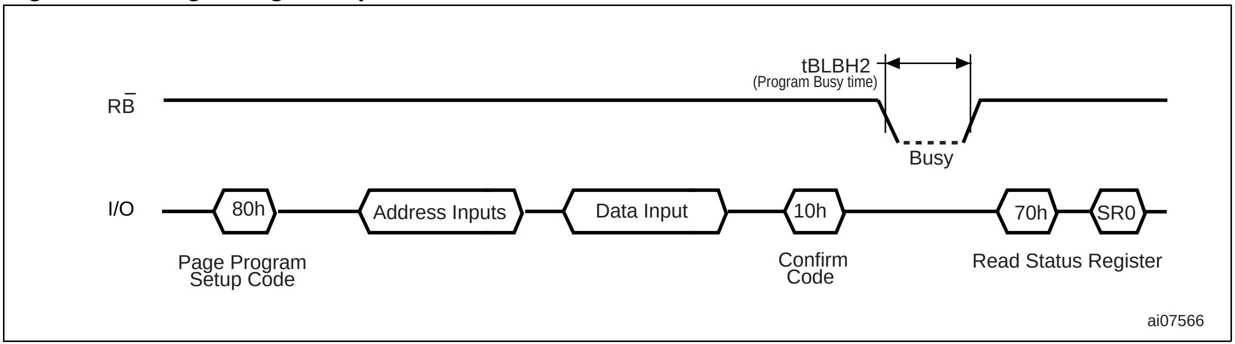
Once the program operation has started the Status Register can be read using the Read Status Register command. During program operations the Status Register will only flag errors for bits set to '1' that have not been successfully programmed to '0'.

During the program operation, only the Read Status Register and Reset commands will be accepted, all other commands will be ignored.

Once the program operation has completed the P/E/R Controller bit SR6 is set to '1' and the Ready/Busy signal goes High.

The device remains in Read Status Register mode until another valid command is written to the Command Interface.

Figure 7. Page Program operation



1. Before starting a Page Program operation a Pointer operation can be performed. Refer to *Section 6.1: Pointer operations* for details.

6.4 Copy Back Program

The Copy Back Program operation is used to copy the data stored in one page and reprogram it in another page.

The Copy Back Program operation does not require external memory and so the operation is faster and more efficient because the reading and loading cycles are not required. The operation is particularly useful when a portion of a block is updated and the rest of the block needs to be copied to the newly assigned block.

If the Copy Back Program operation fails an error is signalled in the Status Register. However as the standard external ECC cannot be used with the Copy Back operation bit error due to charge loss cannot be detected. For this reason it is recommended to limit the number of Copy Back operations on the same data and or to improve the performance of the ECC.

The Copy Back Program operation requires three steps:

1. The source page must be read using the Read A command (one bus write cycle to setup the command and then 4 bus write cycles to input the source page address). This operation copies all 264 Words/ 528 Bytes from the page into the Page Buffer.
2. When the device returns to the ready state (Ready/Busy High), the second bus write cycle of the command is given with the 4 bus cycles to input the target page address. Refer to *Table 9* for the addresses that must be the same for the Source and Target pages.
3. Then the confirm command is issued to start the P/E/R Controller.

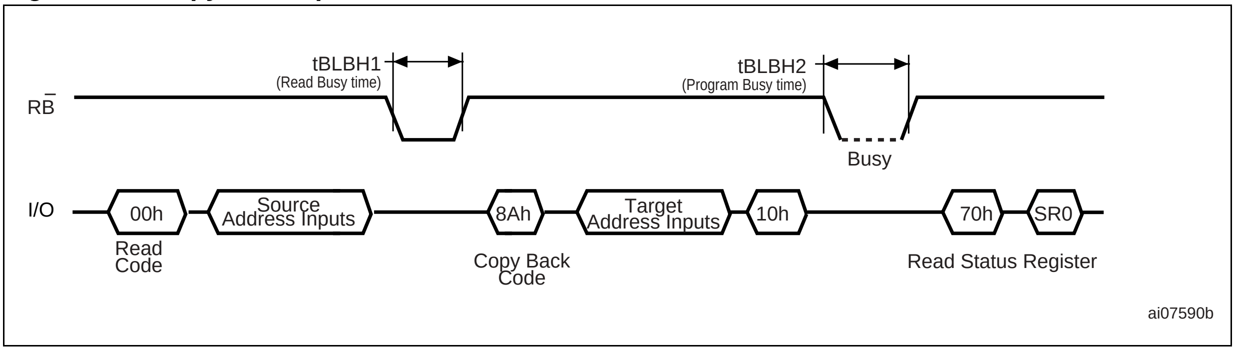
After a Copy Back Program operation, a partial-page program is not allowed in the target page until the block has been erased.

See *Figure 8* for an example of the Copy Back operation.

Table 9. Copy Back Program addresses

Density	Same Address for Source and Target Pages
1 Gbit	A14, A26

Figure 8. Copy Back operation



6.5 Block Erase

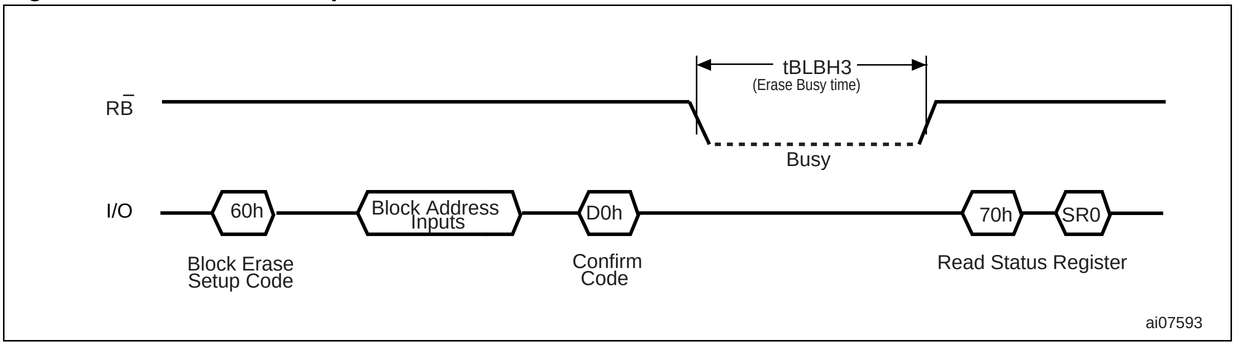
Erase operations are done one block at a time. An erase operation sets all of the bits in the addressed block to ‘1’. All previous data in the block is lost.

An erase operation consists of three steps (refer to *Figure 9*):

1. One bus cycle is required to setup the Block Erase command.
2. Only three bus cycles are required to input the block address. The first cycle (A0 to A7) is not required as only addresses A14 to A26 are valid, A9 to A13 are ignored. In the last address cycle I/O2 to I/O7 must be set to V_{IL}.
3. One bus cycle is required to issue the confirm command to start the P/E/R Controller.

Once the erase operation has completed the Status Register can be checked for errors.

Figure 9. Block Erase operation



6.6 Reset

The Reset command is used to reset the Command Interface and Status Register. If the Reset command is issued during any operation, the operation will be aborted. If it was a program or erase operation that was aborted, the contents of the memory locations being modified will no longer be valid as the data will be partially programmed or erased.

If the device has already been reset then the new Reset command will not be accepted.

The Ready/Busy signal goes Low for t_{BLBH4} after the Reset command is issued. The value of t_{BLBH4} depends on the operation that the device was performing when the command was issued, refer to *Table 20* for the values.

6.7 Read Status Register

The device contains a Status Register which provides information on the current or previous Program or Erase operation. The various bits in the Status Register convey information and errors on the operation.

The Status Register is read by issuing the Read Status Register command. The Status Register information is present on the output data bus (I/O0-I/O7) on the falling edge of Chip Enable or Read Enable, whichever occurs last. When several memories are connected in a system, the use of Chip Enable and Read Enable signals allows the system to poll each device separately, even when the Ready/Busy pins are common-wired. It is not necessary to toggle the Chip Enable or Read Enable signals to update the contents of the Status Register.

After the Read Status Register command has been issued, the device remains in Read Status Register mode until another command is issued. Therefore if a Read Status Register command is issued during a Random Read cycle a new read command must be issued to continue with a Page Read.

The Status Register bits are summarized in *Table 10: Status Register Bits*. Refer to *Table 10* in conjunction with the following text descriptions.

6.7.1 Write Protection bit (SR7)

The Write Protection bit can be used to identify if the device is protected or not. If the Write Protection bit is set to ‘1’ the device is not protected and program or erase operations are allowed. If the Write Protection bit is set to ‘0’ the device is protected and program or erase operations are not allowed.

6.7.2 P/E/R Controller bit (SR6)

The Program/Erase/Read Controller bit indicates whether the P/E/R Controller is active or inactive. When the P/E/R Controller bit is set to ‘0’, the P/E/R Controller is active (device is busy); when the bit is set to ‘1’, the P/E/R Controller is inactive (device is ready).

6.7.3 Error bit (SR0)

The Error bit is used to identify if any errors have been detected by the P/E/R Controller. The Error Bit is set to ’1’ when a program or erase operation has failed to write the correct data to the memory. If the Error Bit is set to ‘0’ the operation has completed successfully.

6.7.4 SR5, SR4, SR3, SR2 and SR1 are reserved

Table 10. Status Register Bits

Bit	Name	Logic level	Definition
SR7	Write Protection	'1'	Not Protected
		'0'	Protected
SR6	Program/ Erase/ Read Controller	'1'	P/E/R C inactive, device ready
		'0'	P/E/R C active, device busy
SR5, SR4, SR3, SR2, SR1	Reserved	Don't care	
SR0	Generic Error	'1'	Error – operation failed
		'0'	No Error – operation successful

6.8 Read Electronic Signature

The device contains a Manufacturer Code and Device Code. To read these codes two steps are required:

1. first use one Bus Write cycle to issue the Read Electronic Signature command (90h), followed by an address input of 00h.
2. then perform two Bus Read operations – the first will read the Manufacturer Code and the second, the Device Code. Further Bus Read operations will be ignored.

Refer to *Table 11: Electronic Signature*, for information on the addresses.

Table 11. Electronic Signature

Part number	Manufacturer code	Device code
NAND01GW3A2B-KGD	20h	79h
NAND01GW4A2B-KGD	0020h	0074h

7 Software algorithms

This section gives information on the software algorithms that Numonyx recommends to implement to manage the Bad Blocks and extend the lifetime of the NAND device.

NAND Flash memories are programmed and erased by Fowler-Nordheim tunneling using a high voltage. Exposing the device to a high voltage for extended periods can cause the oxide layer to be damaged. For this reason, the number of program and erase cycles is limited (see *Table 13* for value) and it is recommended to implement Garbage Collection, a Wear-Leveling Algorithm and an Error Correction Code, to extend the number of program and erase cycles and increase the data retention.

To help integrate a NAND memory into an application Numonyx can provide File System OS Native reference software, which supports the basic commands of file management.

Contact the nearest Numonyx sales office for more details.

7.1 Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor.

The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written prior to shipping. Any block where the 6th byte (x 8 device) / 1st word (x 16 device) in the spare area of the 1st page does not contain FFh is a Bad Block.

The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in *Figure 10*.

7.2 NAND Flash memory failure modes

Over the lifetime of the device additional Bad Blocks may develop.

To implement a highly reliable system, all the possible failure modes must be considered:

- Program/Erase failure: in this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register. As the failure of a Page Program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. The Copy Back Program command can be used to copy the data to a valid block. See *Section 6.4: Copy Back Program* for more details.
- Read failure: in this case, ECC correction must be implemented. To efficiently use the memory space, it is recommended to recover single-bit error in read by ECC, without replacing the whole block.

Refer to *Table 12* for the procedure to follow if an error occurs during an operation.

Table 12. NAND Flash failure modes

Operation	Procedure
Erase	Block Replacement
Program	Block Replacement or ECC
Read	ECC

Figure 10. Bad Block management flowchart

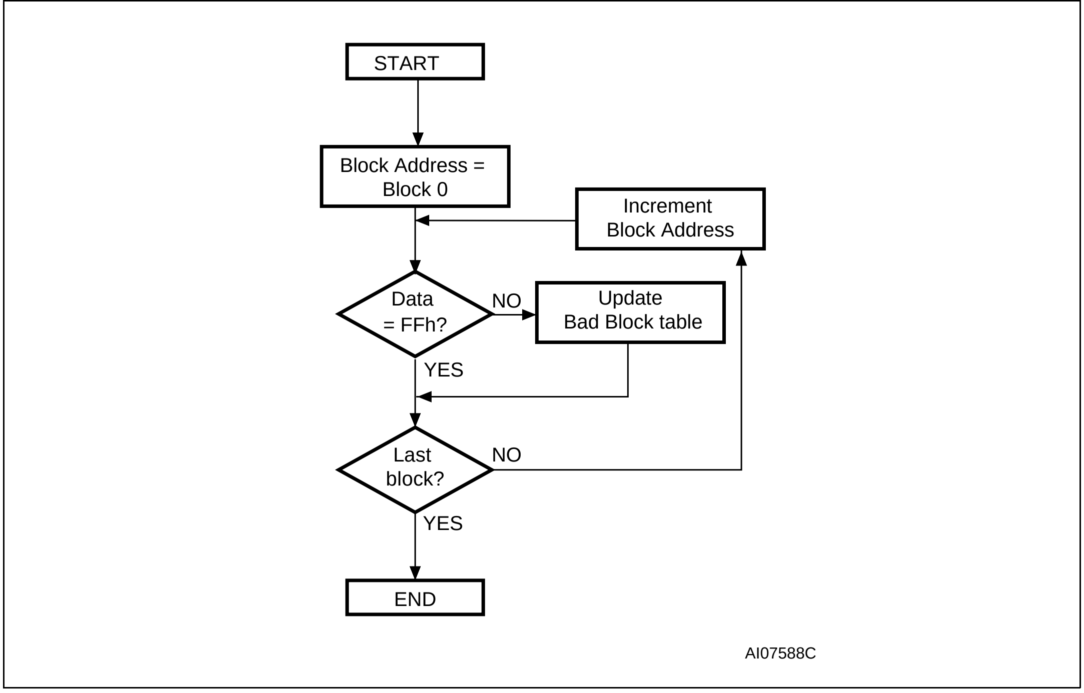
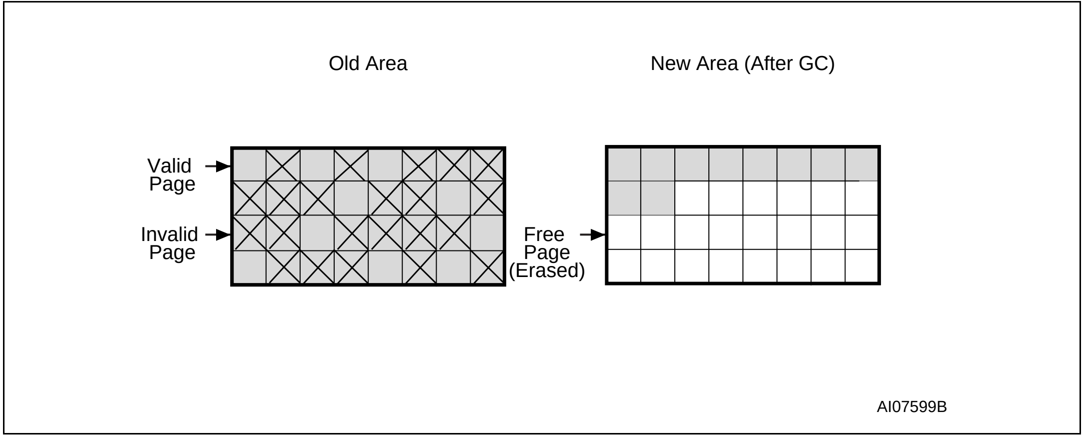


Figure 11. Garbage collection



7.3 Garbage collection

When a data page needs to be modified, it is faster to write to the first available page, and the previous page is marked as invalid. After several updates it is necessary to remove invalid pages to free some memory space.

To free this memory space and allow further program operations it is recommended to implement a Garbage Collection algorithm. In a Garbage Collection software the valid pages are copied into a free area and the block containing the invalid pages is erased (see *Figure 11*).

7.4 Wear-leveling algorithm

For write-intensive applications, it is recommended to implement a Wear-leveling Algorithm to monitor and spread the number of write cycles per block.

In memories that do not use a Wear-Leveling Algorithm not all blocks get used at the same rate.

The Wear-leveling Algorithm ensures that equal use is made of all the available write cycles for each block. There are two wear-leveling levels:

- First Level Wear-leveling, new data is programmed to the free blocks that have had the fewest write cycles
- Second Level Wear-leveling, long-lived data is copied to another block so that the original block can be used for more frequently-changed data.

The Second Level Wear-leveling is triggered when the difference between the maximum and the minimum number of write cycles per block reaches a specific threshold.

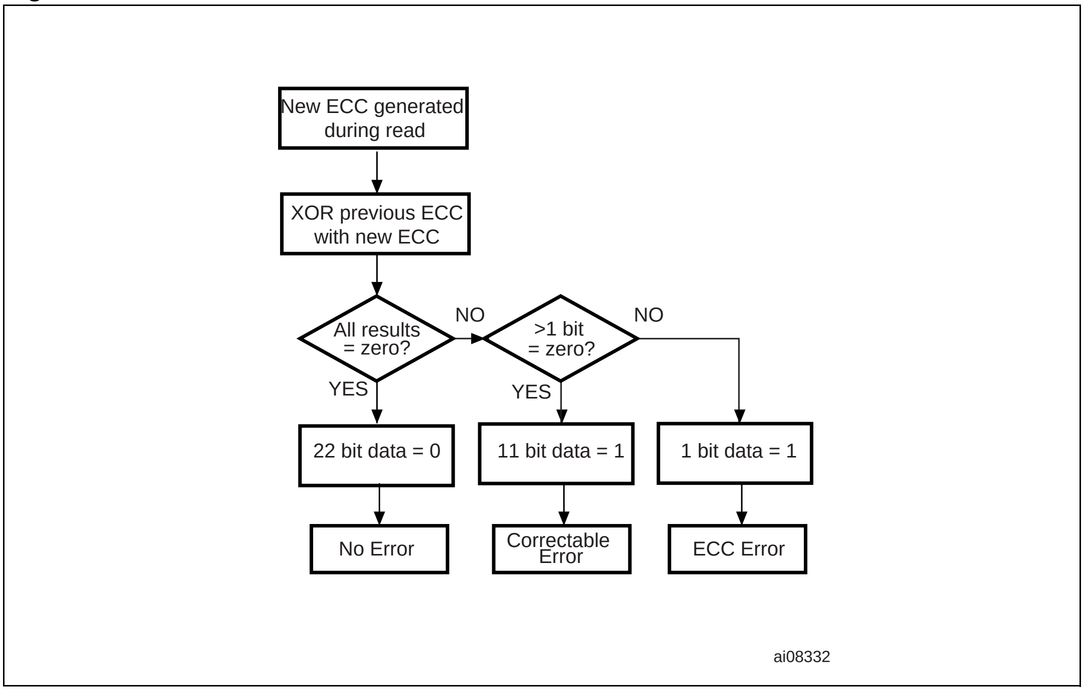
7.5 Error Correction code

An Error Correction Code (ECC) can be implemented in the Nand Flash memories to identify and correct errors in the data.

For every 2048 bits in the device it is recommended to implement 22 bits of ECC (16 bits for line parity plus 6 bits for column parity).

An ECC model is available in VHDL or Verilog. Contact the nearest Numonyx sales office for more details.

Figure 12. Error detection



8 Program and Erase times and endurance cycles

The Program and Erase times and the number of Program/ Erase cycles per block are shown in *Table 13*.

Table 13. Program, Erase Times and Program Erase endurance cycles

Parameters	NAND01GW3A2B-KGD NAND01GW4A2B-KGD			Unit
	Min	Typ	Max	
Page Program Time		200	500	µs
Block Erase Time		2	3	ms
Program/Erase Cycles (per block) (with ECC)	100,000			cycles
Data Retention	10			years

9 Maximum rating

Stressing the device above the ratings listed in *Table 14: Absolute maximum ratings*, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the Numonyx SURE Program and other relevant quality documents.

Table 14. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_{BIAS}	Temperature Under Bias	– 50	125	°C
T_{STG}	Storage Temperature	– 65	150	°C
V_{IO}(1)	Input or Output Voltage	– 0.6	4.6	V
V_{DD}	Supply Voltage	– 0.6	4.6	V

1. Minimum Voltage may undershoot to –2 V for less than 20 ns during transitions on input and I/O pins. Maximum voltage may overshoot to V_{DD} + 2 V for less than 20 ns during transitions on I/O pins.

10 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 15: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 15. Operating and AC measurement conditions

Parameter		Value		Units
		Min	Max	
Supply voltage (V_{DD})	3 V devices	2.7	3.6	V
Ambient temperature (T_A)	Grade 6	–40	85	°C
Load capacitance (C_L) (1 TTL GATE and C_L)	2.7 - 3.6 V	50		pF
	3.0 - 3.6 V	100		pF
Input pulses voltages		0.4	2.4	V
Input and output timing ref. voltages		1.5		V
Input rise and fall times		5		ns
Output circuit resistors, R_{ref}		8.35		kΩ

Table 16. Capacitance[(1)(2)]

Symbol	Parameter	Test condition	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		20	pF
$C_{I/O}$	Input/Output capacitance	V_{IL} = 0 V		20	pF

1. T_A = 25 °C, f = 1 MHz. C_{IN} and $C_{I/O}$ are not 100% tested.
2. Input/output capacitances double on stacked devices.

Figure 13. Equivalent testing circuit for AC characteristics measurement

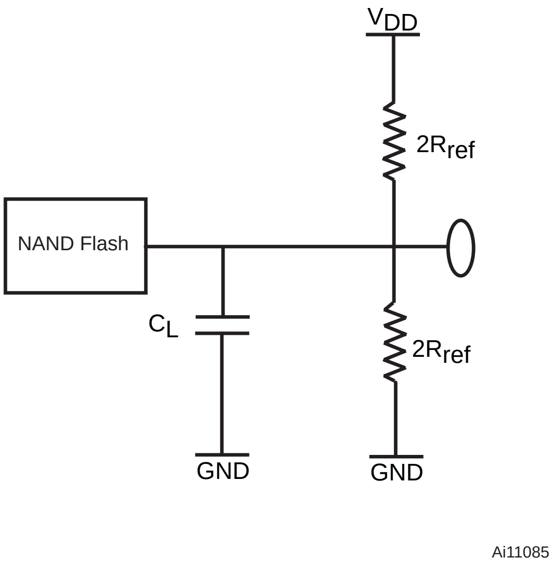


Table 17. DC characteristics(1)

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
I_{DD1}	Operating current	Sequential Read	t_{RLRL} minimum $\overline{E}=V_{IL}, I_{OUT} = 0$ mA	-	10	20	mA
I_{DD2}		Program	-	-	10	20	mA
I_{DD3}		Erase	-	-	10	20	mA
I_{DD4}	Standby current (TTL),		$\overline{E}=V_{IH}$, $\overline{WP}=0V/V_{DD}$	-	-	1	mA
I_{DD5}	Standby current (CMOS)		$\overline{E}=V_{DD}$-0.2, $\overline{WP}=0/V_{DD}$	-	20	100	µA
I_{LI}	Input Leakage current		V_{IN}= 0 to V_{DD}max	-	-	±10	µA
I_{LO}	Output Leakage current		V_{OUT}= 0 to V_{DD}max	-	-	±10	µA
V_{IH}	Input High voltage		-	0.8V_{DD}	-	V_{DD}+0.3	V
V_{IL}	Input Low voltage		-	–0.3	-	0.2V_{DD}	V
V_{OH}	Output High voltage level		I_{OH} = –400 µA	2.4	-	-	V
V_{OL}	Output Low voltage level		I_{OL} = 2.1 mA	-	-	0.4	V
I_{OL} ($R\overline{B}$)	Output Low current ($R\overline{B}$)		V_{OL} = 0.4 V	8	10		mA
V_{LKO}	V_{DD} supply voltage (Erase and Program lockout)		-	-	-	1.7	V

1. Leakage currents double on stacked devices.

Table 18. AC characteristics for command, address, data input

Symbol	Alt.	Parameter			NAND01GW3A2B-KGD, NAND01GW4A2B-KGD	Unit
t_{ALLWL}	t_{ALS}	Address Latch Low to Write Enable Low	AL Setup time	Min	0	ns
t_{ALHWL}		Address Latch High to Write Enable Low				
t_{CLHWL}	t_{CLS}	Command Latch High to Write Enable Low	CL Setup time	Min	0	ns
t_{CLLWL}		Command Latch Low to Write Enable Low				
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Data Setup time	Min	20	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	$\overline{E}$ Setup time	Min	0	ns
t_{WHALH}	t_{ALH}	Write Enable High to Address Latch High	AL Hold time	Min	10	ns
t_{WHALL}		Write Enable High to Address Latch Low				
t_{WHCLH}	t_{CLH}	Write Enable High to Command Latch High	CL hold time	Min	10	ns
t_{WHCLL}		Write Enable High to Command Latch Low				
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	Data Hold time	Min	10	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	$\overline{E}$ Hold time	Min	10	ns
t_{WHWL}	t_{WH}	Write Enable High to Write Enable Low	$\overline{W}$ High Hold time	Min	15	ns
t_{WLWH}(1)	t_{WP}	Write Enable Low to Write Enable High	$\overline{W}$ Pulse Width	Min	25(1)	ns
t_{WLWL}	t_{WC}	Write Enable Low to Write Enable Low	Write Cycle time	Min	50	ns

1. If t_{ELWL} is less than 10ns, t_{WLWH} must be minimum 35 ns, otherwise, t_{WLWH} may be minimum 25 ns.

Table 19. AC characteristics for operations

Symbol	Alt.	Parameter			NAND01GW3A2B-KGD, NAND01GW4A2B-KGD	Unit
t_{ALLRL1}	t_{AR}	Address Latch Low to Read Enable Low	Read Electronic Signature	Min	10	ns
t_{ALLRL2}			Read cycle	Min	10	ns
t_{BHRL}	t_{RR}	Ready/Busy High to Read Enable Low		Min	20	ns
t_{BLBH1}		Ready/Busy Low to Ready/Busy High	Read Busy time	Max	15	µs
t_{BLBH2}	t_{PROG}		Program Busy time	Max	500	µs
t_{BLBH3}	t_{BERS}		Erase Busy time	Max	3	ms
t_{BLBH4}	t_{RST}	Write Enable High to Ready/Busy High	Reset Busy time, during ready	Max	5	µs
			Reset Busy time, during read	Max	5	µs
			Reset Busy time, during program	Max	10	µs
			Reset Busy time, during erase	Max	500	µs
t_{CLLRL}	t_{CLR}	Command Latch Low to Read Enable Low		Min	10	ns
t_{DZRL}	t_{IR}	Data Hi-Z to Read Enable Low		Min	0	ns
t_{EHQZ}	t_{CHZ}	Chip Enable High to Output Hi-Z		Max	20	ns
t_{ELQV}	t_{CEA}	Chip Enable Low to Output Valid		Max	45	ns
t_{RHRL}	t_{REH}	Read Enable High to Read Enable Low	Read Enable High Hold time	Min	15	ns
t_{RHQZ}	t_{RHZ}	Read Enable High to Output Hi-Z		Max	30	ns
t_{EHQX}	T_{OH}	Chip Enable high or Read Enable high to Output Hold		Min	10	ns
t_{RHQX}						
t_{RLRH}	t_{RP}	Read Enable Low to Read Enable High	Read Enable Pulse Width	Min	25	ns
t_{RLRL}	t_{RC}	Read Enable Low to Read Enable Low	Read Cycle time	Min	50	ns
t_{RLQV}	t_{REA}	Read Enable Low to Output Valid	Read Enable Access time	Max	30	ns
			Read ES Access time(1)			
t_{WHBH}	t_{R}	Write Enable High to Ready/Busy High	Read Busy time	Max	15	µs
t_{WHBL}	t_{WB}	Write Enable High to Ready/Busy Low		Max	100	ns
t_{WHRL}	t_{WHR}	Write Enable High to Read Enable Low		Min	60	ns

Table 19. AC characteristics for operations (continued)

Symbol	Alt.	Parameter			NAND01GW3A2B-KGD, NAND01GW4A2B-KGD	Unit
t_{WLWL}	t_{WC}	Write Enable Low to Write Enable Low	Write Cycle time	Min	50	ns
t_{VHWH}, t_{VLWH}(2)	t_{WW}	Write Protection time		Min	100	ns

1. ES = Electronic Signature.
2. During a Program/Erase Enable Operation, t_{VHWH} is the delay from $\overline{WP}$ high to $\overline{W}$ High.
During a Program/Erase Disable Operation, t_{VLWH} is the delay from $\overline{WP}$ Low to $\overline{W}$ High.

Figure 14. Command Latch AC waveforms

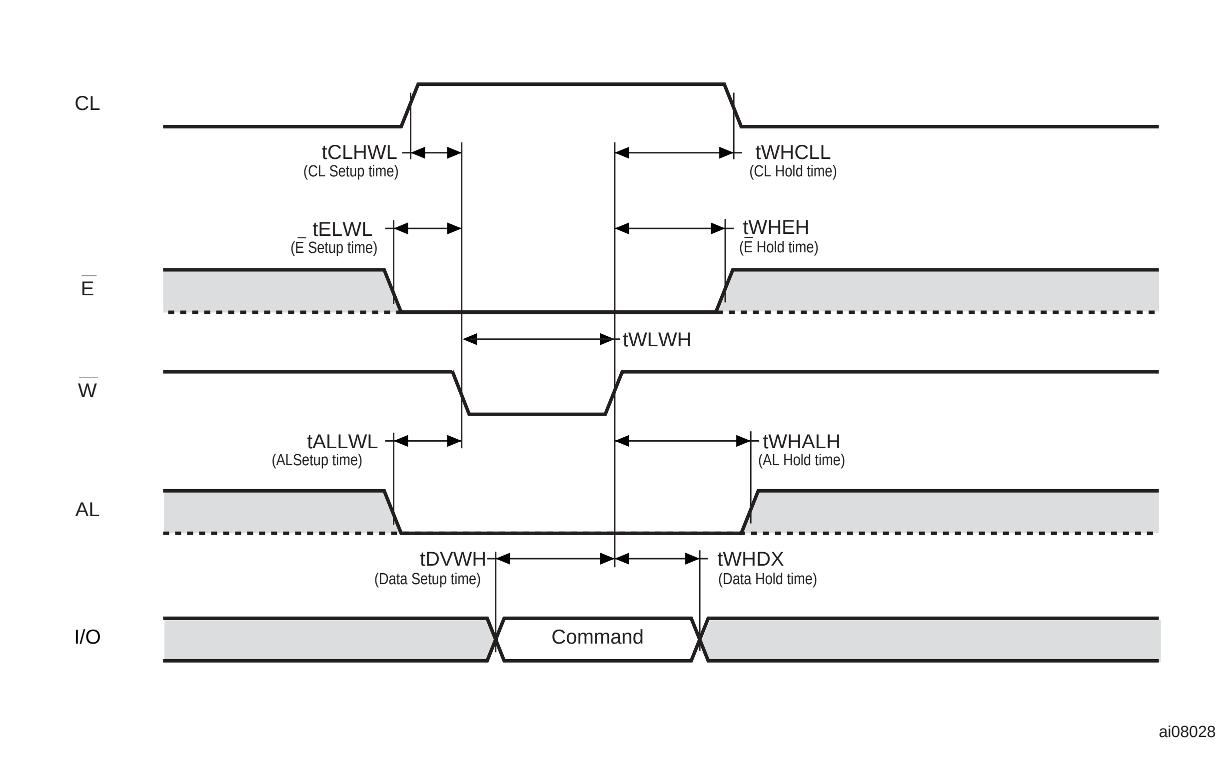


Figure 15. Address Latch AC waveforms

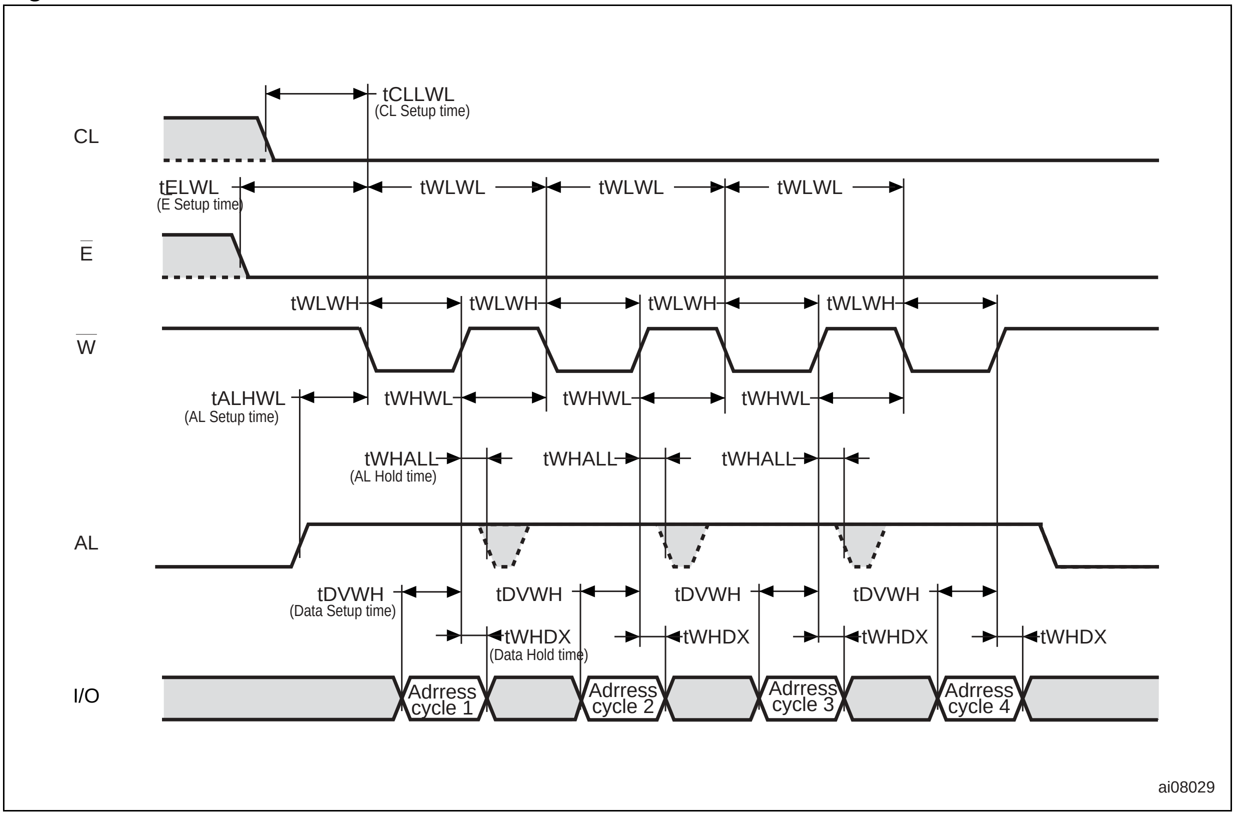


Figure 16. Data Input Latch AC waveforms

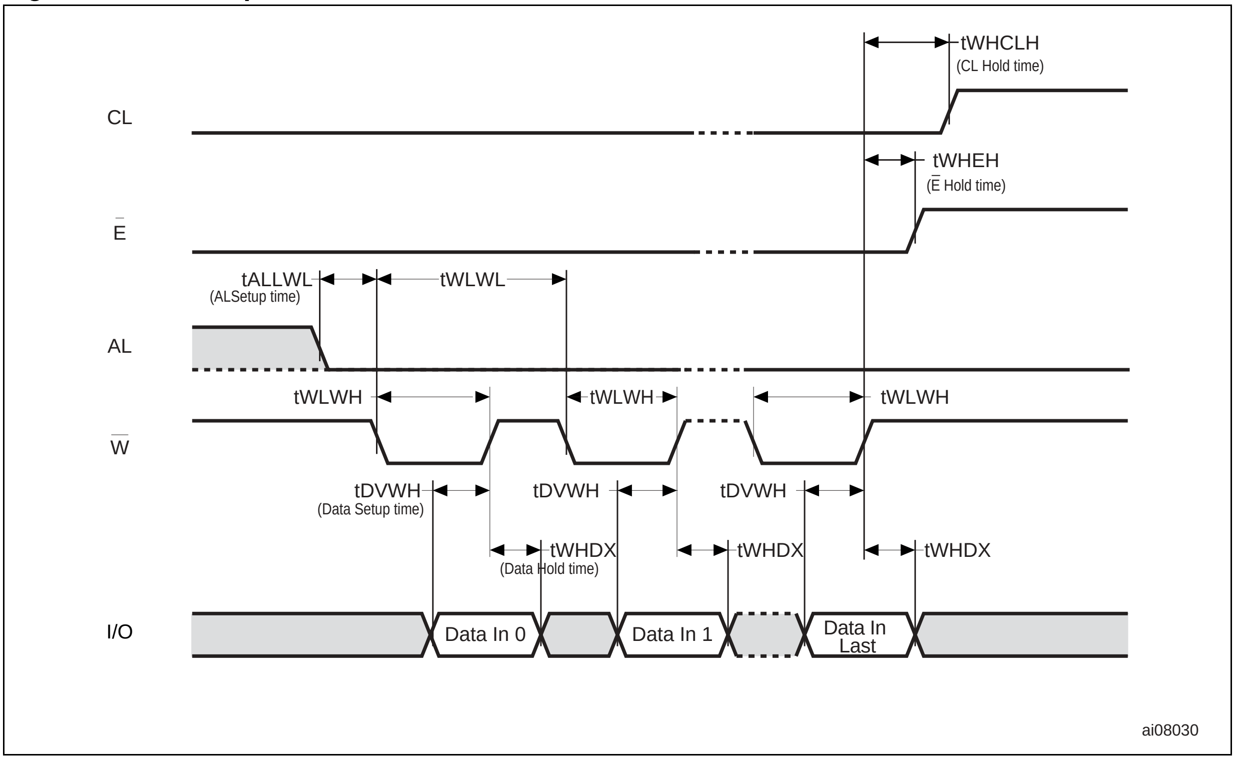
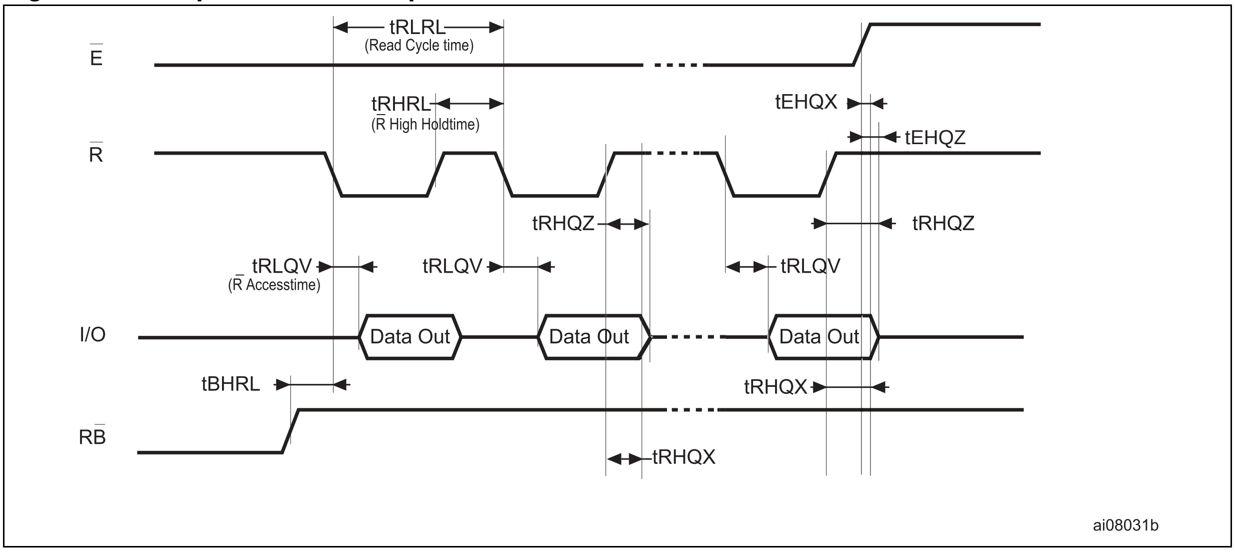


Figure 17. Sequential Data Output after Read AC waveforms



1. CL = Low, AL = Low, $\overline{W}$ = High.

Figure 18. Read Status Register AC waveform

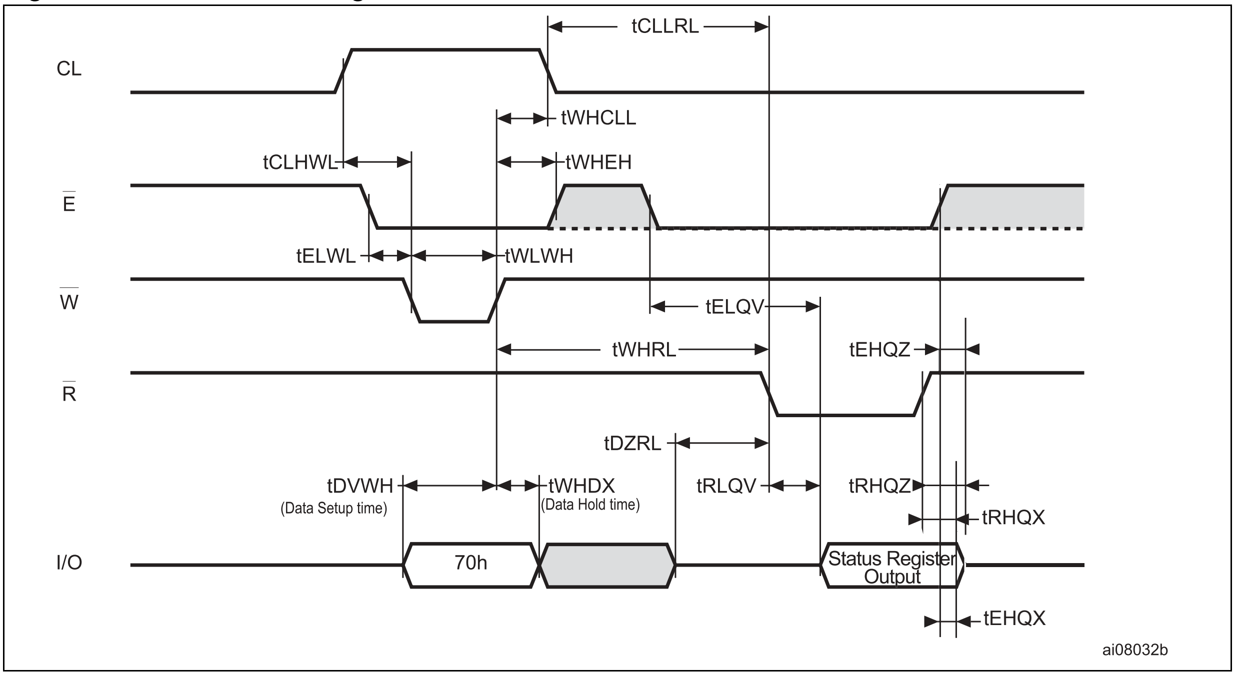
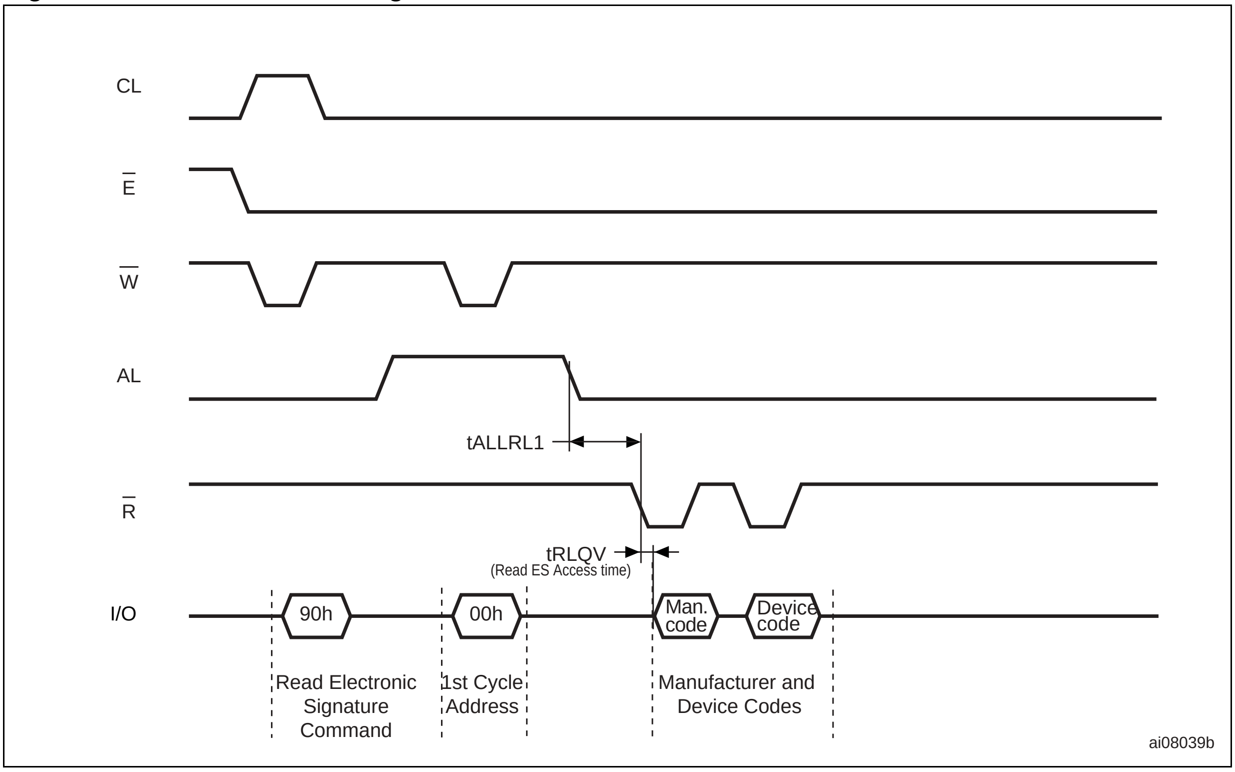


Figure 19. Read Electronic Signature AC waveform



1. Refer to *Table 11* for the values of the Manufacturer and Device Codes.

Figure 20. Page Read A/ Read B Operation AC waveform

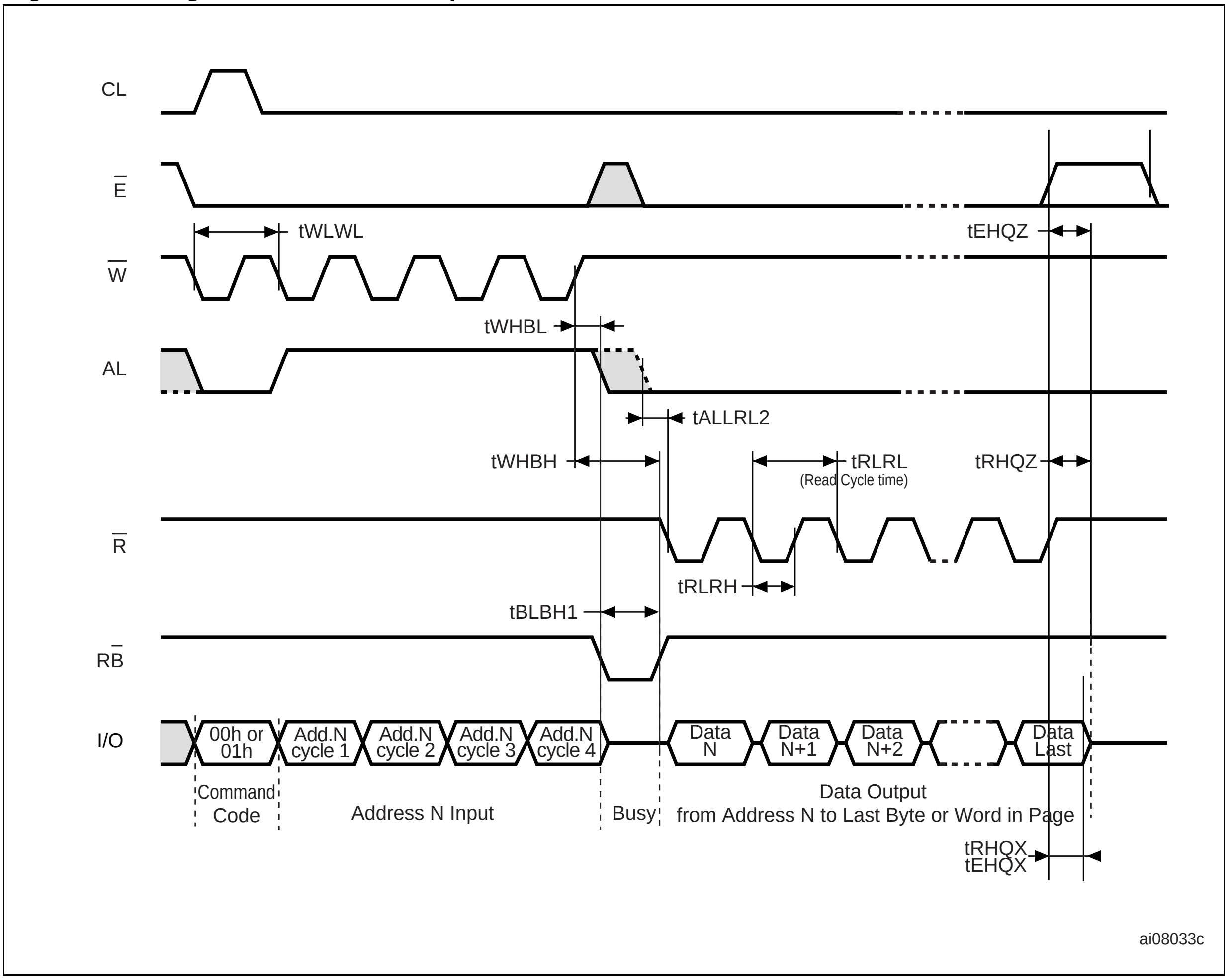
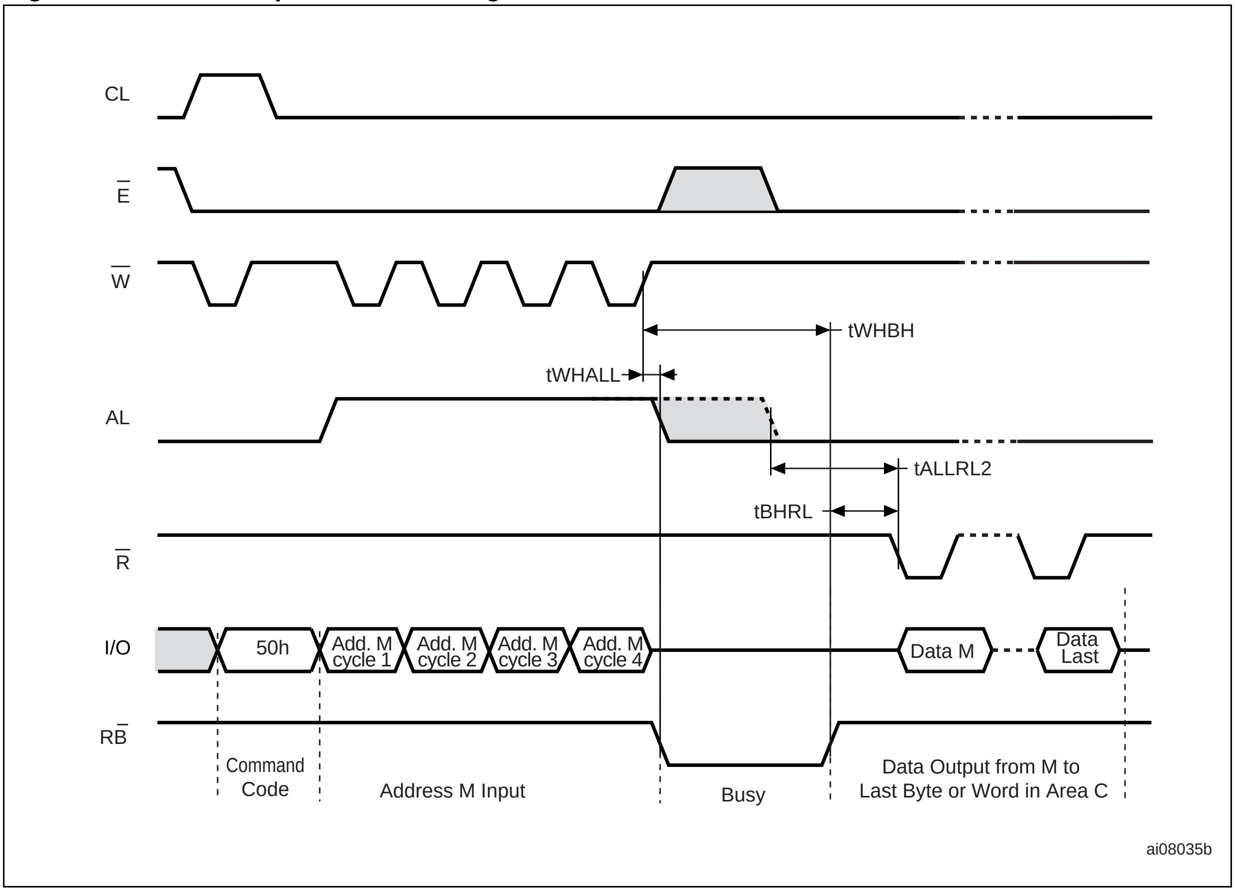


Figure 21. Read C Operation, One Page AC waveform



1. A0-A7 is the address in the Spare Memory area, where A0-A3 are valid and A4-A7 are 'Don't care'.

Figure 22. Page Program AC waveform

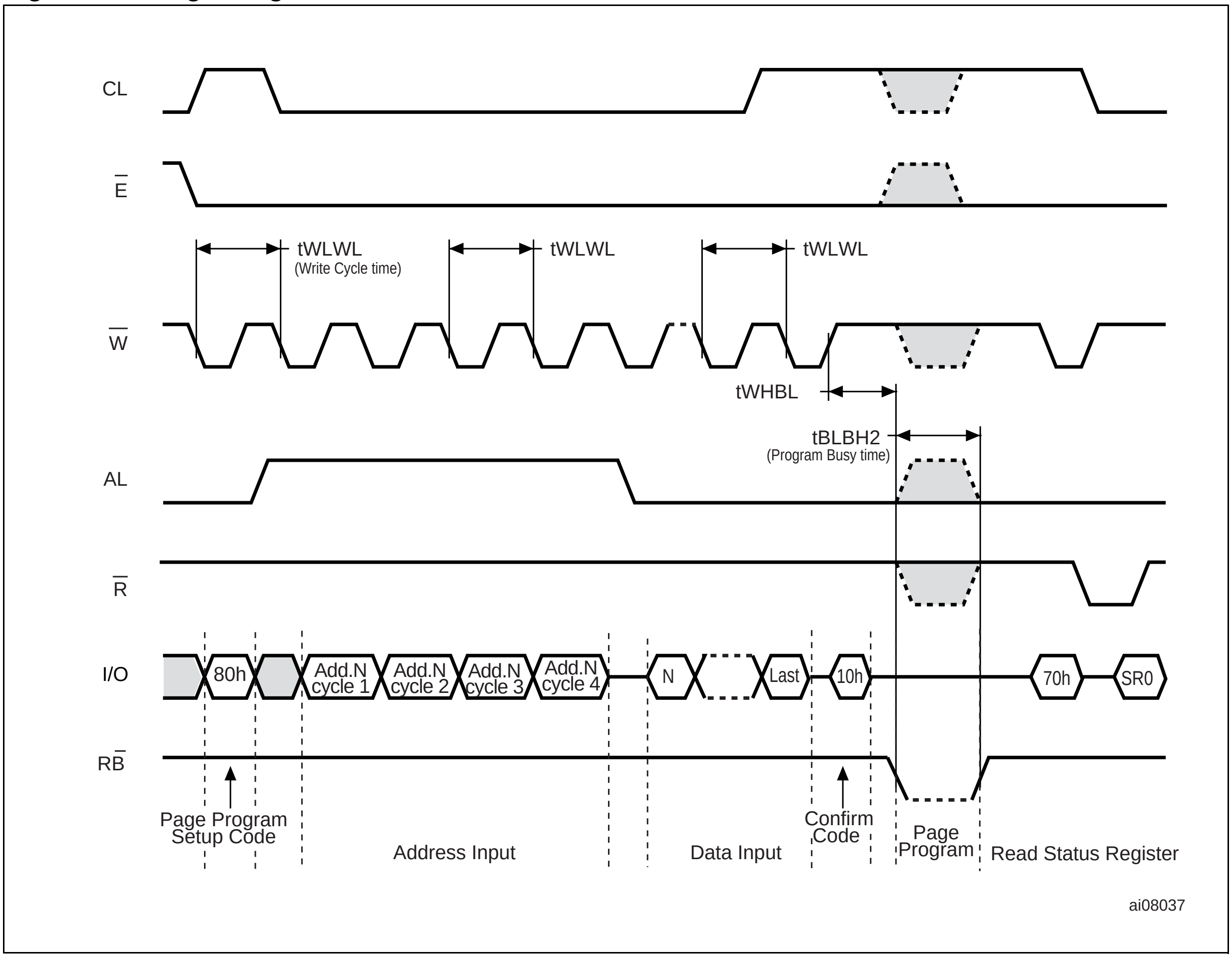


Figure 23. Block Erase AC waveform

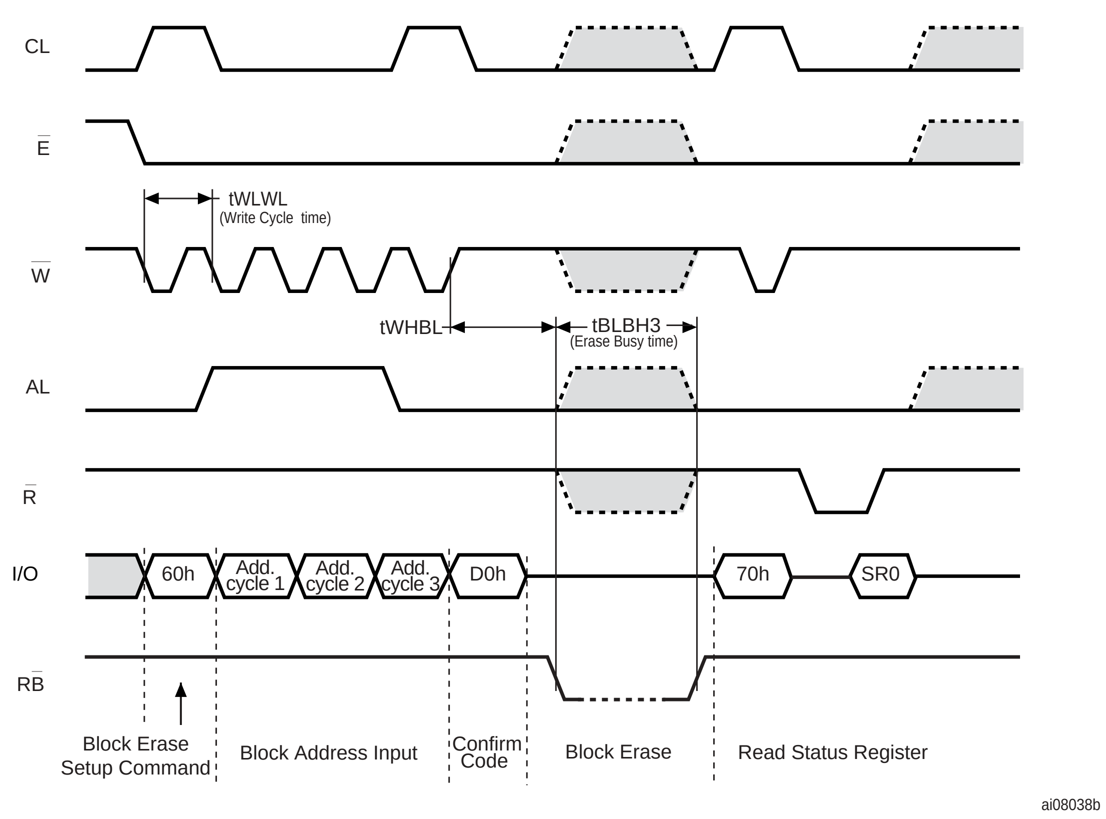


Figure 24. Reset AC waveform

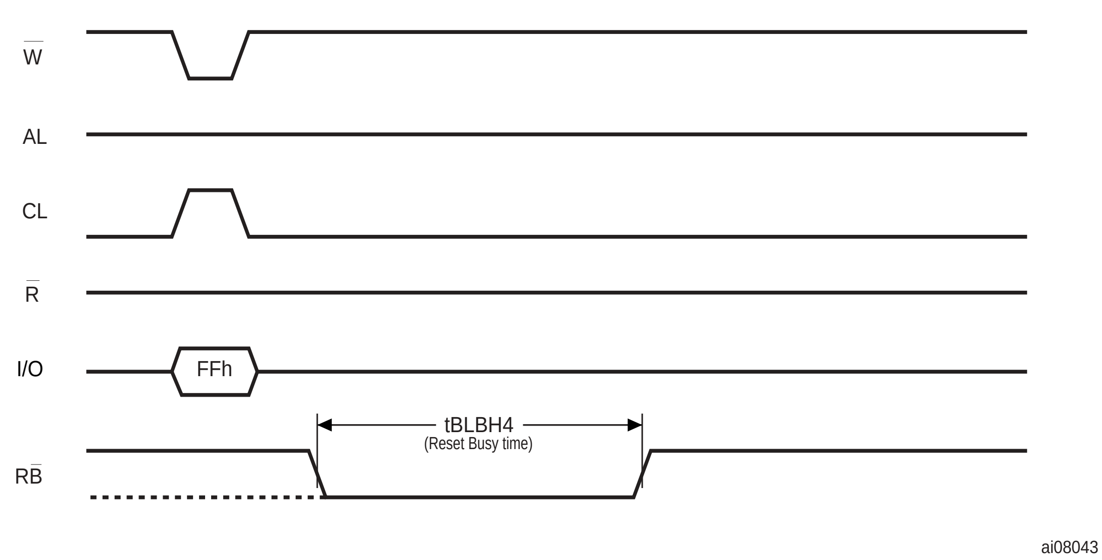


Figure 25. Program/Erase Enable waveform

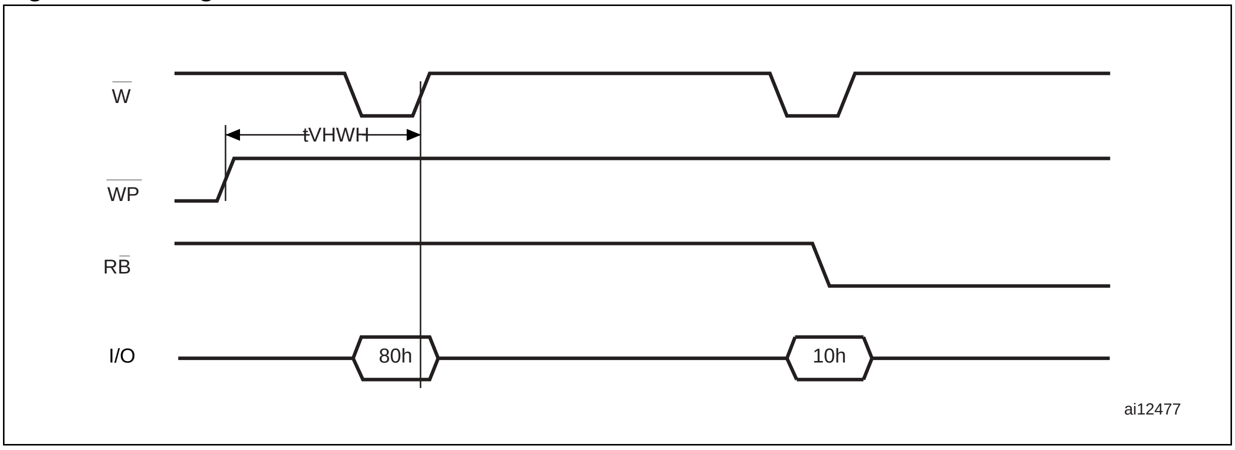
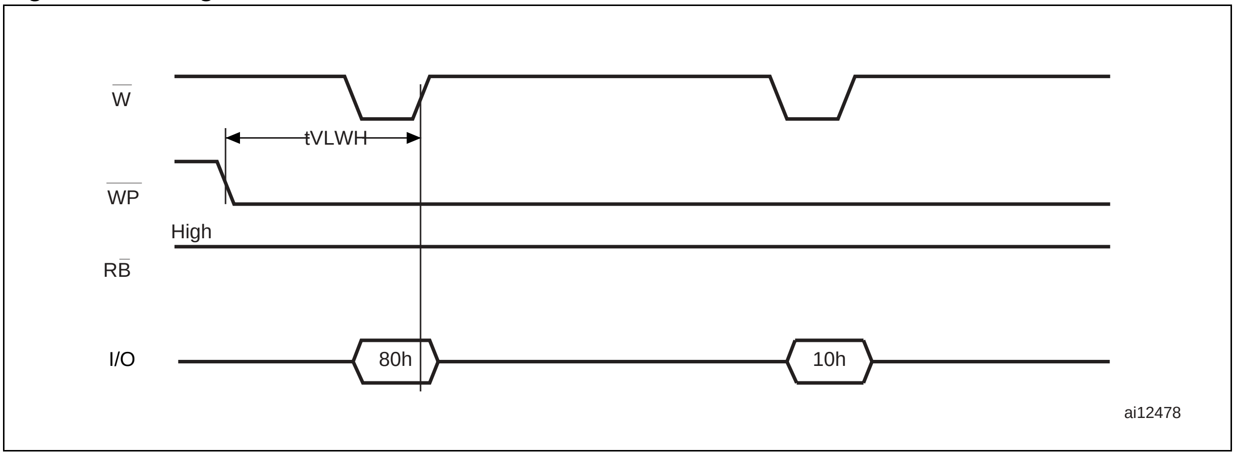


Figure 26. Program/Erase Disable waveform



10.1 Ready/Busy signal electrical characteristics

Figure 28, *Figure 27* and *Figure 29* show the electrical characteristics for the Ready/Busy signal. The value required for the resistor R_P can be calculated using the following equation:

$$R_P min = \frac{(V_{DDmax} - V_{OLmax})}{I_{OL} + I_L}$$

So,

$$R_P min(1.8V) = \frac{1.85V}{3mA + I_L}$$

$$R_P min(3V) = \frac{3.2V}{8mA + I_L}$$

where I_L is the sum of the input currents of all the devices tied to the Ready/Busy signal. R_P max is determined by the maximum value of t_r.

Figure 27. Ready/Busy AC waveform

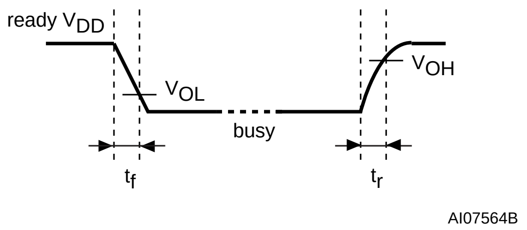


Figure 28. Ready/Busy load circuit

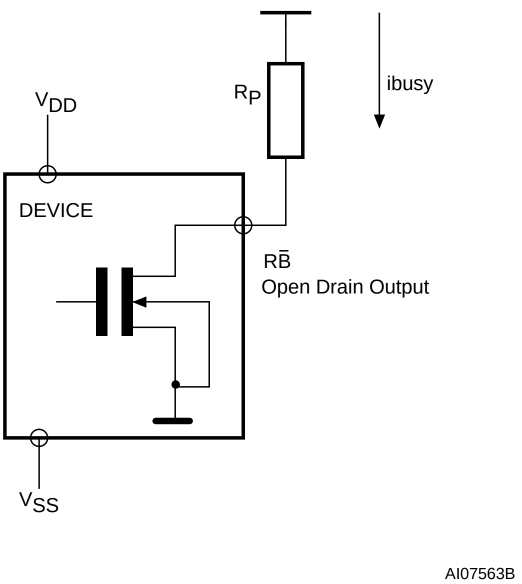
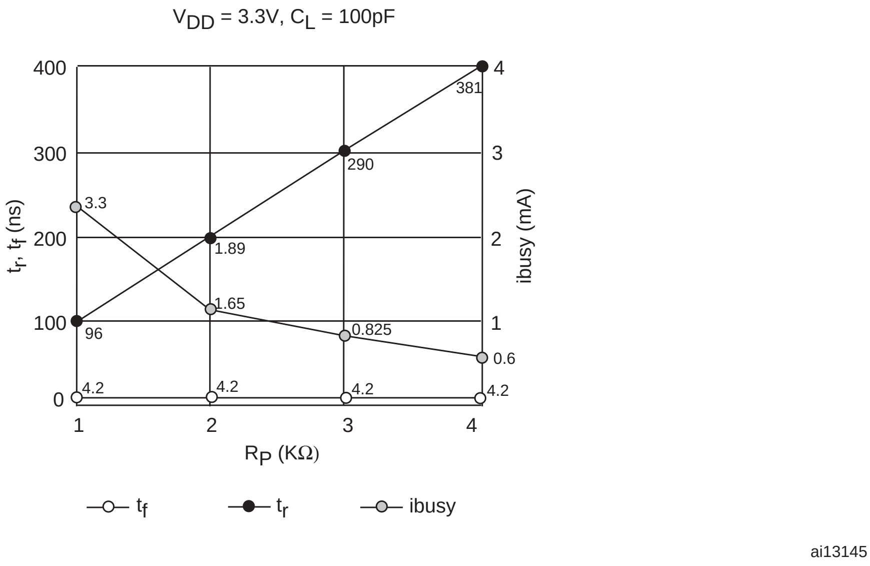


Figure 29. Resistor value versus waveform timings for Ready/Busy signal



1. T = 25°C.

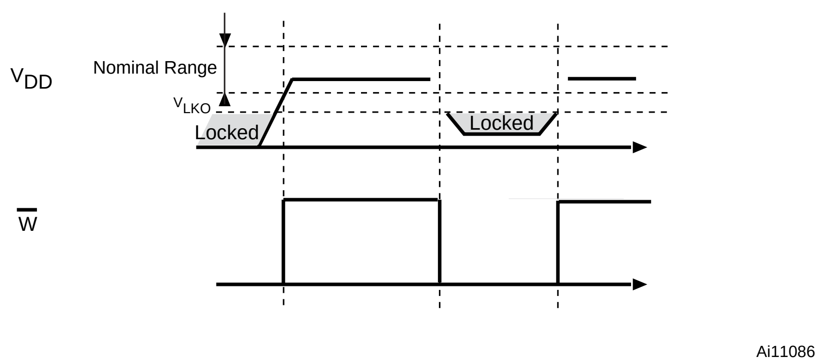
10.2 Data Protection

The Numonyx NAND device is designed to guarantee Data Protection during Power Transitions.

A V_{DD} detection circuit disables all NAND operations, if V_{DD} is below the V_{LKO} threshold.

In the V_{DD} range from V_{LKO} to the lower limit of nominal range, the $\overline{WP}$ pin should be kept low (V_{IL}) to guarantee hardware protection during power transitions as shown in the below figure.

Figure 30. Data protection



11 Ordering information

Table 20. Ordering Information Scheme

Example: NAND01GW3A 2 B E0 6

Device Type

NAND = NAND Flash memory

Density

01G = 1 Gb

Operating voltage

W = V_{DD} = 2.7 to 3.6 V

Bus width

3 = x 8

4 = x 16

Family identifier

A = 528 bytes/ 264 word page

Device options

2 = Chip Enable Don’t Care Enabled

Product version

B = Second version

Package

E0 = Unsawn wafer

Temperature range

6 = –40 to 85 °C

Devices are shipped from the factory with the memory content bits, in valid blocks, erased to ’1’.
For further information on any aspect of this device, please contact your nearest Numonyx Sales Office.

12 Revision history

Table 21. Document revision history

Date	Revision	Changes
10-Aug-2006	0.1	Initial release.
24-Aug-2006	1	Datasheet status updated to Preliminary data. Confidentiality level changed from Restricted Distribution to public.
18-May-2007	2	Datasheet status upgraded to ‘Full datasheet’. Data integrity of 100,000 specified for ECC implemented. Section 7.2 Block replacement replaced by *Section 7.2: NAND Flash memory failure modes*. t_{WHBH1} removed from *Table 21: AC Characteristics for operations*.
04-Jan-2008	3	Applied Numonyx branding.