NCS2566

Six-Channel Video Driver with Triple SD & Triple Selectable SD/HD Filters

The NCS2566 integrates reconstruction filters and video amplifiers. It's a combination of two 3−channel drivers − the first one capable to deal with Standard Definition (SD) video signals and a second one including selectable filters for either Standard or High Definition (HD) video applications. The filters implemented are 6^{th} order Butterworth Low Pass filters particularly effective for rejecting unwanted high frequency components and assuring good linearity of the phase change over frequency with well optimized group delays.

All channels can accept DC− or AC−coupled signals; when AC−coupled the internal clamps are employed. The outputs can drive both AC− and DC−coupled 150 Ω loads.

It is designed to be compatible with most Digital−to−Analog Converters (DAC) embedded in video processors. To further reduce power consumption, two enable pins are provided, one for each triple driver. One pin allows selection of the filter frequency of the SD/HD triple driver.

Features

- 3−Channel with Selectable 6^{th}−Order 8/34 MHz Butterworth Filters
- 3−Channel with Fixed 6^{th}−Order 8 MHz Butterworth Filters
- Transparent Input Clamp for Each Channel
- Integrated Level Shifter
- AC− or DC−Coupled Inputs and Outputs
- Low Quiescent Current
- Shutdown Current 42 μA Typical (Disabled)
- 5 V Power Supply
- Each Channel Capable to Drive 2 by 150 Ω Load
- Internal Gain: 6 dB ± 0.2
- Wide Input Common Mode Range
- 8 kV ESD Protection (IEC61000−4−2 Compatible)
- Operating Temperature Range: −40°C to +85°C
- Available in a TSSOP−20 Package
- These are Pb−Free Devices

Typical Applications

- Set−Top Box
- DVD players and related
- HDTV

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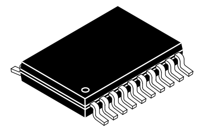
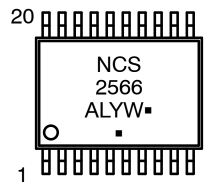


TSSOP−20
DTB SUFFIX
CASE 948E

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS

SD IN1	1	20	SD OUT1
SD IN2	2	19	SD OUT2
SD IN3	3	18	SD OUT3
SD $\overline{EN}$	4	17	GND
VCC	5	16	GND
$\overline{SD}$/HD	6	15	SD/HD $\overline{EN}$
SD/HD IN1	7	14	SD/HD OUT1
SD/HD IN2	8	13	SD/HD OUT2
SD/HD IN3	9	12	SD/HD OUT3
NC	10	11	NC

(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

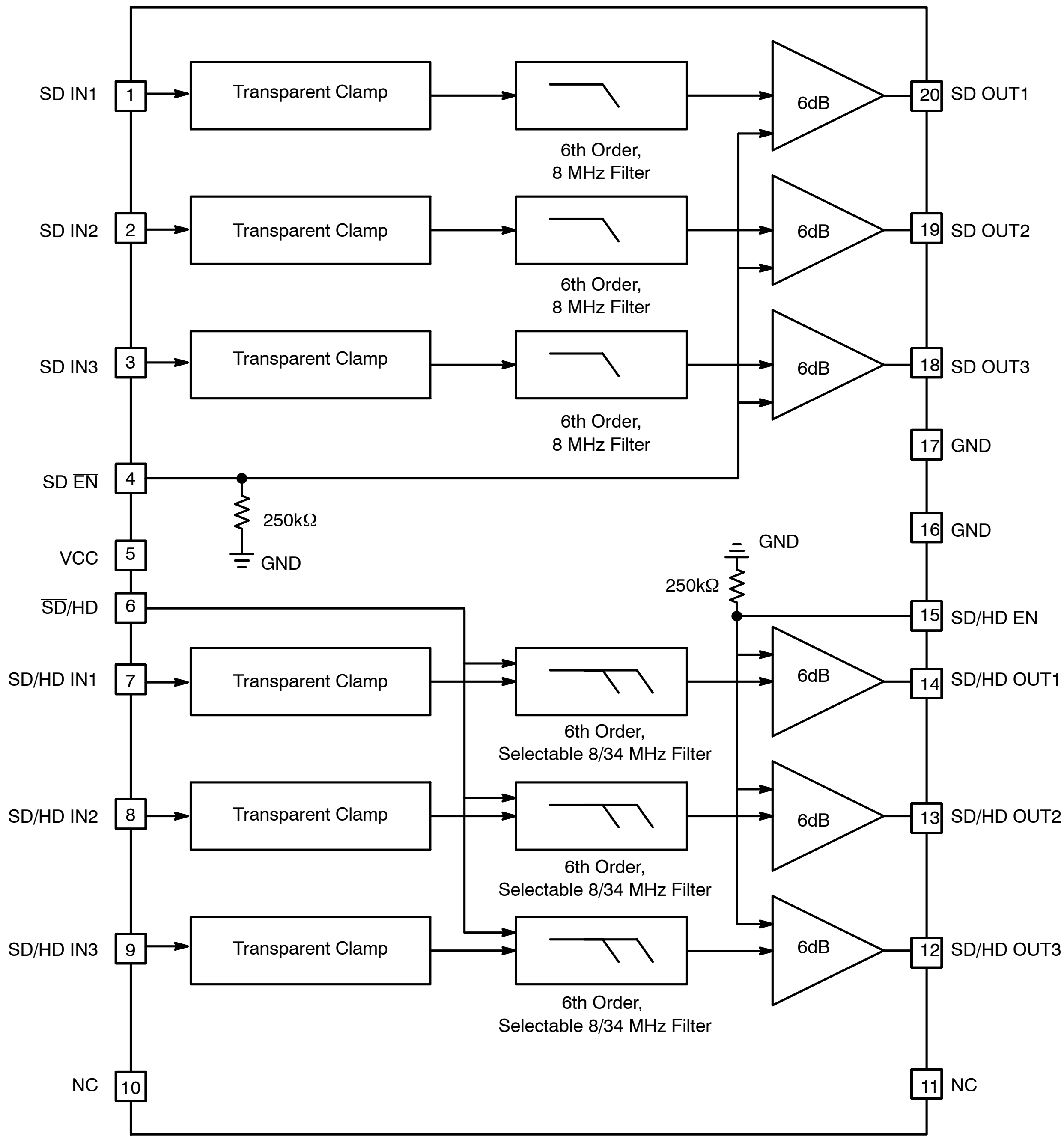


Figure 1. NCS2566 Block Diagram

PIN FUNCTION AND DESCRIPTION

Pin	Name	Type	Description
1	SD IN1	Input	SD Video Input 1 − SD Channel 1
2	SD IN2	Input	SD Video Input 2 − SD Channel 2
3	SD IN3	Input	SD Video Input 3 − SD Channel 3
4	SD $\overline{EN}$	Input	SD−Channel Enable/Disable Function: Low = Enable, High = Disable. When left open the default state is Enable.
5	VCC	Power	Device Power Supply Voltage: +5 V ±5%
6	$\overline{SD}$/HD	Input	Pin of selection enabling the Standard Definition or High Definition Filters (8 MHz / 34 MHz) for channels SD/HD (pins 7−14, 8−13 & 9−12) − when Low SD filters are selected, when High HD filters are selected.
7	SD/HD IN1	Input	Selectable SD or HD Video Input 1 − SD/HD Channel 1
8	SD/HD IN2	Input	Selectable SD or HD Video Input 2 − SD/HD Channel 2
9	SD/HD IN3	Input	Selectable SD or HD Video Input 3 − SD/HD Channel 3
10	NC	Open	Not Connected
11	NC	Open	Not Connected
12	SD/HD OUT3	Output	SD/HD Video Output 3 − SD/HD Channel 3
13	SD/HD OUT2	Output	SD/HD Video Output 2 − SD/HD Channel 2
14	SD/HD OUT1	Output	SD/HD Video Output 1 − SD/HD Channel 1
15	SD/HD $\overline{EN}$	Input	SD/HD Channel Enable /Disable Function: Low = Enable, High = Disable. When left open the default state is Enable.
16	GND	GND	Connected to Ground
17	GND	GND	Connected to Ground
18	SD OUT3	Output	SD Video Output 3 − SD Channel 3
19	SD OUT2	Output	SD Video Output 2 − SD Channel 2
20	SD OUT1	Output	SD Video Output 1 − SD Channel 1

MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power Supply Voltages	V_{CC}	$-0.3 \le V_{CC} \le 5.5$	Vdc
Input Voltage Range	V_I	$-0.3 \le V_I \le V_{CC}$	Vdc
Input Differential Voltage Range	V_{ID}	$-0.3 \le V_I \le V_{CC}$	Vdc
Output Current Per Channel	I_O	50	mA
Maximum Junction Temperature (Note 1)	T_J	150	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
Power Dissipation	P_D	(See Graph)	mW
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	125	°C/W
ESD Protection Voltage	V_{esd}	>8000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 150°C. If the maximum is exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the “overheated” condition for an extended period can result in device burnout. To ensure proper operation, it is important to observe the derating curves.

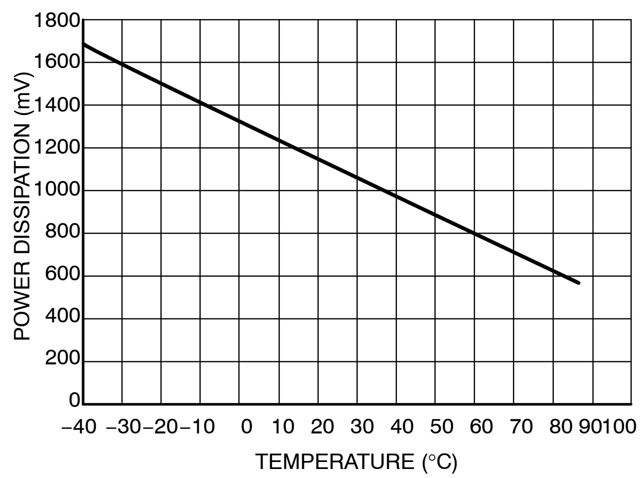


Figure 2. Power Dissipation vs Temperature

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, R_{source} = 37.5 Ω, T_A = 25°C, inputs AC−coupled with 0.1 μF, all outputs AC−coupled with 220 μF into 150 Ω referenced to 400 kHz; unless otherwise specified)

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
V_{CC}	Supply Voltage Range		4.7	5.0	5.3	V
I_{CC}	Supply Current	3 SD Channels Active 3 HD Channels Active 3 SD + 3 SD Channels Active 3 SD + 3 HD Channels Active		25 40 50 65	 80	mA
I_{SD}	Shutdown Current	No Channel Active		42	80	μA
DC PERFORMANCE						
V_i	Input Common Mode Voltage Range		GND		1.4	V_{PP}
V_{IL}	$\overline{SD}$/HD Input Low Level		0		0.8	V
V_{IH}	$\overline{SD}$/HD Input High Level		2.4		V_{CC}	V
R_{pd}	Pulldown Resistors on Pins SD_$\overline{EN}$ and SD/HD_$\overline{EN}$			250		kΩ
OUTPUT CHARACTERISTICS						
V_{OH}	Output Voltage High Level			2.8		V
V_{OL}	Output Voltage Low Level			200		mV
I_O	Output Current			40		mA

AC ELECTRICAL CHARACTERISTICS FOR STANDARD DEFINITION CHANNELS (Pin Numbers (1, 20) (2, 19), (3, 18), (7, 14), (8, 13) & (9, 12)) (V_{CC} = +5.0 V, V_{in} = 1 V_{PP}, R_{source} = 37.5 Ω, T_A = 25°C, Inputs AC−coupled with 0.1 μF, All Outputs AC−coupled with 220 μF into 150 Ω Referenced to 400 kHz; unless otherwise specified, $\overline{SD}$/HD = Low)

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
A_{VSD}	Voltage Gain	V_{in} = 1 V − All SD Channels	5.8	6.0	6.2	dB
BW_{SD}	Low Pass Filter Bandwidth (Note 3)	−1 dB −3 dB	5.5 6.5	7.2 8.0		MHz
A_{RSD}	Stop−Band Attenuation (Note 4)	@ 27 MHz	43	50		dB
dG_{SD}	Differential Gain Error			0.7		%
$d\Phi_{SD}$	Differential Phase Error			0.7		°
THD	Total Harmonic Distortion	V_{out} = 1.4 V_{PP} @ 3.58 MHz		0.35		%
X_{SD}	Channel−to−Channel Crosstalk	@ 1 MHz & V_{in} = 1.4 V_{PP}		−58		dB
SNR_{SD}	Signal−to−Noise Ratio	NTC−7 test signal, 100 kHz to 4.2 MHz (Note 2)		72		dB
Δt_{SD}	Propagation Delay	@ 4.5 MHz		70		ns
ΔGD_{SD}	Group Delay variation	100 kHz to 8 MHz		20		ns

2. SNR = 20 x log (714 mV/RMS Noise)
3. 100% of Tested ICs fit the bandwidth and attenuation tolerance at 25°C.
4. Guaranteed by Characterization.

AC ELECTRICAL CHARACTERISTICS FOR HIGH DEFINITION CHANNELS (Pin Numbers (7, 14), (8, 13) & (9, 12)) (V_{CC} = +5.0 V, V_{in} = 1 V_{PP}, R_{source} = 37.5 Ω, T_A = 25°C, Inputs AC−coupled with 0.1 μF, All Outputs AC−coupled with 220 μF into 150 Ω Referenced to 400 kHz; unless otherwise specified, $\overline{SD}$/HD = High)

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
A_{VHD}	Voltage Gain	V_{in} = 1 V – All HD Channels	5.8	6.0	6.2	dB
BW_{HD}	Low Pass Filter Bandwidth	−1 dB (Note 6) −3 dB (Note 7)	26 30	31 34		MHz
A_{RHD}	Stop−band Attenuation	@ 44.25 MHz (Note 7) @ 74.25 MHz (Note 6)	 33	15 42		dB
THD_{HD}	Total Harmonic Distortion	V_{out} = 1.4 V_{PP} @ 10 MHz V_{out} = 1.4 V_{PP} @ 15 MHz V_{out} = 1.4 V_{PP} @ 22 MHz		0.4 0.6 0.8		%
X_{HD}	Channel−to−Channel Crosstalk	@ 1 MHz & V_{in} = 1.4 V_{PP}		−58		dB
SNR_{HD}	Signal−to−Noise Ratio	white signal, 100 kHz to 30 MHz, (Note 5)		72		dB
Δt_{HD}	Propagation Delay			25		ns
ΔGD_{HD}	Group Delay Variation from	100 kHz to 30 MHz		6.0		ns

5. SNR = 20 x log (714 mV/RMS Noise)
6. Guaranteed by characterization.
7. 100% of tested ICs fit the bandwidth and attenuation tolerance at 25°C.

TYPICAL CHARACTERISTICS

V_{CC} = +5.0 V, V_{in} = 1 V_{PP}, R_{source} = 37.5 Ω, T_A = 25°C, Inputs AC−coupled with 0.1 μF, All Outputs AC−coupled with 220 μF into 150 Ω
Referenced to 400 kHz; unless otherwise specified

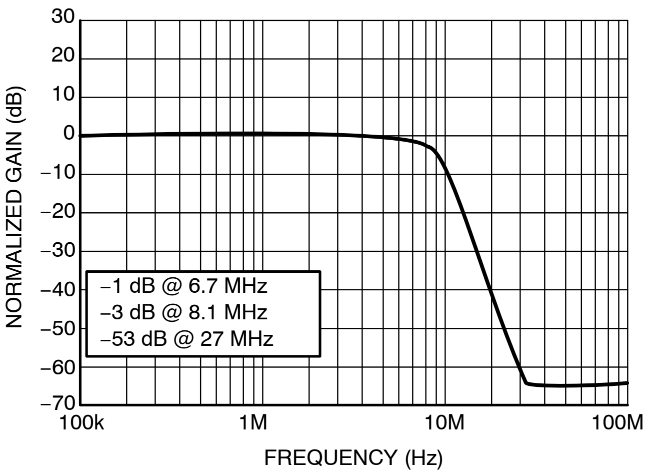


Figure 3. SD Normalized Frequency Response

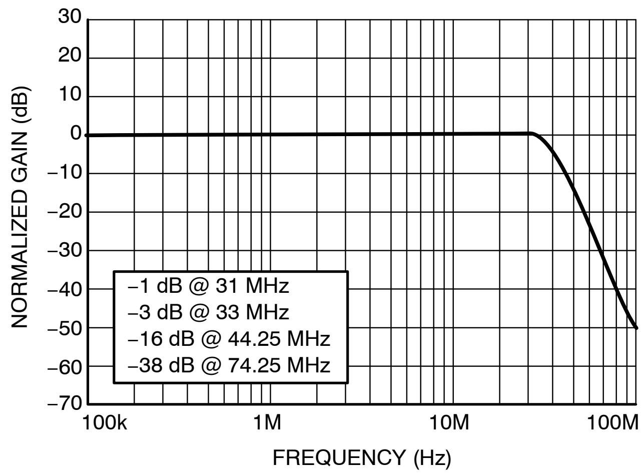


Figure 4. HD Normalized Frequency Response

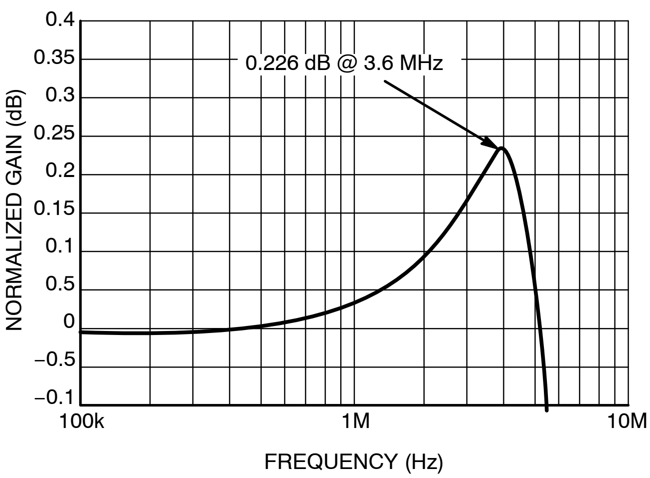


Figure 5. SD Passband Flatness

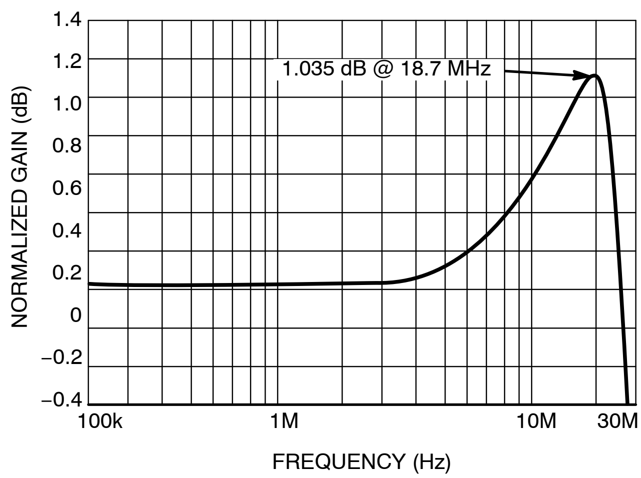


Figure 6. HD Passband Flatness

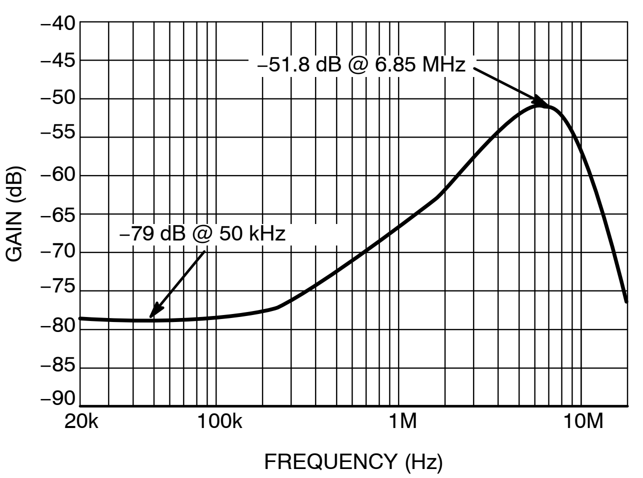


Figure 7. SD Channel−to−Channel Crosstalk

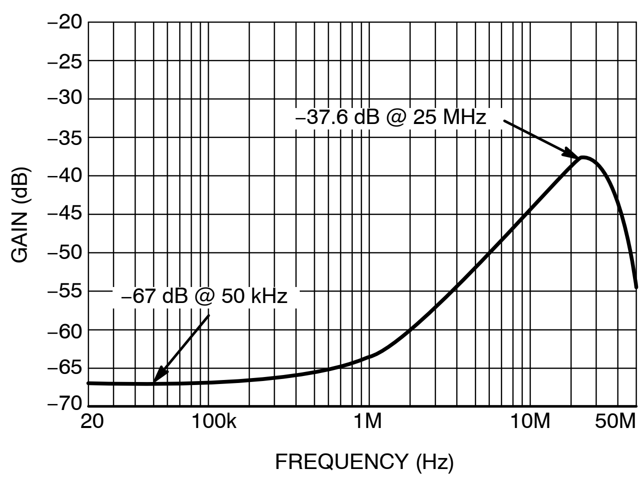


Figure 8. HD Channel−to−Channel Crosstalk

TYPICAL CHARACTERISTICS

V_{CC} = +5.0 V, V_{in} = 1 V_{PP}, R_{source} = 37.5 Ω, T_A = 25°C, Inputs AC−coupled with 0.1 μF, All Outputs AC−coupled with 220 μF into 150 Ω
Referenced to 400 kHz; unless otherwise specified

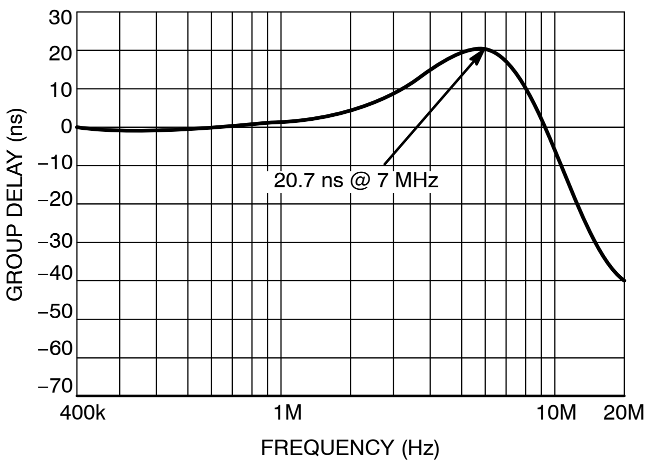


Figure 9. SD Normalized Group Delay

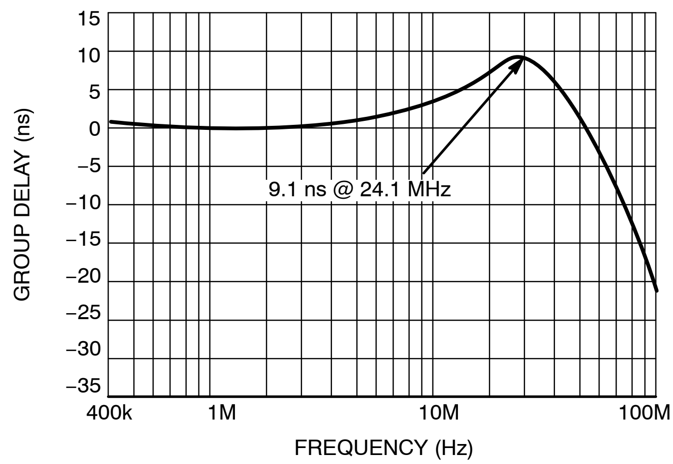


Figure 10. HD Normalized Group Delay

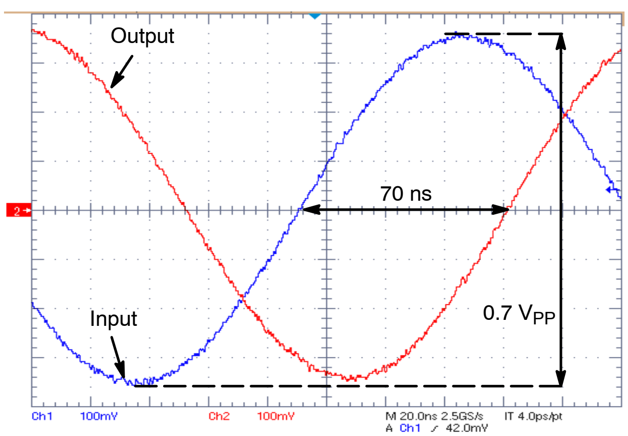


Figure 11. SD Propagation Delay

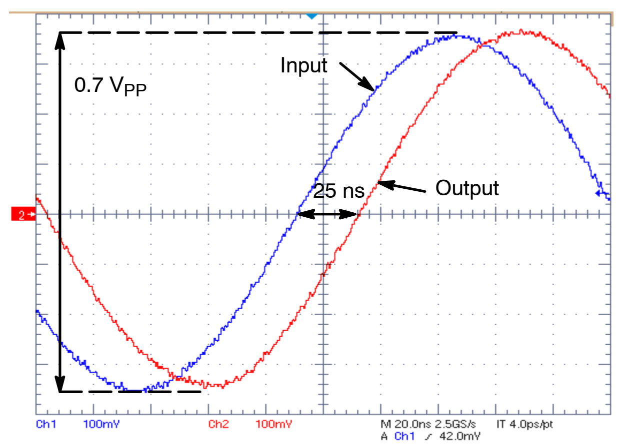


Figure 12. HD Propagation Delay

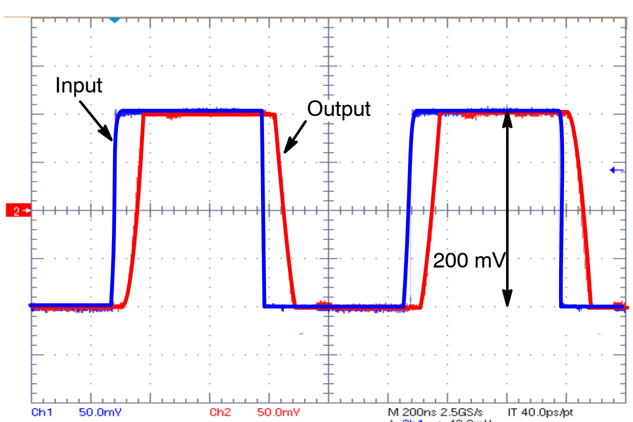


Figure 13. SD Small Signal Response

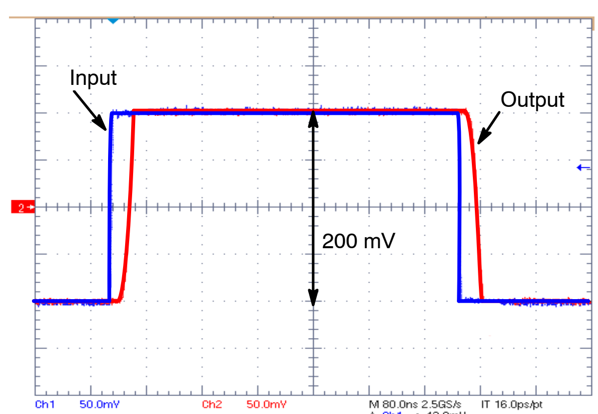


Figure 14. HD Small Signal Response

TYPICAL CHARACTERISTICS

V_{CC} = +5.0 V, V_{in} = 1 V_{PP}, R_{source} = 37.5 Ω, T_A = 25°C, Inputs AC−coupled with 0.1 μF, All Outputs AC−coupled with 220 μF into 150 Ω
Referenced to 400 kHz; unless otherwise specified

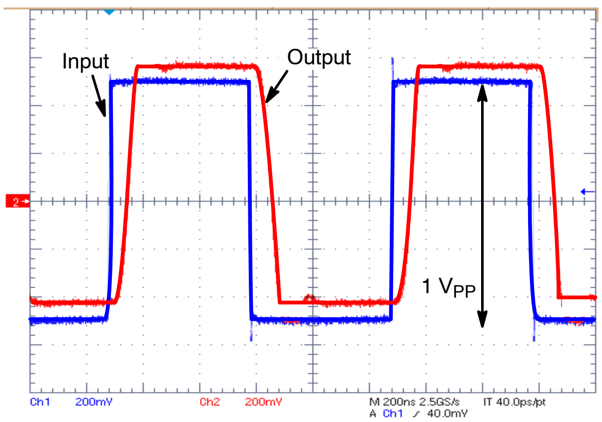


Figure 15. SD Large Signal Response

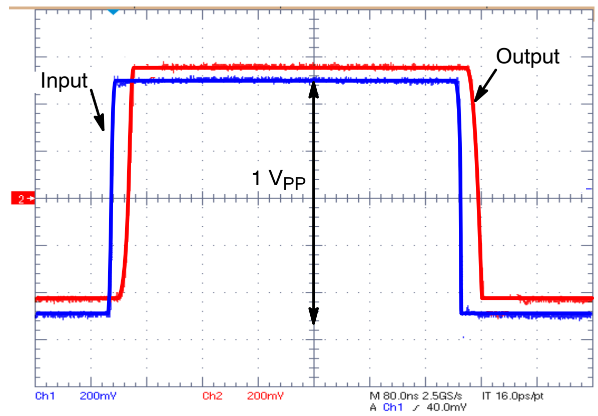


Figure 16. HD Large Signal Response

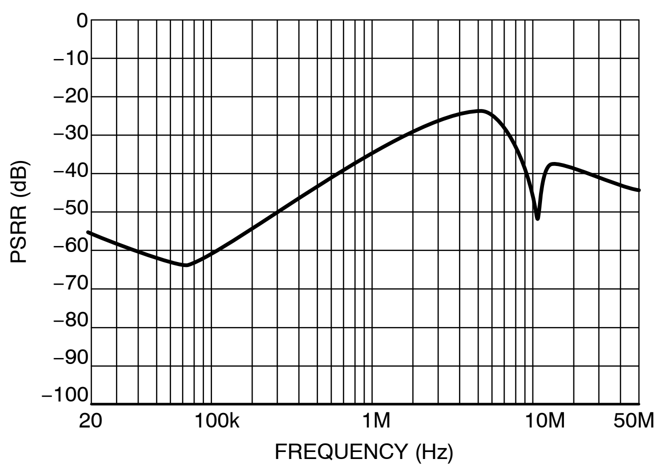


Figure 17. SD and HD V_{CC} PSRR vs. Frequency

TYPICAL CHARACTERISTICS

V_{CC} = +5.0 V, V_{in} = 1 V_{PP}, R_{source} = 37.5 Ω, T_A = 25°C, Inputs AC-coupled with 0.1 μF, All Outputs AC−coupled with 220 μF into 150 Ω
Referenced to 400 kHz; unless otherwise specified

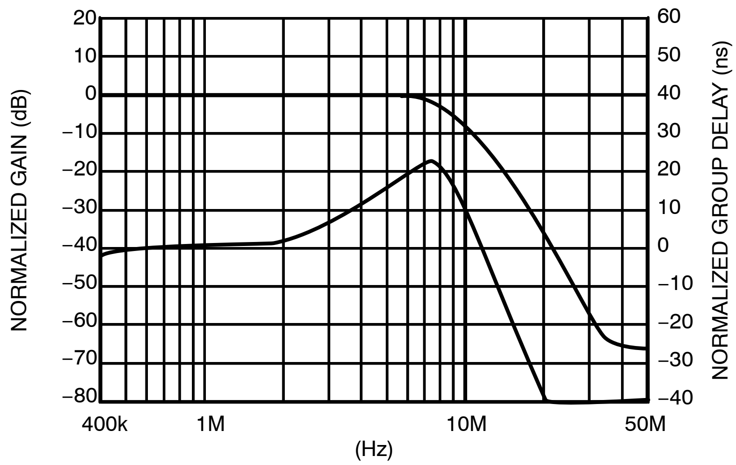


Figure 18. SD Frequency Response and Group Delay

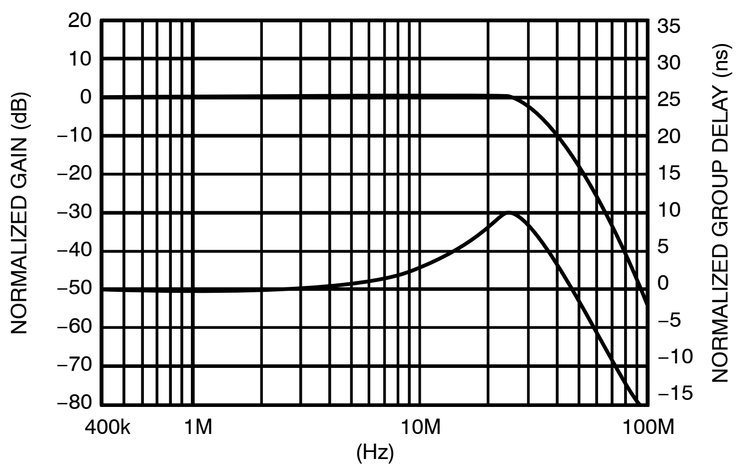


Figure 19. HD Frequency Response and Group Delay

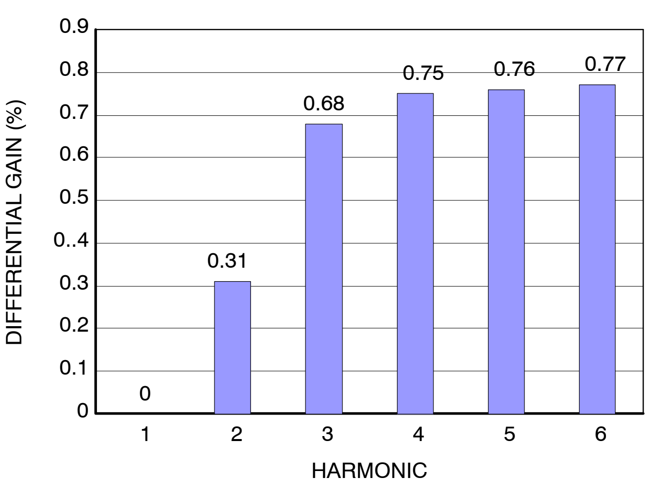


Figure 20. SD Differential Gain

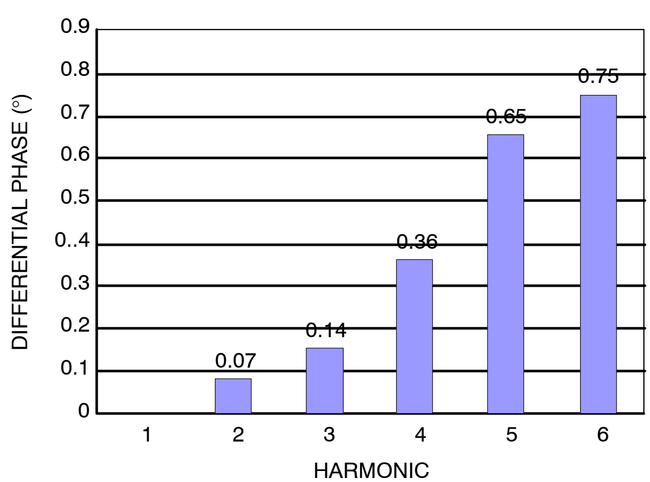


Figure 21. SD Differential Phase

APPLICATIONS INFORMATION

The NCS2566 6−channel video filter driver has been optimized for Standard and High Definition video applications covering the requirements of the standards Composite video (CVBS), S−Video, Component Video (480i/525i, 576i/625i, 720p/1080i) and related (RGB). The first 3−channels (SD1, SD2, SD3) are dedicated for Standard Definition, CVBS and S−Video applications for which the frequency bandwidth required does not exceed 8 MHz. The 3 other channels (SD/HD1, SD/HD2, SD/HD3) have selectable filters (8 MHz and 34 MHz) for covering either standard−definition−like video applications or High Definition video applications. These frequencies are selectable using the pin $\overline{\text{SD}}$/HD. If the application requires, the video driver outputs may also be disabled using the SD $\overline{\text{EN}}$ or SD/HD $\overline{\text{EN}}$ required by the application the pins SD $\overline{\text{EN}}$ or SD/HD $\overline{\text{EN}}$.

In the regular mode of operation each channel provides an internal voltage−to−voltage gain of 2 from input to output. This effectively reduces the number of external components required as compared to discrete approaches implemented with stand−alone op amps. An internal level shifter is employed shifting up the output voltage by adding an offset of 200 mV. This prevents sync pulse clipping and allows DC−coupled output to the 150 Ω video load. In addition the NCS2566 integrates a 6^{th}−order Butterworth filter for each channel. This allows rejection of aliases or unwanted over−sampling effects produced by the video DAC. Similary for DVD recorders which uses an ADC, this anti−aliasing filter (reconstruction filter) will avoid picture quality issues and will aide filtration of parasitic signals caused by EMI interference.

A built−in diode−like clamp is used in the chip for each channel to support the AC−coupled mode of operation. The clamp is active when the input signal goes below 0 V.

The built−in clamp and level shifter allow the device to operate in different configuration modes depending on the DAC output signal level and the input common mode voltage of the video driver. When the configuration is DC−Coupled at the Inputs and Outputs the 0.1 μF and 220 μF coupling capacitors are no longer used and the clamps are in that case inactive; this configuration provides a low cost solution which can be implemented with few external components.

The input is AC−coupled when either the input−signal amplitude goes over the range 0 V to 1.4 V or if the video source requires such a coupling. In some circumstances it may be necessary to auto−bias signals with the addition of a pull−up and pull−down resistors or only pull−up resistor (Typical 7.5 MΩ combined with the internal 800 kΩ pulldown) making the clamp inactive.

The output AC−coupling configuration is advantageous for eliminating DC ground loop, but may have the drawback of increasing sensitivity to video line or field tilt issues if the output coupling capacitor is too small. DC ground loop with the drawback of making the device more sensitive to video line or field tilt issues in the case of a too low output coupling capacitor. In some cases it may be necessary to increase the nominal 220 μF capacitor value.

All the device pins are protected against electrostatic discharge at a level of 8kV. This feature has been considered with a particular attention with ESD structure able to sustain the typical values requested by the systems like Set Top Boxes or Blue-Ray players. This parameter is particularly important for video driver which usually constitutes the last stage in the video chain before the video output connector. The IEC61000-4-2 standard has been used to test our devices. Test methodology can be provided on request.

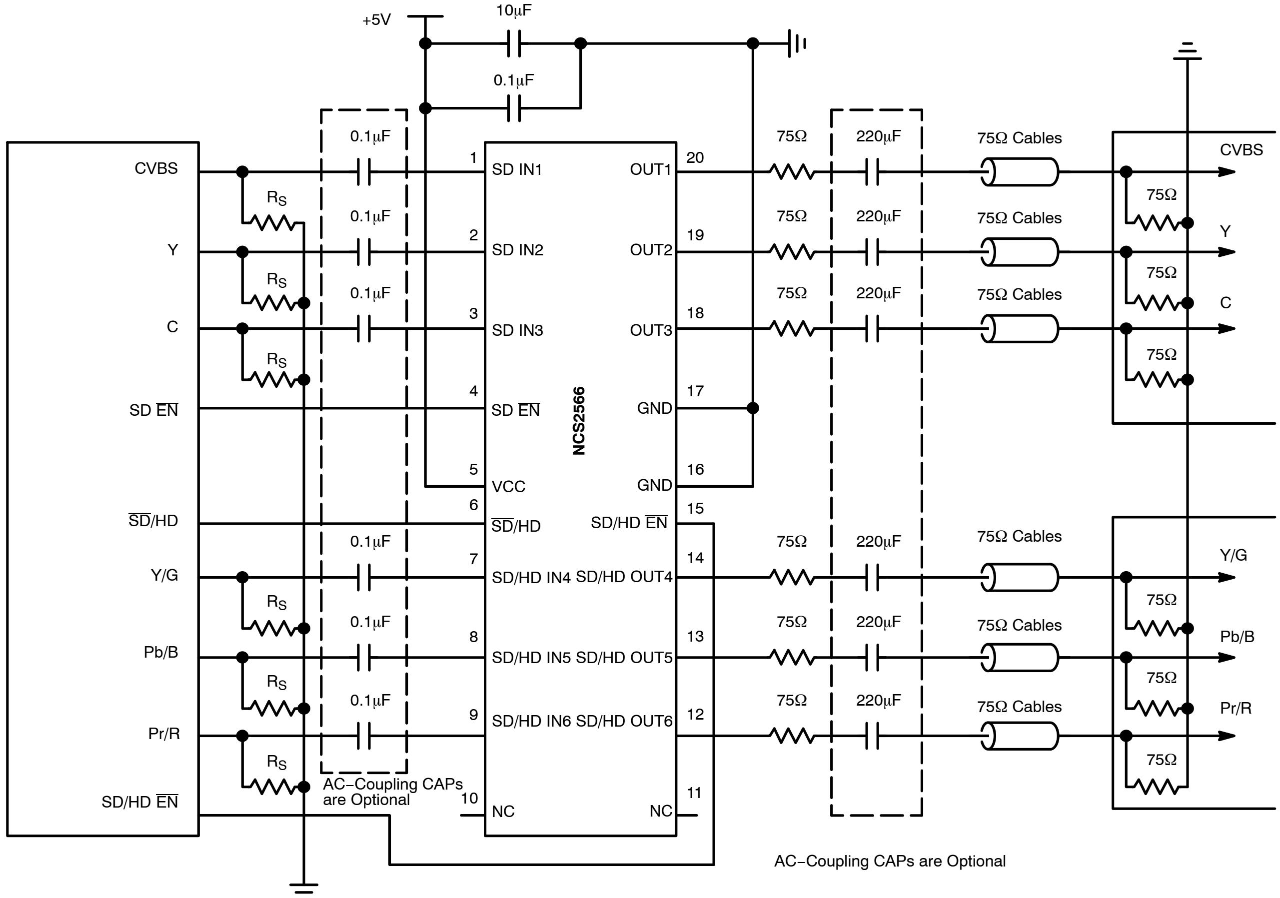


Figure 22. Typical Application

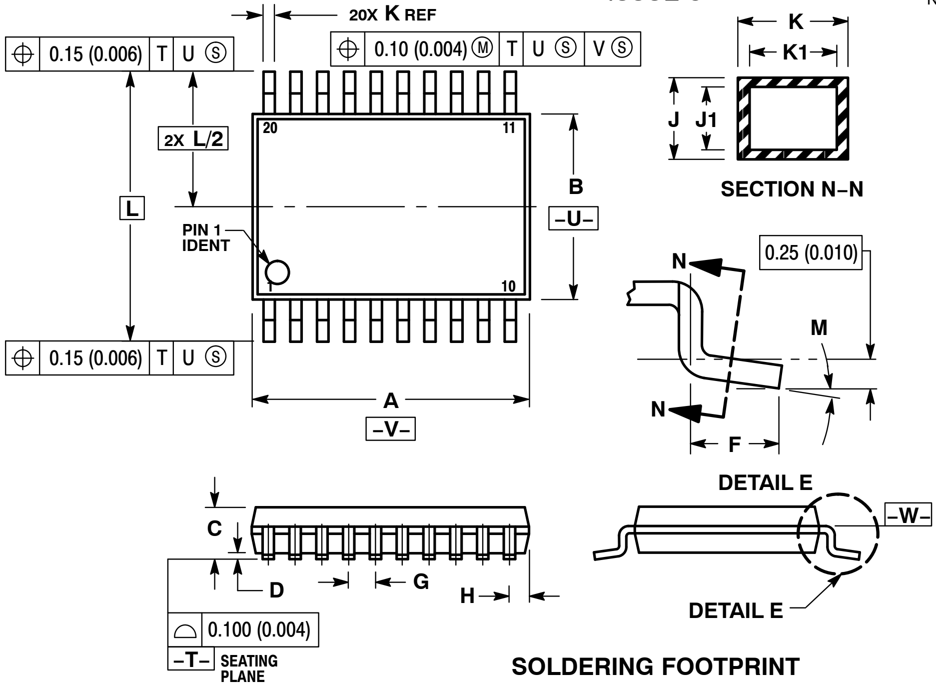
ORDERING INFORMATION

Device	Package	Shipping†
NCS2566DTBR2G	TSSOP−20 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

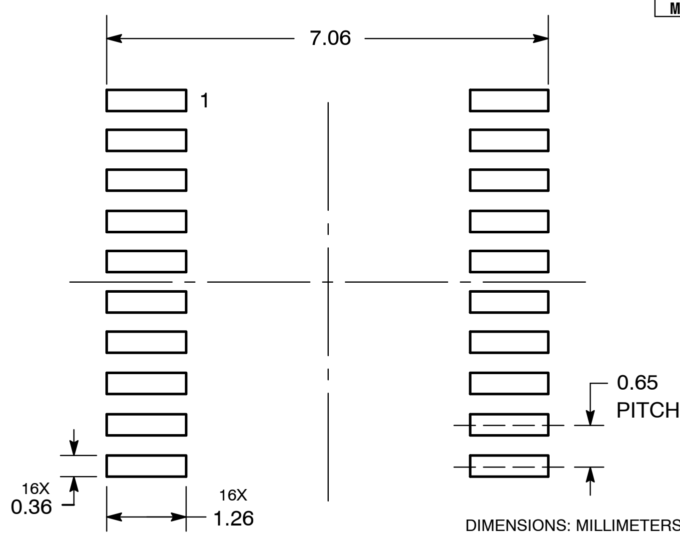
TSSOP−20
CASE 948E−02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



PUBLICATION ORDERING INFORMATION

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Phone: 81−3−5773−3850

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