# **Power MOSFET**

# 20 V, 285 mA, N-Channel with ESD Protection, SOT-723

# **Features**

- Enables High Density PCB Manufacturing
- 44% Smaller Footprint than SC-89 and 38% Thinner than SC-89
- Low Voltage Drive Makes this Device Ideal for Portable Equipment
- Low Threshold Levels, V<sub>GS(TH)</sub> < 1.3 V
- Low Profile (< 0.5 mm) Allows It to Fit Easily into Extremely Thin Environments such as Portable Electronics
- Operated at Standard Logic Level Gate Drive, Facilitating Future Migration to Lower Levels Using the Same Basic Topology
- These are Pb-Free Devices

# **Applications**

- Interfacing, Switching
- High Speed Switching
- Cellular Phones, PDAs

# MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise stated)

Param	Symbol	Value	Unit			
Drain-to-Source Voltage	V <sub>DSS</sub>	20	V			
Gate-to-Source Voltag	V <sub>GS</sub>	±10	V			
Continuous Drain	Steady	T <sub>A</sub> = 25°C		255		
Current (Note 1)	State	T <sub>A</sub> = 85°C	I <sub>D</sub>	185	mA	
	t ≤ 5 s	T <sub>A</sub> = 25°C		285		
Power Dissipation	Steady			440	mW	
(Note 1)	State	T <sub>A</sub> = 25°C	PD			
	t ≤ 5 s			545		
Continuous Drain		T <sub>A</sub> = 25°C	I <sub>D</sub>	210	mA	
Current (Note 2)	Steady State	T <sub>A</sub> = 85°C		155		
Power Dissipation (Note 2)		T <sub>A</sub> = 25°C	P <sub>D</sub>	310	mW	
Pulsed Drain Current	Pulsed Drain Current t <sub>p</sub> = 10 μs			400	mA	
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>STG</sub>	–55 to 150	°C	
Source Current (Body D	I <sub>S</sub>	286	mA			
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)			TL	260	°C	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
- 2. Surface-mounted on FR4 board using the minimum recommended pad size.

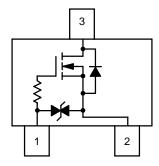


# ON Semiconductor®

# http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> Max
20 V	1.5 Ω @ 4.5 V	
	2.4 Ω @ 2.5 V	285 mA
	5.1 Ω @ 1.8 V	2031117
	6.8 Ω @ 1.65 V	

### Top View



- 1 Gate
- 2 Source
- 3 Drain

# MARKING DIAGRAM



SOT-723 CASE 631AA



KA = Device Code
M = Date Code

# ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>		
NTK3043NT1G	SOT-723*	4000 / Tape & Reel		
NTK3043NT5G	SOT-723*	8000 / Tape & Reel		

- †For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
- \*These packages are inherently Pb-Free.

# THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 3)	$R_{\theta JA}$	280	
Junction-to-Ambient - t = 5 s (Note 3)	$R_{\theta JA}$	228	°C/W
Junction-to-Ambient - Steady State Minimum Pad (Note 4)	$R_{\theta JA}$	400	

Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
 Surface-mounted on FR4 board using the minimum recommended pad size.

# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Test Condi	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS			1				
Drain-to-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 100 \mu\text{A}$		V <sub>(BR)DSS</sub>	20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 100 μA, Refere	V <sub>(BR)DSS</sub> /T <sub>J</sub>		27		mV/°C	
Zero Gate Voltage Drain Current	$V_{GS} = 0 V$	T <sub>J</sub> = 25°C	I <sub>DSS</sub>			1	
	$V_{DS} = 16 \text{ V}$	T <sub>J</sub> = 125°C				10	μΑ
Gate-to-Source Leakage Current	$V_{DS} = 0 \text{ V}, V_{GS}$	s = ±5 V	I <sub>GSS</sub>			1	μΑ
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	., ., .		V <sub>GS(TH)</sub>	0.4		1.3	V
Gate Threshold Temperature Coefficient	$V_{GS} = V_{DS}, I_D =$	= 250 μΑ	V <sub>GS(TH)</sub> /T <sub>J</sub>		-2.4		mV/°C
Drain-to-Source On Resistance	$V_{GS} = 4.5V, I_D$	= 10 mA	R <sub>DS(ON)</sub>		1.5	3.4	
	$V_{GS} = 4.5V, I_{D} =$	= 255 mA	_		1.6	3.8	-
	$V_{GS} = 2.5 \text{ V}, I_{D}$	_		2.4	4.5	Ω	
	V <sub>GS</sub> = 1.8 V, I <sub>D</sub> = 1 mA				5.1		10
	V <sub>GS</sub> = 1.65 V, I <sub>[</sub>	_		6.8	15		
Forward Transconductance	$V_{DS} = 5 \text{ V}, I_D =$	9FS		0.275		S	
CHARGES, CAPACITANCES AND GAT	E RESISTANCE		II.		1		II.
Input Capacitance			C <sub>ISS</sub>		11		
Output Capacitance	$V_{GS} = 0 \text{ V, f} = 1 \text{ MHz}$	C <sub>OSS</sub>		8.3		pF	
Reverse Transfer Capacitance		C <sub>RSS</sub>		2.7			
SWITCHING CHARACTERISTICS, VGS	<b>S= 4.5 V</b> (Note 4)		II.		1		II.
Turn-On Delay Time			t <sub>d(ON)</sub>		13		
Rise Time	V <sub>GS</sub> = 4.5 V, V <sub>DD</sub> = 5	t <sub>r</sub>		15		ns	
Turn-Off Delay Time	$R_G = 6.9$	t <sub>d(OFF)</sub>		94			
Fall Time		t <sub>f</sub>		55			
DRAIN-SOURCE DIODE CHARACTER	ISTICS		1				
Forward Diode Voltage		T <sub>J</sub> = 25°C	V <sub>SD</sub>		0.83	1.2	.,
	$V_{GS} = 0 \text{ V, } I_{S} = 286 \text{ mA}$ $T_{J} = 125^{\circ}\text{C}$		_		0.69		V
Reverse Recovery Time			t <sub>RR</sub>		9.1		
Charge Time	$V_{GS} = 0 \text{ V}, V_{DD} = 20 \text{ V}, d$	t <sub>a</sub>		7.1		ns	
Discharge Time	$I_{S} = 286 \text{ r}$	t <sub>b</sub>		2.0			
Reverse Recovery Charge		Q <sub>RR</sub>		3.7		nC	

<sup>5.</sup> Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
6. Switching characteristics are independent of operating junction temperatures

# **TYPICAL PERFORMANCE CURVES**

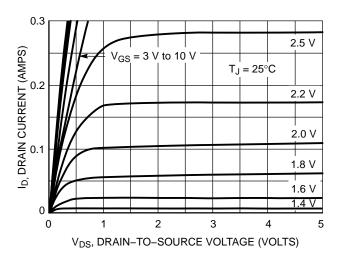


Figure 1. On-Region Characteristics

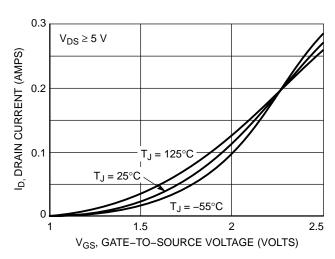


Figure 2. Transfer Characteristics

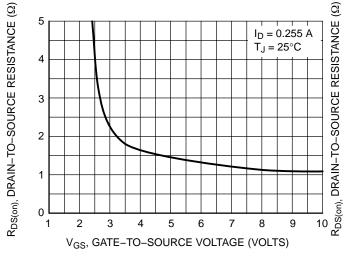


Figure 3. On-Resistance vs. Gate-to-Source Voltage

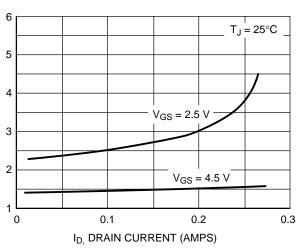


Figure 4. On–Resistance vs. Drain Current and Gate Voltage

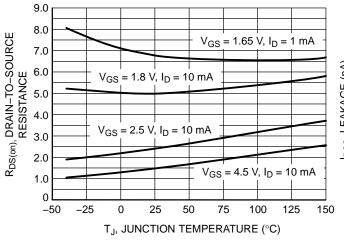


Figure 5. On–Resistance Variation with Temperature

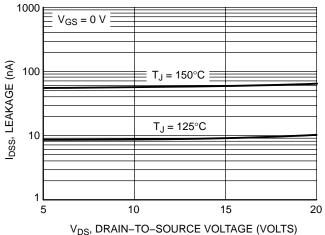
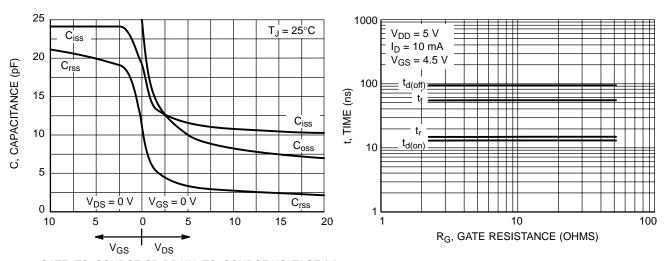


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# **TYPICAL PERFORMANCE CURVES**



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (V)

Figure 7. Capacitance Variation

Figure 8. Resistive Switching Time Variation vs. Gate Resistance

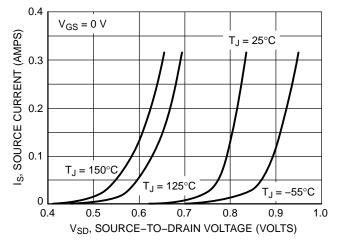
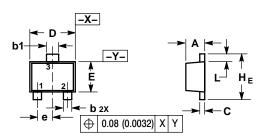


Figure 9. Diode Forward Voltage vs. Current

# PACKAGE DIMENSIONS

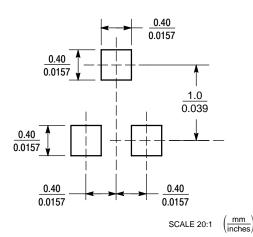
SOT-723 CASE 631AA-01 ISSUE B



- DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	0.45	0.50	0.55	0.018	0.020	0.022	
b	0.15	0.21	0.27	0.0059	0.0083	0.0106	
b1	0.25	0.31	0.37	0.010	0.012	0.015	
С	0.07	0.12	0.17	0.0028	0.0047	0.0067	
D	1.15	1.20	1.25	0.045	0.047	0.049	
E	0.75	0.80	0.85	0.03	0.032	0.034	
е	0.40 BSC			0.016 BSC			
ΗE	1.15	1.20	1.25	0.045	0.047	0.049	
٦	0.15	0.20	0.25	0.0059	0.0079	0.0098	

### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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