SD1727 (THX15)

RF POWER BIPOLAR TRANSISTORS
HF SSB APPLICATIONS

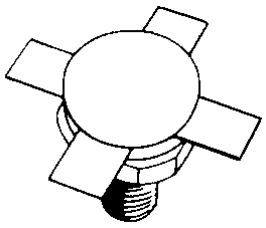
FEATURES SUMMARY

- OPTIMIZED FOR SSB
- 30 MHz
- 50 VOLTS
- IMD –30 dB
- COMMON EMITTER
- GOLD METALLIZATION
- P_{OUT} = 150 W PEP MIN. WITH 14 dB GAIN

DESCRIPTION

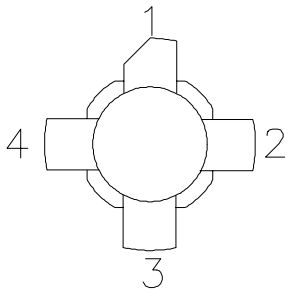
The SD1727 is a 50 V epitaxial silicon NPN planar transistor designed primarily for SSB communications. This device utilizes emitter ballasting to achieve extreme ruggedness under severe operating conditions.

Figure 1. Package



.500 4L FL (M164)
epoxy sealed

Figure 2. Pin Connection



1. Collector
2. Emitter
3. Base
4. Emitter

Table 1. Order Codes

Order Codes	Marking	Package	Packaging
SD1727 (THX15)	SD1727	M164	BLACK CARDBOARDS

Table 2. Absolute Maximum Ratings (T_{case} = 25°C)

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage	110	V
V_{CEO}	Collector-Emitter Voltage	55	V
V_{EBO}	Emitter-Base Voltage	4.0	V
I_C	Device Current	10	A
P_{DISS}	Power Dissipation	233	W
T_J	Junction Temperature	+200	°C
T_{STG}	Storage Temperature	– 65 to +150	°C

Table 3. Thermal Data

Symbol	Parameter	Value	Unit
$R_{TH(j-c)}$	Junction-Case Thermal Resistance	0.75	°C/W

ELECTRICAL SPECIFICATIONS (T_{case} = 25°C)

Table 4. Static

Symbol	Test Conditions	Value			Unit
		Min.	Typ.	Max.	
BV_{CBO}	I_C = 100 mA; I_E = 0 mA	110	—	—	V
BV_{CES}	I_C = 100 mA; V_{BE} = 0 V	110	—	—	V
BV_{CEO}	I_C = 100 mA; I_B = 0 mA	55	—	—	V
BV_{EBO}	I_E = 10 mA; I_C = 0 mA	4.0	—	—	V
I_{CEO}	V_{CE} = 30 V; I_E = 0 mA	—	—	5	mA
I_{CES}	V_{CE} = 60 V; I_E = 0 mA	—	—	5	mA
h_{FE}	V_{CE} = 6 V; I_C = 1.4 A	18	—	43.5	—

Table 5. Dynamic

Symbol	Test Conditions	Value			Unit
		Min.	Typ.	Max.	
P_{OUT}	f = 30 MHz; V_{CE} = 50 V; I_{CQ} = 100 mA	150	—	—	W
G_P (1)	P_{OUT} = 150 W PEP; V_{CE} = 50 V; I_{CQ} = 100 mA	14	—	—	dB
IMD (1)	P_{OUT} = 150 W PEP; V_{CE} = 50 V; I_{CQ} = 100 mA	—	—	–30	dBc
η_c (1)	P_{OUT} = 150 W PEP; V_{CE} = 50 V; I_{CQ} = 100 mA	37	—	—	%
C_{OB}	f = 1 MHz; V_{CB} = 50 V	—	—	220	pF

Note: The SD1727 is also usable in Class A at 40 V. Typical performance is:
P_{OUT} = 30 W PEP, G_P = 14 dB, IMD = – 40dBc

Note: 1. f_1 = 30.00 MHz; f_2 = 30.001 MHz

TYPICAL PERFORMANCE

Figure 3. Intermodulation Distortion vs Power Output PEP

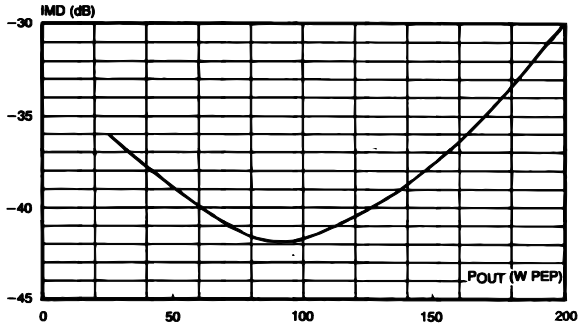


Figure 4. Power Output PEP vs Power Input

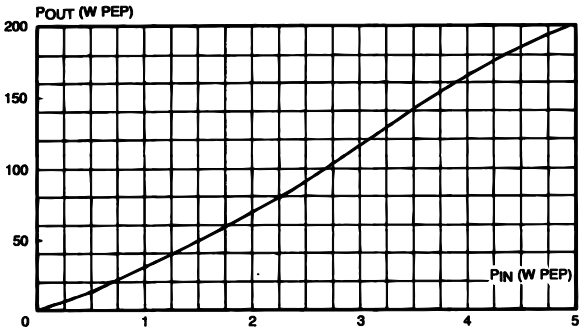


Figure 5. Collector Efficiency vs Power Output PEP

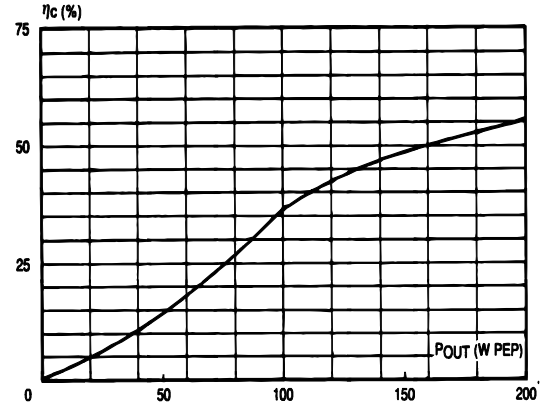


Figure 6. Power Gain vs Frequency

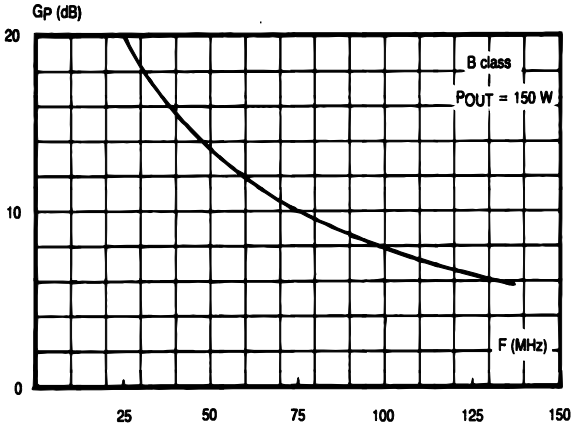


Figure 7. Power Gain vs Power Output PEP

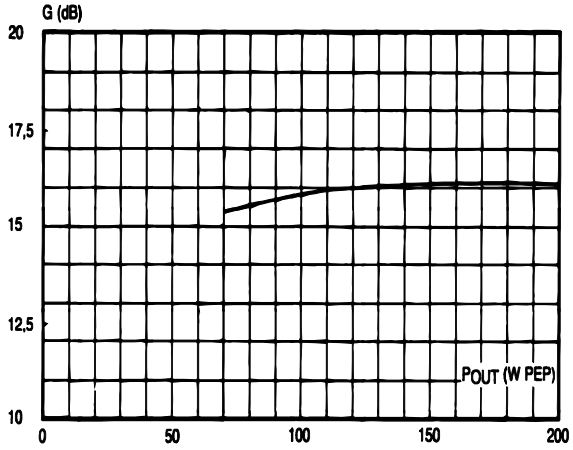
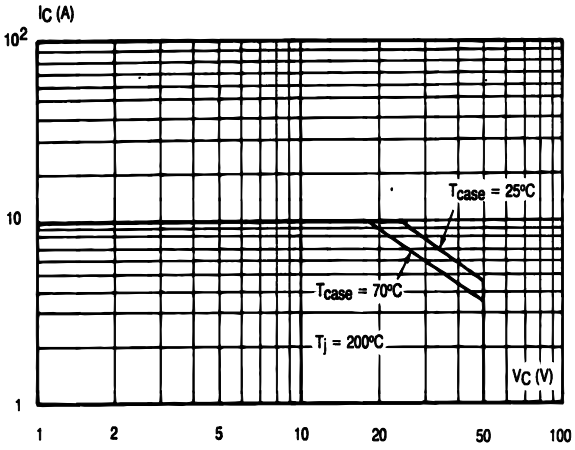
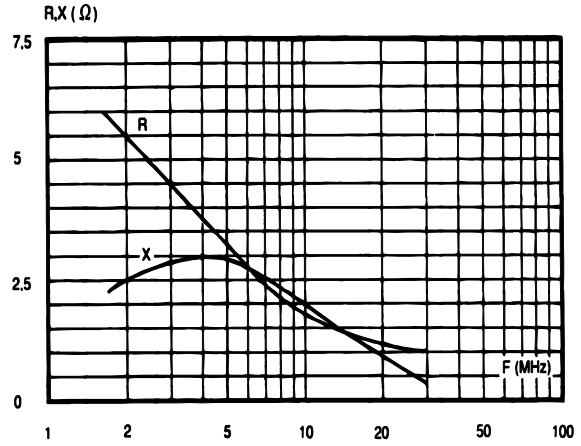


Figure 8. Safe Operating Area



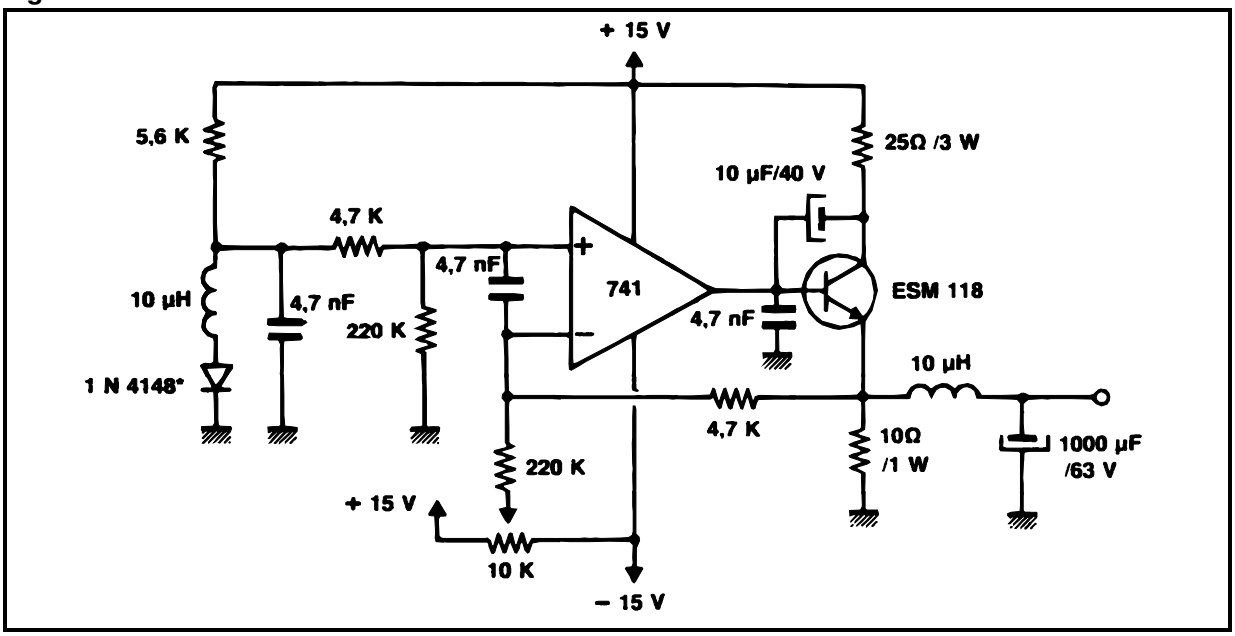
IMPEDANCE DATA

Figure 9. Typical Input Impedance



BIAS CIRCUIT

Figure 10. Bias Circuit



TEST CIRCUIT - CLASS AB – 30 MHZ

Figure 11. Test Circuit - Class AB – 30 Mhz

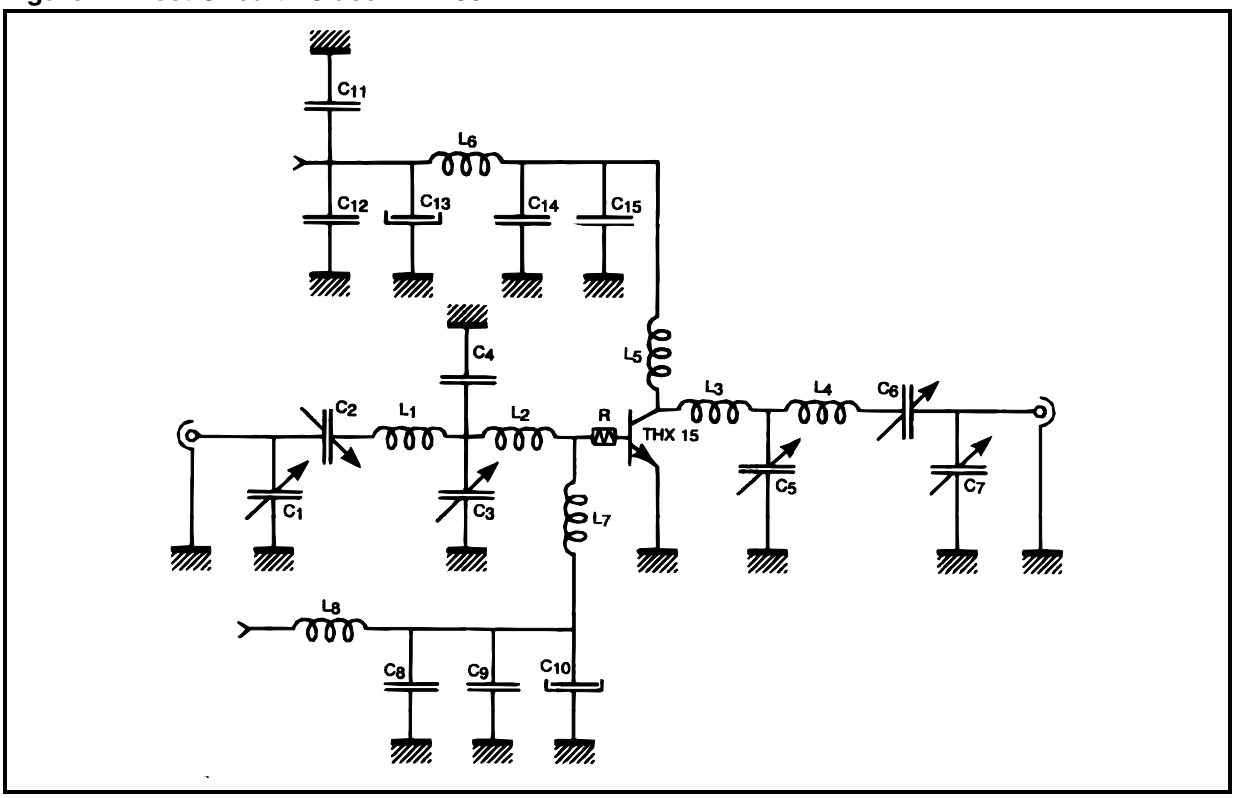
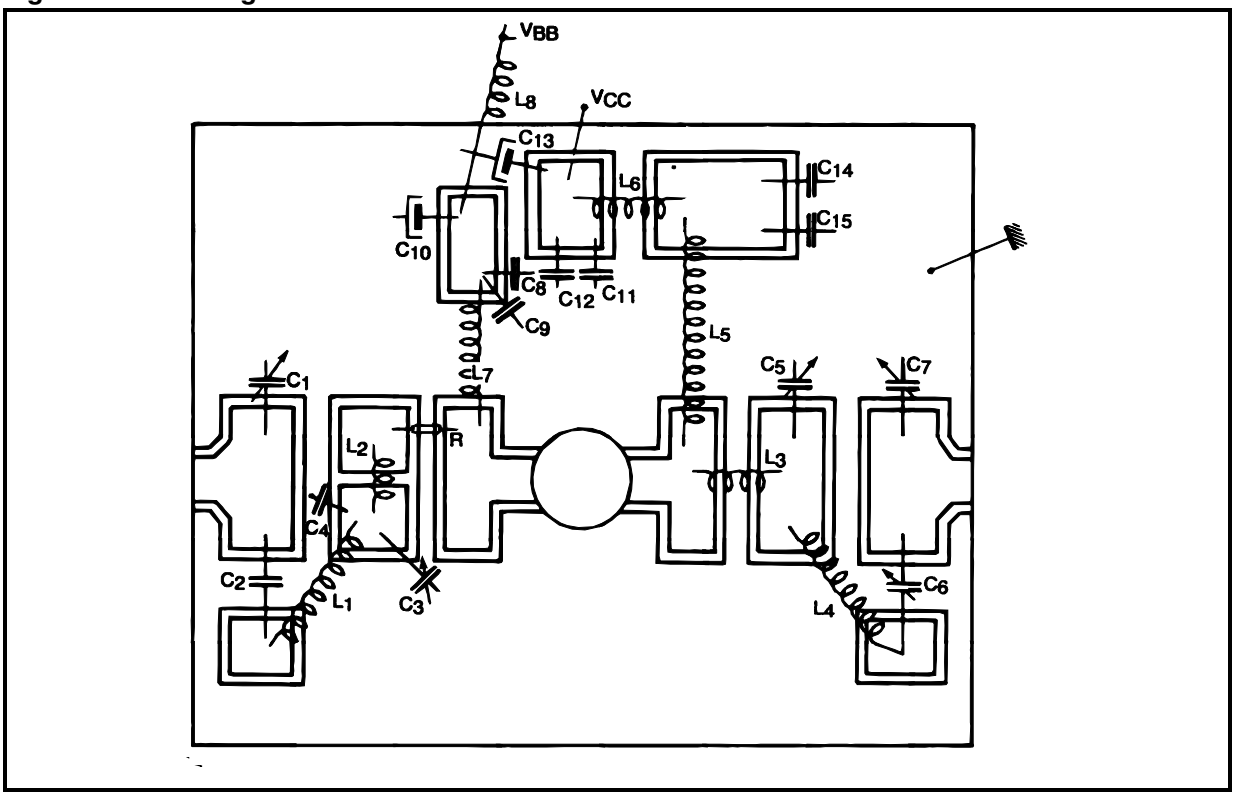


Table 6. Test Circuit - Class AB – 30 Mhz

C1	Arco 427
C2	Arco 4611
C3	Arco 4615
C4	220pF
C5, C6	Arco 4215
C7	Arco 426
C8. C12	100nF 63V
C9, C11, C15	1nF
C10	470µF 40V
C13	220µF 63V
C14	10nF
L1	5 Turns Diameter 8mm, 1.3mm Wire, Length 15mm
L2	Hair Pin Copper Foil 20 x 5mm, 0.2mm Thick
L3	1 Turn Diameter 10mm, 1.3mm Wire, Length 8mm
L4	6 Turns Diameter 8mm, 1.3mm Wire, Length 25mm
L5	4 Turns Diameter 12mm, 2mm Wire, Length 25mm
L6, L7, L8	Choke
R	0.6Ω

MOUNTING CIRCUIT - CLASS AB – 30 MHZ

Figure 12. Mounting Circuit - Class AB – 30 Mhz

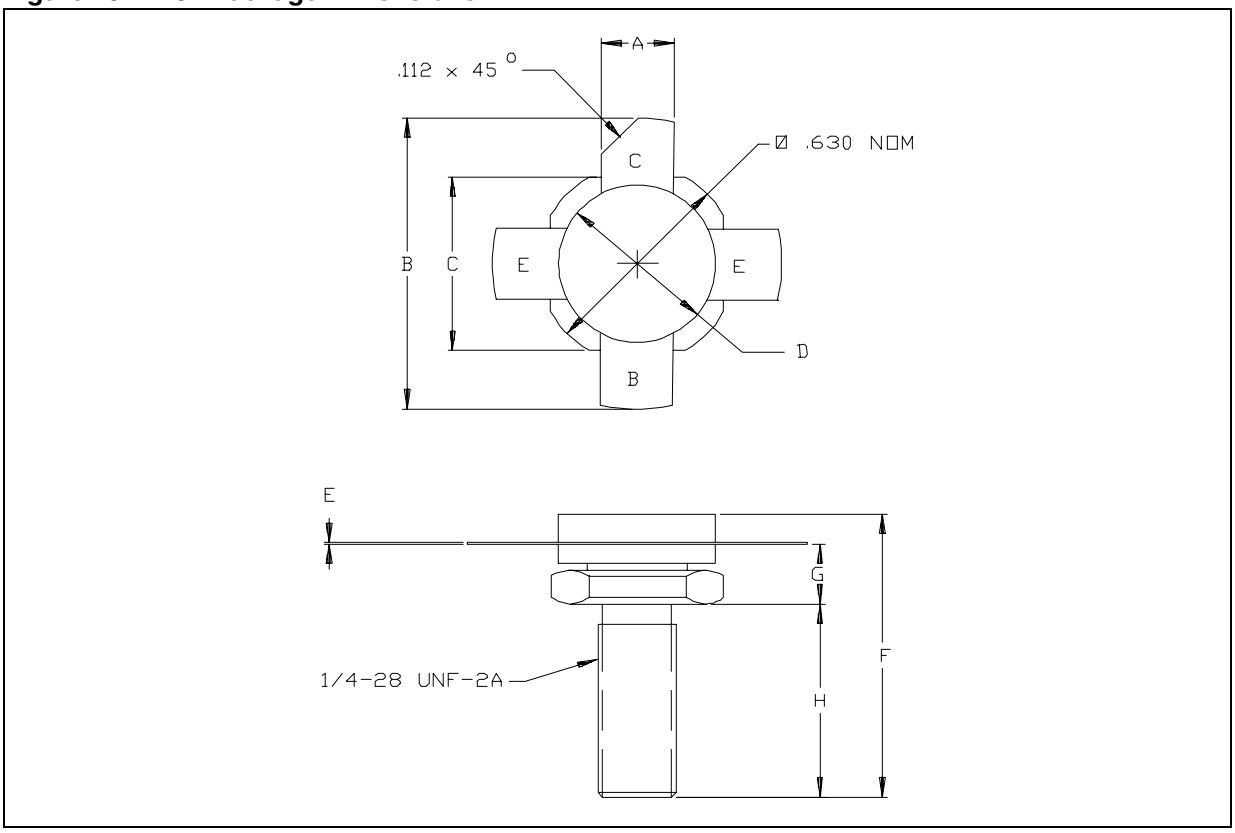


PACKAGE MECHANICAL

Table 7. M164 Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	5.59		5.84	0.220		0.230
B			26.67			1.050
C	13.84		14.10	0.545		0.555
D	12.57		12.83	0.495		0.505
E	0.08		0.18	0.003		0.007
F			21.08			0.830
G	4.70		5.03	0.185		0.198
H	12.62		13.46	0.497		0.530

Figure 13. M164 Package Dimensions



Note: Drawing is not to scale.

REVISION HISTORY

Table 8. Revision History

Date	Revision	Description of Changes
November-1992	1	First Issue
8-June-2004	2	Stylesheet update. No content change.