

# PHD36N03LT

## N-channel TrenchMOS logic level FET

Rev. 03 — 29 March 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Simple gate drive required due to low gate charge
- Suitable for logic level gate drive sources

### 1.3 Applications

- DC-to-DC convertors
- Switched-mode power supplies

### 1.4 Quick reference data

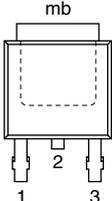
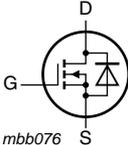
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	30	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a> and <a href="#">3</a>	-	-	43.4	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	-	57.6	W
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 36\text{ A};$ $V_{DS} = 15\text{ V}; T_j = 25\text{ °C};$ see <a href="#">Figure 11</a> and <a href="#">12</a>	-	2.9	-	nC
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ see <a href="#">Figure 9</a> and <a href="#">10</a>	-	14	17	m $\Omega$



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

**SOT428 (DPAK)**

[1] It is not possible to make a connection to pin 2.

## 3. Ordering information

Table 3. Ordering information

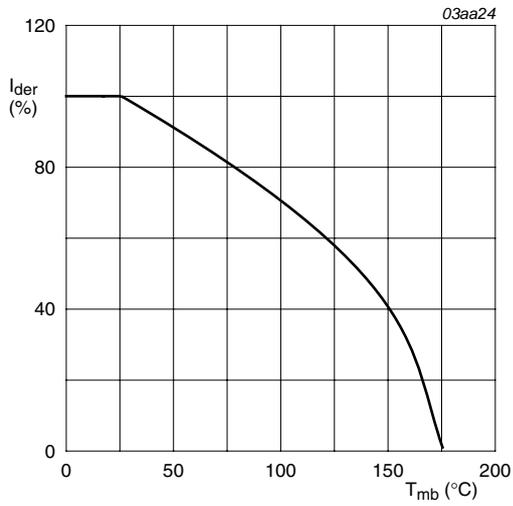
Type number	Package		Version
	Name	Description	
PHD36N03LT	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

## 4. Limiting values

Table 4. Limiting values

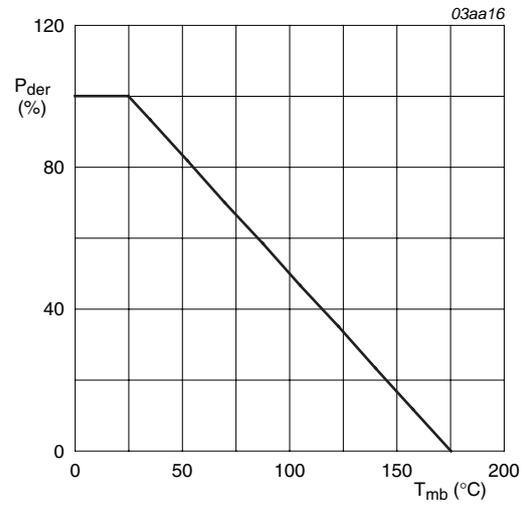
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	30	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	-	30.7	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> and <a href="#">3</a>	-	43.4	A
$I_{DM}$	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	173.6	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	57.6	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	43.4	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	173.6	A



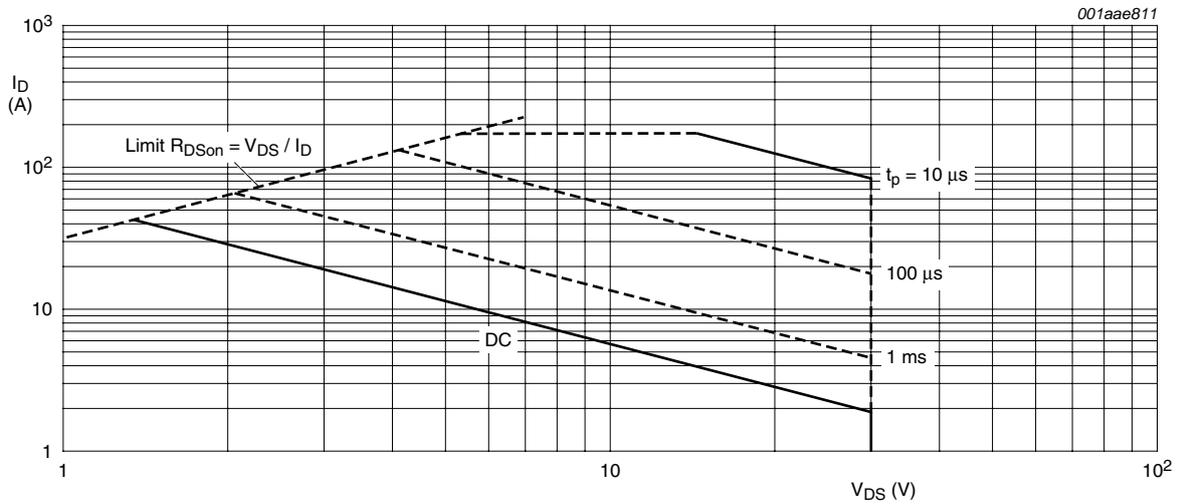
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



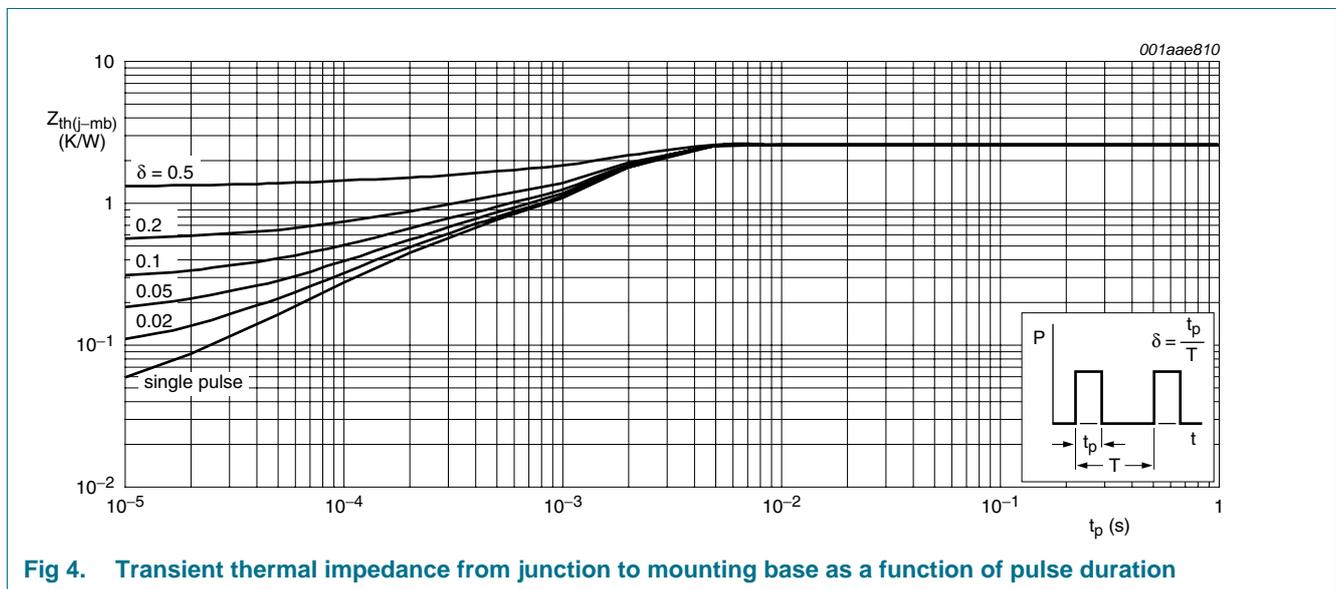
$T_{mb} = 25^\circ\text{C}$ ;  $I_{DM}$  is single pulse;  $V_{GS} = 10 \text{ V}$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

Table 5. Thermal characteristics

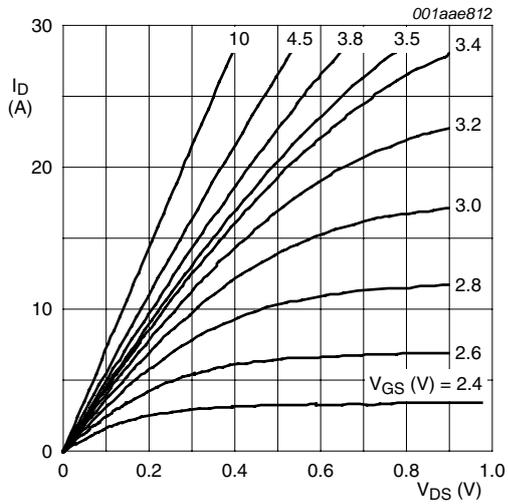
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	2.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board; vertical in still air	-	75	-	K/W
		SOT404 minimum footprint; mounted on a printed-circuit board; vertical in still air	-	50	-	K/W



## 6. Characteristics

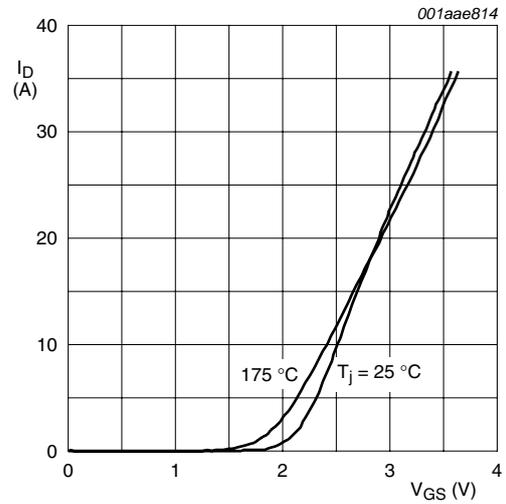
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	27	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> and <a href="#">8</a>	0.5	-	-	V
		$I_D = 250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> and <a href="#">8</a>	1	1.5	2	V
		$I_D = 250 \mu\text{A}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> and <a href="#">8</a>	-	-	2.2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	1	$\mu\text{A}$
		$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a> and <a href="#">10</a>	-	14	17	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 12 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a> and <a href="#">10</a>	-	32.4	39.6	m $\Omega$
		$V_{GS} = 3.5 \text{ V}; I_D = 5.2 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a> and <a href="#">10</a>	-	22	40	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 12 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a> and <a href="#">10</a>	-	18	22	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 36 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a> and <a href="#">12</a>	-	18.5	-	nC
$Q_{GS}$	gate-source charge		-	4.2	-	nC
$Q_{GD}$	gate-drain charge		-	2.9	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a>	-	690	-	pF
$C_{oss}$	output capacitance	$V_{DS} = 0 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a>	-	160	-	pF
$C_{rss}$	reverse transfer capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a>	-	110	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 \text{ V}; R_L = 0.6 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 10 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	6	-	ns
$t_r$	rise time		-	10	-	ns
$t_{d(off)}$	turn-off delay time		-	33	-	ns
$t_f$	fall time		-	19	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 14</a>	-	0.97	1.2	V



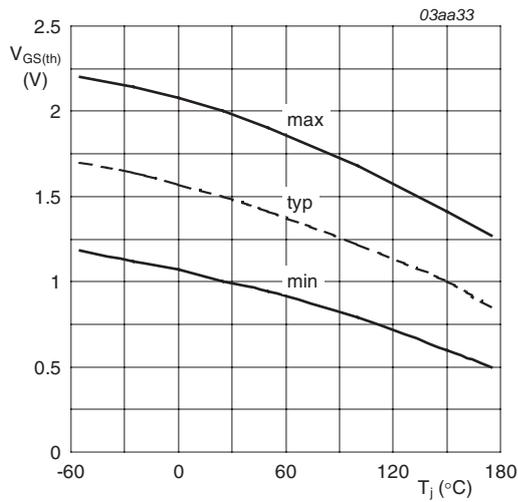
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



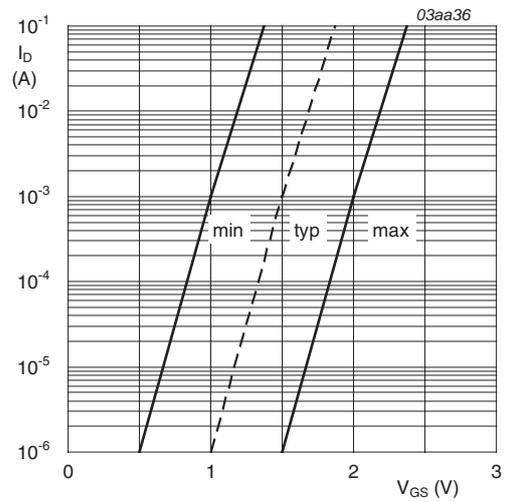
$V_{DS} > I_D \times R_{DS(on)}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



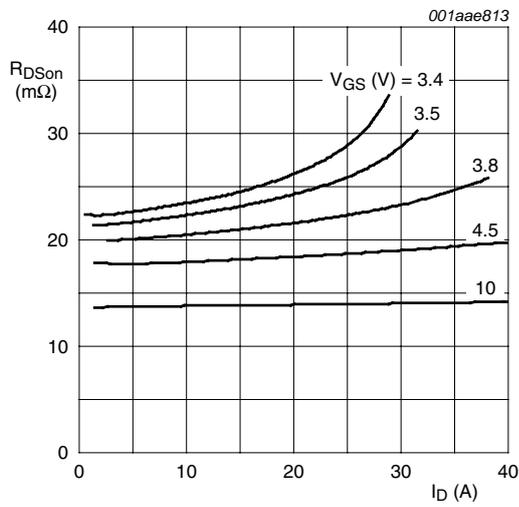
$I_D = 1\text{mA}; V_{DS} = V_{GS}$

Fig 7. Gate-source threshold voltage as a function of junction temperature



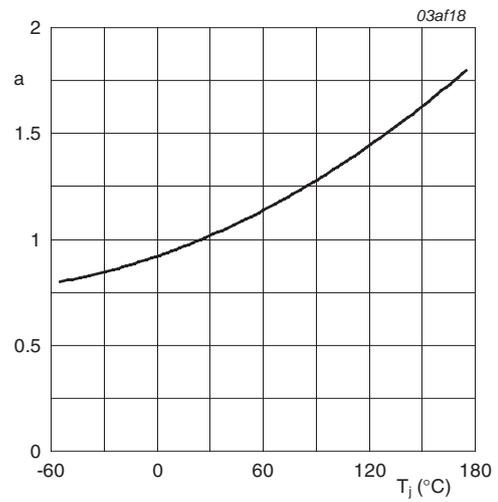
$T_j = 25^\circ\text{C}; V_{DS} = V_{GS}$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



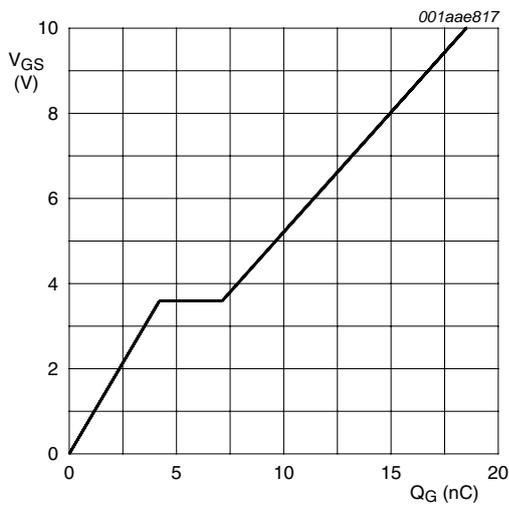
$T_j = 25^\circ\text{C}$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



$I_D = 36\text{ A}; V_{DS} = 15\text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

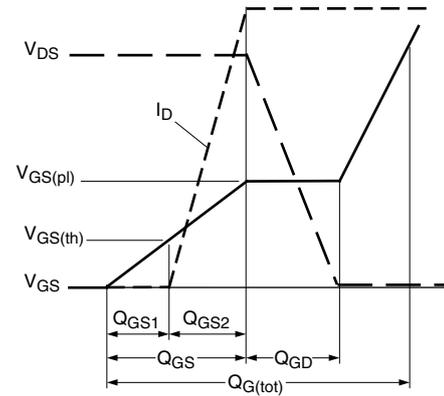
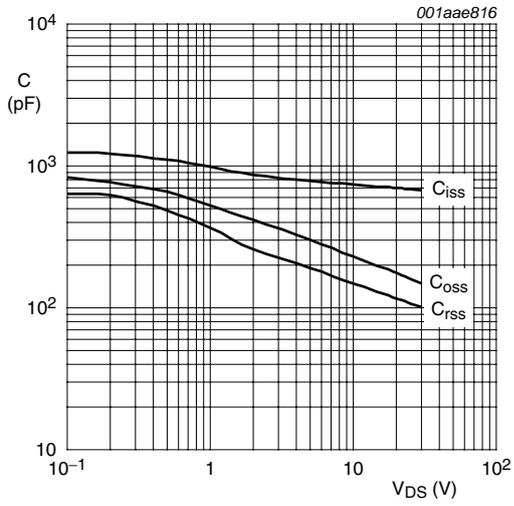
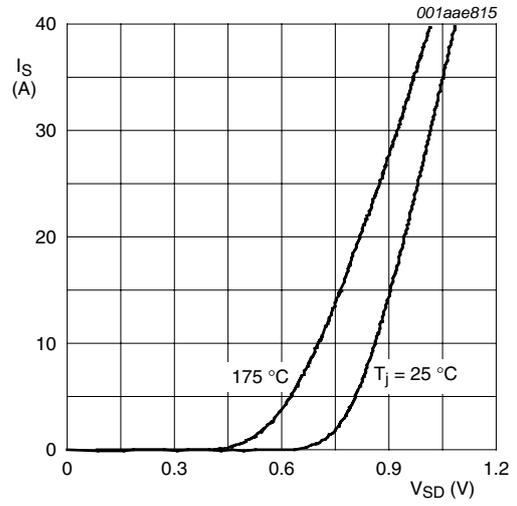


Fig 12. Gate charge waveform definitions



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$V_{GS} = 0\text{ V}$

**Fig 14. Source current as a function of source-drain voltage; typical values**

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

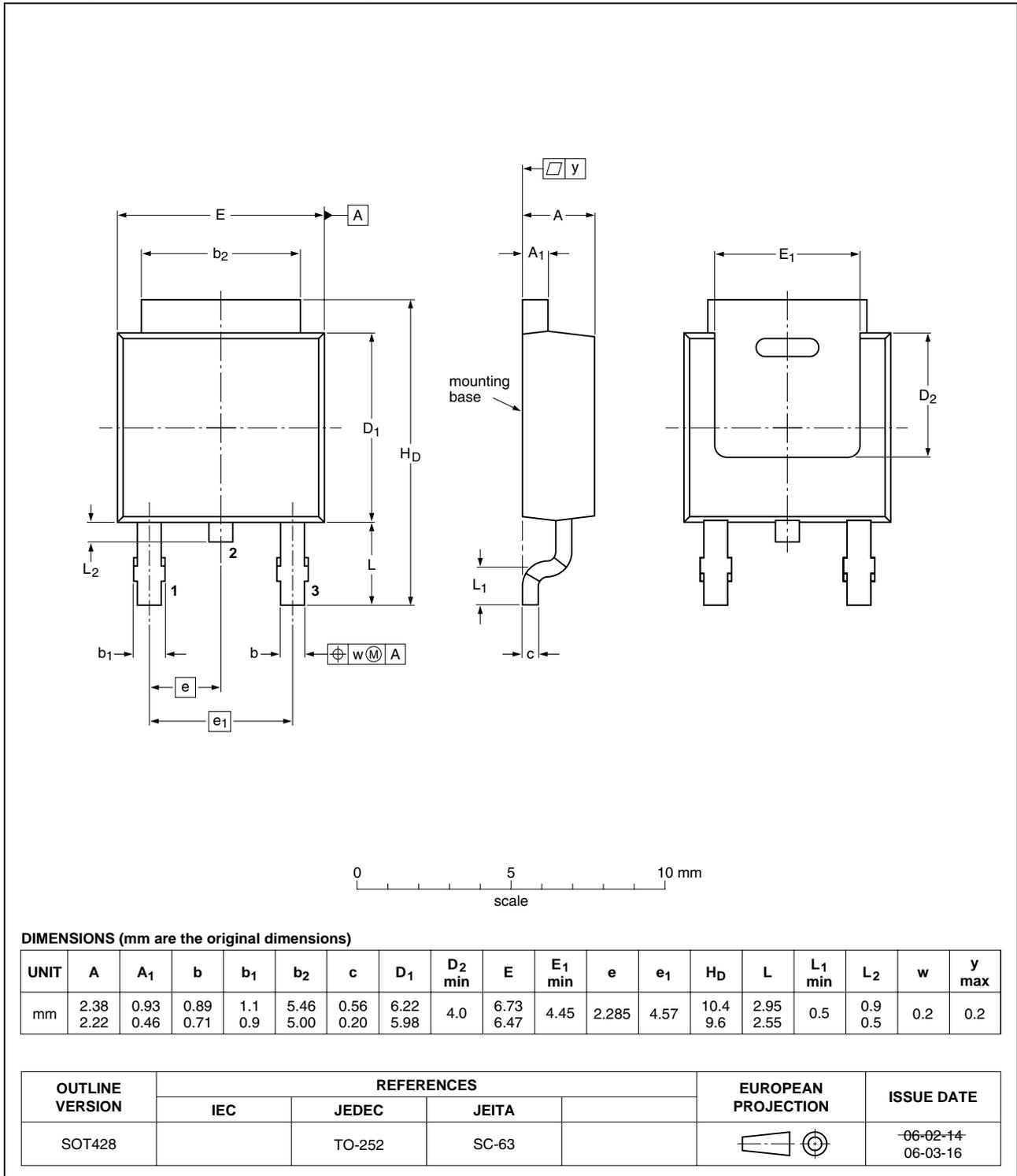


Fig 15. Package outline SOT428 (DPAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD36N03LT_3	20100329	Product data sheet	-	PHD_PHP36N03LT_2
Modifications:		<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Type number PHD36N03LT separated from data sheet PHD_PHP36N03LT_2.</li></ul>		
PHD_PHP36N03LT_2	20060608	Product data sheet	-	PHD36N03LT-01
PHD36N03LT-01 (9397 750 11613)	20030630	Product data	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 11. Contents

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<b>1</b>	<b>Product profile</b> . . . . .	<b>1</b>
1.1	General description . . . . .	1
1.2	Features and benefits . . . . .	1
1.3	Applications . . . . .	1
1.4	Quick reference data . . . . .	1
<b>2</b>	<b>Pinning information</b> . . . . .	<b>2</b>
<b>3</b>	<b>Ordering information</b> . . . . .	<b>2</b>
<b>4</b>	<b>Limiting values</b> . . . . .	<b>2</b>
<b>5</b>	<b>Thermal characteristics</b> . . . . .	<b>4</b>
<b>6</b>	<b>Characteristics</b> . . . . .	<b>5</b>
<b>7</b>	<b>Package outline</b> . . . . .	<b>9</b>
<b>8</b>	<b>Revision history</b> . . . . .	<b>10</b>
<b>9</b>	<b>Legal information</b> . . . . .	<b>11</b>
9.1	Data sheet status . . . . .	11
9.2	Definitions . . . . .	11
9.3	Disclaimers . . . . .	11
9.4	Trademarks . . . . .	12
<b>10</b>	<b>Contact information</b> . . . . .	<b>12</b>

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