



# Spread Spectrum System Frequency Synthesizer

## Features

- Maximized EMI suppression using Cypress's spread spectrum technology
- Intel® CK98 Specification compliant
- 0.5% downspread outputs deliver up to 10 dB lower EMI
- Four skew-controlled copies of CPU output
- Eight copies of PCI output (synchronous w/CPU output)
- Four copies of 66-MHz fixed frequency 3.3V clock
- Two copies of CPU/2 outputs for synchronous memory reference
- Three copies of 16.67-MHz IOAPIC clock, synchronous to CPU clock
- One copy of 48-MHz USB output
- Two copies of 14.31818-MHz reference clock
- Programmable to 133- or 100-MHz operation
- Power management control pins for clock stop and shut down
- Available in 56-pin SSOP

## Key Specifications

Supply Voltages: .....  $V_{DDQ3} = 3.3V \pm 5\%$   
 $V_{DDQ2} = 2.5V \pm 5\%$

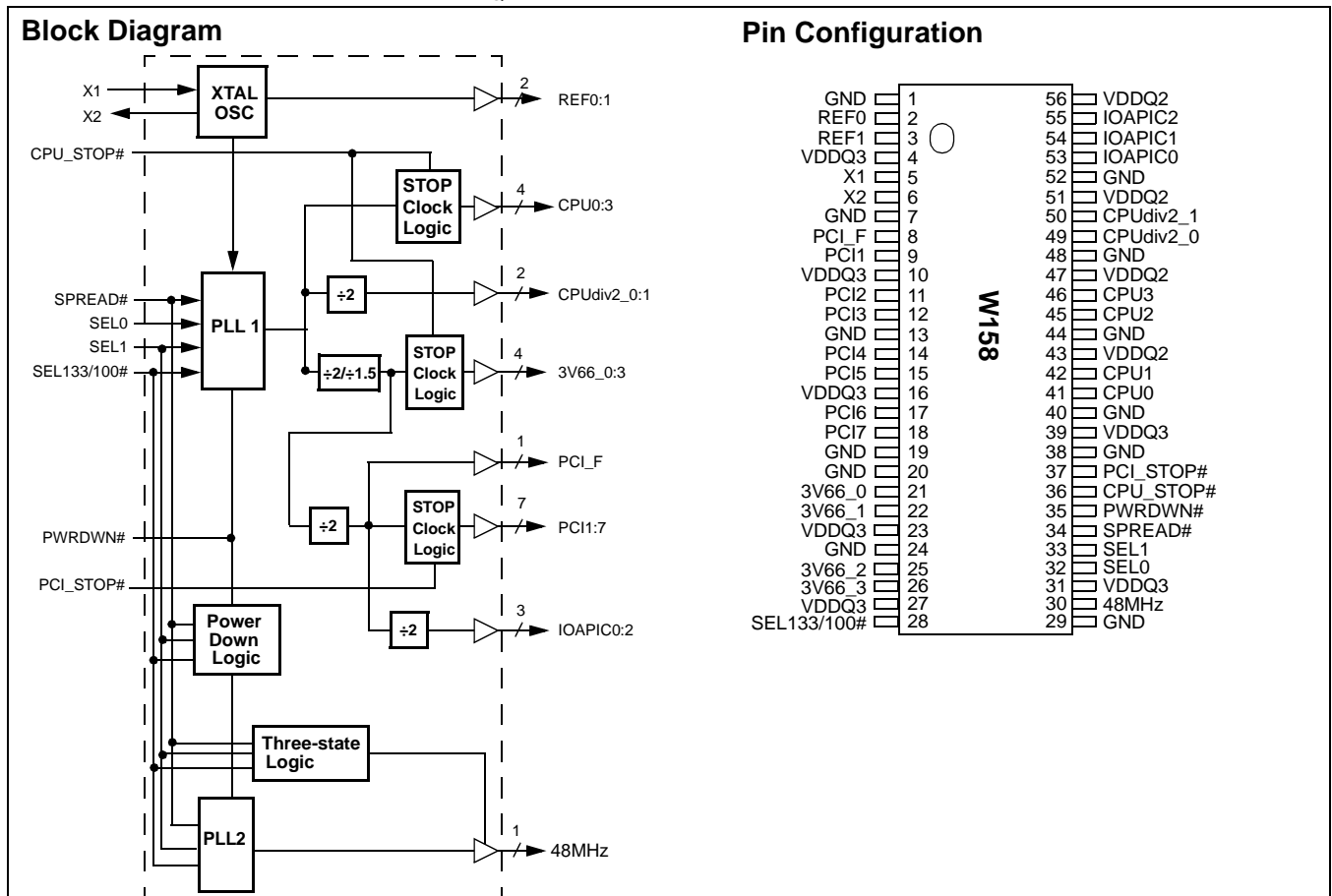
CPU Output Jitter: ..... 150 ps  
 CPUdiv2, IOAPIC Output Jitter: ..... 250 ps  
 48 MHz, 3V66, PCI Output Jitter: ..... 500 ps  
 CPU0:3, CPUdiv2\_0:1 Output Skew: ..... 175 ps  
 PCI\_F, PCI1:7 Output Skew: ..... 500 ps  
 3V66\_0:3, IOAPIC0:2 Output Skew: ..... 250 ps  
 CPU to 3V66 Output Offset: ..... 0.0 to 1.5 ns (CPU leads)  
 3V66 to PCI Output Offset: ..... 1.5 to 3.0 ns (3V66 leads)  
 CPU to IOAPIC Output Offset: ..... 1.5 to 4.0 ns (CPU leads)  
 CPU to PCI Output Offset: ..... 1.5 to 4.0 ns (CPU leads)  
 Logic inputs, except SEL133/100#, have 250-kΩ pull-up resistors

Table 1. Pin Selectable Frequency<sup>[1]</sup>

| SEL133/100# | CPU0:3 (MHz) | PCI      |
|-------------|--------------|----------|
| 1           | 133 MHz      | 33.3 MHz |
| 0           | 100 MHz      | 33.3 MHz |

Note:

1. See Table 2 for complete mode selection details.



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**Pin Definitions**

| Pin Name    | Pin No.                                      | Pin Type | Pin Description   |
|-------------|--|----------|---|
| CPU0:3      | 41, 42, 45, 46                               | O        | <b>CPU Clock Outputs 0 through 3:</b> These four CPU clocks run at a frequency set by SEL133/100#. Output voltage swing is set by the voltage applied to VDDQ2.   |
| CPUdiv2_0:1 | 49, 50                                       | O        | <b>Synchronous Memory Reference Clock Output 0 through 1:</b> Reference clock for Direct RDRAM clock generators running at 1/2 CPU clock frequency. Output voltage swing is set by the voltage applied to VDDQ2.      |
| PCI1:7      | 9, 11, 12, 14, 15, 17, 18                    | O        | <b>PCI Clock Outputs 1 through 7:</b> These seven PCI clock outputs run synchronously to the CPU clock. Voltage swing is set by the power connection to VDDQ3. PCI1:7 outputs are stopped when PCI_STOP# is held LOW. |
| PCI_F       | 8  | O        | <b>PCI_F (PCI Free-running):</b> This PCI clock output runs synchronously to the CPU clock. Voltage swing is set by the power connection to VDDQ3. PCI_F is not affected by the state of PCI_STOP#.                   |
| REF0:1      | 2, 3   | O        | <b>14.318-MHz Reference Clock Output:</b> 3.3V copies of the 14.318-MHz reference clock.  |
| IOAPIC0:2   | 53, 54, 55                                   | O        | <b>I/O APIC Clock Output:</b> Provides 16.67-MHz fixed frequency. The output voltage swing is set by the power connection to VDDQ2.   |
| 48MHz       | 30   | O        | <b>48-MHz Output:</b> Fixed 48-MHz USB output. Output voltage swing is controlled by voltage applied to VDDQ3.  |
| 3V66_0:3    | 21, 22, 25, 26                               | O        | <b>66-MHz Output 0 through 3:</b> Fixed 66-MHz outputs. Output voltage swing is controlled by voltage applied to VDDQ3.   |
| SEL0:1      | 32, 33                                       | I        | <b>Mode Select Input 0 through 1:</b> 3.3V LVTTTL-compatible input for selecting clock output modes.  |
| SEL133/100# | 28   | I        | <b>Frequency Selection Input:</b> 3.3V LVTTTL-compatible input that selects CPU output frequency as shown in Table 1.   |
| X1          | 5  | I        | <b>Crystal Connection or External Reference Frequency Input:</b> Connect to either a 14.318-MHz crystal or an external reference signal.  |
| X2          | 6  | O        | <b>Crystal Connection:</b> An output connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.  |
| SPREAD#     | 34   | I        | <b>Active LOW Spread Spectrum Enable:</b> 3.3V LVTTTL-compatible input that enables spread spectrum mode when held LOW.   |
| PWRDWN#     | 35   | I        | <b>Active LOW Power Down Input:</b> 3.3V LVTTTL-compatible asynchronous input that requests the device to enter power-down mode.  |
| CPU_STOP#   | 36   | I        | <b>Active LOW CPU Clock Stop:</b> 3.3V LVTTTL-compatible asynchronous input that stops all CPU and 3V66 clocks when held LOW. CPUdiv2 outputs are unaffected by this input.   |
| PCI_STOP#   | 37   | I        | <b>Active LOW PCI Clock Stop:</b> 3.3V LVTTTL-compatible asynchronous input that stops all PCI outputs except PCI_F when held LOW.  |
| VDDQ3       | 4, 10, 16, 23, 27, 31, 39                    | P        | <b>Power Connection:</b> Power supply for PCI output buffers, 48-MHz USB output buffer, Reference output buffers, 3V66 output buffers, core logic, and PLL circuitry. Connect to 3.3V supply.                         |
| VDDQ2       | 43, 47, 51, 56                               | P        | <b>Power Connection:</b> Power supply for IOAPIC, CPU, and CPUdiv2 output buffers. Connect to 2.5V supply.  |
| GND         | 1, 7, 13, 19, 20, 24, 29, 38, 40, 44, 48, 52 | G        | <b>Ground Connection:</b> Connect all ground pins to the common system ground plane.  |

**Overview**

The W158 is designed to provide the essential frequency sources to work with advanced multiprocessing Intel architecture platforms. Split voltage supply signaling provides 2.5V and 3.3V clock frequencies operating up to 133 MHz.

From a low-cost 14.31818-MHz reference crystal oscillator, the W158 generates 2.5V clock outputs to support CPUs, core logic chip set, and Direct RDRAM clock generators. It also provides skew-controlled PCI and IOAPIC clocks synchronous to CPU clock, 48-MHz Universal Serial Bus (USB) clock, and replicates the 14.31818-MHz reference clock.

All CPU, PCI, and IOAPIC clocks can be synchronously modulated for spread spectrum operations. Cypress employs proprietary techniques that provide the maximum EMI reduction while minimizing the clock skews that could reduce system timing margins. Spread Spectrum modulation is enabled by the active LOW control signal SPREAD#.

The W158 also includes power management control inputs. By using these inputs, system logic can stop CPU and/or PCI clocks or power down the entire device to conserve system power.

### Spread Spectrum Clocking

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 1*.

As shown in *Figure 1*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is:

$$dB = 6.5 + 9 \cdot \log_{10}(P) + 9 \cdot \log_{10}(F)$$

Where P is the percentage of deviation and F is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 2*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is -0.5% downspread. *Figure 2* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

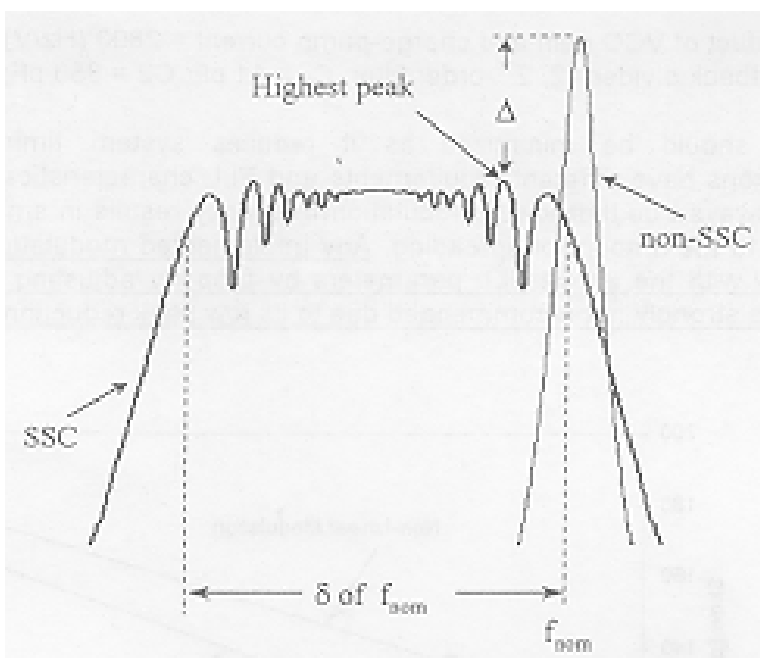


Figure 1. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

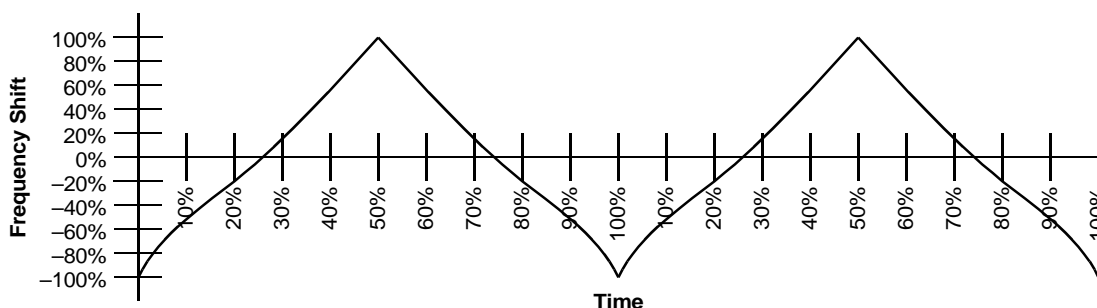


Figure 2. Modulation Waveform Profile

## Mode Selection Functions

The W158 supports the following operating modes controlled through the SEL133/100#, SEL0, and SEL1 inputs.

**Table 2. Select Functions**

| SEL133/100# | SEL1 | SEL0 | Function                            |
|-------------|------|------|-------------------------------------|
| 0           | 0    | 0    | All Outputs Three-State             |
| 0           | 0    | 1    | (Reserved)                          |
| 0           | 1    | 0    | Active 100-MHz, 48-MHz PLL Inactive |
| 0           | 1    | 1    | Active 100-MHz, 48-MHz PLL Active   |
| 1           | 0    | 0    | Test Mode                           |
| 1           | 0    | 1    | (Reserved)                          |
| 1           | 1    | 0    | Active 133-MHz, 48-MHz PLL Inactive |
| 1           | 1    | 1    | Active 133-MHz, 48-MHz PLL Active   |

**Table 3. Truth Table**

| SEL 133/100# | SEL1 | SEL0 | CPU     | CPUdiv2 | 3V66   | PCI    | 48MHz  | REF        | IOAPIC    | Notes   |
|--------------|------|------|---------|---------|--------|--------|--------|------------|-----------|---------|
| 0            | 0    | 0    | HI-Z    | HI-Z    | HI-Z   | HI-Z   | HI-Z   | HI-Z       | HI-Z      | 2       |
| 0            | 0    | 1    | n/a     | n/a     | n/a    | n/a    | n/a    | n/a        | n/a       |         |
| 0            | 1    | 0    | 100 MHz | 50 MHz  | 66 MHz | 33 MHz | HI-Z   | 14.318 MHz | 16.67 MHz | 3       |
| 0            | 1    | 1    | 100 MHz | 50 MHz  | 66 MHz | 33 MHz | 48 MHz | 14.318 MHz | 16.67 MHz | 4, 7, 8 |
| 1            | 0    | 0    | TCLK/2  | TCLK/4  | TCLK/4 | TCLK/8 | TCLK/2 | TCLK       | TCLK16    | 5, 6    |
| 1            | 0    | 1    | n/a     | n/a     | n/a    | n/a    | n/a    | n/a        | n/a       |         |
| 1            | 1    | 0    | 133 MHz | 66 MHz  | 66 MHz | 33 MHz | HI-Z   | 14.318 MHz | 16.67 MHz | 3       |
| 1            | 1    | 1    | 133 MHz | 66 MHz  | 66 MHz | 33 MHz | 48 MHz | 14.318 MHz | 16.67 MHz | 4, 7, 8 |

**Table 4. Maximum Supply Current**

| Condition  | Max. 2.5V supply consumption<br>Max. discrete cap loads,<br>V <sub>DDQ2</sub> =2.625V<br>All static inputs=V <sub>DDQ3</sub> or GND | Max. 3.3V supply consumption<br>Max. discrete cap loads,<br>V <sub>DDQ3</sub> =3.465V or GND |
|--|---|--|
| Powerdown Mode<br>(PWRDWN#=0)  | 100 $\mu$ A   | 200 $\mu$ A  |
| Full Active 100 MHz<br>SEL133/100#=0<br>SEL1, 0=11<br>CPU_STOP#, PCI_STOP#=1 | 75 mA   | 160 mA   |
| Full Active 133 MHz<br>SEL133/100#=0<br>SEL1, 0=11<br>CPU_STOP#, PCI_STOP#=1 | 90 mA   | 160 mA   |

**Notes:**

2. Provided for board level "bed of nails" testing.
3. 48-MHz PLL disabled to reduce component jitter.
4. Normal mode of operation.
5. TCLK is a test clock over driven on the X1 input during test mode. TCLK mode is based on 133-MHz CPU select logic.
6. Required for DC output impedance verification.
7. Range of reference frequency is min.=14.316, nominal = 14.31818 MHz, max.=14.32 MHz.
8. Frequency accuracy of 48 MHz is +167 PPM to match USB default.

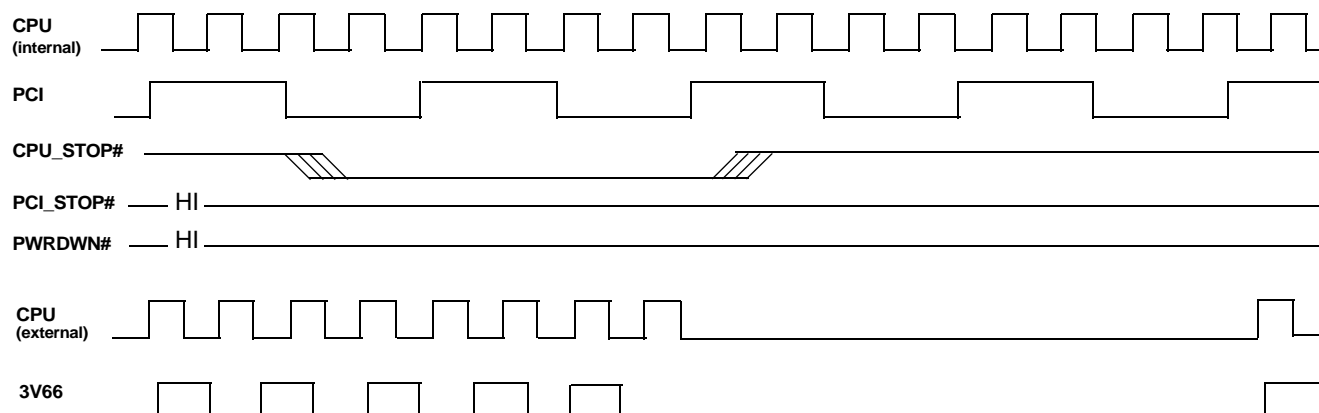
**Table 5. Clock Enable Configuration**<sup>[9, 10, 11, 12, 13, 14]</sup>

| CPU_STOP# | PWRDWN# | PCI_STOP# | CPU | CPUdiv2 | IOAPIC | 3V66 | PCI | PCI_F | REF, 48MHz | OSC. | VCOs |
|-----------|---------|-----------|-----|---------|--------|------|-----|-------|------------|------|------|
| X         | 0       | X         | LOW | LOW     | LOW    | LOW  | LOW | LOW   | LOW        | OFF  | OFF  |
| 0         | 1       | 0         | LOW | ON      | ON     | LOW  | LOW | ON    | ON         | ON   | ON   |
| 0         | 1       | 1         | LOW | ON      | ON     | LOW  | ON  | ON    | ON         | ON   | ON   |
| 1         | 1       | 0         | ON  | ON      | ON     | ON   | LOW | ON    | ON         | ON   | ON   |
| 1         | 1       | 1         | ON  | ON      | ON     | ON   | ON  | ON    | ON         | ON   | ON   |

**Table 6. Power Management State Transition**<sup>[15, 16]</sup>

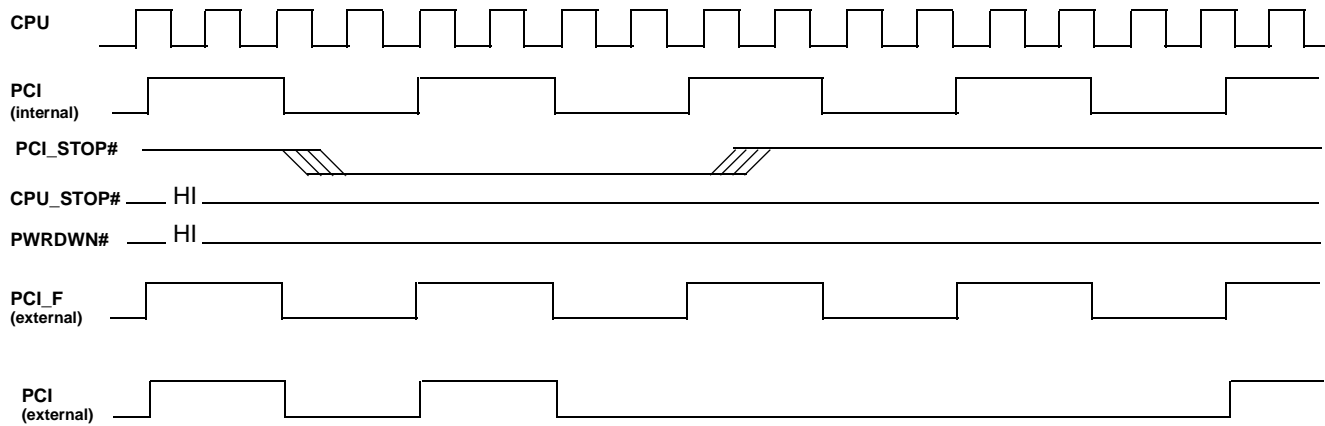
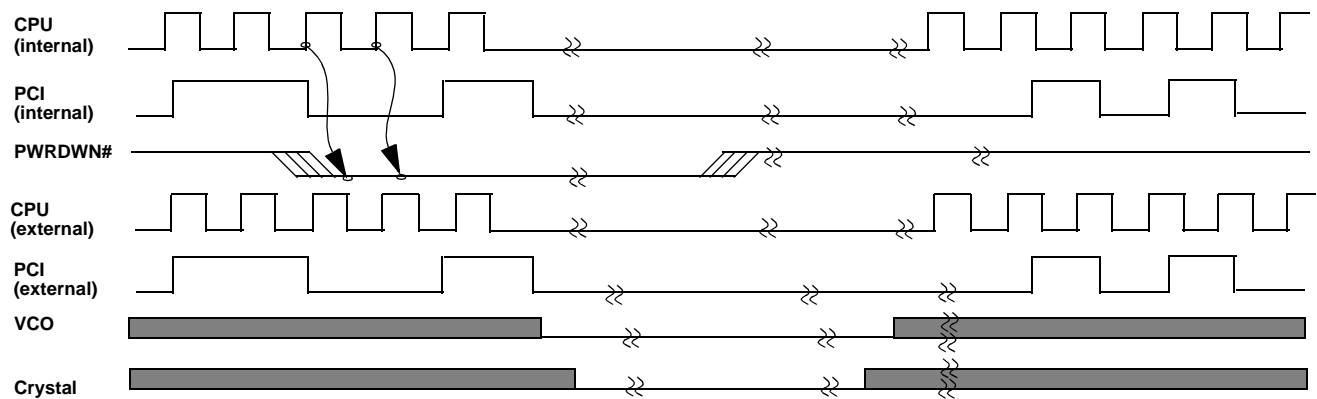
| Signal    | Signal State         | Latency                          |
|-----------|----------------------|----------------------------------|
|           |                      | No. of rising edges of PCI Clock |
| CPU_STOP# | 0 (disabled)         | 1                                |
|           | 1 (enabled)          | 1                                |
| PCI_STOP# | 0 (disabled)         | 1                                |
|           | 1 (enabled)          | 1                                |
| PWRDWN#   | 1 (normal operation) | 3 ms                             |
|           | 0 (power down)       | 2 max.                           |

## Timing Diagrams

**CPU\_STOP# Timing Diagram**<sup>[17, 18, 19, 20, 21, 22]</sup>


### Notes:

9. LOW means outputs held static LOW as per latency requirement below.
10. ON means active.
11. PWRDWN# pulled LOW, impacts all outputs including REF and 48-MHz outputs.
12. All 3V66 as well as all CPU clocks stop cleanly when CPU\_STOP# is pulled LOW.
13. CPUdiv2, IOAPIC, REF, 48MHz signals are not controlled by the CPU\_STOP# functionality and are enabled in all conditions except PWRDWN#=LOW.
14. An "x" indicates a "don't care" condition.
15. Clock on/off latency is defined in the number of rising edges of the free-running PCI clock between when the clock disable goes LOW/HIGH to when the first valid clock comes out of the device.
16. Power up latency is from when PWRDWN# goes inactive (HIGH) to when the first valid clocks are driven from the device.
17. All internal timing is referenced to the CPU clock.
18. The internal label means inside the chip and is a reference only. This, in fact, may not be the way that the control is designed.
19. CPU\_STOP# signal is an input signal that must be made synchronous to free-running PCI\_F.
20. 3V66 clocks also stop/start before.
21. PWRDWN# and PCI\_STOP# are shown in a HIGH state.
22. Diagrams shown with respect to 133 MHz. Similar operation when CPU clock is 100 MHz.

**Timing Diagrams (continued)**
**PCI\_STOP# Timing Diagram** [18, 22, 23, 24, 25, 26]

**PWRDWN# Timing Diagram** [18, 22, 23, 27, 28]

**Notes:**

23. All internal timing is referenced to the CPU clock.
24. PCI\_STOP# signal is an input signal that must be made synchronous to PCI\_F output.
25. All other clocks continue to run undisturbed.
26. PWRDWN# and CPU\_STOP# are shown in a HIGH state.
27. PWRDWN is an asynchronous input and metastable conditions could exist. This signal must be synchronized.
28. The shaded Sections on the VCO and the Crystal signals indicate an active clock.

**Absolute Maximum Ratings<sup>[29]</sup>**

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions

above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

| Parameter                         | Description                            | Rating       | Unit |
|-----------------------------------|--|--------------|------|
| V <sub>DD</sub> , V <sub>IN</sub> | Voltage on any pin with respect to GND | -0.5 to +7.0 | V    |
| T <sub>STG</sub>                  | Storage Temperature                    | -65 to +150  | °C   |
| T <sub>A</sub>                    | Operating Temperature                  | 0 to +70     | °C   |
| T <sub>B</sub>                    | Ambient Temperature under Bias         | -55 to +125  | °C   |
| ESD <sub>PROT</sub>               | Input ESD Protection                   | 2 (min.)     | kV   |

**DC Electrical Characteristics: T<sub>A</sub> = 0°C to +70°C, V<sub>DDQ3</sub> = 3.3V±5%, V<sub>DDQ2</sub> = 2.5V±5%**

| Parameter   | Description                                     | Test Condition                  | Min.        | Typ.        | Max.                     | Unit        |
|---|---|---------------------------------|-------------|-------------|--------------------------|-------------|
| <b>Supply Current</b>   |   |                                 |             |             |                          |             |
| I <sub>DD-3.3V</sub>  | Combined 3.3V Supply Current                    | CPU0:3 =133 MHz <sup>[30]</sup> |             |             | 160                      | mA          |
| I <sub>DD-2.5</sub>   | Combined 2.5V Supply Current                    | CPU0:3 =133 MHz <sup>[30]</sup> |             |             | 90                       | mA          |
| <b>Logic Inputs (All referenced to V<sub>DDQ3</sub> = 3.3V)</b> |   |                                 |             |             |                          |             |
| V <sub>IL</sub>   | Input Low Voltage                               |                                 | GND<br>-0.3 |             | 0.8                      | V           |
| V <sub>IH</sub>   | Input High Voltage                              |                                 | 2.0         |             | V <sub>DD</sub> +<br>0.3 | V           |
| I <sub>IL</sub>   | Input Low Current <sup>[31]</sup>               |                                 |             |             | -25                      | µA          |
| I <sub>IH</sub>   | Input High Current <sup>[31]</sup>              |                                 |             |             | 10                       | µA          |
| I <sub>IL</sub>   | Input Low Current, SEL133/100# <sup>[31]</sup>  |                                 |             |             | -5                       | µA          |
| I <sub>IH</sub>   | Input High Current, SEL133/100# <sup>[31]</sup> |                                 |             |             | 5                        | µA          |
| <b>Clock Outputs</b>  |   |                                 |             |             |                          |             |
| <b>CPU, CPUdiv2, IOAPIC (Referenced to V<sub>DDQ2</sub>)</b>    |   | <b>Test Condition</b>           | <b>Min.</b> | <b>Typ.</b> | <b>Max.</b>              | <b>Unit</b> |
| V <sub>OL</sub>   | Output Low Voltage                              | I <sub>OL</sub> = 1 mA          |             |             | 50                       | mV          |
| V <sub>OH</sub>   | Output High Voltage                             | I <sub>OH</sub> = -1 mA         | 2.2         |             |                          | V           |
| I <sub>OL</sub>   | Output Low Current                              | V <sub>OL</sub> = 1.25V         | 45          | 65          | 100                      | mA          |
| I <sub>OH</sub>   | Output High Current                             | V <sub>OH</sub> = 1.25V         | 45          | 65          | 100                      | mA          |
| <b>48MHz, REF (Referenced to V<sub>DDQ3</sub>)</b>              |   | <b>Test Condition</b>           | <b>Min.</b> | <b>Typ.</b> | <b>Max.</b>              | <b>Unit</b> |
| V <sub>OL</sub>   | Output Low Voltage                              | I <sub>OL</sub> = 1 mA          |             |             | 50                       | mV          |
| V <sub>OH</sub>   | Output High Voltage                             | I <sub>OH</sub> = -1 mA         | 3.1         |             |                          | V           |
| I <sub>OL</sub>   | Output Low Current                              | V <sub>OL</sub> = 1.5V          | 45          | 65          | 100                      | mA          |
| I <sub>OH</sub>   | Output High Current                             | V <sub>OH</sub> = 1.5V          | 45          | 65          | 100                      | mA          |
| <b>PCI, 3V66 (Referenced to V<sub>DDQ3</sub>)</b>               |   | <b>Test Condition</b>           | <b>Min.</b> | <b>Typ.</b> | <b>Max.</b>              | <b>Unit</b> |
| V <sub>OL</sub>   | Output Low Voltage                              | I <sub>OL</sub> = 1 mA          |             |             | 50                       | mV          |
| V <sub>OH</sub>   | Output High Voltage                             | I <sub>OH</sub> = -1 mA         | 3.1         |             |                          | V           |
| I <sub>OL</sub>   | Output Low Current                              | V <sub>OL</sub> = 1.5V          | 70          | 100         | 145                      | mA          |
| I <sub>OH</sub>   | Output High Current                             | V <sub>OH</sub> = 1.5V          | 65          | 95          | 135                      | mA          |

**Notes:**

29. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

30. All clock outputs loaded with 6" 60Ω transmission lines with 20-pF capacitors.

31. W158 logic inputs have internal pull-up devices, except SEL133/100# (pull-ups not CMOS level).

**DC Electrical Characteristics:**  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{DDQ3} = 3.3\text{V} \pm 5\%$ ,  $V_{DDQ2} = 2.5\text{V} \pm 5\%$ 

| Parameter                         | Description   | Test Condition     | Min. | Typ. | Max. | Unit |
|-----------------------------------|---|--------------------|------|------|------|------|
| <b>Crystal Oscillator</b>         |   |                    |      |      |      |      |
| $V_{TH}$                          | X1 Input threshold Voltage <sup>[32]</sup>                    |                    |      | 1.65 |      | V    |
| $C_{LOAD}$                        | Load Capacitance, Imposed on External Crystal <sup>[33]</sup> |                    |      | 18   |      | pF   |
| $C_{IN,X1}$                       | X1 Input Capacitance <sup>[34]</sup>                          | Pin X2 unconnected |      | 28   |      | pF   |
| <b>Pin Capacitance/Inductance</b> |   |                    |      |      |      |      |
| $C_{IN}$                          | Input Pin Capacitance   | Except X1 and X2   |      |      | 5    | pF   |
| $C_{OUT}$                         | Output Pin Capacitance  |                    |      |      | 6    | pF   |
| $L_{IN}$                          | Input Pin Inductance  |                    |      |      | 7    | nH   |

**3.3V AC Electrical Characteristics**

$T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{DDQ3} = 3.3\text{V} \pm 5\%$ ,  $V_{DDQ2} = 2.5\text{V} \pm 5\%$ ,  $f_{XTL} = 14.31818\text{ MHz}$   
**Spread Spectrum function turned off**

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.<sup>[35]</sup>

**3V66 Clock Outputs, 3V66\_0:3 (Lump Capacitance Test Load = 30 pF)**

| Parameter | Description  | Test Condition/Comments   | Min. | Typ. | Max. | Unit     |
|-----------|--|---|------|------|------|----------|
| f         | Frequency  | Note 36   |      | 66.6 |      | MHz      |
| $t_R$     | Output Rise Edge Rate                              | Measured from 0.4V to 2.4V  | 1    |      | 4    | V/ns     |
| $t_F$     | Output Fall Edge Rate                              | Measured from 2.4V to 0.4V  | 1    |      | 4    | V/ns     |
| $t_D$     | Duty Cycle   | Measured on rising and falling edge at 1.5V   | 45   |      | 55   | %        |
| $f_{ST}$  | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |      |      | 3    | ms       |
| $Z_o$     | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           |      | 15   |      | $\Omega$ |

**Notes:**

32. X1 input threshold voltage (typical) is  $V_{DD}/2$ .
33. The W158 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 18 pF; this includes typical stray capacitance of short PCB traces to crystal.
34. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).
35. Period, jitter, offset, and skew measured on rising edge at 1.5V.
36. 3V66 is CPU/2 for CPU = 133 MHz and (2 x CPU)/3 for CPU = 100 MHz.



**PCI Clock Outputs, PCI\_F and PCI1:7 (Lump Capacitance Test Load = 30 pF)**

| Parameter       | Description  | Test Condition/Comments   | Min. | Typ. | Max. | Unit |
|-----------------|--|---|------|------|------|------|
| t <sub>P</sub>  | Period   | Measured on rising edge at 1.5V <sup>[37]</sup>   | 30   |      |      | ns   |
| t <sub>H</sub>  | High Time  | Duration of clock cycle above 2.4V  | 12   |      |      | ns   |
| t <sub>L</sub>  | Low Time   | Duration of clock cycle below 0.4V  | 12   |      |      | ns   |
| t <sub>R</sub>  | Output Rise Edge Rate                              | Measured from 0.4V to 2.4V  | 1    |      | 4    | V/ns |
| t <sub>F</sub>  | Output Fall Edge Rate                              | Measured from 2.4V to 0.4V  | 1    |      | 4    | V/ns |
| t <sub>D</sub>  | Duty Cycle   | Measured on rising and falling edge at 1.5V   | 45   |      | 55   | %    |
| t <sub>JC</sub> | Jitter, Cycle-to-Cycle                             | Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.                      |      |      | 500  | ps   |
| t <sub>SK</sub> | Output Skew  | Measured on rising edge at 1.5V   |      |      | 500  | ps   |
| t <sub>O</sub>  | 3V66 to PCI Clock Skew                             | Covers all 3V66/PCI outputs. Measured on rising edge at 1.5V. 3V66 leads PCI output.                                | 1.5  |      | 3    | ns   |
| t <sub>q</sub>  | CPU to PCI Clock Skew                              | Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.                                  | 1.5  |      | 4    | ns   |
| f <sub>ST</sub> | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |      |      | 3    | ms   |
| Z <sub>O</sub>  | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           |      | 15   |      | Ω    |

**REF Clock Outputs, REF0:1 (Lump Capacitance Test Load = 20 pF)**

| Parameter       | Description  | Test Condition/Comments   | Min. | Typ.   | Max. | Unit |
|-----------------|--|---|------|--------|------|------|
| f               | Frequency, Actual                                  | Frequency generated by crystal oscillator   |      | 14.318 |      | MHz  |
| t <sub>R</sub>  | Output Rise Edge Rate                              | Measured from 0.4V to 2.4V  | 0.5  |        | 2    | V/ns |
| t <sub>F</sub>  | Output Fall Edge Rate                              | Measured from 2.4V to 0.4V  | 0.5  |        | 2    | V/ns |
| t <sub>D</sub>  | Duty Cycle   | Measured on rising and falling edge at 1.5V   | 45   |        | 55   | %    |
| f <sub>ST</sub> | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |      |        | 3    | ms   |
| Z <sub>O</sub>  | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           |      | 25     |      | Ω    |

**48-MHZ Clock Output (Lump Capacitance Test Load = 20 pF)**

| Parameter       | Description  | Test Condition/Comments   | Min. | Typ.   | Max. | Unit |
|-----------------|--|---|------|--------|------|------|
| f               | Frequency, Actual                                  | Determined by PLL divider ratio (see m/n below)   |      | 48.008 |      | MHz  |
| f <sub>D</sub>  | Deviation from 48 MHz                              | (48.008 – 48)/48  |      | +167   |      | ppm  |
| m/n             | PLL Ratio  | (14.31818 MHz x 57/17 = 48.008 MHz)   |      | 57/17  |      |      |
| t <sub>R</sub>  | Output Rise Edge Rate                              | Measured from 0.4V to 2.4V  | 0.5  |        | 2    | V/ns |
| t <sub>F</sub>  | Output Fall Edge Rate                              | Measured from 2.4V to 0.4V  | 0.5  |        | 2    | V/ns |
| t <sub>D</sub>  | Duty Cycle   | Measured on rising and falling edge at 1.5V   | 45   |        | 55   | %    |
| f <sub>ST</sub> | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |      |        | 3    | ms   |
| Z <sub>O</sub>  | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           |      | 25     |      | Ω    |

**Note:**

37. PCI clock is CPU/4 for CPU = 133 MHz and CPU/3 for CPU = 100 MHz.

## 2.5V AC Electrical Characteristics

$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ ,  $V_{DDQ3} = 3.3\text{V} \pm 5\%$ ,  $V_{DDQ2} = 2.5\text{V} \pm 5\%$

$f_{XTL} = 14.31818\text{ MHz}$

Spread Spectrum function turned off

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.<sup>[38]</sup>

### CPU Clock Outputs, CPU0:3 (Lump Capacitance Test Load = 20 pF)

| Parameter | Description  | Test Condition/Comments   | CPU = 133 MHz |      |      | CPU = 100 MHz |      |      | Unit     |
|-----------|--|---|---------------|------|------|---------------|------|------|----------|
|           |  |   | Min.          | Typ. | Max. | Min.          | Typ. | Max. |          |
| $t_P$     | Period   | Measured on rising edge at 1.25V  | 7.5           |      | 7.65 | 10            |      | 10.2 | ns       |
| $t_H$     | High Time  | Duration of clock cycle above 2.0V  | 1.87          |      |      | 3.0           |      |      | ns       |
| $t_L$     | Low Time   | Duration of clock cycle below 0.4V  | 1.67          |      |      | 2.8           |      |      | ns       |
| $t_R$     | Output Rise Edge Rate                              | Measured from 0.4V to 2.0V  | 1             |      | 4    | 1             |      | 4    | V/ns     |
| $t_F$     | Output Fall Edge Rate                              | Measured from 2.0V to 0.4V  | 1             |      | 4    | 1             |      | 4    | V/ns     |
| $t_D$     | Duty Cycle   | Measured on rising and falling edge at 1.25V  | 45            |      | 55   | 45            |      | 55   | %        |
| $t_{JC}$  | Jitter, Cycle-to-Cycle                             | Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.                     |               |      | 150  |               |      | 150  | ps       |
| $t_{SK}$  | Output Skew  | Measured on rising edge at 1.25V  |               |      | 175  |               |      | 175  | ps       |
| $f_{ST}$  | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |               |      | 3    |               |      | 3    | ms       |
| $Z_o$     | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           |               | 20   |      |               | 20   |      | $\Omega$ |

### CPUdiv2 Clock Outputs, CPUdiv2\_0:1 (Lump Capacitance Test Load = 20 pF)

| Parameter | Description  | Test Condition/Comments   | CPU = 133 MHz |      |      | CPU = 100 MHz |      |      | Unit     |
|-----------|--|---|---------------|------|------|---------------|------|------|----------|
|           |  |   | Min.          | Typ. | Max. | Min.          | Typ. | Max. |          |
| $t_P$     | Period   | Measured on rising edge at 1.25V  | 15            |      | 15.3 | 20            |      | 20.4 | ns       |
| $t_H$     | High Time  | Duration of clock cycle above 2.0V  | 5.25          |      |      | 7.5           |      |      | ns       |
| $t_L$     | Low Time   | Duration of clock cycle below 0.4V  | 5.05          |      |      | 7.3           |      |      | ns       |
| $t_R$     | Output Rise Edge Rate                              | Measured from 0.4V to 2.0V  | 1             |      | 4    | 1             |      | 4    | V/ns     |
| $t_F$     | Output Fall Edge Rate                              | Measured from 2.0V to 0.4V  | 1             |      | 4    | 1             |      | 4    | V/ns     |
| $t_D$     | Duty Cycle   | Measured on rising and falling edge at 1.25V  | 45            |      | 55   | 45            |      | 55   | %        |
| $t_{JC}$  | Jitter, Cycle-to-Cycle                             | Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.                     |               |      | 250  |               |      | 250  | ps       |
| $t_{SK}$  | Output Skew  | Measured on rising edge at 1.25V  |               |      | 175  |               |      | 175  | ps       |
| $f_{ST}$  | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |               |      | 3    |               |      | 3    | ms       |
| $Z_o$     | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           |               | 20   |      |               | 20   |      | $\Omega$ |

**Note:**

38. Period, Jitter, offset, and skew measured on rising edge at 1.25V.

**IOAPIC Clock Outputs, IOAPIC0:2 (Lump Capacitance Test Load = 20 pF)**

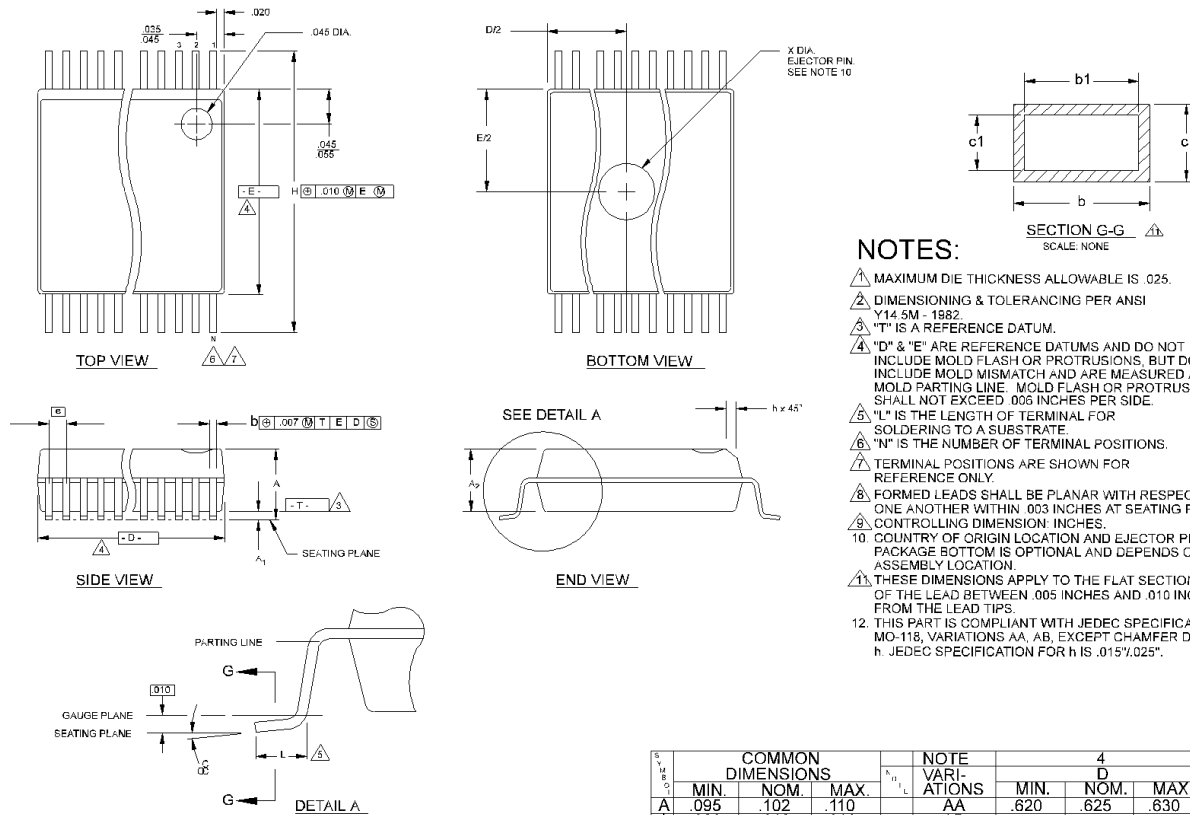
| Parameter       | Description  | Test Condition/Comments   | Min | Typ   | Max | Unit |
|-----------------|--|---|-----|-------|-----|------|
| f               | Frequency  | Note 39   |     | 16.67 |     | MHz  |
| t <sub>R</sub>  | Output Rise Edge Rate                              | Measured from 0.4V to 2.0V  | 1   |       | 4   | V/ns |
| t <sub>F</sub>  | Output Fall Edge Rate                              | Measured from 2.0V to 0.4V  | 1   |       | 4   | V/ns |
| t <sub>D</sub>  | Duty Cycle   | Measured on rising and falling edge at 1.25V  | 45  |       | 55  | %    |
| f <sub>ST</sub> | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |     |       | 3   | ms   |
| Z <sub>O</sub>  | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           |     | 20    |     | Ω    |

**Note:**

39. IOAPIC clock is CPU/8 for CPU = 133 MHz and CPU/6 for CPU = 100 MHz.

**Ordering Information**

| Ordering Code | Package Name | Package Type           |
|---------------|--------------|------------------------|
| W158          | H            | 56-pin SSOP (300 mils) |

**Package Diagram**
**56-Pin Small Shrink Outline Package (SSOP, 300 mils)**

**NOTES:**

- △ MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
- △ DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
- △ "T" IS A REFERENCE DATUM.
- △ "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
- △ "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
- △ "N" IS THE NUMBER OF TERMINAL POSITIONS.
- △ TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
- △ FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
- △ CONTROLLING DIMENSION: INCHES.
- 10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
- △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
- 12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"(.025").

**Summary of nominal dimensions in inches:**

**Body Width: 0.296**  
**Lead Pitch: 0.025**  
**Body Length: 0.625**  
**Body Height: 0.102**

| SYMBOL         | COMMON DIMENSIONS |      |       | NOTE VARIATIONS | 4    |      |      | 6  |
|----------------|-------------------|------|-------|-----------------|------|------|------|----|
|                | MIN.              | NOM. | MAX.  |                 | MIN. | NOM. | MAX. | N  |
| A              | .095              | .102 | .110  | AA              | .620 | .625 | .630 | 48 |
| A <sub>1</sub> | .088              | .090 | .092  | AB              | .720 | .725 | .730 | 56 |
| b              | .008              | .010 | .0135 |                 |      |      |      |    |
| b <sub>1</sub> | .008              | .010 | .012  |                 |      |      |      |    |
| c              | .005              | -    | .010  |                 |      |      |      |    |
| c <sub>1</sub> | .005              | .006 | .0085 |                 |      |      |      |    |
| D              | SEE VARIATIONS    |      |       | 4               |      |      |      |    |
| E              | .292              | .296 | .299  |                 |      |      |      |    |
| e              | .025 BSC          |      |       |                 |      |      |      |    |
| H              | .400              | .406 | .410  |                 |      |      |      |    |
| h              | .010              | .013 | .016  |                 |      |      |      |    |
| L              | .024              | .032 | .040  |                 |      |      |      |    |
| N              | SEE VARIATIONS    |      |       | 6               |      |      |      |    |
| X              | .085              | .093 | .100  | 10              |      |      |      |    |
| α              | 0°                | 5°   | 8°    |                 |      |      |      |    |

THIS TABLE IN INCHES

| SYMBOL         | COMMON DIMENSIONS |       |       | NOTE VARIATIONS | 4     |       |       | 6  |
|----------------|-------------------|-------|-------|-----------------|-------|-------|-------|----|
|                | MIN.              | NOM.  | MAX.  |                 | MIN.  | NOM.  | MAX.  | N  |
| A              | 2.41              | 2.59  | 2.79  | AA              | 15.75 | 15.88 | 16.00 | 48 |
| A <sub>1</sub> | 0.20              | 0.31  | 0.41  | AB              | 18.29 | 18.42 | 18.54 | 56 |
| b              | 0.203             | 0.254 | 0.343 |                 |       |       |       |    |
| b <sub>1</sub> | 0.203             | 0.254 | 0.305 |                 |       |       |       |    |
| c              | 0.127             | -     | 0.254 |                 |       |       |       |    |
| c <sub>1</sub> | 0.127             | 0.152 | 0.216 |                 |       |       |       |    |
| D              | SEE VARIATIONS    |       |       | 4               |       |       |       |    |
| E              | 7.42              | 7.52  | 7.59  |                 |       |       |       |    |
| e              | 0.635 BSC         |       |       |                 |       |       |       |    |
| H              | 10.16             | 10.31 | 10.41 |                 |       |       |       |    |
| h              | 0.25              | 0.33  | 0.41  |                 |       |       |       |    |
| L              | 0.61              | 0.81  | 1.02  |                 |       |       |       |    |
| N              | SEE VARIATIONS    |       |       | 6               |       |       |       |    |
| X              | 2.16              | 2.36  | 2.54  | 10              |       |       |       |    |
| α              | 0°                | 5°    | 8°    |                 |       |       |       |    |

THIS TABLE IN MILLIMETERS

**Document Title: W158 Spread Spectrum System Frequency Synthesizer**  
**Document Number: 38-07164**

| <b>REV.</b> | <b>ECN NO.</b> | <b>Issue Date</b> | <b>Orig. of Change</b> | <b>Description of Change</b>                                  |
|-------------|----------------|-------------------|------------------------|---|
| **          | 110274         | 11/04/01          | SZV                    | Change from Spec number: 38-00819 to 38-07164                 |
| *A          | 122805         | 12/14/02          | RBI                    | Add Power up Requirements to Operating Conditions Information |