



AOTF409

P-Channel Enhancement Mode Field Effect Transistor

General Description

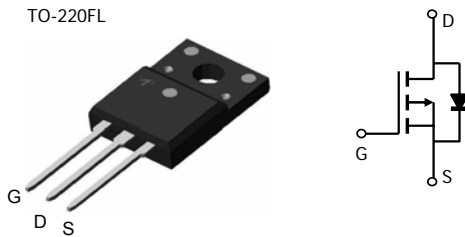
The AOTF409/L uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance. With the excellent thermal resistance of the TO220FL package, this device is well suited for high current load applications. AOTF409 and AOTF409L are electrically identical.

- RoHS Compliant
- AOTF409L Halogen Free

Features

V_{DS} (V) = -60V
 I_D = -24A (V_{GS} = -10V)
 $R_{DS(ON)}$ < 40m Ω (V_{GS} = -10V)
 $R_{DS(ON)}$ < 54m Ω (V_{GS} = -4.5V)

100% UIS Tested!



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	$T_C=25^\circ\text{C}$	-24	A
	$T_C=100^\circ\text{C}$	-17	
Pulsed Drain Current ^C	I_{DM}	-60	
Continuous Drain Current	$T_A=25^\circ\text{C}$	-5.4	A
	$T_A=70^\circ\text{C}$	-4.3	
Avalanche Current ^C	I_{AR}	-37	A
Repetitive avalanche energy $L=0.1\text{mH}^C$	E_{AR}	68	mJ
Power Dissipation ^B	$T_C=25^\circ\text{C}$	43	W
	$T_C=100^\circ\text{C}$	21	
Power Dissipation ^A	$T_A=25^\circ\text{C}$	2.16	W
	$T_A=70^\circ\text{C}$	1.38	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10\text{s}$	$R_{\theta JA}$	10	12	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A,D}	Steady-State		48.5	58	$^\circ\text{C/W}$
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	2.9	3.5	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-60			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-60\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1.2	-2.1	-2.4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}$, $V_{DS}=-5\text{V}$	-60			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$, $I_D=-20\text{A}$ $T_J=125^\circ\text{C}$		33	40	m Ω
		$V_{GS}=-4.5\text{V}$, $I_D=-20\text{A}$		52.4	63	
				43	54	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-20\text{A}$		33		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}$, $V_{GS}=0\text{V}$		-0.73	-1	V
I_S	Maximum Body-Diode Continuous Current				-30	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=-30\text{V}$, $f=1\text{MHz}$	1969	2461	2953	pF
C_{oss}	Output Capacitance		125	178	231	pF
C_{rss}	Reverse Transfer Capacitance		72	120	168	pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$	1	2	4.0	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge (10V)	$V_{GS}=-10\text{V}$, $V_{DS}=-30\text{V}$, $I_D=-20\text{A}$	34	43	52	nC
$Q_g(4.5\text{V})$	Total Gate Charge (4.5V)		16	19.7	24	nC
Q_{gs}	Gate Source Charge		8	10.2	12	nC
Q_{gd}	Gate Drain Charge		5	8.9	12.5	nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=-10\text{V}$, $V_{DS}=-30\text{V}$, $R_L=1.5\Omega$, $R_{GEN}=3\Omega$		12		ns
t_r	Turn-On Rise Time			14.5		ns
$t_{D(off)}$	Turn-Off Delay Time			38		ns
t_f	Turn-Off Fall Time			15		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-20\text{A}$, $di/dt=500\text{A}/\mu\text{s}$	18	25.68	33	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-20\text{A}$, $di/dt=500\text{A}/\mu\text{s}$	117	167.12	217	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on $T_{J(MAX)}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=175^\circ\text{C}$. The SOA curve provides a single pulse rating.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

Rev 0 : Aug-08

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

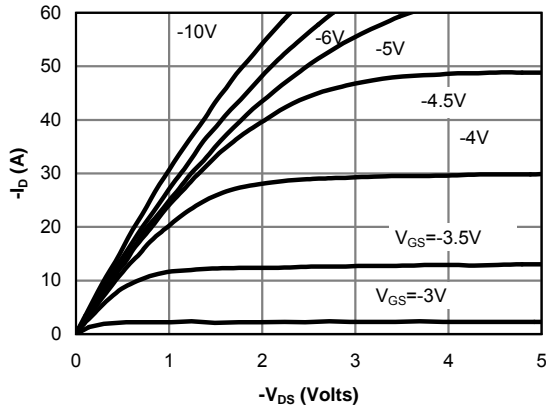


Fig 1: On-Region Characteristics (Note E)

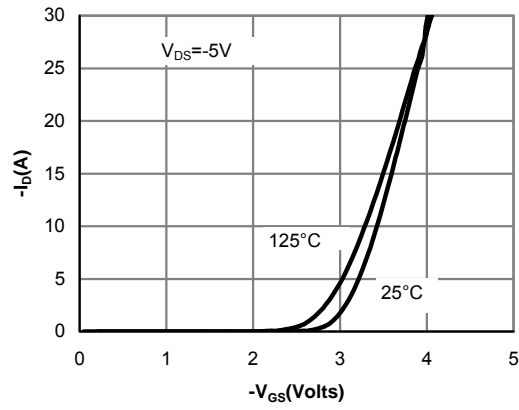


Figure 2: Transfer Characteristics (Note E)

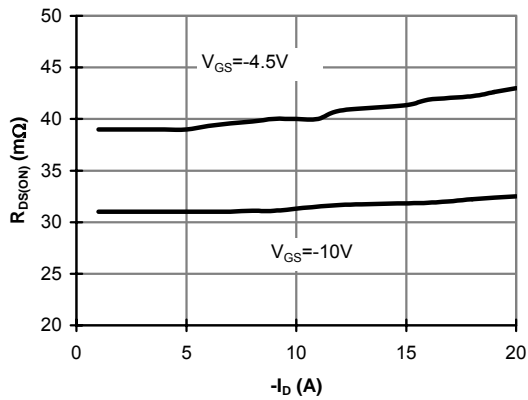


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

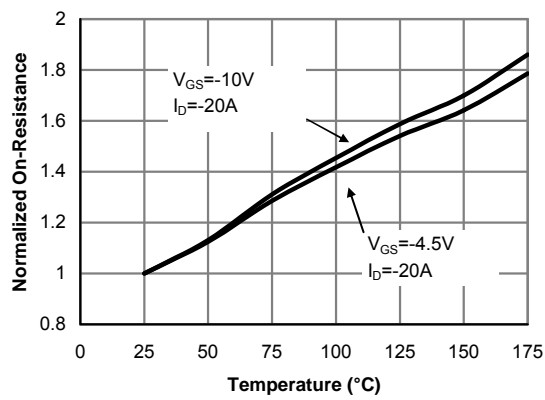


Figure 4: On-Resistance vs. Junction Temperature (Note E)

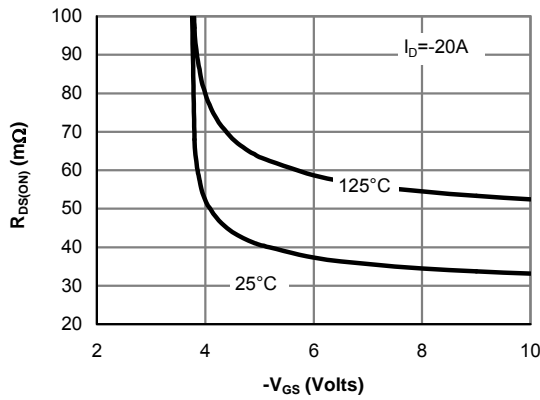


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

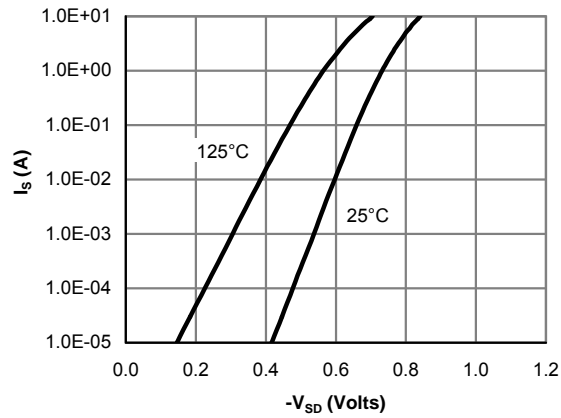


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

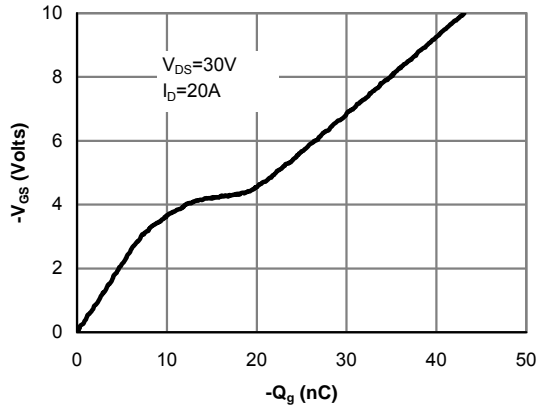


Figure 7: Gate-Charge Characteristics

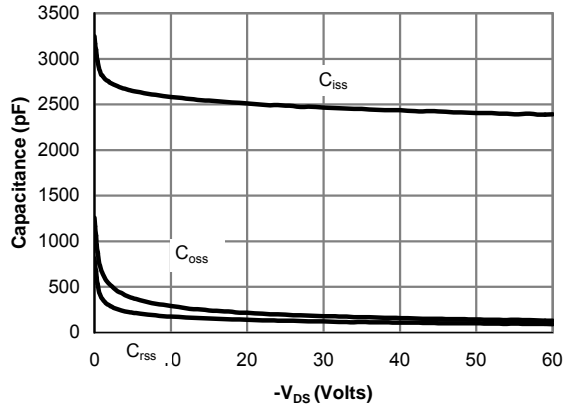


Figure 8: Capacitance Characteristics

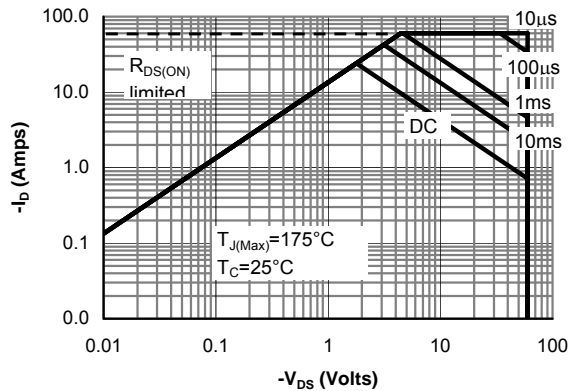


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

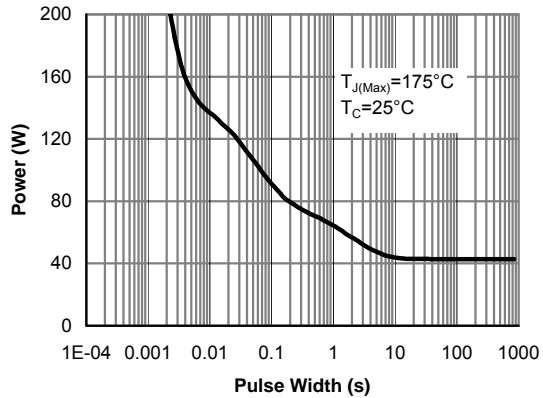


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

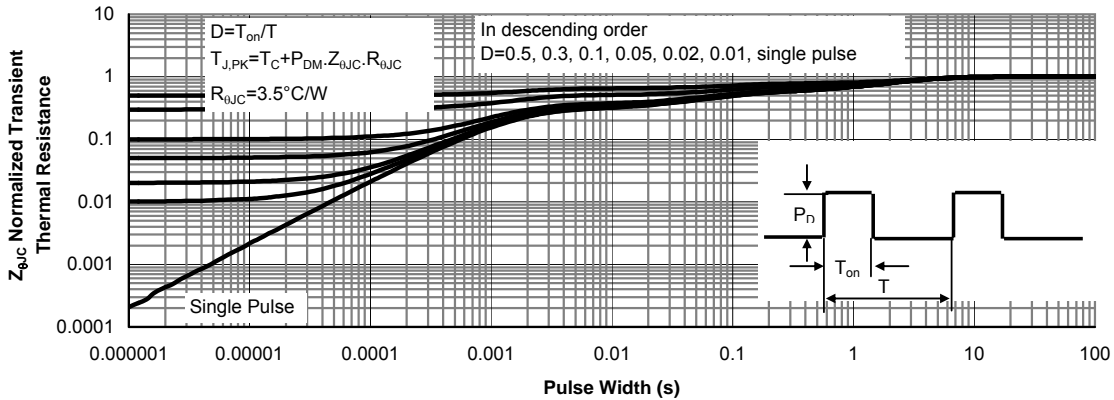


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

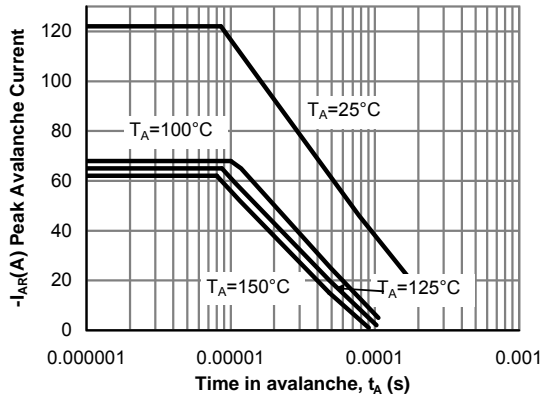


Figure 12: Single Pulse Avalanche capability (Note C)

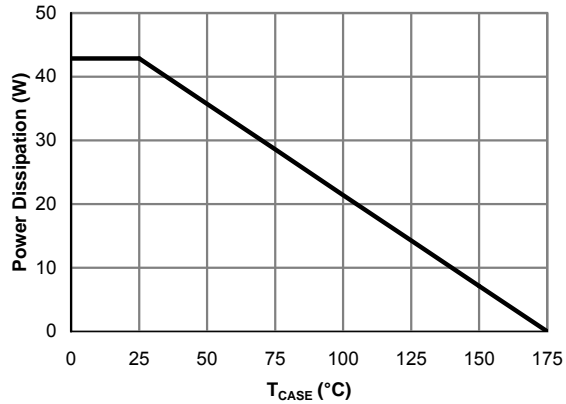


Figure 13: Power De-rating (Note F)

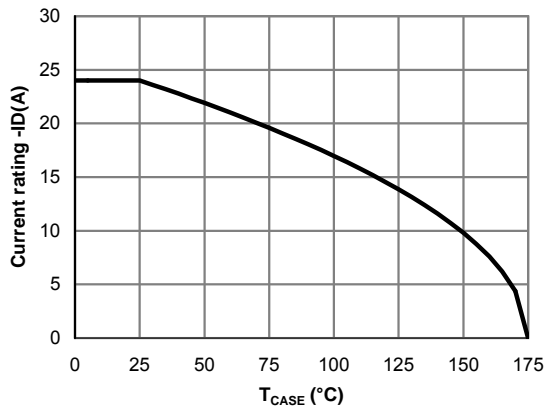


Figure 14: Current De-rating (Note F)

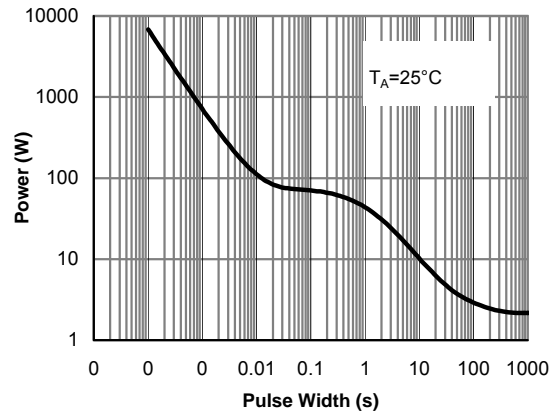


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

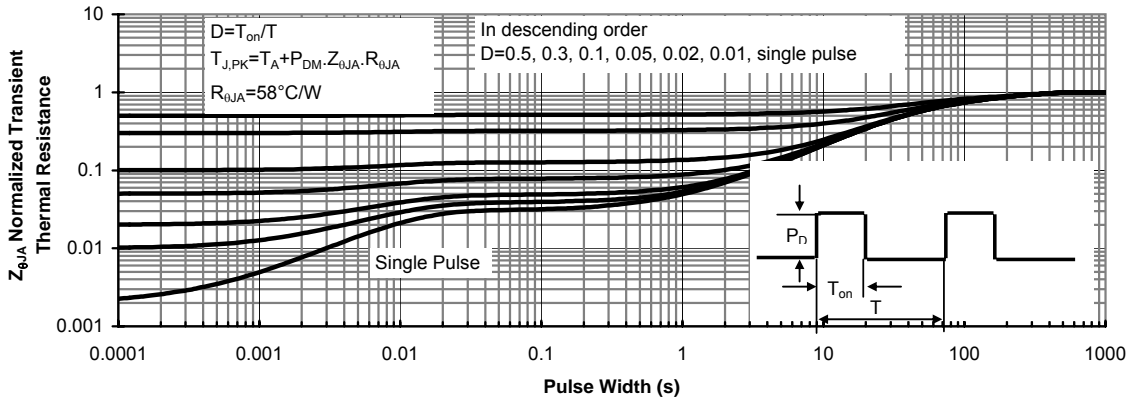
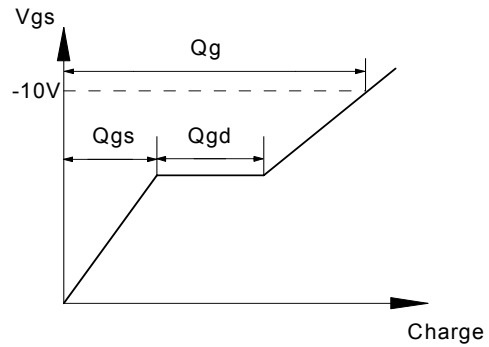
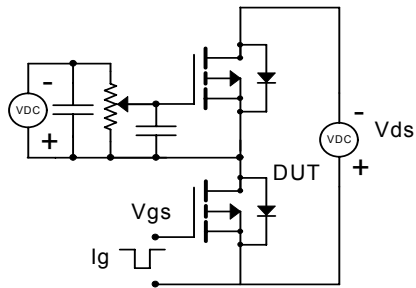
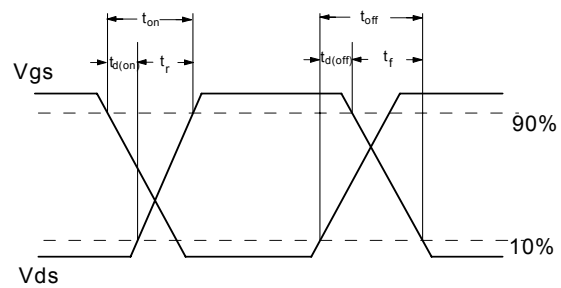
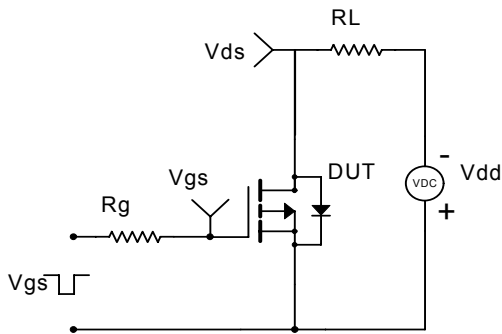


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

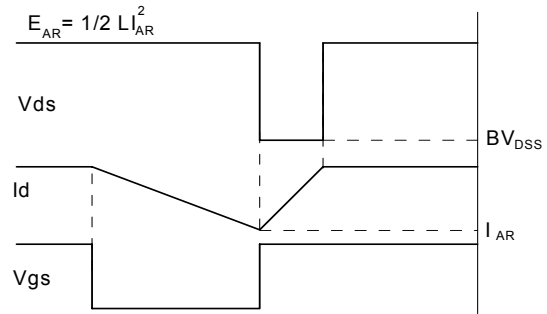
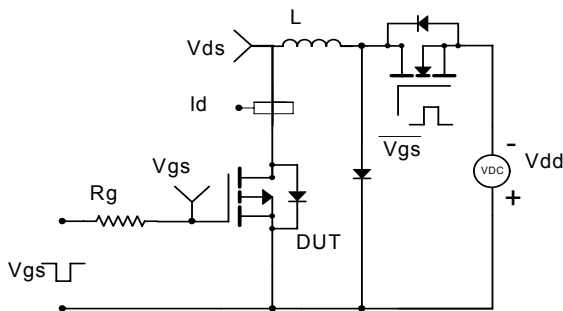
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

