

CRYSTAL CONTROLLED OSCILLATORS

3.3V SURFACE MOUNT CLOCK OSCILLATOR



FPLD54TE1

ABSOLUTE MAXIMUM RATINGS

TABLE 1.0

PARAMETER	UNITS	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Storage Temperature		-40	-	85	°C	
Supply Voltage	(Vcc)	-0.5	-	7.0	Vdc	
Enable/Disable Voltage	(Vc)	-0.5	-	Vcc+0.5	Vdc	

OPERATING SPECIFICATIONS

TABLE 2.0

PARAMETER		MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Center Frequency	(Fo)	-	622.08000 644.53125 666.51430 669.32660 672.16270	-	MHz	
Total Frequency Tolerance		-20	-	20	ppm	1
Operating Temperature Range		0	-	70	°C	
Supply Voltage	(Vcc)	3.135	3.3	3.465	Vdc	
Supply Current	(Icc)	-	-	100	mA	
Jitter (BW=10Hz to 20MHz)		-	-	5	ps rms	
Jitter (BW=12kHz to 80MHz)		-	-	1	ps rms	
SSB Phase Noise at 100Hz offset		-	-60	-	dBc/Hz	
SSB Phase Noise at 1KHz offset		-	-90	-	dBc/Hz	
SSB Phase Noise at 10KHz offset		-	-130	-	dBc/Hz	
SSB Phase Noise at 100KHz offset		-	-135	-	dBc/Hz	

INPUT CHARACTERISTICS

TABLE 3.0

PARAMETER		MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Enable Input Voltage (Low) (Default)	(Vil)	-	-	1.68	Vdc	2
Disable Input Voltage (High)	(Vih)	2.275	-	-	Vdc	2

LOW VOLTAGE PECL OUTPUT CHARACTERISTICS

TABLE 4.0

PARAMETER		MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
LOAD		-	-	50	Ohms	3
Voltage (High)	(Voh)	2.275	-	-	Vdc	
(Low)	(Vol)	-	-	1.68	Vdc	
Duty Cycle at 50% Level		45	50	55	%	
Rise / Fall Time 20% to 80%		-	-	1	nS	

PACKAGE CHARACTERISTICS

TABLE 5.0

Package	Non-hermetic package consisting of an FR4 substrate with grounded metal cover.
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PROCESS RECOMMENDATIONS

TABLE 6.0

Soldering Process	See solder profile on page 2.
Wash	Ultrasonic cleaning is not recommended.

Notes

- Inclusive of calibration @ 25°C, frequency stability vs. temperature, supply and load variations, shock, vibration and aging for twenty years. Control voltage (Vc) = 1.65 Vdc.
- When oscillator is disabled the true output is in a low state (Vol) and the complementary output is in the high state (Voh). Outputs are enabled with no connection on enable pad.
- 50 ohm termination into Vcc-2V or Thevein equivalent.

DESCRIPTION

The Connor-Winfield FPLD54TE1 is a 3.3V Clock Oscillator with Differential LVPECL outputs and Enable/Disable function. The FPLD54TE1 is designed for use with PLL systems in SONET/SDH systems requiring low jitter and tight frequency stability. No PLL multiplication schemes are used in this oscillator design.

FEATURES

LOW PROFILE, SURFACE MOUNT PACKAGE

3.3V OPERATION

LOW JITTER <1ps RMS

TOTAL FREQUENCY TOLERANCE ±20ppm

TEMPERATURE RANGE 0 to 70°C

DIFFERENTIAL LVPECL OUTPUTS

ENABLE / DISABLE FUNCTION

RoHS 5/6 COMPLIANT

ORDERING INFORMATION

FPLD54TE1 - 622.08M

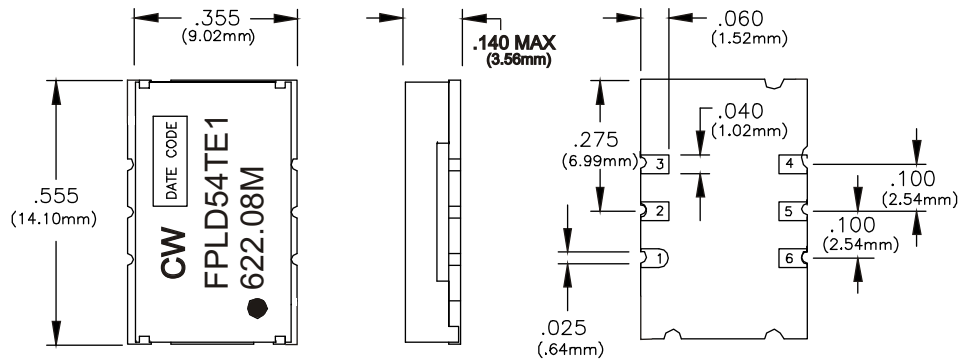
LVPECL
CLOCK
SERIES

CENTER
FREQUENCY

Specifications subject to change without notice.

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Package Outline

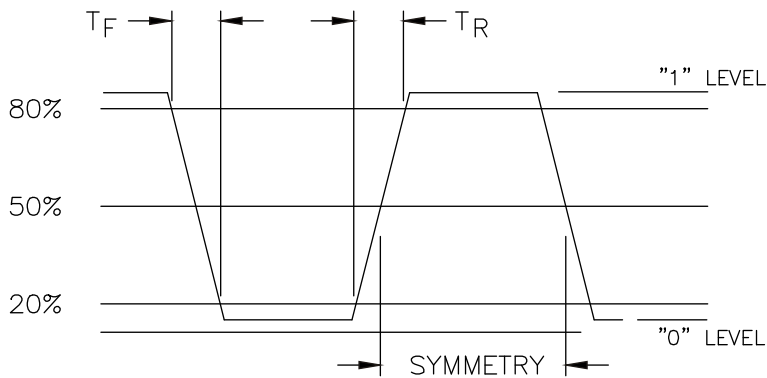


Pad Connections

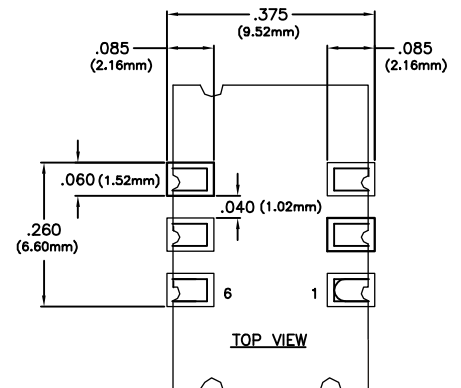
PIN	CONNECTION
1	N/C
2	ENABLE / DISABLE
3	GROUND
4	Q OUTPUT
5	\bar{Q} OUTPUT
6	Vcc

Dimensional Tolerance:
 $\pm .005$ (.127mm)

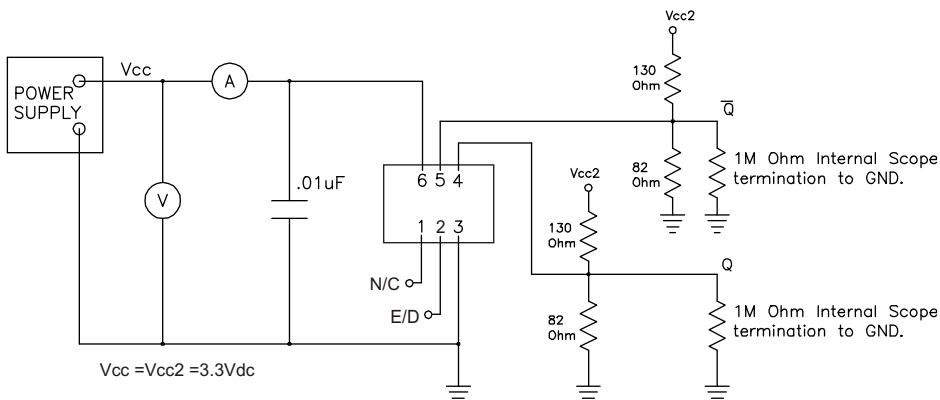
Output Waveform



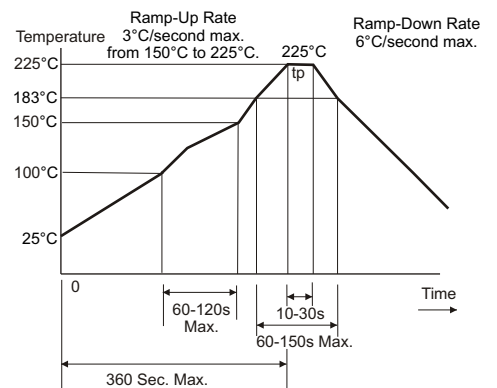
Suggested Pad Layout



Test Circuit



Solder Profile



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