

7 A V-I Chip EMI Filter

Description

The QPI-11 EMI filter is specifically designed to attenuate conducted common-mode (CM) and differential-mode (DM) noise of the VICOR V-I Chip products to comply with the CISPR22 standard requirements for conducted noise measurements. The filter is designed to operate up to 36 Vdc and supports 7 A loads up to 60°C without derating.

Designed for the military and industrial bus range, the V-I Chip EMI Filter supports the PICMG® 3.0 specification for filtering system boards to the EN55022 Class B limits.

Features

- >50 dB CM attenuation at 1 MHz
- >70 dB DM attenuation at 1 MHz
- 50 Vdc (max input)
- 100 Vdc surge 100 ms
- 750 Vdc Hi-pot hold off to shield plane
- 7 A rating
- 12.4 x 25 x 4.5 mm SiP (System-in-a-Package)
- Low profile LGA package
- -40° to +100°C PCB temperature (see Figure 6)
- Efficiency >99%

Applications

- COTS Military and Industrial
- V-I Chip input power filter



Figure 1 – QPI-11 actual size.

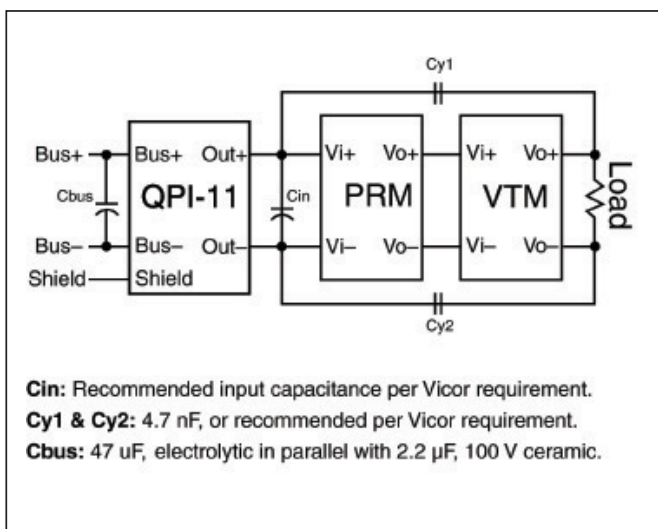


Figure 2 – QPI-11 Typical application schematic

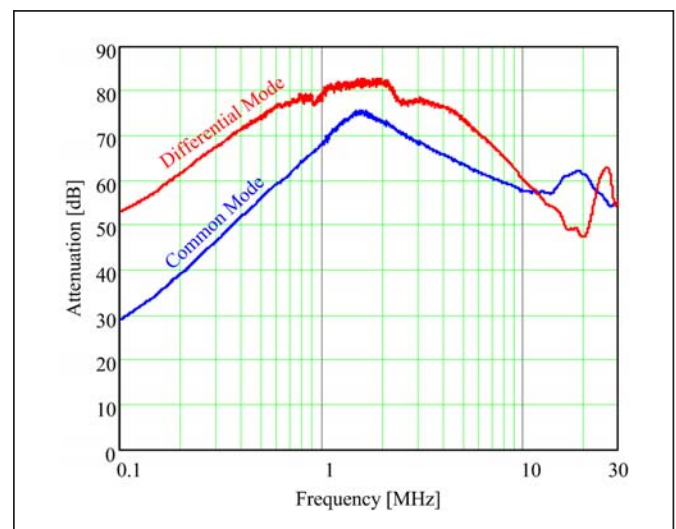


Figure 3 – QPI-11 network analyzer attenuation curves

EMI Performance

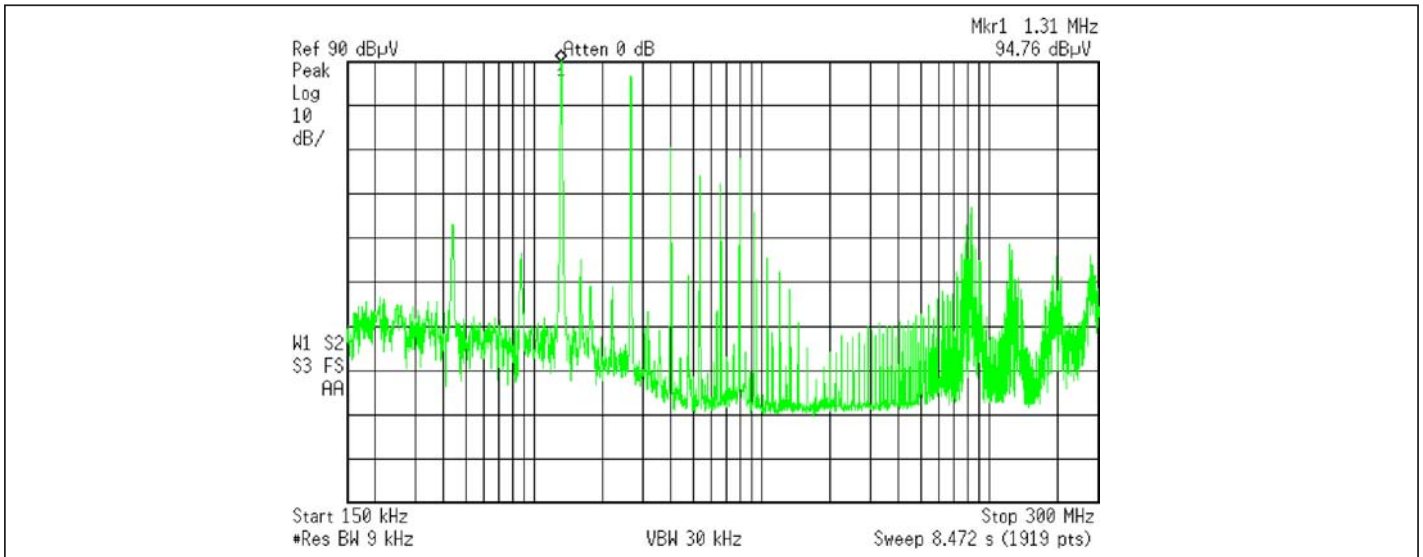


Figure 4 – Total Noise: PRM (MP028F036M12AL) and VTM (MV036F120M010) with 9.6 A load, no QPI-11.

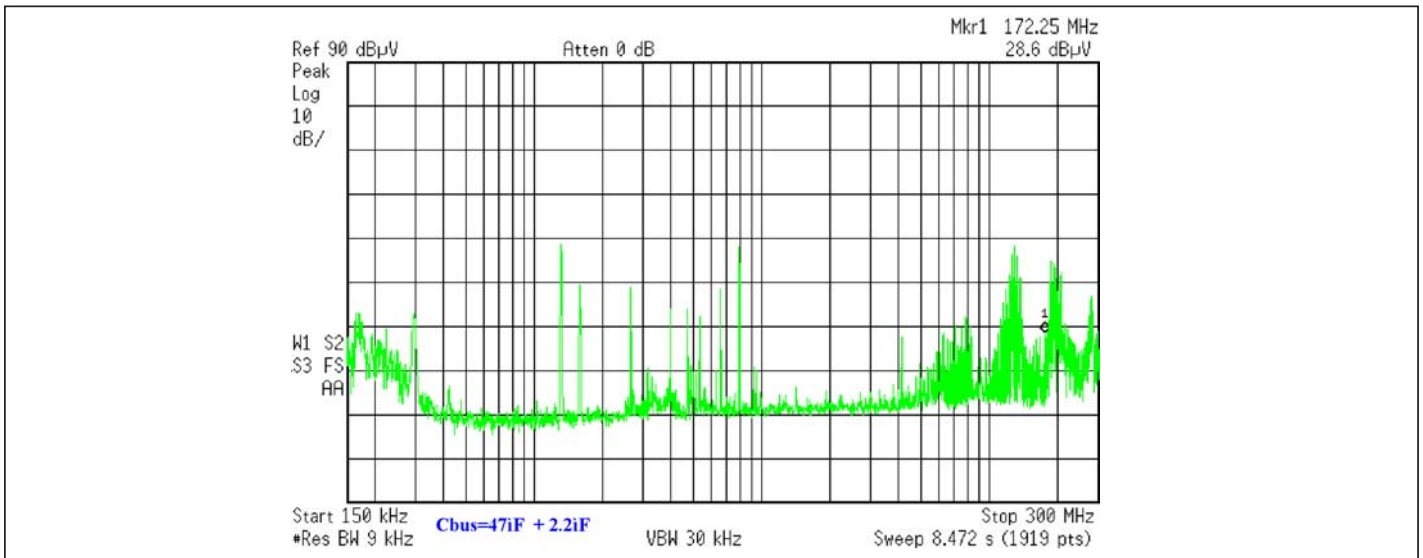


Figure 5 – Total Noise: PRM (MP028F036M12AL) and VTM (MV036F120M010) with 9.6 A load and QPI-11.

When laying out the QPI-11L, care must be taken such that the input and output signal polygons do not overlap each other on lower layers.

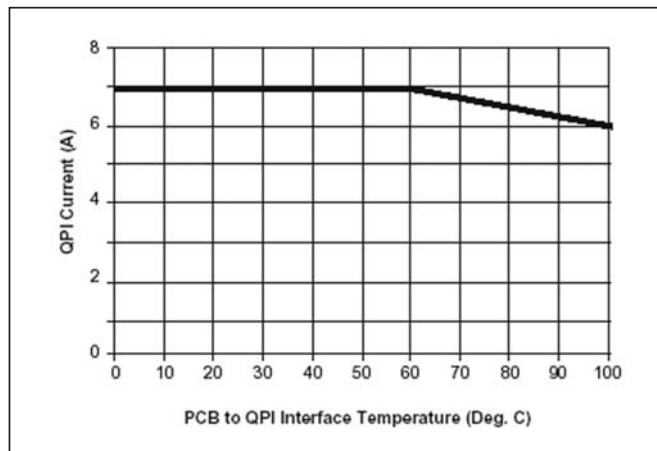


Figure 6 – Current vs. PCB temperature derating curve.

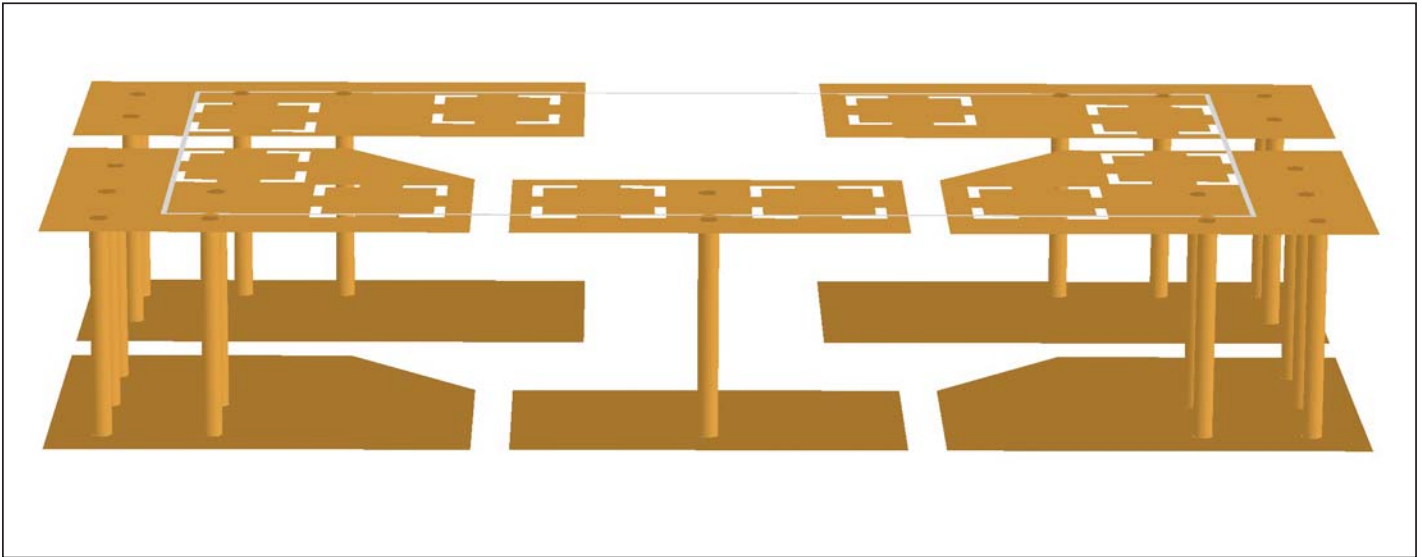


Figure 5 – Recommended mounting on a 2 layer board

QPI-11 PCB Layout Recommendations

The filtering performance of the QPI-11 and –12 is sensitive to capacitive coupling between its input and output pins. Parasitic plane capacitance must be kept below 1 pico-Farad between inputs and outputs using the layout shown above and the recommendations described below to achieve maximum conducted EMI performance.

To avoid capacitive coupling between input and output pins, there should not be any planes or large traces that run under both input and output pins, such as a ground plane or power plane. For example, if there are two signal planes or large traces where one trace runs under the input pins, and the other under the output pins, and both planes overlap in another area, they will cause capacitive coupling between input and output pins. Also, planes that run under both input and outputs pins, but do not cross, can cause capacitive coupling if they are capacitively by-passed together.

Figure 5 shows the recommended pcb layout on a 2 layer board. Here, the top layer planes are duplicated on the bottom layer so that there can be no overlapping of input and output planes. This method can be used for boards of greater layer count.

Post Solder Cleaning

Picor lidded QP SIPs are not hermetically sealed and must not be exposed to liquid, including but not limited to cleaning solvents, aqueous washing solutions or pressurized sprays.

When soldering, it is recommended that no-clean flux solder be used, as this will insure that potentially corrosive mobile ions will not remain on, around, or under the module following the soldering process.

For applications requiring water wash compatibility the “-01” open frame version should be used.

Vicor's comprehensive line of power solutions includes high-density AC-DC & DC-DC modules and accessory components, fully configurable AC-DC & DC-DC power supplies, and complete custom power systems.

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