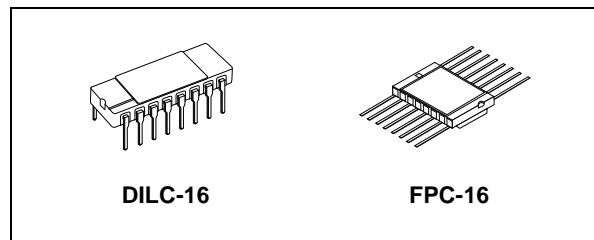


RAD-HARD DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED :
 $f_{MAX} = 67\text{MHz}$ (TYP.) at $V_{CC} = 6\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 2\mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4\text{mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES 109
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS IRRADIATION
- DEVICE FULLY COMPLIANT WITH SCC-9306-048

DESCRIPTION

The M54HC109 is an high speed CMOS DUAL J-K FLIP FLOP WITH PRESET AND CLEAR fabricated with silicon gate C²MOS technology. In accordance with the logic level on the J and K



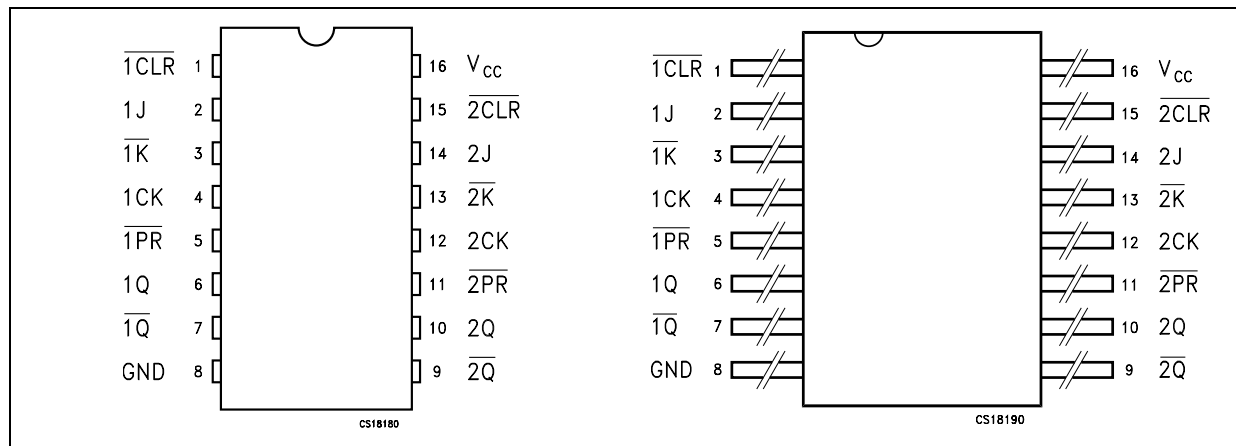
ORDER CODES

PACKAGE	FM	EM
DILC	M54HC109D	M54HC109D1
FPC	M54HC109K	M54HC109K1

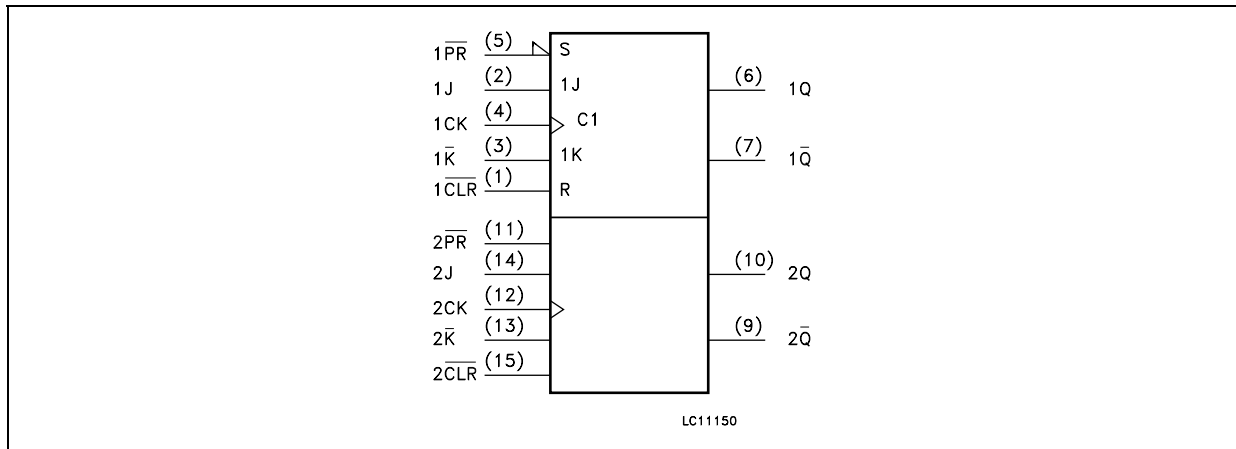
input this device changes state on positive going transition of the clock pulse. CLEAR and PRESET are independent of the clock and are accomplished by a logic low on the corresponding input.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

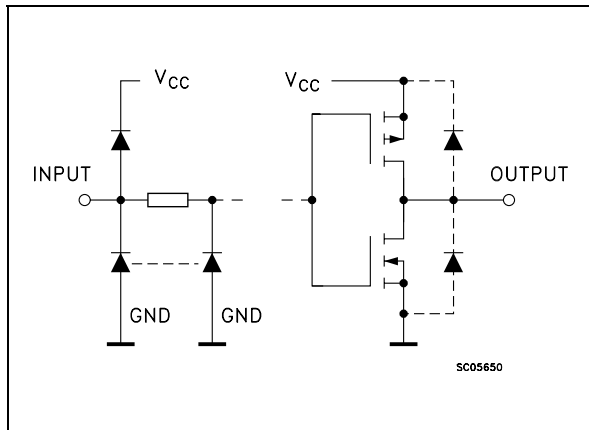
PIN CONNECTION



IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

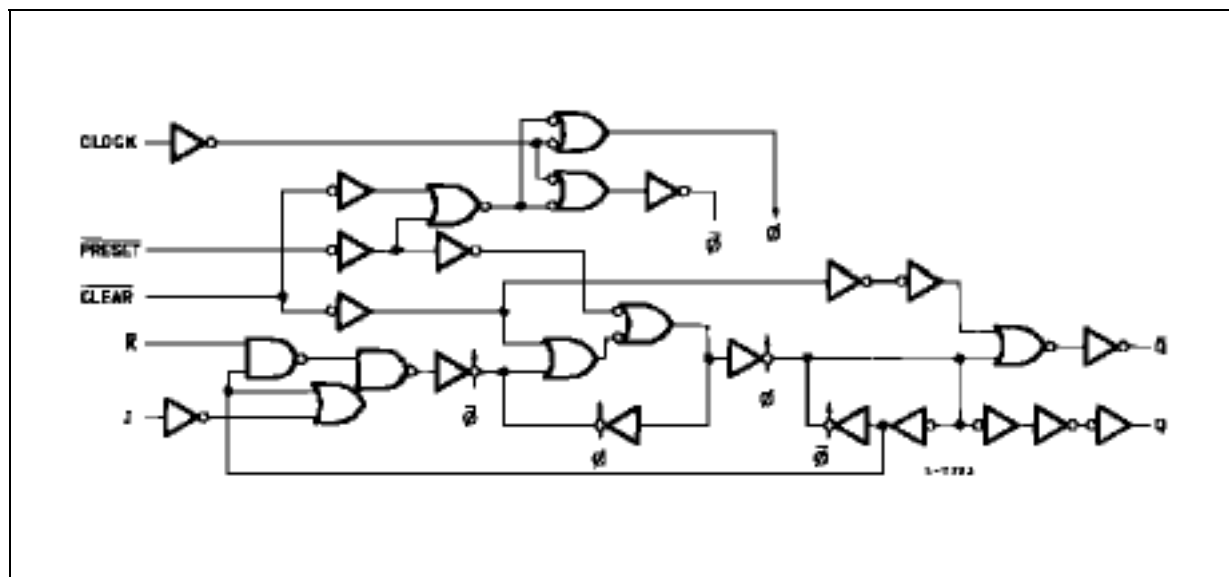
PIN N°	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{1CLR}, \overline{2CLR}$	Asynchronous Reset Direct Input
2, 14, 3, 13	$1J, \overline{2J}, \overline{1K}, 2K$	Synchronous Inputs; Flip-Flops 1 and 2
4, 12	$1CK, 2CK$	Clock Input
5, 11	$\overline{1PR}, \overline{2PR}$	Asynchronous Set Direct Input (Active Low)
6, 10	$1Q, 2Q$	True Flip-Flop Outputs
7, 9	$\overline{1Q}, \overline{2Q}$	Complement Flip-Flop Outputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
\overline{CLR}	\overline{PR}	J	\overline{K}	CK	Q	\overline{Q}	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	----
H	H	L	H		Qn	\overline{Qn}	NO CHANGE
H	H	L	L		L	H	----
H	H	H	H		H	L	----
H	H	H	L		\overline{Qn}	Qn	TOGGLE
H	H	X	X		Qn	\overline{Qn}	NO CHANGE

X : Don't Care

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	300	mW
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$
T_L	Lead Temperature (10 sec)	265	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V_{CC}	Supply Voltage	2 to 6	V	
V_I	Input Voltage	0 to V_{CC}	V	
V_O	Output Voltage	0 to V_{CC}	V	
T_{op}	Operating Temperature	-55 to 125	$^{\circ}C$	
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V _{OH}	High Level Output Voltage	2.0	I _O =-20 μA	1.9	2.0		1.9		1.9		V
		4.5	I _O =-20 μA	4.4	4.5		4.4		4.4		
		6.0	I _O =-20 μA	5.9	6.0		5.9		5.9		
		4.5	I _O =-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I _O =-5.2 mA	5.68	5.8		5.63		5.60		
V _{OL}	Low Level Output Voltage	2.0	I _O =20 μA		0.0	0.1		0.1		0.1	V
		4.5	I _O =20 μA		0.0	0.1		0.1		0.1	
		6.0	I _O =20 μA		0.0	0.1		0.1		0.1	
		4.5	I _O =4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I _O =5.2 mA		0.18	0.26		0.33		0.40	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND			2		20		40	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

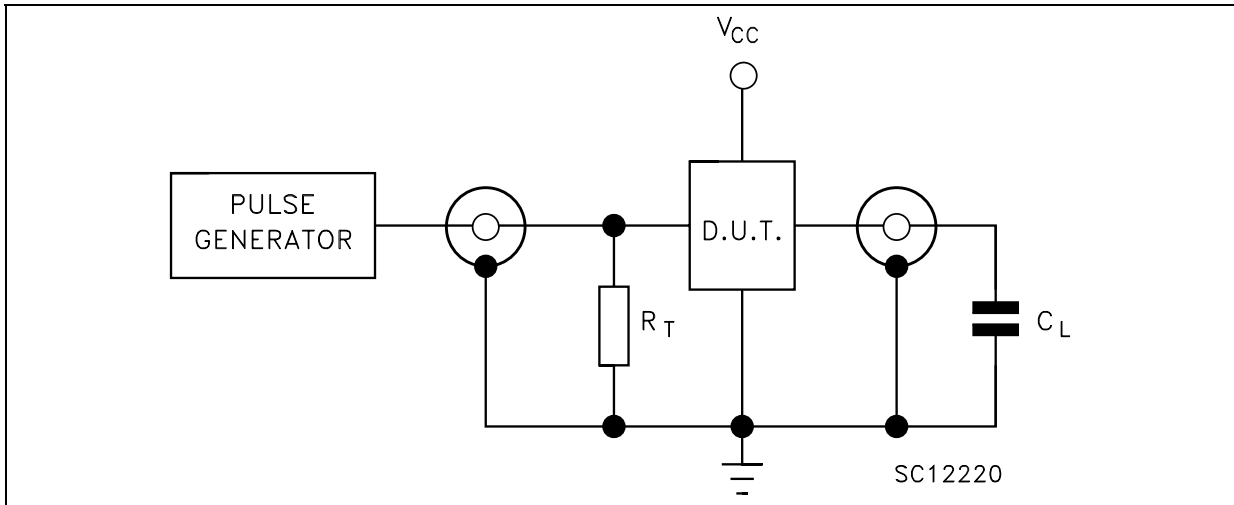
Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CK - Q, \bar{Q})	2.0			50	150		190		225	ns
		4.5			16	30		38		45	
		6.0			13	26		32		38	
t_{PLH} t_{PHL}	Propagation Delay Time (CLR, PR - Q, \bar{Q})	2.0			50	150		190		225	ns
		4.5			16	30		38		45	
		6.0			13	26		32		38	
f_{MAX}	Maximum Clock Frequency	2.0		6.2	17		5		4.2		MHz
		4.5		31	59		25		21		
		6.0		37	67		30		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK)	2.0			15	75		95		110	ns
		4.5			6	15		19		22	
		6.0			6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (CLR, PR)	2.0			15	75		95		110	ns
		4.5			6	15		19		22	
		6.0			6	13		16		19	
t_s	Minimum Set-Up Time	2.0			17	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time (CLR, PR)	2.0			13	50		65		75	ns
		4.5			4	10		13		15	
		6.0			3	9		11		13	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C_{IN}	Input Capacitance	5.0			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			41						pF

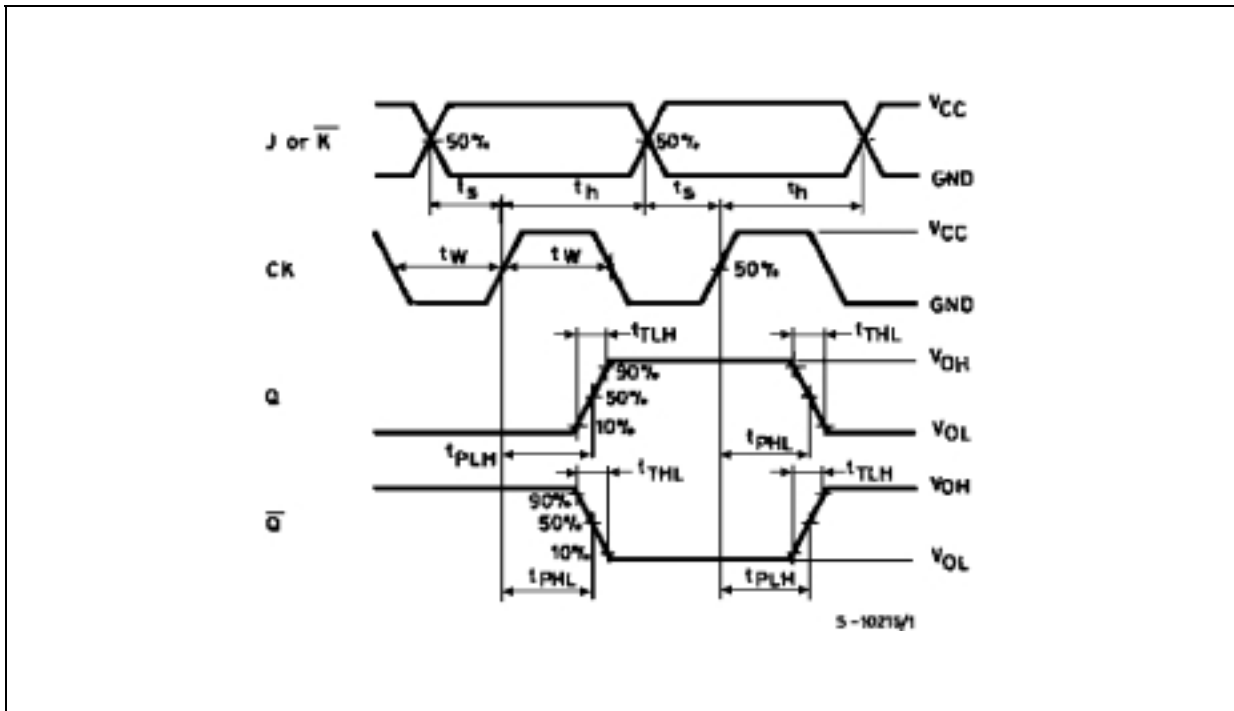
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

TEST CIRCUIT

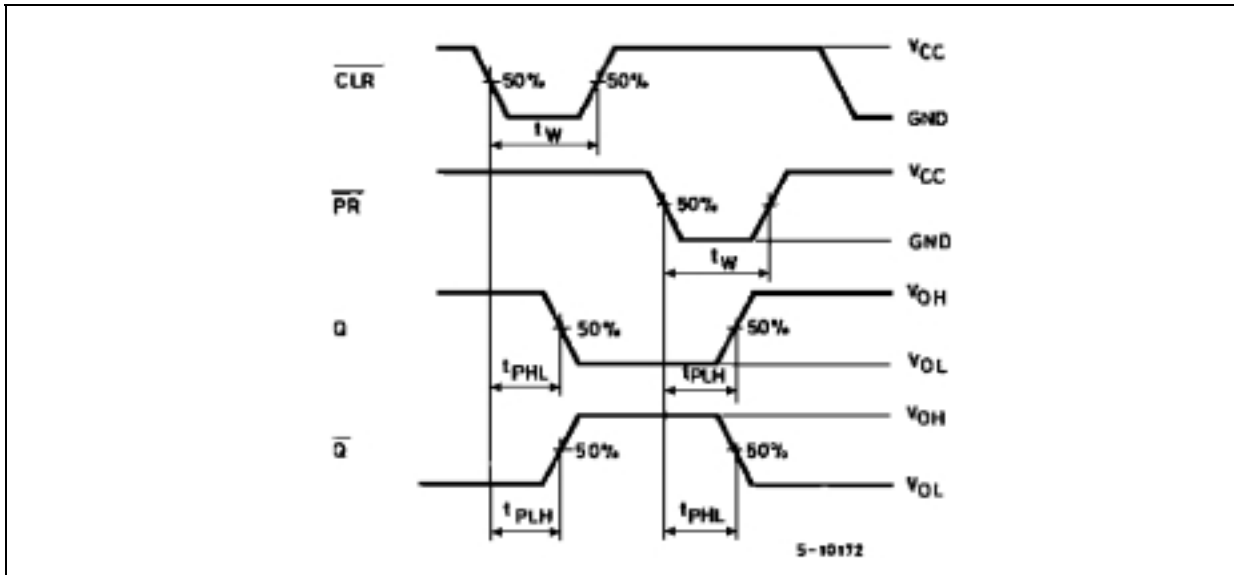


$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

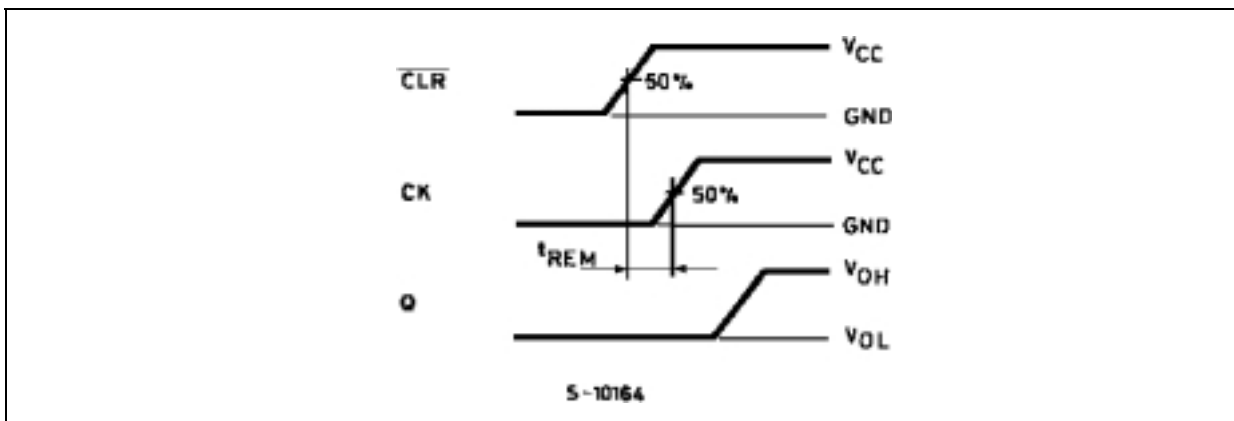
WAVEFORM 1: PROPAGATION DELAY TIMES, SETUP AND HOLD TIMES, MINIMUM PULSE WIDTH (CK) ($f=1\text{MHz}$; 50% duty cycle)



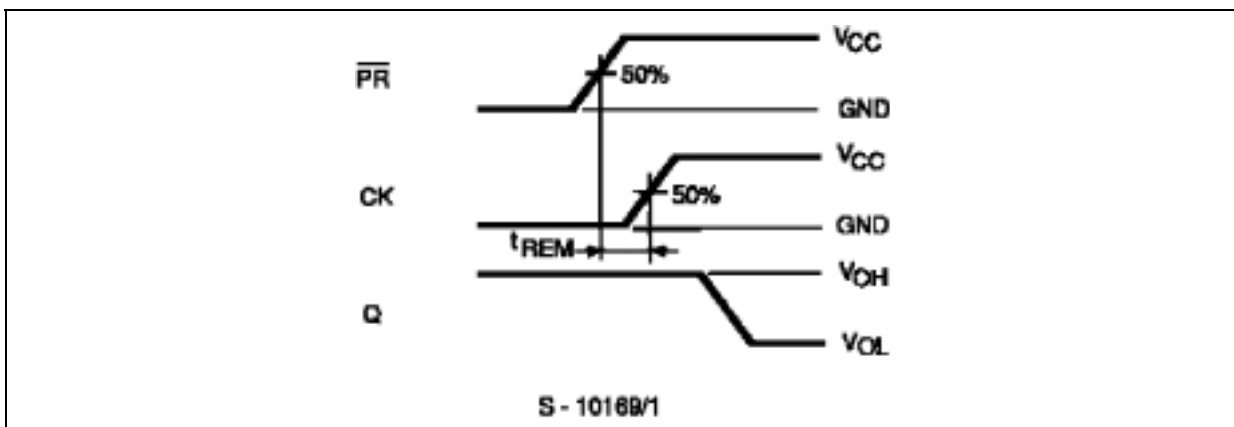
WAVEFORM 2 : PROPAGATION DELAY TIMES , MINIMUM PULSE WIDTH ($\overline{\text{CLR}}$), ($\overline{\text{PR}}$)
(f=1MHz; 50% duty cycle)



WAVEFORM 3 : MINIMUM REMOVAL TIME ($\overline{\text{CLR}}$ to CK) (f=1MHz; 50% duty cycle)

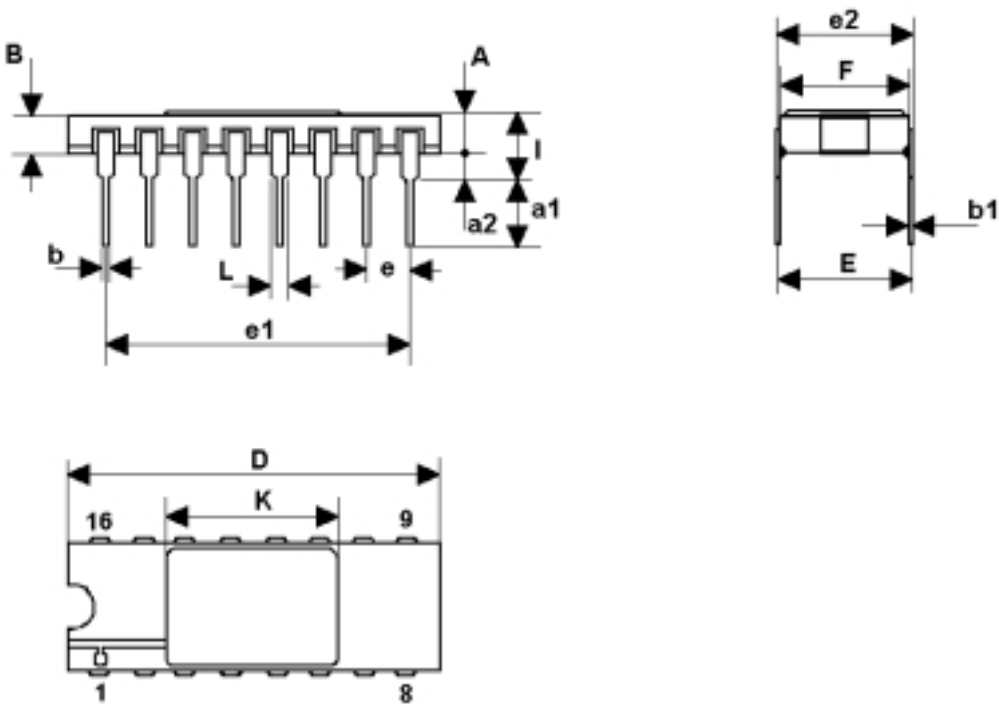


WAVEFORM 4 : MINIMUM REMOVAL TIME ($\overline{\text{PR}}$ to CK) (f=1MHz; 50% duty cycle)



DILC-16 MECHANICAL DATA

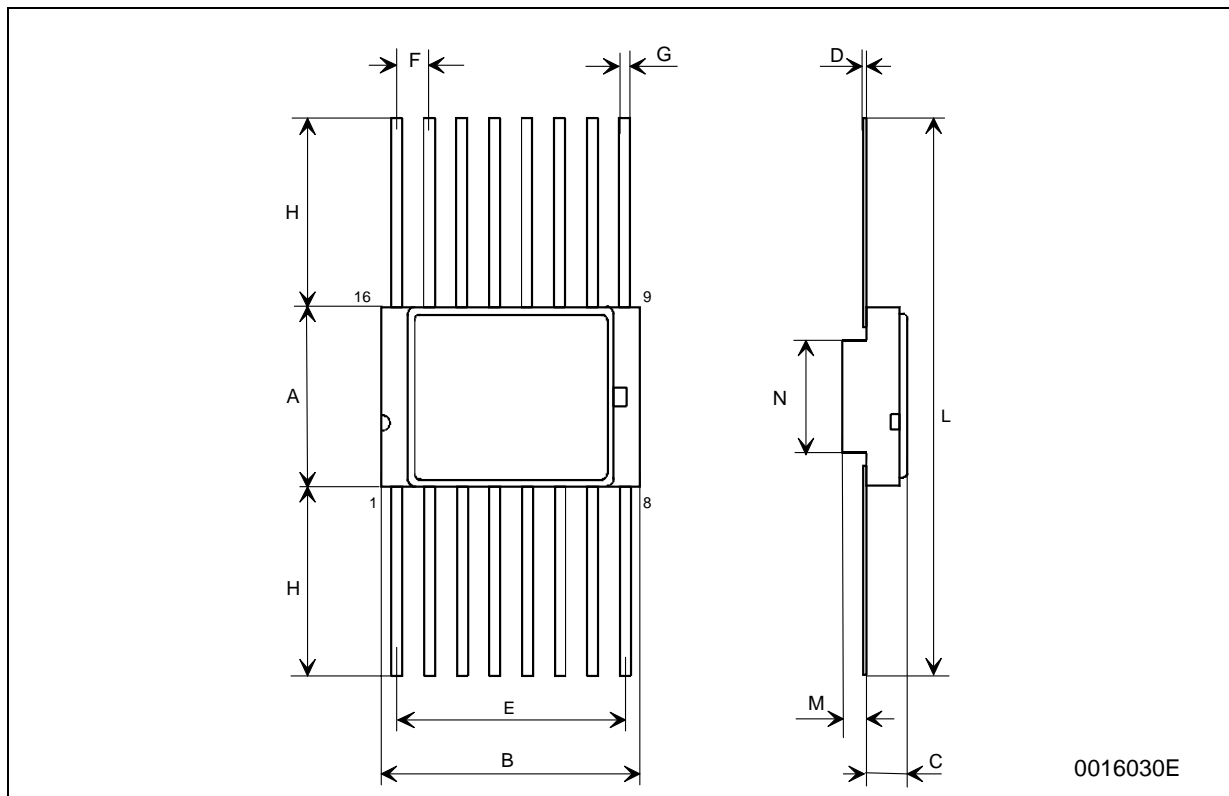
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.1		2.71	0.083		0.107
a1	3.00		3.70	0.118		0.146
a2	0.63	0.88	1.14	0.025	0.035	0.045
B	1.82		2.39	0.072		0.094
b	0.40	0.45	0.50	0.016	0.018	0.020
b1	0.20	0.254	0.30	0.008	0.010	0.012
D	20.06	20.32	20.58	0.790	0.800	0.810
e	7.36	7.62	7.87	0.290	0.300	0.310
e1		2.54			0.100	
e2	17.65	17.78	17.90	0.695	0.700	0.705
e3	7.62	7.87	8.12	0.300	0.310	0.320
F	7.29	7.49	7.70	0.287	0.295	0.303
I			3.83			0.151
K	10.90		12.1	0.429		0.476
L	1.14		1.5	0.045		0.059



0056437F

FPC-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	6.75	6.91	7.06	0.266	0.272	0.278
B	9.76	9.94	10.14	0.384	0.392	0.399
C	1.49		1.95	0.059		0.077
D	0.102	0.127	0.152	0.004	0.005	0.006
E	8.76	8.89	9.01	0.345	0.350	0.355
F		1.27			0.050	
G	0.38	0.43	0.48	0.015	0.017	0.019
H	6.0			0.237		
L	18.75		22.0	0.738		0.867
M	0.33	0.38	0.43	0.013	0.015	0.017
N		4.31			0.170	



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