19-3164; Rev 3; 7/07

EVALUATION KIT AVAILABLE

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

General Description

The MAX5580–MAX5585 quad, 12-/10-/8-bit, voltage-output, digital-to-analog converters (DACs) offer buffered outputs and a 3µs maximum settling time at the 12-bit level. The DACs operate from a +2.7V to +5.25V analog supply and a separate +1.8V to +5.25V digital supply. The 20MHz, 3-wire, serial interface is compatible with SPI™, QSPI™, MICROWIRE™, and digital signal processor (DSP) protocol applications. Multiple devices can share a common serial interface in direct-access or daisy-chained configuration. The MAX5580–MAX5585 provide two multifunctional, user-programmable, digital I/O ports. The externally selectable power-up states of the DAC outputs are either zero scale, midscale, or full scale. Software-selectable FAST and SLOW settling modes decrease settling time in FAST mode, or reduce supply current in SLOW mode.

The MAX5580/MAX5581 are 12-bit DACs, the MAX5582/MAX5583 are 10-bit DACs, and the MAX5584/MAX5585 are 8-bit DACs. The MAX5580/MAX5582/MAX5584 provide unity-gain-configured output buffers, while the MAX5581/MAX5583/MAX5585 provide force-sense-configured output buffers. The MAX5580–MAX5585 operate over the extended -40°C to +85°C temperature range and are available in space-saving, 5mm x 5mm x 0.8mm, 20-pin, thin QFN and TSSOP packages.

Applications

Portable Instrumentation
Automatic Test Equipment (ATE)
Digital Offset and Gain Adjustment
Automatic Tuning
Programmable Voltage and Current Sources
Programmable Attenuators
Industrial Process Controls
Motion Control
Microprocessor (µP)-Controlled Systems
Power Amplifier Control
Fast Parallel-DAC to Serial-DAC Upgrades

Pin Configurations appear at end of data sheet.

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MICROWIRE is a trademark of National Semiconductor Corp.

Features

- **3µs (max) 12-Bit Settling Time to 0.5 LSB**
- **Quad, 12-/10-/8-Bit Serial DACs in TSSOP and Thin QFN (5mm x 5mm x 0.8mm) Packages**
- **±1 LSB (max) INL and DNL at 12-Bit Resolution**
- **Two User-Programmable Digital I/O Ports**
- **Single +2.7V to +5.25V Analog Supply**
- **+1.8V to AV_{DD} Digital Supply**
- **20MHz, 3-Wire, SPI-/QSPI-/MICROWIRE-/DSP-Compatible Serial Interface**
- **Glitch-Free Outputs Power Up to Zero Scale, Midscale, or Full Scale Controlled by PU Pin**
- **Unity-Gain or Force-Sense-Configured Output Buffers**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5580AEUP	-40°C to +85°C	20 TSSOP-EP*
MAX5580AETP	-40°C to +85°C	20 Thin QFN-EP*

**EP = Exposed paddle.*

Ordering Information continued at end of data sheet.

Selector Guide

PART	OUTPUT BUFFER CONFIGURATION	RESOLUTION (BITS)	INL (LSB max)
MAX5580AEUP	Unity gain	12	±1
MAX5580AETP	Unity gain	12	±1
MAX5580BEUP	Unity gain	12	±4
MAX5580BETP	Unity gain	12	±4
MAX5581AEUP	Force sense	12	±1
MAX5581AETP	Force sense	12	±1
MAX5581BEUP	Force sense	12	±4
MAX5581BETP	Force sense	12	±4
MAX5582EUP	Unity gain	10	±1
MAX5582ETP	Unity gain	10	±1
MAX5583EUP	Force sense	10	±1
MAX5583ETP	Force sense	10	±1
MAX5584EUP	Unity gain	8	±0.5
MAX5584ETP	Unity gain	8	±0.5
MAX5585EUP	Force sense	8	±0.5
MAX5585ETP	Force sense	8	±0.5

For pricing delivery, and ordering information please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to DV_{DD} .....±6V
AGND to DGND .....±0.3V
AV_{DD} to AGND, DGND.....-0.3V to +6V
DV_{DD} to AGND, DGND .....-0.3V to +6V
FB_, OUT_,
REF to AGND .....-0.3V to the lower of (AV_{DD} + 0.3V) or +6V
SCLK, DIN, $\overline{CS}$, PU,
$\overline{DSP}$ to DGND .....-0.3V to the lower of (DV_{DD} + 0.3V) or +6V
UPIO1, UPIO2
to DGND .....-0.3V to the lower of (DV_{DD} + 0.3V) or +6V
Maximum Current into Any Pin .....±50mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 21.7mW/°C above +70°C).....1739mW
20-Pin Thin QFN (derate 20.8mW/°C above +70°C) 1667mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = 2.7V to 5.25V, DV_{DD} = 1.8V to AV_{DD}, AGND = 0, DGND = 0, V_{REF} = 2.5V (for AV_{DD} = 2.7V to 5.25V), V_{REF} = 4.096V (for AV_{DD} = 4.5V to 5.25V), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution	N	MAX5580/MAX5581		12			Bits
		MAX5582/MAX5583		10			
		MAX5584/MAX5585		8			
Integral Nonlinearity	INL	V_{REF} = 2.5V at AV_{DD} = 2.7V and V_{REF} = 4.096V at AV_{DD} = 5.25V (Note 2)	MAX5580A/MAX5581A (12 bit)			±1	LSB
			MAX5580B/MAX5581B (12 bit)		±2	±4	
			MAX5582/MAX5583 (10 bit)		±0.5	±1	
			MAX5584/MAX5585 (8 bit)		±0.125	±0.5	
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 2)				±1	LSB
Offset Error	V_{OS}	MAX5580A/MAX5581A (12 bit), decimal code = 250				±5	mV
		MAX5580B/MAX5581B (12 bit), decimal code = 40			±5	±25	
		MAX5582/MAX5583 (10 bit), decimal code = 20			±5	±25	
		MAX5584/MAX5585 (8 bit), decimal code = 5			±5	±25	
Offset-Error Drift					5		ppm of FS/°C
Gain Error	GE	Full-scale output	MAX5580A, V_{REF} = 4.096V		±1	±5	LSB
			MAX5580A, V_{REF} = 2.5V		±1.5	±7	
			MAX5581A, V_{REF} = 4.096V		±0.5	±4	
			MAX5581A, V_{REF} = 2.5V		±1	±5	
			MAX5580B/MAX5581B (12 bit)		±20	±40	
			MAX5582/MAX5583 (10 bit)		±5	±10	
			MAX5584/MAX5585 (8 bit)		±2	±3	
Gain-Error Drift					1		ppm of FS/°C

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 2.7V to 5.25V, DV_{DD} = 1.8V to AV_{DD}, AGND = 0, DGND = 0, V_{REF} = 2.5V (for AV_{DD} = 2.7V to 5.25V), V_{REF} = 4.096V (for AV_{DD} = 4.5V to 5.25V), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	PSRR	Full-scale output, AV_{DD} = 2.7V to 5.25V			200		µV/V
REFERENCE INPUT							
Reference-Input Range	V_{REF}			0.25		AV_{DD}	V
Reference-Input Resistance	R_{REF}	Normal operation (no code dependence)		145	200		kΩ
Reference Leakage Current		Shutdown mode			0.5	1	µA
DAC OUTPUT CHARACTERISTICS							
Output-Voltage Noise		SLOW mode, full scale	Unity gain		85		$µV_{RMS}$
			Force sense		67		
		FAST mode, full scale	Unity gain		140		
			Force sense		110		
Output-Voltage Range (Note 3)		Unity-gain output		0		AV_{DD}	V
		Force-sense output		0		AV_{DD} / 2	
DC Output Impedance					38		Ω
Short-Circuit Current		AV_{DD} = 5V, OUT_ to AGND, full scale, FAST mode			57		mA
		AV_{DD} = 3V, OUT_ to AGND, full scale, FAST mode			45		
Power-Up Time		From DV_{DD}, applied until interface is functional			30	60	µs
Wake-Up Time		Coming out of shutdown, outputs settled			40		µs
Output OUT_ and FB_ Open-Circuit Leakage Current		Programmed in shutdown mode, force-sense outputs only			0.01		µA
DIGITAL OUTPUTS (UPIO_)							
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA		DV_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA				0.4	V
DIGITAL INPUTS (SCLK, $\overline{CS}$, DIN, $\overline{DSP}$, UPIO_)							
Input High Voltage	V_{IH}	DV_{DD} ≥ 2.7V		2.4			V
		DV_{DD} < 2.7V		0.7 x DV_{DD}			
Input Low Voltage	V_{IL}	DV_{DD} > 3.6V				0.8	V
		2.7V ≤ DV_{DD} ≤ 3.6V				0.6	
		DV_{DD} < 2.7V				0.2	
Input Leakage Current	I_{IN}				±0.1	±1	µA
Input Capacitance	C_{IN}				10		pF

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 2.7V to 5.25V, DV_{DD} = 1.8V to AV_{DD}, AGND = 0, DGND = 0, V_{REF} = 2.5V (for AV_{DD} = 2.7V to 5.25V), V_{REF} = 4.096V (for AV_{DD} = 4.5V to 5.25V), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PU INPUT							
Input High Voltage	V_{IH-PU}			DV_{DD} - 200mV			V
Input Low Voltage	V_{IL-PU}					200	mV
Input Leakage Current	I_{IN-PU}	PU still considered floating when connected to a tri-state bus				±200	nA
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate	SR	FAST mode			3.6		V/µs
		SLOW mode			1.6		
Voltage-Output Settling Time (Note 4), Figure 5	t_S	FAST mode	MAX5580/MAX5581 from code 322 to code 4095 to 0.5 LSB		2	3	µs
			MAX5582/MAX5583 from code 10 to code 1023 to 0.5 LSB		1.5	3	
			MAX5584/MAX5585 from code 3 to code 255 to 0.5 LSB		1	2	
		SLOW mode	MAX5580/MAX5581 from code 322 to code 4095 to 0.5 LSB		3	6	
			MAX5582/MAX5583 from code 10 to code 1023 0.5 LSB		2.5	6	
			MAX5584/MAX5585 from code 3 to code 255 to 0.5 LSB		2	4	
FB_ Input Voltage				0		V_{REF} / 2	V
FB_ Input Current						0.1	µA
Reference -3dB Bandwidth (Note 5)		Unity gain			200		kHz
		Force sense			150		
Digital Feedthrough		$\overline{CS}$ = DV_{DD}, code = zero scale, any digital input from 0 to DV_{DD} and DV_{DD} to 0, f = 100kHz			0.1		nV-s
Digital-to-Analog Glitch Impulse		Major carry transition			2		nV-s
DAC-to-DAC Crosstalk		(Note 6)			15		nV-s

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 2.7V to 5.25V, DV_{DD} = 1.8V to AV_{DD}, AGND = 0, DGND = 0, V_{REF} = 2.5V (for AV_{DD} = 2.7V to 5.25V), V_{REF} = 4.096V (for AV_{DD} = 4.5V to 5.25V), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Analog Supply Voltage Range	AV_{DD}			2.70		5.25	V
Digital Supply Voltage Range	DV_{DD}			1.8		AV_{DD}	V
Operating Supply Current	I_{AVDD} + I_{DVDD}	SLOW mode, all digital inputs at DGND or DV_{DD}, no load, V_{REF} = 4.096V	Unity gain		0.9	1.6	mA
			Force sense		1.6	2.4	
		FAST mode, all digital inputs at DGND or DV_{DD}, no load, V_{REF} = 4.096V	Unity gain		1.6	4	
			Force sense		2.3	4	
Shutdown Supply Current	$I_{AVDD(SHDN)}$ + $I_{DVDD(SHDN)}$	No clocks, all digital inputs at DGND or DV_{DD}, all DACs in shutdown mode			0.5	1	µA

Note 1: For the force-sense versions, FB_ is connected to its respective OUT_, and V_{OUT} (max) = V_{REF} / 2, unless otherwise noted.

Note 2: Linearity guaranteed from decimal code 250 to code 4095 for the MAX5580A/MAX5581A (12 bit, A grade), code 40 to code 4095 for the MAX5580B/MAX5581B (12 bit, B grade), code 20 to code 1023 for the MAX5582/MAX5583 (10 bit), and code 5 to code 255 for the MAX5584/MAX5585 (8 bit).

Note 3: Represents the functional range. The linearity is guaranteed at V_{REF} = 2.5V (for AV_{DD} from 2.7V to 5.25V), and V_{REF} = 4.096V (for AV_{DD} = 4.5V to 5.25V). See the *Typical Operating Characteristics* section for linearity at other voltages.

Note 4: Guaranteed by design.

Note 5: The reference -3dB bandwidth is measured with a $0.1V_{P-P}$ sine wave on V_{REF} and with full-scale input code.

Note 6: DC crosstalk is measured as follows: outputs of DACA–DACD are set to full scale and the output of DACD is measured. While keeping DACD unchanged, the outputs of DACA–DACC are transitioned to zero scale and the ΔV_{OUT} of DACD is measured.

TIMING CHARACTERISTICS—DSP Mode Disabled (3V, 3.3V, 5V Logic) (Figure 1)

(DV_{DD} = 2.7V to 5.25V, AGND = DGND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{SCLK}	2.7V < DV_{DD} < 5.25V			20	MHz
SCLK Pulse-Width High	t_{CH}	(Note 7)	20			ns
SCLK Pulse-Width Low	t_{CL}	(Note 7)	20			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		10			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		5			ns
SCLK Rise to $\overline{CS}$ Fall Setup Time	t_{CS0}		10			ns
DIN to SCLK Rise Setup Time	t_{DS}		12			ns
DIN to SCLK Rise Hold Time	t_{DH}		5			ns
SCLK Rise to DOUTDC1 Valid Propagation Delay	t_{DO1}	C_L = 20pF, UPIO_ = DOUTDC1 mode			30	ns
SCLK Fall to DOUT_ Valid Propagation Delay	t_{DO2}	C_L = 20pF, UPIO_ = DOUTDC0 or DOUTRB mode			30	ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}	MICROWIRE and SPI modes 0 and 3	10			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		45			ns
UPIO_ TIMING CHARACTERISTICS						
DOUT Tri-State Time when Exiting DOUTDC0, DOUTDC1, and UPIO Modes	t_{DOZ}	C_L = 20pF, from end of write cycle to UPIO_ in high impedance			100	ns
DOUTRB Tri-State Time from $\overline{CS}$ Rise	t_{DRBZ}	C_L = 20pF, from rising edge of $\overline{CS}$ to UPIO_ in high impedance			20	ns
DOUTRB Tri-State Enable Time from 8th SCLK Rise	t_{ZEN}	C_L = 20pF, from 8th rising edge of SCLK to UPIO_ driven out of tri-state	0			ns
$\overline{LDAC}$ Pulse-Width Low	t_{LDL}	Figure 5	20			ns
$\overline{LDAC}$ Effective Delay	t_{LDS}	Figure 6	100			ns
$\overline{CLR}$, $\overline{MID}$, $\overline{SET}$ Pulse-Width Low	t_{CMS}	Figure 5	20			ns
GPO Output Settling Time	t_{GP}	Figure 6			100	ns
GPO Output High-Impedance Time	t_{GPZ}				100	ns

TIMING CHARACTERISTICS—DSP Mode Disabled (1.8V Logic) (Figure 1)

(DV_{DD} = 1.8V to 2.7V, AGND = DGND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{SCLK}	1.8V < DV_{DD} < 2.7V			10	MHz
SCLK Pulse-Width High	t_{CH}	(Note 7)	40			ns
SCLK Pulse-Width Low	t_{CL}	(Note 7)	40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		20			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		5			ns
SCLK Rise to $\overline{CS}$ Fall Setup TIme	t_{CS0}		10			ns
DIN to SCLK Rise Setup Time	t_{DS}		20			ns
DIN to SCLK Rise Hold Time	t_{DH}		5			ns
SCLK Rise to DOUTDC1 Valid Propagation Delay	t_{DO1}	C_L = 20pF, UPIO_ = DOUTDC1 mode			60	ns
SCLK Fall to DOUT_ Valid Propagation Delay	t_{DO2}	C_L = 20pF, UPIO_ = DOUTDC0 or DOUTRB mode			60	ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}	MICROWIRE and SPI modes 0 and 3	20			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		90			ns
UPIO_ TIMING CHARACTERISTICS						
DOUT Tri-State Time when Exiting DOUTDC0, DOUTDC1, and UPIO Modes	t_{DOZ}	C_L = 20pF, from end of write cycle to UPIO_ in high impedance			200	ns
DOUTRB Tri-State Time from $\overline{CS}$ Rise	t_{DRBZ}	C_L = 20pF, from rising edge of $\overline{CS}$ to UPIO_ in high impedance			40	ns
DOUTRB Tri-State Enable Time from 8th SCLK Rise	t_{ZEN}	C_L = 20pF, from 8th rising edge of SCLK to UPIO_ driven out of tri-state	0			ns
$\overline{LDAC}$ Pulse-Width Low	t_{LDL}	Figure 5	40			ns
$\overline{LDAC}$ Effective Delay	t_{LDS}	Figure 6	200			ns
$\overline{CLR}$, $\overline{MID}$, $\overline{SET}$ Pulse-Width Low	t_{CMS}	Figure 5	40			ns
GPO Output Settling Time	t_{GP}	Figure 6			200	ns
GPO Output High-Impedance Time	t_{GPZ}				200	ns

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

TIMING CHARACTERISTICS—DSP Mode Enabled (3V, 3.3V, 5V Logic) (Figure 2)

(DV_{DD} = 2.7V to 5.25V, AGND = DGND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{SCLK}	2.7V < DV_{DD} < 5.25V			20	MHz
SCLK Pulse-Width High	t_{CH}	(Note 7)	20			ns
SCLK Pulse-Width Low	t_{CL}	(Note 7)	20			ns
$\overline{CS}$ Fall to SCLK Fall Setup Time	t_{CSS}		10			ns
$\overline{DSP}$ Fall to SCLK Fall Setup Time	t_{DSS}		10			ns
SCLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH}		5			ns
SCLK Fall to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
SCLK Fall to $\overline{DSP}$ Fall Delay	t_{DS0}		10			ns
DIN to SCLK Fall Setup Time	t_{DS}		12			ns
DIN to SCLK Fall Hold Time	t_{DH}		5			ns
SCLK Rise to DOUT_ Valid Propagation Delay	t_{DO1}	C_L = 20pF, UPIO_ = DOUTDC1 or DOUTRB mode			30	ns
SCLK Fall to DOUT_ Valid Propagation Delay	t_{DO2}	C_L = 20pF, UPIO_ = DOUTDC0 mode			30	ns
$\overline{CS}$ Rise to SCLK Fall Hold Time	t_{CS1}	MICROWIRE and SPI modes 0 and 3	10			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		45			ns
$\overline{DSP}$ Pulse-Width High	t_{DSW}		20			ns
$\overline{DSP}$ Pulse-Width Low	t_{DSPWL}	(Note 8)	20			ns
UPIO_ TIMING CHARACTERISTICS						
DOUT Tri-State Time when Exiting DOUTDC0, DOUTDC1, and UPIO Modes	t_{DOZ}	C_L = 20pF, from end of write cycle to UPIO_ in high impedance			100	ns
DOUTRB Tri-State Time from $\overline{CS}$ Rise	t_{DRBZ}	C_L = 20pF, from rising edge of $\overline{CS}$ to UPIO_ in high impedance			20	ns
DOUTRB Tri-State Enable Time from 8th SCLK Fall	t_{ZEN}	C_L = 20pF, from 8th falling edge of SCLK to UPIO_ driven out of tri-state	0			ns
$\overline{LDAC}$ Pulse-Width Low	t_{LDL}	Figure 5	20			ns
$\overline{LDAC}$ Effective Delay	t_{LDS}	Figure 6	100			ns
$\overline{CLR}$, $\overline{MID}$, $\overline{SET}$ Pulse-Width Low	t_{CMS}	Figure 5	20			ns
GPO Output Settling Time	t_{GP}	Figure 6			100	ns
GPO Output High-Impedance Time	t_{GPZ}				100	ns

TIMING CHARACTERISTICS—DSP Mode Enabled (1.8V Logic) (Figure 2)

(DV_{DD} = 1.8V to 2.7V, AGND = DGND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{SCLK}	1.8V < DV_{DD} < 2.7V			10	MHz
SCLK Pulse-Width High	t_{CH}	(Note 7)	40			ns
SCLK Pulse-Width Low	t_{CL}	(Note 7)	40			ns
$\overline{CS}$ Fall to SCLK Fall Setup Time	t_{CSS}		20			ns
$\overline{DSP}$ Fall to SCLK Fall Setup Time	t_{DSS}		20			ns
SCLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH}		5			ns
SCLK Fall to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
SCLK Fall to $\overline{DSP}$ Fall Delay	t_{DS0}		15			ns
DIN to SCLK Fall Setup Time	t_{DS}		20			ns
DIN to SCLK Fall Hold Time	t_{DH}		5			ns
SCLK Rise to DOUT_ Valid Propagation Delay	t_{DO1}	C_L = 20pF, UPIO_ = DOUTDC1 or DOUTRB mode			60	ns
SCLK Fall to DOUT_ Valid Propagation Delay	t_{DO2}	C_L = 20pF, UPIO_ = DOUTDC0 mode			60	ns
$\overline{CS}$ Rise to SCLK Fall Hold Time	t_{CS1}	MICROWIRE and SPI modes 0 and 3	20			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		90			ns
$\overline{DSP}$ Pulse-Width High	t_{DSW}		40			ns
$\overline{DSP}$ Pulse-Width Low	t_{DSPWL}	(Note 8)	40			ns
UPIO_ TIMING CHARACTERISTICS						
DOUT Tri-State Time when Exiting DOUTDC0, DOUTDC1, and UPIO Modes	t_{DOZ}	C_L = 20pF, from end of write cycle to UPIO_ in high impedance			200	ns
DOUTRB Tri-State Time from $\overline{CS}$ Rise	t_{DRBZ}	C_L = 20pF, from rising edge of $\overline{CS}$ to UPIO_ in high impedance			40	ns
DOUTRB Tri-State Enable Time from 8th SCLK Fall	t_{ZEN}	C_L = 20pF, from 8th falling edge of SCLK to UPIO_ driven out of tri-state	0			ns
$\overline{LDAC}$ Pulse-Width Low	t_{LDL}	Figure 5	40			ns
$\overline{LDAC}$ Effective Delay	t_{LDS}	Figure 6	200			ns
$\overline{CLR}$, $\overline{MID}$, $\overline{SET}$ Pulse-Width Low	t_{CMS}	Figure 5	40			ns
GPO Output Settling Time	t_{GP}	Figure 6			200	ns
GPO Output High-Impedance Time	t_{GPZ}				200	ns

Note 7: In some daisy-chain modes, data is required to be clocked in on one clock edge and the shifted data clocked out on the following edge. In the case of a 0.5 clock-period delay, it is necessary to increase the minimum high/low clock times to 25ns (2.7V) or 50ns (1.8V).

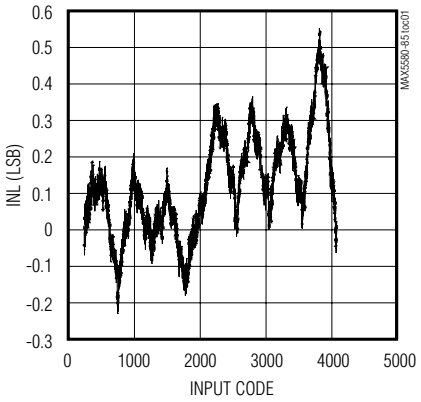
Note 8: The falling edge of $\overline{DSP}$ starts a DSP-type bus cycle, provided that $\overline{CS}$ is also active low to select the device. $\overline{DSP}$ active low and $\overline{CS}$ active low must overlap by a minimum of 10ns (2.7V) or 20ns (1.8V). $\overline{CS}$ can be permanently low in this mode of operation.

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

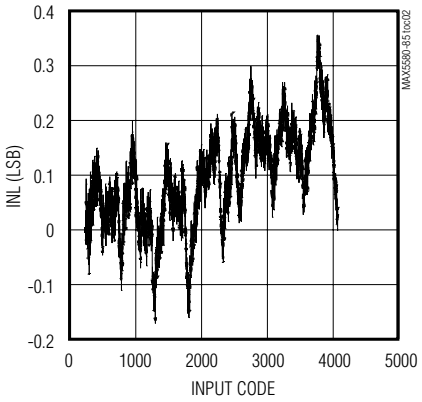
Typical Operating Characteristics

(AV_{DD} = DV_{DD} = 5V, V_{REF} = 4.096V, R_L = 10kΩ, C_L = 100pF, speed mode = FAST, PU = floating, T_A = +25°C, unless otherwise noted.)

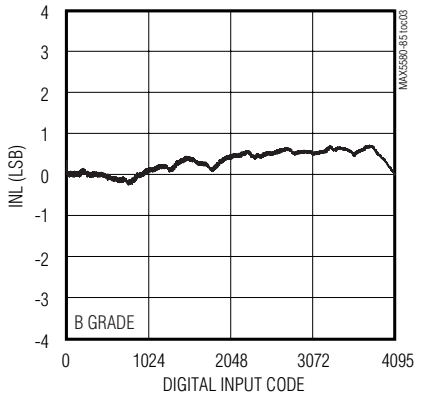
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (MAX5580A)



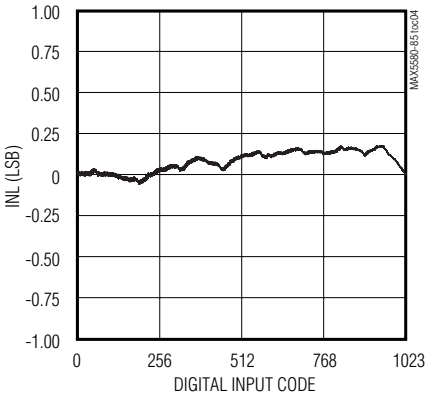
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (MAX5581A)



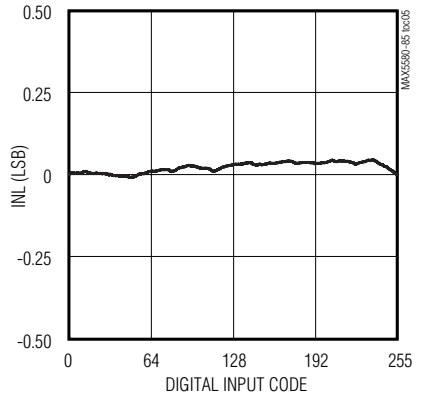
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (12 BIT)



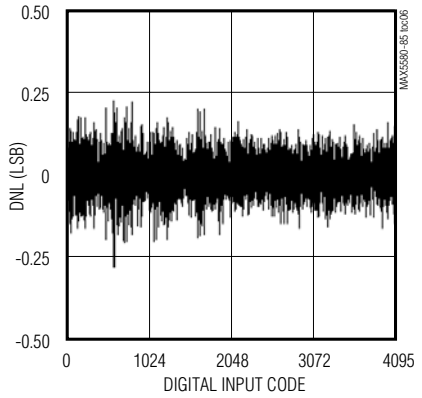
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (10 BIT)



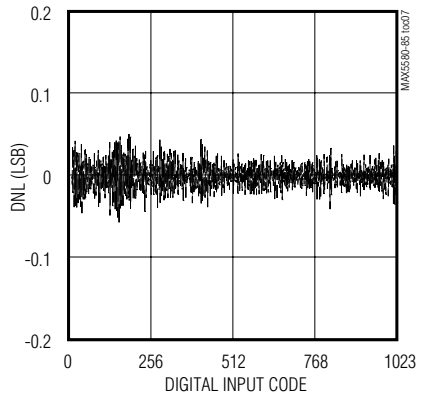
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (8 BIT)



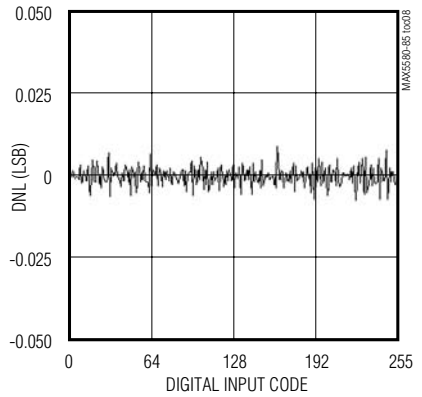
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE (12 BIT)



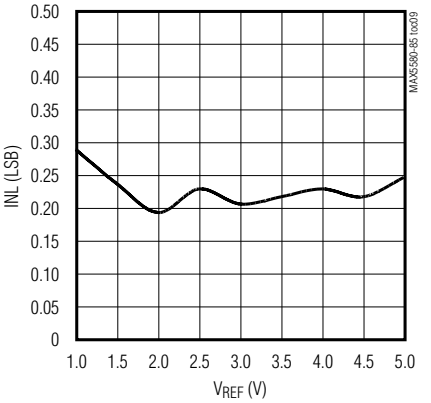
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE (10 BIT)



DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE (8 BIT)



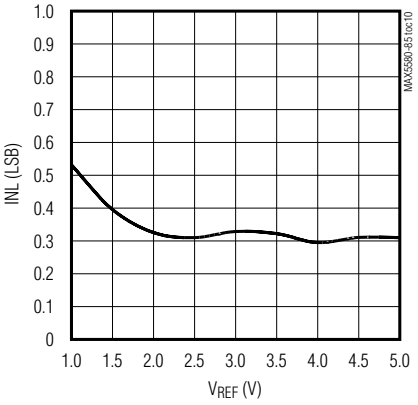
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE (MAX5580A)



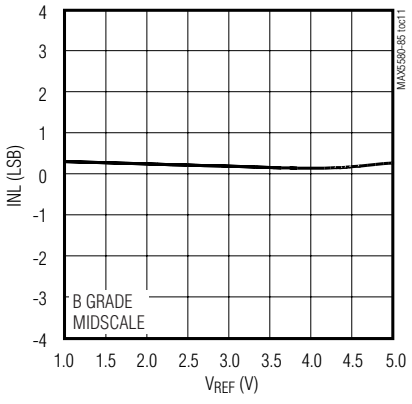
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = 5V, V_{REF} = 4.096V, R_L = 10kΩ, C_L = 100pF, speed mode = FAST, PU = floating, T_A = +25°C, unless otherwise noted.)

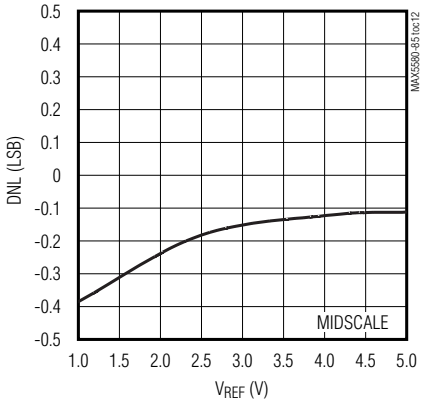
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE (MAX5581A)



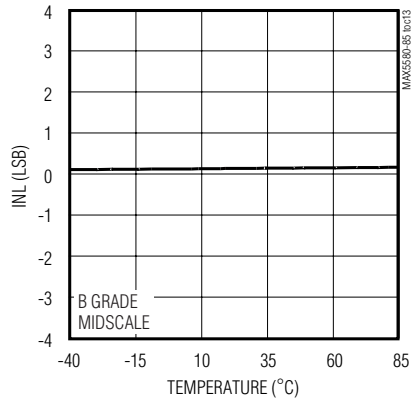
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE (12 BIT)



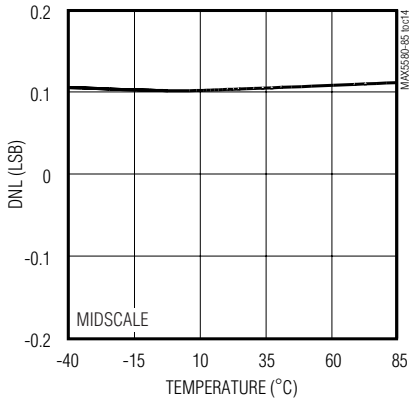
DIFFERENTIAL NONLINEARITY vs. REFERENCE VOLTAGE (12 BIT)



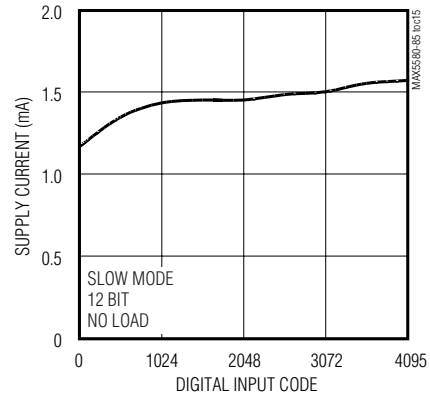
INTEGRAL NONLINEARITY vs. TEMPERATURE (12 BIT)



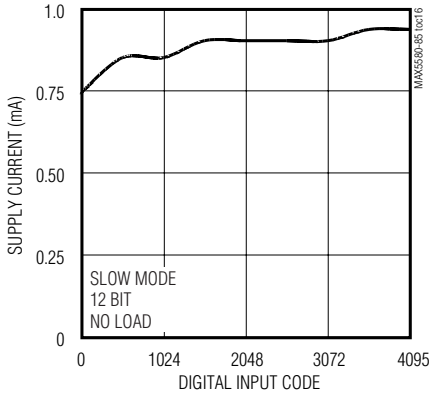
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE (12 BIT)



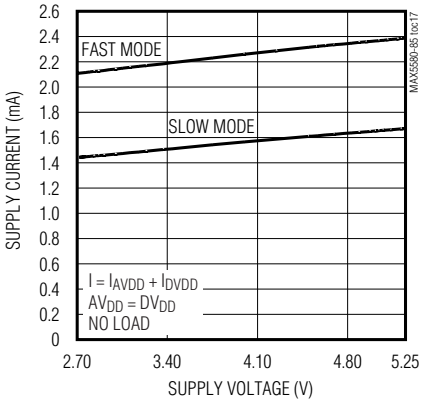
SUPPLY CURRENT vs. DIGITAL INPUT CODE (FORCE SENSE)



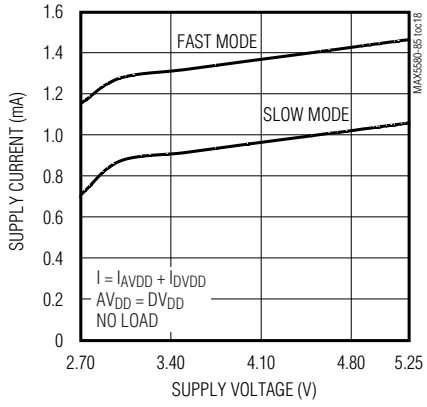
SUPPLY CURRENT vs. DIGITAL INPUT CODE (UNITY GAIN)



SUPPLY CURRENT vs. SUPPLY VOLTAGE (FORCE SENSE)



SUPPLY CURRENT vs. SUPPLY VOLTAGE (UNITY GAIN)

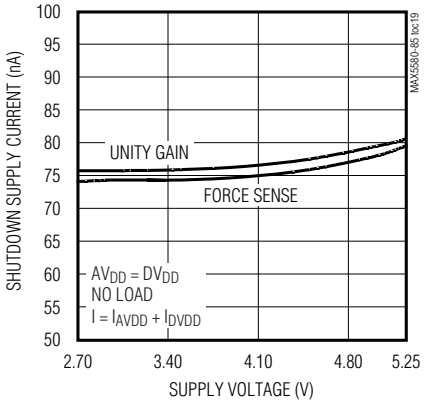


Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

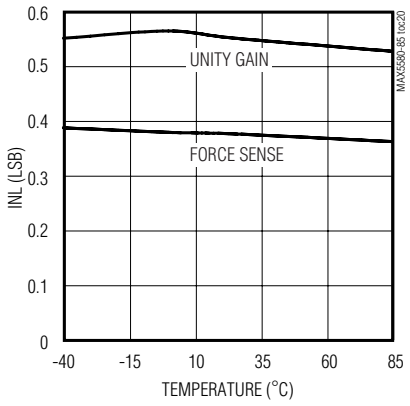
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = 5V, V_{REF} = 4.096V, R_L = 10kΩ, C_L = 100pF, speed mode = FAST, PU = floating, T_A = +25°C, unless otherwise noted.)

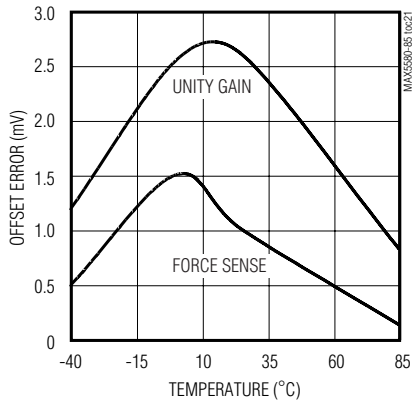
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



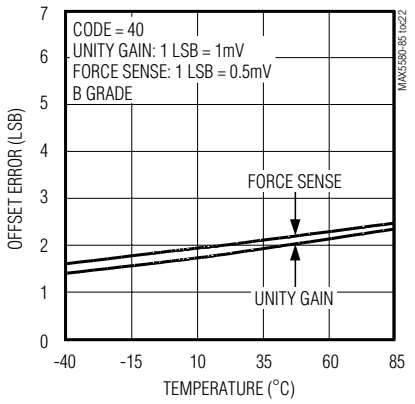
INTEGRAL NONLINEARITY vs. TEMPERATURE (A GRADE)



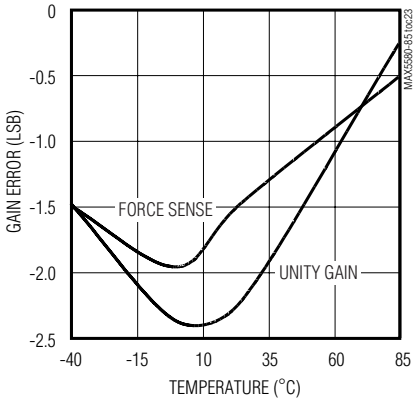
OFFSET ERROR vs. TEMPERATURE (A GRADE)



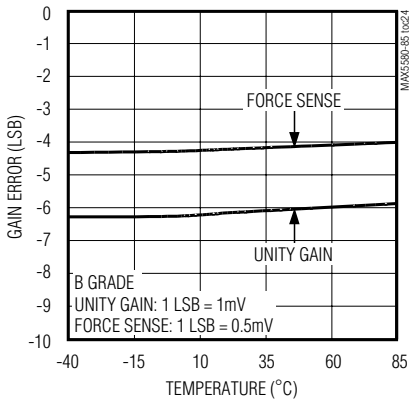
OFFSET ERROR vs. TEMPERATURE



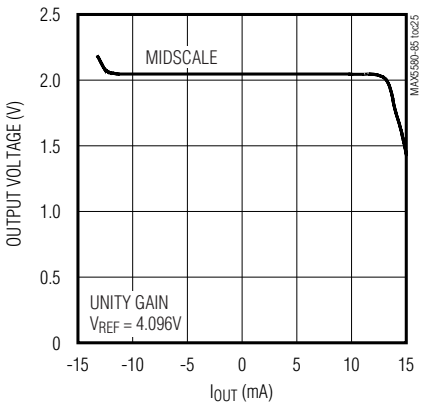
GAIN ERROR vs. TEMPERATURE (A GRADE)



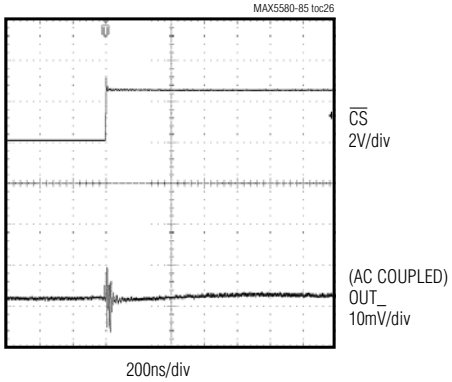
GAIN ERROR vs. TEMPERATURE



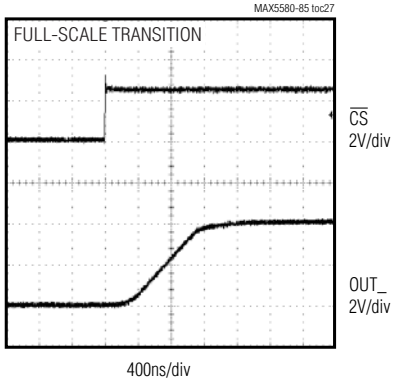
OUTPUT VOLTAGE vs. OUTPUT SOURCE/SINK CURRENT



MAJOR-CARRY TRANSITION GLITCH



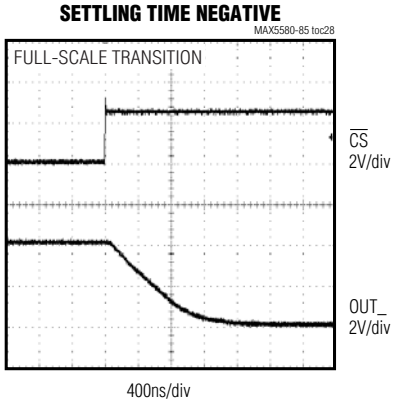
SETTLING TIME POSITIVE



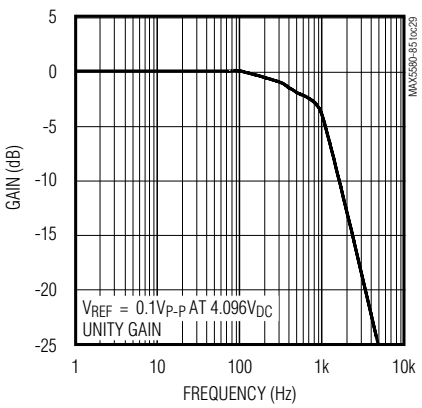
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = 5V, V_{REF} = 4.096V, R_L = 10kΩ, C_L = 100pF, speed mode = FAST, PU = floating, T_A = +25°C, unless otherwise noted.)

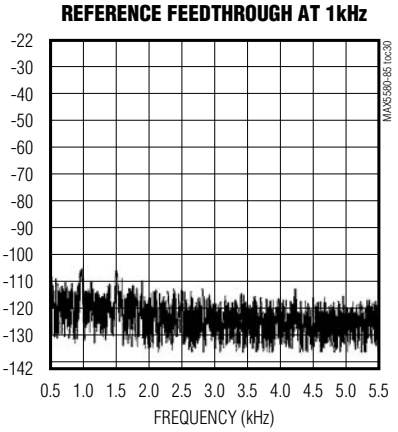
SETTLING TIME NEGATIVE



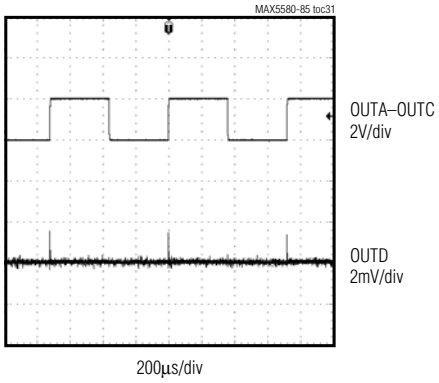
REFERENCE INPUT BANDWIDTH



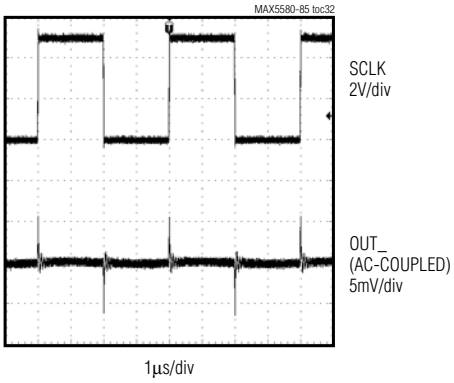
REFERENCE FEEDTHROUGH AT 1kHz



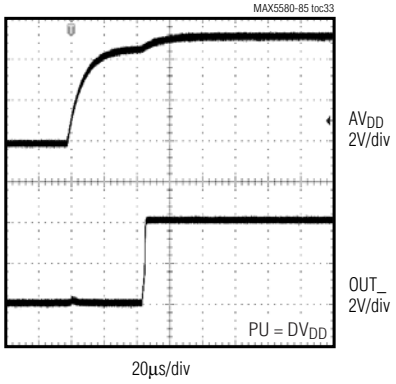
DAC-TO-DAC CROSSTALK



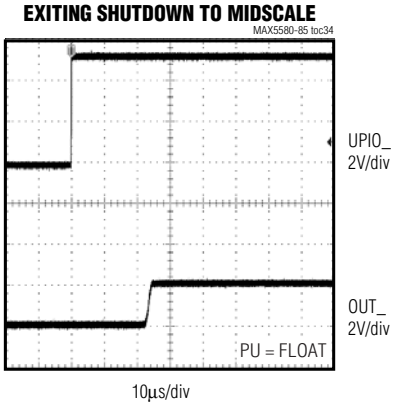
DIGITAL FEEDTHROUGH



POWER-UP GLITCH



EXITING SHUTDOWN TO MIDSCALE

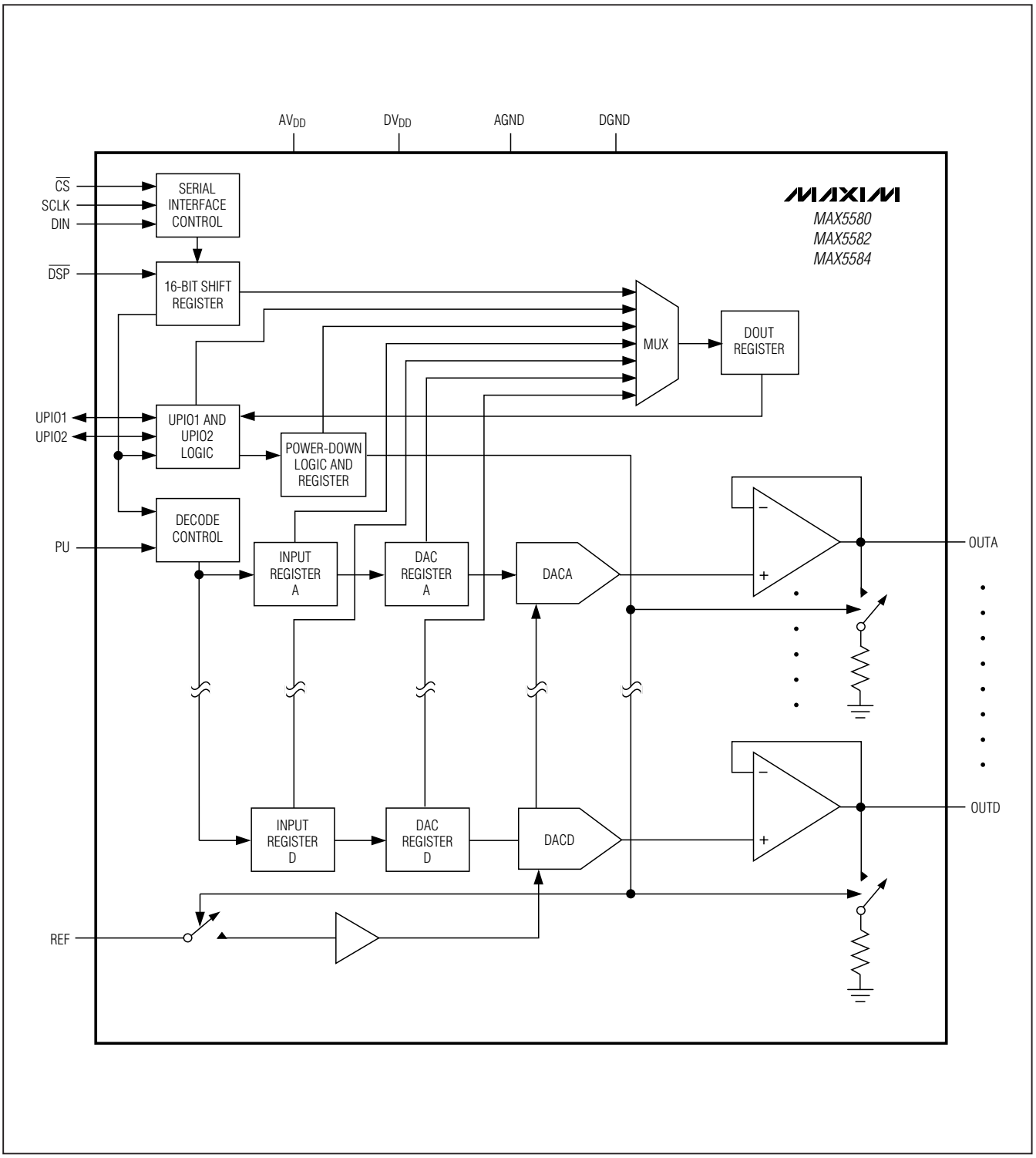


Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

Pin Description

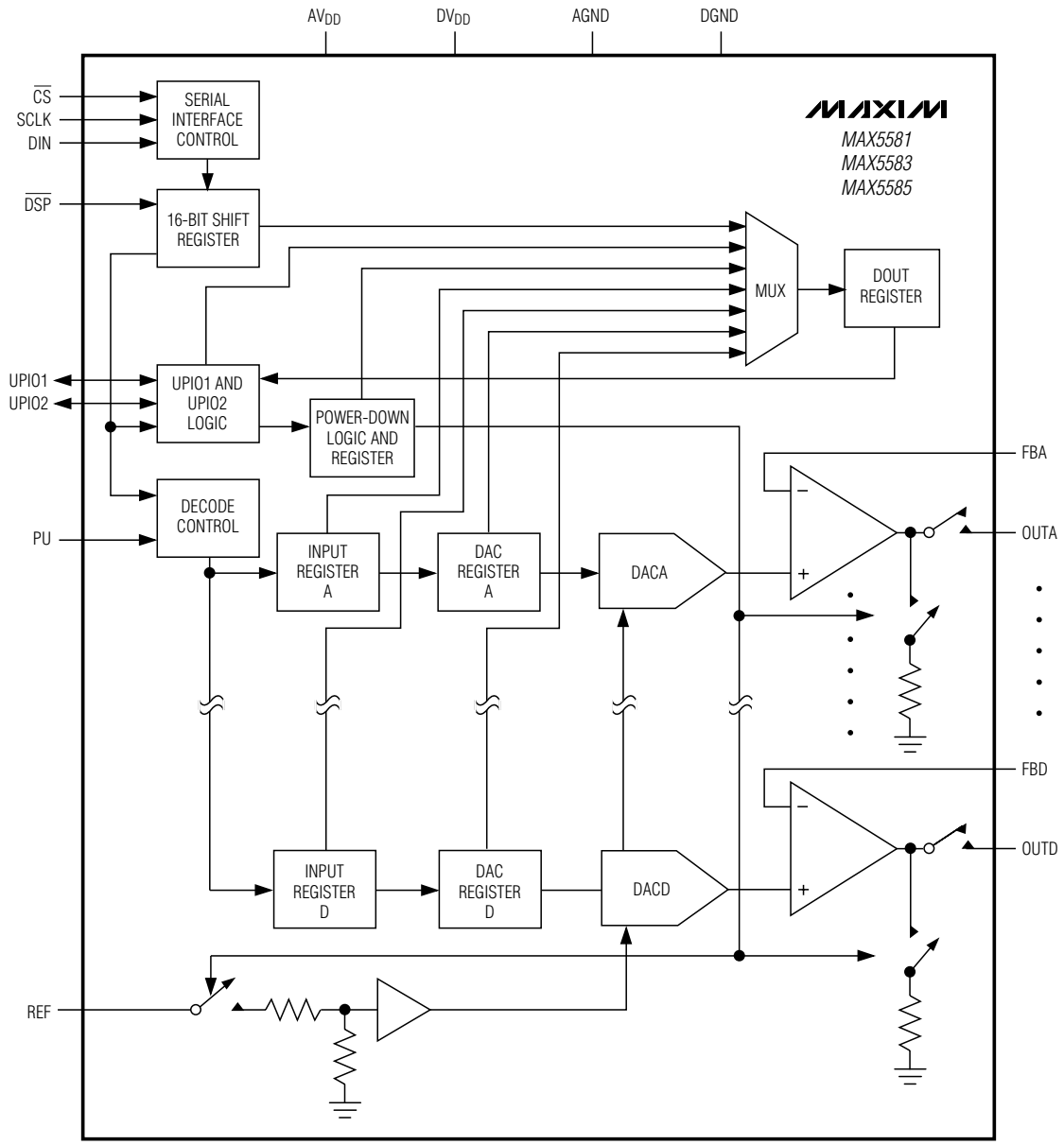
PIN				NAME	FUNCTION
MAX5580 MAX5582 MAX5584		MAX5581 MAX5583 MAX5585			
TSSOP	THIN QFN	TSSOP	THIN QFN		
1	19	1	19	AGND	Analog Ground
2	20	2	20	AV_{DD}	Analog Supply
3, 5, 17, 19	1, 3, 15, 17	—	—	N.C.	No Connection. Not internally connected.
—	—	3	1	FBB	Feedback for DACB
4	2	4	2	OUTB	DACB Output
—	—	5	3	FBA	Feedback for DACA
6	4	6	4	OUTA	DACA Output
7	5	7	5	PU	Power-Up State Select Input. Connect PU to DV_{DD} to set OUT_ to full scale upon power-up. Connect PU to DGND to set OUT_ to zero scale upon power-up. Float PU to set OUT_ to midscale upon power-up.
8	6	8	6	$\overline{CS}$	Active-Low Chip-Select Input
9	7	9	7	SCLK	Serial Clock Input
10	8	10	8	DIN	Serial Data Input
11	9	11	9	UPIO1	User-Programmable Input/Output 1
12	10	12	10	UPIO2	User-Programmable Input/Output 2
13	11	13	11	DV_{DD}	Digital Supply
14	12	14	12	DGND	Digital Ground
15	13	15	13	$\overline{DSP}$	Clock Enable. Connect $\overline{DSP}$ to DV_{DD} to clock in data on the rising edge of SCLK. Connect $\overline{DSP}$ to DGND to clock in data on the falling edge of SCLK.
16	14	16	14	OUTD	DACD Output
—	—	17	15	FBD	Feedback for DACD
18	16	18	16	OUTC	DACC Output
—	—	19	17	FBC	Feedback for DACC
20	18	20	18	REF	Reference Input
EP	EP	EP	EP	Exposed Pad	Exposed Pad. Connect to AGND.

Functional Diagrams



Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

Functional Diagrams (continued)



Detailed Description

The MAX5580–MAX5585 quad, 12-/10-/8-bit, voltage-output DACs offer buffered outputs and a 3µs maximum settling time at the 12-bit level. The DACs operate from a single 2.7V to 5.25V analog supply and a separate 1.8V to AV_{DD} digital supply. The MAX5580–MAX5585 include an input register and DAC register for each channel and a 16-bit data-in/data-out shift register. The 3-wire serial interface is compatible with SPI, QSPI, MICROWIRE, and DSP applications. The MAX5580–MAX5585 provide two user-programmable digital I/O ports, which are programmed through the serial interface. The externally selectable power-up states of the DAC outputs are either zero scale, midscale, or full scale.

Reference Input

The reference input, REF, accepts both AC and DC values with a voltage range extending from analog ground (AGND) to AV_{DD}. The voltage at REF sets the full-scale output of the DACs. Determine the output voltage using the following equations:

Unity-gain versions:

$$V_{OUT_} = (V_{REF} \times CODE) / 2^N$$

Force-sense versions (FB_ connected to OUT_):

$$V_{OUT} = 0.5 \times (V_{REF} \times CODE) / 2^N$$

where CODE is the numeric value of the DAC's binary input code and N is the bits of resolution. For the MAX5580/MAX5581, N = 12 and CODE ranges from 0 to 4095. For the MAX5582/MAX5583, N = 10 and CODE ranges from 0 to 1023. For the MAX5584/MAX5585, N = 8 and CODE ranges from 0 to 255. Use the minature MAX6126 low-dropout, ultra-low-noise reference for optimum performance.

Output Buffers

The DACA–DACD output-buffer amplifiers of the MAX5580–MAX5585 are unity-gain stable with rail-to-rail output voltage swings and a typical slew rate of 3.6V/µs (FAST mode). The MAX5580/MAX5582/MAX5584 provide unity-gain outputs, while the MAX5581/MAX5583/MAX5585 provide force-sense outputs. For the MAX5581/MAX5583/MAX5585, access to the output amplifier's inverting input provides flexibility in output gain setting and signal conditioning (see the *Applications Information* section).

The MAX5580–MAX5585 offer FAST and SLOW settling-time modes. In the SLOW mode, the settling time is 6µs (max), and the supply current is 1.6mA (max). In the FAST mode, the settling time is 3µs (max), and the supply current is 4mA (max). See the *Digital Interface* section for settling-time mode programming details.

Use the serial interface to set the shutdown output impedance of the amplifiers to 1kΩ or 100kΩ for the MAX5580/MAX5582/MAX5584 and 1kΩ or high impedance for the MAX5581/MAX5583/MAX5585. The DAC outputs can drive a 10kΩ (typ) load and are stable with up to 500pF (typ) of capacitive load.

Power-On Reset

At power-up, all DAC outputs power up to full scale, midscale, or zero scale, depending on the configuration of the PU input. Connect PU to DV_{DD} to set OUT_ to full scale upon power-up. Connect PU to digital ground (DGND) at power-up to set OUT_ to zero scale. Leave PU floating to set OUT_ to midscale.

Digital Interface

The MAX5580–MAX5585 use a 3-wire serial interface that is compatible with SPI, QSPI, MICROWIRE, and DSP protocol applications (Figures 1 and 2). Connect $\overline{DSP}$ to DV_{DD} before power-up to clock data in on the rising edge of SCLK. Connect $\overline{DSP}$ to DGND before power-up to clock data in on the falling edge of SCLK. After power-up, the device enters DSP frame-sync mode on the first rising edge of $\overline{DSP}$. Refer to the *MAX5580–MAX5585 Programmer's Handbook* for details.

The MAX5580–MAX5585 include a 16-bit input shift register. The data is loaded into the input shift register through the serial interface. The 16 bits can be sent in two serial 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until all 16 bits are transferred). The data is loaded MSB first. For the MAX5580/MAX5581, the 16 bits consist of 4 control bits (C3–C0) and 12 data bits (D11–D0) (see Table 1). For the 10-bit MAX5582/MAX5583 devices, D11–D2 are the data bits and D1 and D0 are sub-bits. For the 8-bit MAX5584/MAX5585 devices, D11–D4 are the data bits and D3–D0 are sub-bits. Set all sub-bits to zero for optimum performance.

Each DAC channel includes two registers: an input register and the DAC register. At power-up, the DAC output is set according to the state of PU. The DACs are double-buffered, which allows any of the following for each channel:

- Loading the input register without updating the DAC register
- Loading and updating the DAC register without updating the input register
- Updating the DAC register from the input register
- Updating the input and DAC registers simultaneously

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

Table 1. Serial Write Data Format

MSB				16 BITS OF SERIAL DATA											LSB
CONTROL BITS				DATA BITS											
C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

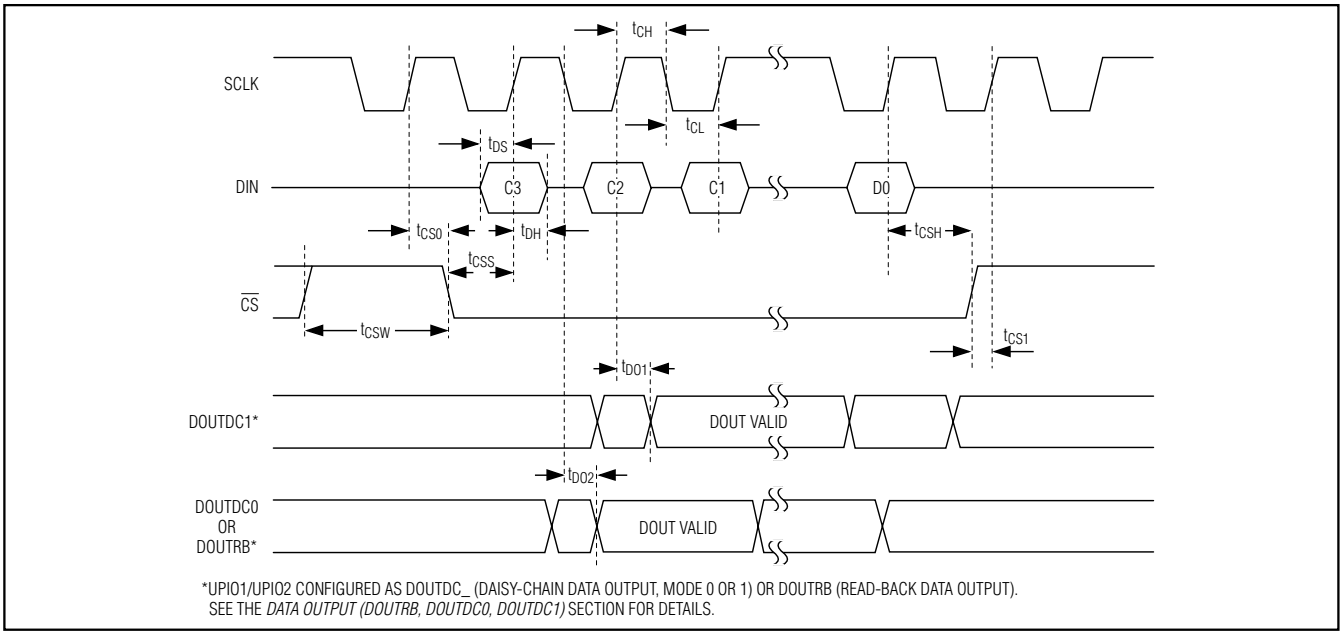


Figure 1. Serial-Interface Timing Diagram (DSP Mode Disabled)

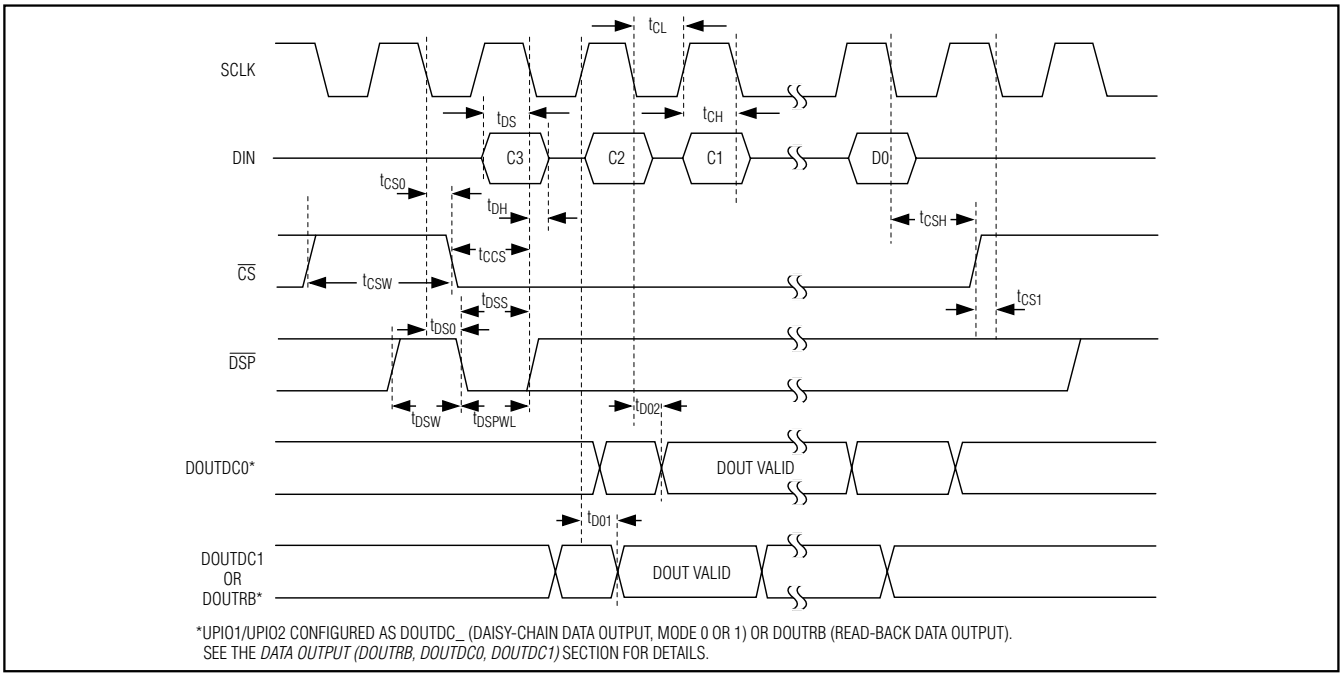


Figure 2. Serial-Interface Timing Diagram (DSP Mode Enabled)

Serial-Interface Programming Commands

Tables 2a, 2b, and 2c provide all the serial-interface programming commands for the MAX5580–MAX5585. Table 2a shows the basic DAC programming commands, Table 2b gives the advanced-feature programming commands, and Table 2c provides the 24-bit read commands. Figures 3 and 4 provide serial-interface diagrams for write operations.

Loading Input and DAC Registers

The MAX5580–MAX5585 contain a 16-bit shift register that is followed by a 12-bit input register and a 12-bit DAC register for each channel (see the *Functional Diagrams*). Tables 3, 4, and 5 highlight a few of the commands that handle the loading of the input and DAC registers. See Table 2a for all DAC programming commands.

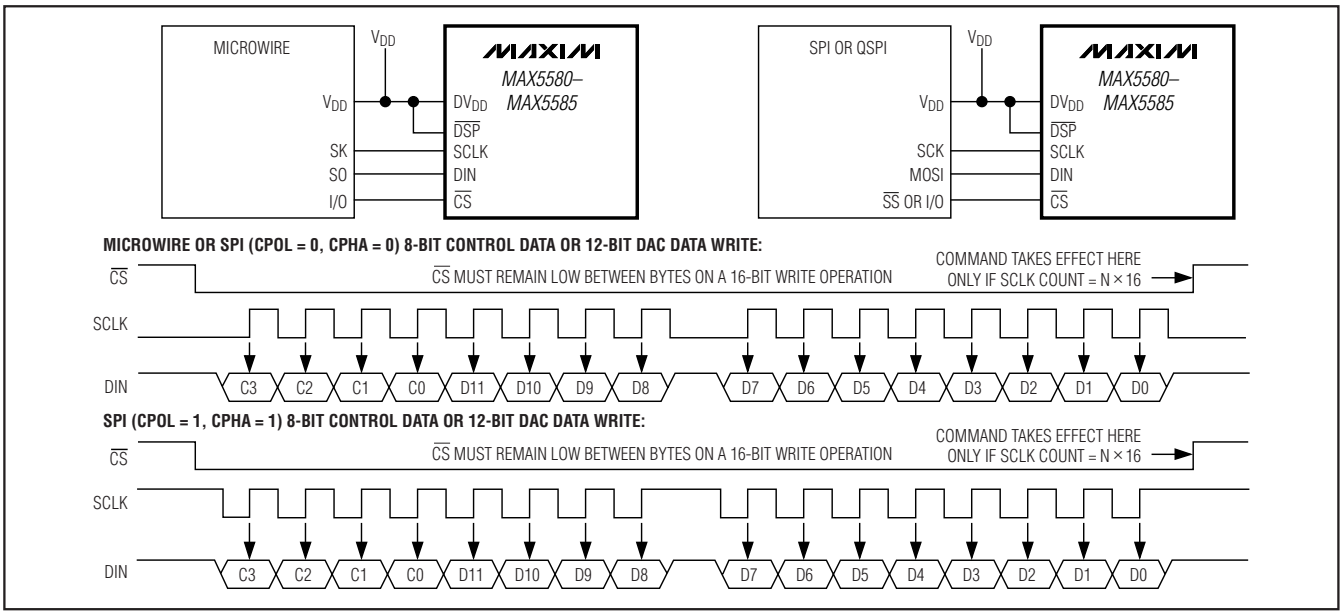


Figure 3. MICROWIRE and SPI Single DAC Writes (CPOL = 0, CPHA = 0 or CPOL = 1, CPHA = 1)

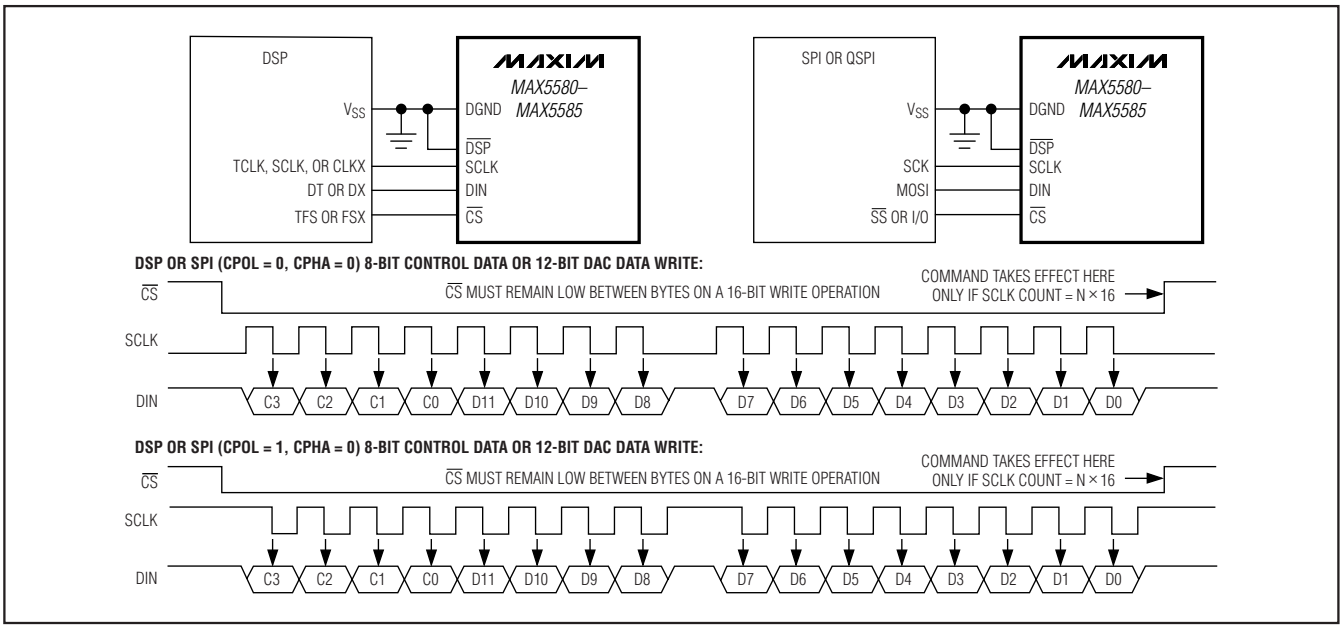


Figure 4. DSP and SPI Single DAC Writes (CPOL = 0, CPHA = 1 or CPOL = 1, CPHA = 0)

Table 2a. DAC Programming Commands

DATA	CONTROL BITS				DATA BITS												FUNCTION
	C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
INPUT REGISTERS (A–D)																	
DIN	0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACA input register from shift register; DACA output register is unchanged; DACA output is unchanged.*
DIN	0	0	0	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACA output register from shift register; input register is unchanged; DACA output is updated.*
DIN	0	0	1	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACA input register and output register from shift register; DACA output is updated.*
DIN	0	0	1	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACB input register from shift register; DACB output register is unchanged; DACB output is unchanged.*
DIN	0	1	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACB output register from shift register; input register is unchanged. DACB output is updated.*
DIN	0	1	0	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACB input register and output register from shift register; DACB output is updated.*
DIN	0	1	1	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACC input register from shift register; DACC output register is unchanged; DACC output is unchanged.*
DIN	0	1	1	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACC output register from shift register; input register is unchanged; DACC output is updated.*
DIN	1	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACC input register and output register from shift register; DACC output is updated.*
DIN	1	0	0	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACD input register from shift register; DACD output register is unchanged; DACD output is unchanged.*
DIN	1	0	1	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACD output register from shift register; input register is unchanged; DACD output is updated.*

Table 2a. DAC Programming Commands (continued)

DATA	CONTROL BITS				DATA BITS												FUNCTION
	C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
INPUT REGISTERS (A–D)																	
DIN	1	0	1	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load DACD input register and output register from shift register; DACD output is updated.*
DIN	1	1	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load all DAC input registers from the shift register; all DAC output registers are unchanged; all DAC outputs are unchanged.*
DIN	1	1	0	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load all DAC input and output registers from shift register; DAC outputs are updated.*

**For the MAX5582/MAX5583 (10-bit version), D11–D2 are the significant bits and D1 and D0 are sub-bits. For the MAX5584/MAX5585 (8-bit version), D11–D4 are the significant bits and D3–D0 are sub-bits. Set all sub-bits to zero during the write commands.*

Table 2b. Advanced-Feature Programming Commands

DATA	CONTROL BITS				DATA BITS												Function
	C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
SELECT BITS																	
DIN	1	1	1	0	0	0	X	X	X	X	X	X	MD	MC	MB	MA	Load DAC_ output register from input register when M_ is one; DAC_ output register is unchanged if M_ is zero.
SHUTDOWN-MODE BITS																	
DIN	1	1	1	0	0	1	0	X	PDD1	PDD0	PDC1	PDC0	PDB1	PDB0	PDA1	PDA0	Write DAC_ shutdown-mode bits; see Table 8.
DIN	1	1	1	0	0	1	1	X	X	X	X	X	X	X	X	X	Read DAC_ shutdown-mode bits.
DOUTR	X	X	X	X	X	X	X	X	PDD1	PDD0	PDC1	PDC0	PDB1	PDB0	PDA1	PDA0	
UPIO CONFIGURATION BITS																	
DIN	1	1	1	0	1	0	0	X	UPSL2	UPSL1	UP3	UP2	UP1	UP0	X	X	Write UPIO configuration bits; see Table 18.
DIN	1	1	1	0	1	0	1	X	X	X	X	X	X	X	X	X	Read UPIO configuration bits.
DOUTR	X	X	X	X	X	X	X	X	UP3-2	UP2-2	UP1-2	UP0-2	UP3-1	UP2-1	UP1-1	UP0-1	
SETTLING-TIME-MODE BITS																	
DIN	1	1	1	0	1	1	0	X	X	X	X	X	SPDD	SPDC	SPDB	SPDA	Write DAC_ settling-time-mode bits; see Table 11.

Table 2b. Advanced-Feature Programming Commands (continued)

DATA	CONTROL BITS				DATA BITS												Function
	C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
DIN	1	1	1	0	1	1	1	X	X	X	X	X	X	X	X	X	Read DAC_ settling-time-mode bits.
DOUTR	X	X	X	X	X	X	X	X	X	X	X	X	SPDD	SPDC	SPDB	SPDA	
DAC CPOL/CPHA BITS																	
DIN	1	1	1	1	0	0	0	0	X	X	X	X	X	X	CPOL	CPHA	Write CPOL, CPHA control bits.
DIN	1	1	1	1	0	0	0	1	X	X	X	X	X	X	X	X	Read CPOL, CPHA control bits.
DOUTR	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CPOL	CPHA	
UPIO_ AS GPI (GENERAL-PURPOSE INPUT)																	
DIN	1	1	1	1	0	0	1	X	X	X	X	X	X	X	X	X	Read UPIO_ inputs (valid only when UPIO1 or UPIO2 is configured as a general-purpose input); see Table 21.
DOUTRB	X	X	X	X	X	X	X	X	X	X	RTP2	LF2	LR2	RTP1	LF1	LR1	
OTHER COMMANDS																	
DIN	1	1	1	1	1	1	0	0	X	X	X	X	X	X	X	X	Command is ignored.
DIN	1	1	1	1	1	1	0	1	X	X	X	X	X	X	X	X	Command is ignored.
DIN	1	1	1	1	1	1	1	0	X	X	X	X	X	X	X	X	Command is ignored.
DIN	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	16-bit no-op command. all DACs are unaffected.

X = Don't care.

Table 2c. 24-Bit Read Commands

DATA	CONTROL BITS				DATA BITS																												FUNCTION
	C3	C2	C1	C0	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
READ INPUT AND DAC REGISTERS A—D																																	
DIN	1	1	1	1	0	1	0	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	Read input register A and DAC register A (all 24 bits).**†
DOUTRB	X	X	X	X	X	X	X	X	D23	D22	D21	D20	D19	D18	D17	D16	D15/X	D14/X	D13/X	D12/X	D11	D10	D9	D8	D7	D6	D5	D4	D3/X	D2/X	D1/X	D0/X	
DIN	1	1	1	1	0	1	1	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	Read input register B and DAC register B (all 24 bits).**†
DOUTRB	X	X	X	X	X	X	X	X	D23	D22	D21	D20	D19	D18	D17	D16	D15/X	D14/X	D13/X	D12/X	D11	D10	D9	D8	D7	D6	D5	D4	D3/X	D2/X	D1/X	D0/X	
DIN	1	1	1	1	1	0	0	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	Read input register C and DAC register C (all 24 bits).**†
DOUTRB	X	X	X	X	X	X	X	X	D23	D22	D21	D20	D19	D18	D17	D16	D15/X	D14/X	D13/X	E12/X	D11	D10	D9	D8	D7	D6	D5	D4	D3/X	D2/X	D1/X	D0/X	
DIN	1	1	1	1	1	0	1	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	Read input register D and DAC register D (all 24 bits).**†
DOUTRB	X	X	X	X	X	X	X	X	D23	D22	D21	D20	D19	D18	D17	D16	D15/X	D14/X	D13/X	E12/X	D11	D10	D9	D8	D7	D6	D5	D4	D3/X	D2/X	D1/X	D0/X	

X = Don't care.

***D23–D12 represent the 12-bit data from the appropriate DAC output register. D11–D0 represent the 12-bit data from the corresponding input register. For the MAX5582/MAX5583, bits D13, D12, D1, and D0 are don't-care bits. For the MAX5584/MAX5585, bits D15–D12 and D3–D0 are don't-care bits.*

†During readback, all ones (0xFF) must be clocked into DIN for all 24 bits. No command can be issued before all 24 bits have been clocked out. CS must be kept low while all 24 bits are clocked out.

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

DAC Programming Examples:
To load input register A from the shift register, leaving DAC register A unchanged (DAC output unchanged), use the command in Table 3.

The MAX5580–MAX5585 can load all the input registers (A–D) simultaneously from the shift register, leaving the DAC registers unchanged (DAC output unchanged), by using the command in Table 4.

To load all the input registers (A–D) and all the DAC registers (A–D) simultaneously, use the command in Table 5.

For the 10-bit and 8-bit versions, set sub-bits = 0 for best performance.

Advanced-Feature Programming Commands

Select Bits (M_)

The select bits allow synchronous updating of any combination of channels. The select bits command the loading of the DAC register from the input register of each channel. Set the select bit M_ = 1 to load the DAC register "_" with data from the input register "_", where "_" is replaced with A, B, C, or D, depending on the selected channel. Setting the select bit M_ = 0 results in no action for that channel (Table 6).

Select Bits Programming Example:
To load DAC register B from input register B while keeping other channels (A, C, D) unchanged, set MB = 1 and M_ = 0 (Table 7).

Table 3. Load Input Register A from Shift Register

DATA	CONTROL BITS				DATA BITS											
DIN	0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0

Table 4. Load Input Registers (A–D) from Shift Register

DATA	CONTROL BITS				DATA BITS											
DIN	1	1	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0

Table 5. Load Input Registers (A–D) and DAC Registers (A–D) from Shift Register

DATA	CONTROL BITS				DATA BITS											
DIN	1	1	0	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0

Table 6. Select Bits (M_)

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	0	0	0	X	X	X	X	X	X	MD	MC	MB	MA

X = Don't care.

Table 7. Select Bits Programming Example

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	0	0	0	X	X	X	X	X	X	0	0	1	0

X = Don't care.

Shutdown-Mode Bits (PD_0, PD_1)

Use the shutdown-mode bits and control bits to shut down each DAC independently. The shutdown-mode bits determine the output state of the selected channels. The shutdown-control bits put the selected channels into shutdown mode. To select the shutdown mode for DACA–DACD, set PD_0 and PD_1 according to Table 8 (where "_" is replaced with one of the selected channels (A–D)). The three possible states for unity-gain versions are 1) normal operation, 2) shutdown with 1kΩ output impedance, and 3) shutdown with 100kΩ output impedance. The three possible states for force-sense versions are 1) normal operation, 2) shutdown with 1kΩ output impedance, and 3) shutdown with the output in a high-impedance state. Table 9 shows the commands for writing to the shutdown-mode bits. Table 10 shows an example of writing the shutdown-control bits. This command shuts down DACA with 1kΩ to ground and shuts down DACB–DACD with 100kΩ to ground.

Always write the shutdown-mode-bits command first and then write the shutdown-control-bits command to properly shut down the selected channels. The shutdown-control-bits command can be written at any time after the shutdown-mode-bits command. It does not have to immediately follow the shutdown-mode-bits command.

Settling-Time-Mode Bits (SPD_)

The settling-time-mode bits select the settling time (FAST mode or SLOW mode) of the MAX5580–MAX5585. Set SPD_ = 1 to select FAST mode or set SPD_ = 0 to select SLOW mode, where "_" is replaced by A, B, C, or D, depending on the selected channel (Table 11). FAST mode provides a 3µs maximum settling time, and SLOW mode provides a 6µs maximum settling time.

Table 8. Shutdown-Mode Bits

PD_1	PD_0	DESCRIPTION
0	0	Shutdown with 1kΩ termination to ground on DAC_ output.
0	1	Shutdown with 100kΩ termination to ground on DAC_ output for unity-gain versions. Shutdown with high-impedance output for force-sense versions.
1	0	Ignored.
1	1	DAC_ is powered up in its normal operating mode.

Table 9. Shutdown-Mode Write Command

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	0	0	1	0	X	PDD1	PDD0	PDC1	PDC0	PDB1	PDB0	PDA1	PDA0

X = Don't care.

Table 10. Shutdown-Mode-Bits Write Example

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	0	0	1	0	X	0	1	0	1	0	1	0	0

X = Don't care.

Table 11. Settling-Time-Mode Write Command

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	0	1	1	0	X	X	X	X	X	SPDD	SPDC	SPDB	SPDA

X = Don't care.

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

Settling-Time-Mode Write Example:
To configure DACA and DACD into FAST mode and DACB and DACC into SLOW mode, use the command in Table 12.

To read back the settling-time-mode bits, use the command in Table 13.

CPOL and CPHA Control Bits

The CPOL and CPHA control bits of the MAX5580–MAX5585 are defined the same as the CPOL and CPHA bits in the SPI standard. Set the DAC's CPOL and CPHA bits to CPOL = 0 and CPHA = 0 or CPOL = 1 and CPHA = 1 for MICROWIRE and SPI applications requiring the clocking of data in on the rising edge of SCLK. Set the DAC's CPOL and CPHA bits to CPOL = 0 and CPHA = 1 or CPOL = 1 and CPHA = 0 for DSP and SPI applications, requiring the clocking of data in on the falling edge of SCLK (refer to the *Programmer's Handbook* and see Table 14 for details). At power-up, if $\overline{DSP}$ = DV_{DD}, the default value of CPHA is zero and if $\overline{DSP}$ = DGND, the default value of CPHA is one. The default value of CPOL is zero at power-up.

To write to the CPOL and CPHA bits, use the command in Table 15.

To read back the device's CPOL and CPHA bits, use the command in Table 16.

Table 12. Settling-Time-Mode Write Example

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	0	1	1	0	X	X	X	X	X	1	0	0	1

X = Don't care.

Table 13. Settling-Time-Mode Read Command

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	0	1	1	1	1	X	X	X	X	X	X	X	X
DOUTRB	X	X	X	X	X	X	X	X	X	X	X	X	SPDD	SPDC	SPDB	SPDA

X = Don't care.

Table 14. CPOL and CPHA Bits

CPOL	CPHA	DESCRIPTION
0	0	Default values at power-up when $\overline{DSP}$ is connected to DV_{DD}. Data is clocked in on the rising edge of SCLK.
0	1	Default values at power-up when $\overline{DSP}$ is connected to DGND. Data is clocked in on the falling edge of SCLK.
1	0	Data is clocked in on the falling edge of SCLK.
1	1	Data is clocked in on the rising edge of SCLK.

Table 15. CPOL and CPHA Write Command

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	1	0	0	0	0	X	X	X	X	X	X	CPOL	CPHA

X = Don't care.

Table 16. CPOL and CPHA Read Command

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	1	0	0	0	1	X	X	X	X	X	X	X	X
DOUTRB	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CPOL	CPHA

X = Don't care.

UPIO Bits (UPSL1, UPSL2, UP0–UP3)

The MAX5580–MAX5585 provide two user-programmable input/output (UPIO) ports: UPIO1 and UPIO2. These ports have 15 possible configurations, as shown in Table 21. UPIO1 and UPIO2 can be programmed independently or simultaneously by writing to the UPSL1, UPSL2, and UP0–UP3 bits (Table 17).

Table 18 shows how UPIO1 and UPIO2 are selected for configuration. The UP0–UP3 bits select the desired functions for UPIO1 and/or UPIO2 (Table 21).

UPIO Programming Example:

To set only UPIO1 as $\overline{LDAC}$ and leave UPIO2 unchanged, use the command in Table 19.

The UPIO selection and configuration bits can be read back from the MAX5580–MAX5585 when UPIO1 or UPIO2 is configured as a DOUTRB output. Table 20 shows the read-back data format for the UPIO bits. Writing the command in Table 20 initiates a read operation of the UPIO bits. The data is clocked out starting on the 9th clock cycle of the sequence. Bits UP3-2 through UP0-2 provide the UP3–UP0 configuration bits for UPIO2 (Table 21), and bits UP3-1 through UP0-1 provide the UP3–UP0 configuration bits for UPIO1.

Table 17. UPIO Write Command

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	0	1	0	0	X	UPSL2	UPSL1	UP3	UP2	UP1	UP0	X	X

X = Don't care.

Table 18. UPIO Selection Bits (UPSL1 and UPSL2)

UPSL2	UPSL1	UPIO PORT SELECTED
0	0	None selected
0	1	UPIO1 selected
1	0	UPIO2 selected
1	1	Both UPIO1 and UPIO2 selected

Table 19. UPIO Programming Example

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	0	1	0	0	X	0	1	0	0	0	0	X	X

X = Don't care.

Table 20. UPIO Read Command

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	0	1	0	1	X	X	X	X	X	X	X	X	X
DOUTRB	X	X	X	X	X	X	X	X	UP3-2	UP2-2	UP1-2	UP0-2	UP3-1	UP2-1	UP1-1	UP0-1

X = Don't care.

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

UPIO Configuration

Table 21 lists the possible configurations for UPIO1 and UPIO2. UPIO1 and UPIO2 use the selected function when configured by the UP3–UP0 configuration bits.

$\overline{LDAC}$

$\overline{LDAC}$ controls the loading of the DAC registers. When $\overline{LDAC}$ is high, the DAC registers are latched, and any change in the input registers does not affect the contents of the DAC registers or the DAC outputs. When $\overline{LDAC}$ is low, the DAC registers are transparent, and the values stored in the input registers are fed directly to the DAC registers, and the DAC outputs are updated.

Drive $\overline{LDAC}$ low to asynchronously load the DAC registers from their corresponding input registers (DACs that are in shutdown remain shut down). The $\overline{LDAC}$ input does not require any activity on $\overline{CS}$, SCLK, or DIN to take effect. If $\overline{LDAC}$ is brought low coincident with a rising edge of $\overline{CS}$ (which executes a serial command modifying the value of either DAC input register), then $\overline{LDAC}$ must remain asserted for at least 120ns following the $\overline{CS}$ rising edge. This requirement applies only for serial commands that modify the value of the DAC input registers. See Figures 5 and 6 for timing details.

Table 21. UPIO Configuration Register Bits (UP3–UP0)

UPIO CONFIGURATION BITS				FUNCTION	DESCRIPTION
UP3	UP2	UP1	UP0		
0	0	0	0	$\overline{LDAC}$	Active-Low Load DAC Input. Drive low to asynchronously load all DAC registers with data from input registers.
0	0	0	1	$\overline{SET}$	Active-Low Input. Drive low to set all input and DAC registers to full scale.
0	0	1	0	$\overline{MID}$	Active-Low Input. Drive low to set all input and DAC registers to midscale.
0	0	1	1	$\overline{CLR}$	Active-Low Input. Drive low to set all input and DAC registers to zero scale.
0	1	0	0	$\overline{PDL}$	Active-Low Power-Down Lockout Input. Drive low to disable software shutdown.
0	1	0	1	Reserved	This mode is reserved. Do not use.
0	1	1	0	$\overline{SHDN1K}$	Active-Low 1kΩ Shutdown Input. Overrides PD_1 and PD_0 settings. For the MAX5580/MAX5582/MAX5584, drive $\overline{SHDN1K}$ low to pull OUTA–OUTD to AGND with 1kΩ. For the MAX5581/MAX5583/MAX5585, drive $\overline{SHDN1K}$ low to leave OUTA–OUTD high impedance.
0	1	1	1	$\overline{SHDN100K}$	Active-Low 100kΩ Shutdown Input. Overrides PD_1 and PD_0 settings. For the MAX5580/MAX5582/MAX5584, drive $\overline{SHDN100K}$ low to pull OUTA–OUTD to AGND with 100kΩ. For the MAX5581/MAX5583/MAX5585, drive low to leave OUTA–OUTD high impedance.
1	0	0	0	DOUTRB	Data Read-Back Output
1	0	0	1	DOUTDC0	Mode 0 Daisy-Chain Data Output. Data is clocked out on the falling edge of SCLK.
1	0	1	0	DOUTDC1	Mode 1 Daisy-Chain Data Output. Data is clocked out on the rising edge of SCLK.
1	0	1	1	GPI	General-Purpose Logic Input
1	1	0	0	GPOL	General-Purpose Logic-Low Output
1	1	0	1	GPOH	General-Purpose Logic-High Output
1	1	1	0	TOGG	Toggle Input. Toggles DAC outputs between data in input registers and data in DAC registers. Drive low to set all DAC outputs to values stored in input registers. Drive high to set all DAC outputs to values stored in DAC registers.
1	1	1	1	$\overline{FAST}$	Fast/Slow Settling-Time-Mode Input. Drive low to select FAST (3µs) mode or drive high to select SLOW (6µs) settling mode. Overrides the SPDA–SPDD settings.

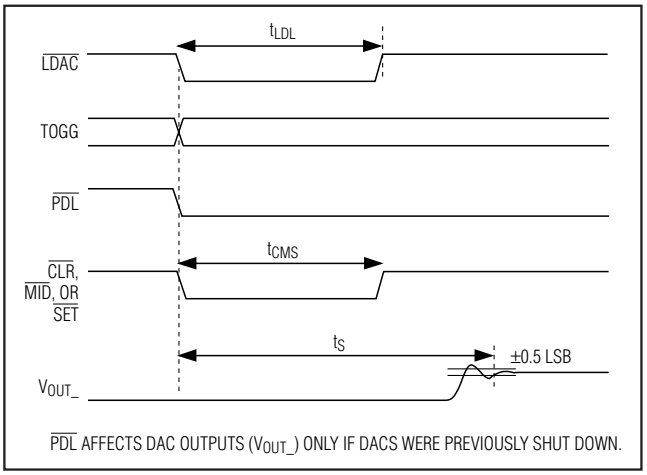


Figure 5. Asynchronous Signal Timing

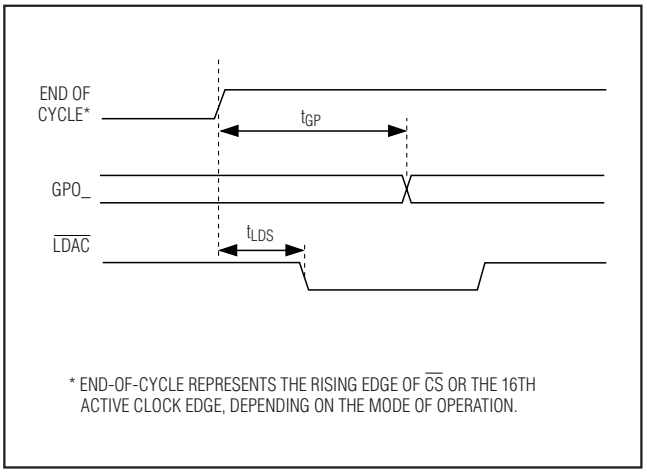


Figure 6. GPO_ and LDAC Signal Timing

SET, MID, CLR

The SET, MID, and CLR signals force the DAC outputs to full scale, midscale, or zero scale (Figure 5). These signals cannot be active at the same time.

The active-low SET input forces the DAC outputs to full scale when SET is low. When SET is high, the DAC outputs follow the data in the DAC registers.

The active-low MID input forces the DAC outputs to midscale when MID is low. When MID is high, the DAC outputs follow the data in the DAC registers.

The active-low CLR input forces the DAC outputs to zero scale when CLR is low. When CLR is high, the DAC outputs follow the data in the DAC registers.

If CLR, MID, or SET signals go low during a write command, reload the data to ensure accurate results.

Power-Down Lockout (PDL)

The PDL active-low, software-shutdown lockout input overrides (not overwrites) the PD_0 and PD_1 shutdown-mode bits. PDL cannot be active at the same time as SHDN1K or SHDN100K (see the *Shutdown Mode (SHDN1K, SHDN100K)* section).

If the PD_0 and PD_1 bits command the DAC to shut down prior to PDL going low, the DAC returns to shutdown mode immediately after PDL goes high, unless the PD_0 and PD_1 bits were modified through the serial interface in the meantime.

Shutdown Mode (SHDN1K, SHDN100K)

The SHDN1K and SHDN100K are active-low signals that override (not overwrite) the PD_1 and PD_0 bit settings. For the MAX5580/MAX5582/MAX5584, drive SHDN1K low to select shutdown mode with OUTA–OUTD internally terminated with 1kΩ to ground, or drive SHDN100K low to select shutdown with an internal 100kΩ termination. For the MAX5581/MAX5583/MAX5585, drive SHDN1K low for shutdown with 1kΩ output termination, or drive SHDN100K low for shutdown with high-impedance outputs.

Data Output (DOUTRB, DOUTDC0, DOUTDC1)

UPIO1 and UPIO2 can be configured as serial data outputs, DOUTRB (data out for read back), DOUTDC0 (data out for daisy-chaining, mode 0), and DOUTDC1 (data out for daisy-chaining, mode 1). The differences between DOUTRB and DOUTDC0 (or DOUTDC1) are as follows:

- The source of read-back data on DOUTRB is the DOUT register. Daisy-chain DOUTDC_ data comes directly from the shift register.
- Read-back data on DOUTRB is only present after a DAC read command. Daisy-chain data is present on DOUTDC_ for any DAC write after the first 16 bits are written.
- The DOUTRB idle state (CS = high) for read back is high impedance. Daisy-chain DOUTDC_ idles high when inactive to avoid floating the data input in the next device in the daisy-chain.

See Figures 1 and 2 for timing details.

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

GPI, GPOL, GPOH

UPIO1 and UPIO2 can each be configured as a general-purpose input (GPI), a general-purpose output low (GPOL), or a general-purpose output high (GPOH).

The GPI can serve to detect interrupts from µPs or microcontrollers. The GPI has three functions:

1) Sample the signal at GPI at the time of the read (RTP1 and RTP2).
2) Detect whether a falling edge has occurred since the last read or reset (LF1 and LF2).
3) Detect whether a rising edge has occurred since the last read or reset (LR1 and LR2).

RTP1, LF1, and LR1 represent the data read from UPIO1; RTP2, LF2, and LR2 represent the data read from UPIO2.

To issue a read command for the UPIO configured as GPI, use the command in Table 22.

Once the command is issued, RTP1 and RTP2 provide the real-time status (0 or 1) of the inputs at UPIO1 or UPIO2, respectively, at the time of the read. If LF2 or LF1 is one, then a falling edge has occurred on the respective UPIO1 or UPIO2 input since the last read or reset. If LR2 or LR1 is one, then a rising edge has occurred since the last read or reset.

GPOL outputs a constant low, and GPOH outputs a constant high. See Figure 6.

TOGG

Use the TOGG input to toggle the DAC outputs between the values in the input registers and DAC registers. A delay of greater than 100ns from the end of the previous write command is required before the TOGG signal can be correctly switched between the new value and the previously stored value. When TOGG = 0, the output follows the information in the input registers. When TOGG = 1, the output follows the information in the DAC register (Figure 5).

$\overline{FAST}$

The MAX5580–MAX5585 have two settling-time-mode options: FAST (3µs max) and SLOW (6µs max). To select the FAST mode, drive $\overline{FAST}$ low, and to select SLOW mode, drive $\overline{FAST}$ high. This overrides (not overwrites) the SPDA–SPDD bit settings.

Table 22. GPI Read Command

DATA	CONTROL BITS								DATA BITS							
DIN	1	1	1	1	0	0	1	X	X	X	X	X	X	X	X	X
DOUTRB	X	X	X	X	X	X	X	X	X	X	RTP2	LF2	LR2	RTP1	LF1	LR1

X = Don't care.

Table 23. Unipolar Code Table (Gain = +1)

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+V_{REF}$ (4095 / 4096)
1000	0000	0001	$+V_{REF}$ (2049 / 4096)
1000	0000	0000	$+V_{REF}$ (2048 / 4096) = V_{REF} / 2
0111	1111	1111	$+V_{REF}$ (2047 / 4096)
0000	0000	0001	$+V_{REF}$ (1 / 4096)
0000	0000	0000	0

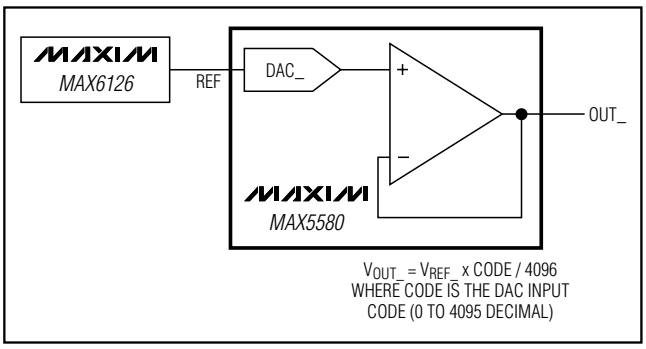


Figure 7. Unipolar Output Circuit

Applications Information

Unipolar Output

Figure 7 shows the unity-gain MAX5580 in a unipolar output configuration. Table 23 lists the unipolar output codes.

Bipolar Output

The MAX5580 outputs can be configured for bipolar operation, as shown in Figure 8. The output voltage is given by the following equation:

$$V_{OUT_} = V_{REF} \times (CODE - 2048) / 2048$$

where CODE represents the numeric value of the DAC's binary input code (0 to 4095 decimal). Table 24 shows digital codes and the corresponding output voltage for the circuit in Figure 8.

Configurable Output Gain

The MAX5581/MAX5583/MAX5585 have force-sense outputs, which provide a direct connection to the inverting terminal of the output op amp, yielding the most flexibility. The force-sense output has the advantage that specific gains can be set externally for a given application. The gain error for the MAX5581/MAX5583/MAX5585 is specified in a unity-gain configuration (op-amp output and inverting terminals connected), and additional gain error results from external resistor tolerances. The force-sense DACs allow many useful circuits to be created with only a few simple external components.

An example of a custom, fixed gain using the MAX5581's force-sense output is shown in Figure 9. In this example, the external reference is set to 1.25V, and the gain is set to +1.1V/V with external discrete resistors to provide an approximate 0 to 1.375V DAC output voltage range.

$$V_{OUT} = [(0.5 \times V_{REF_} \times CODE) / 4096] \times [1 + (R2 / R1)]$$

where CODE represents the numeric value of the DAC's binary input code (0 to 4095 decimal).

In this example, R2 = 12kΩ and R1 = 10kΩ to set the gain = 1.1V/V:

$$V_{OUT} = [(0.5 \times 1.25V \times CODE) / 4096] \times 2.2$$

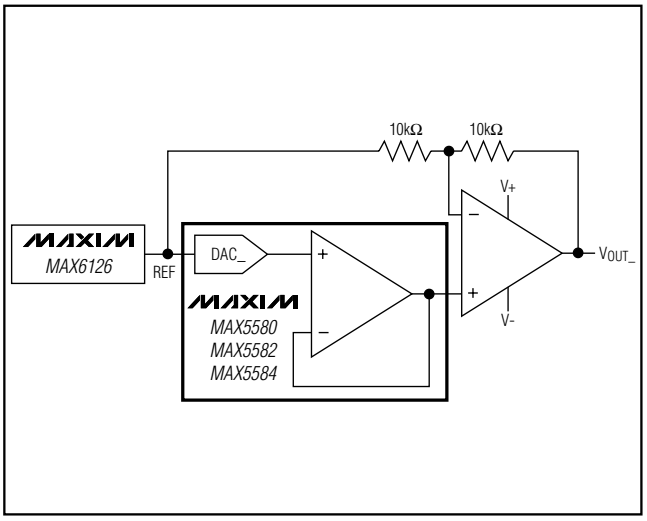


Figure 8. Bipolar Output Circuit

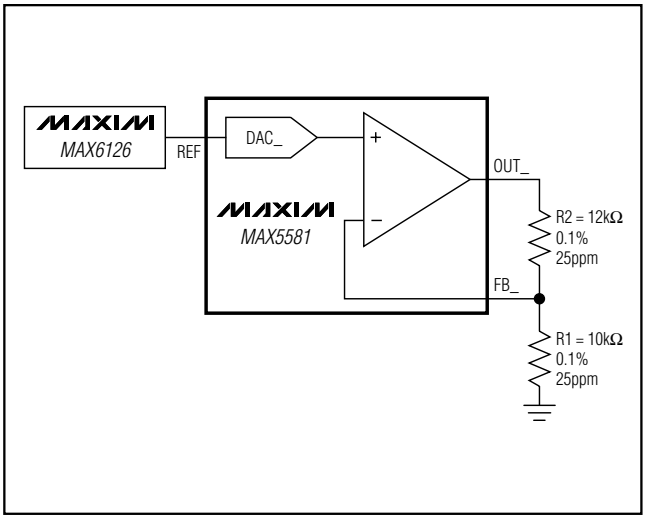


Figure 9. Configurable Output Gain

Table 24. Bipolar Code Table (Gain = +1)

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+V_{REF}$ (2047 / 2048)
1000	0000	0001	$+V_{REF}$ (1 / 2048)
1000	0000	0000	0
0111	1111	1111	$-V_{REF}$ (1 / 2048)
0000	0000	0001	$-V_{REF}$ (2047 / 2048)
0000	0000	0000	$-V_{REF}$ (2048 / 2048) = $-V_{REF}$

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

Power-Supply and Layout Considerations

Bypass the analog and digital power supplies by using a 10µF capacitor in parallel with a 0.1µF capacitor to AGND and DGND (Figure 10). Minimize lead lengths to reduce lead inductance. Use shielding and/or ferrite beads to further increase isolation.

Digital and AC transient signals coupling to AGND can create noise at the output. Connect AGND to the highest quality ground available. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane. Wire-wrapped boards and sockets are not recommended. For optimum system performance, use PC boards with separate analog and digital ground planes. Connect the two ground planes together at the low-impedance power-supply source.

Using separate power supplies for AV_{DD} and DV_{DD} improves noise immunity. Connect AGND and DGND at the low-impedance power-supply sources (Figure 11).

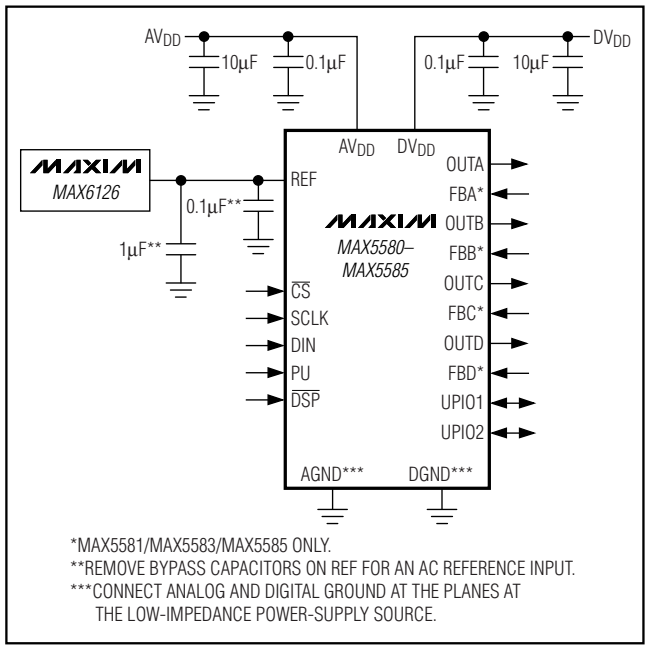


Figure 10. Bypassing Power Supplies AV_{DD}, DV_{DD}, and REF

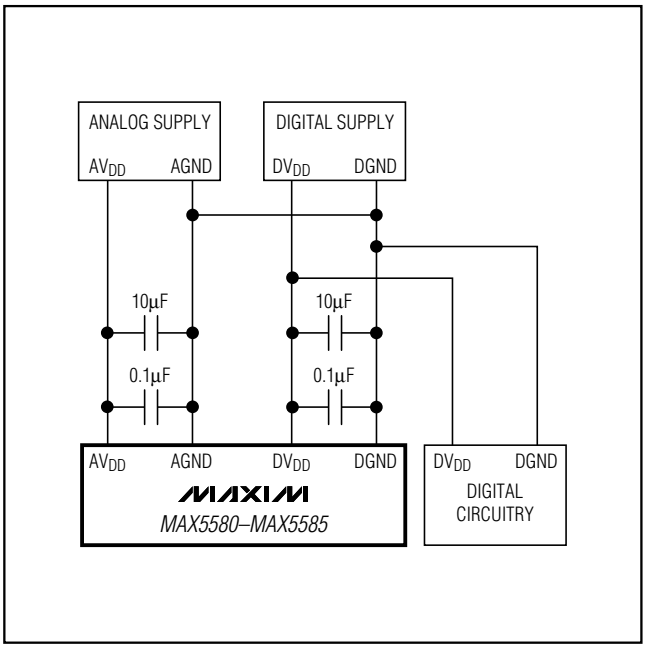
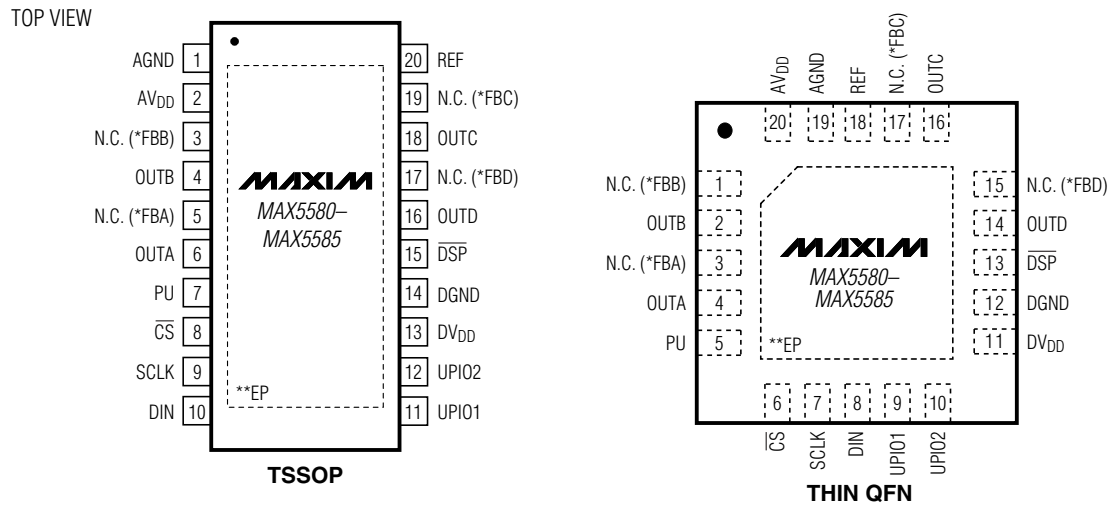


Figure 11. Separate Analog and Digital Power Supplies

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

Pin Configurations



*FOR THE MAX5581/MAX5583/MAX5585
**EXPOSED PADDLE CONNECTED TO AGND

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX5580BEUP	-40°C to +85°C	20 TSSOP-EP*
MAX5580BETP	-40°C to +85°C	20 Thin QFN-EP*
MAX5581AEUP	-40°C to +85°C	20 TSSOP-EP*
MAX5581AETP	-40°C to +85°C	20 Thin QFN-EP*
MAX5581BEUP	-40°C to +85°C	20 TSSOP-EP*
MAX5581BETP	-40°C to +85°C	20 Thin QFN-EP*
MAX5582EUP	-40°C to +85°C	20 TSSOP-EP*
MAX5582ETP	-40°C to +85°C	20 Thin QFN-EP*
MAX5583EUP	-40°C to +85°C	20 TSSOP-EP*
MAX5583ETP	-40°C to +85°C	20 Thin QFN-EP*
MAX5584EUP	-40°C to +85°C	20 TSSOP-EP*
MAX5584ETP	-40°C to +85°C	20 Thin QFN-EP*
MAX5585EUP	-40°C to +85°C	20 TSSOP-EP*
MAX5585ETP	-40°C to +85°C	20 Thin QFN-EP*

*EP = Exposed paddle.

Chip Information

TRANSISTOR COUNT: 24,393

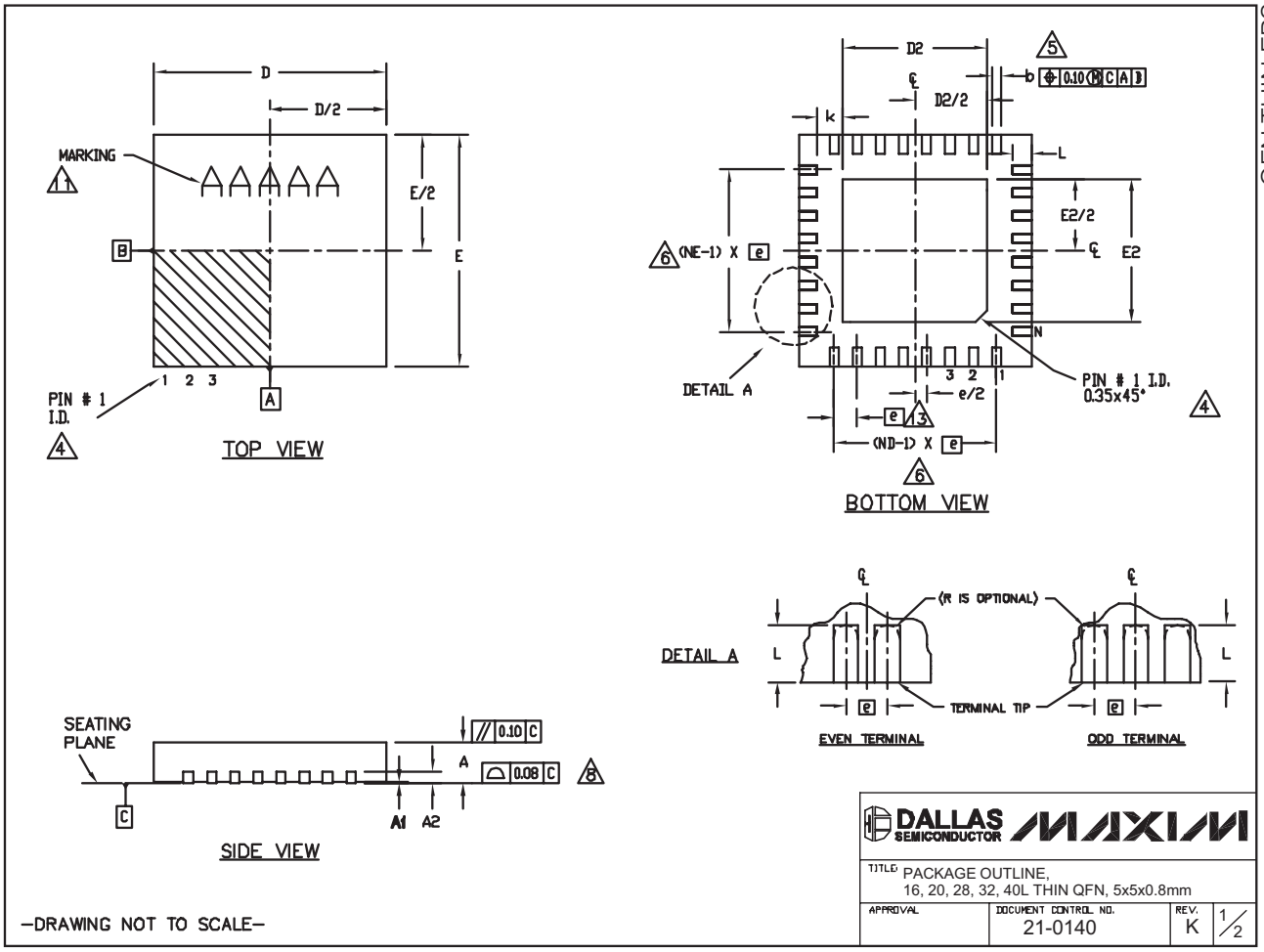
PROCESS: BiCMOS

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25	
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	16			20			28			32			40			
ND	4			5			7			8			10			
NE	4			5			7			8			10			
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055M-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

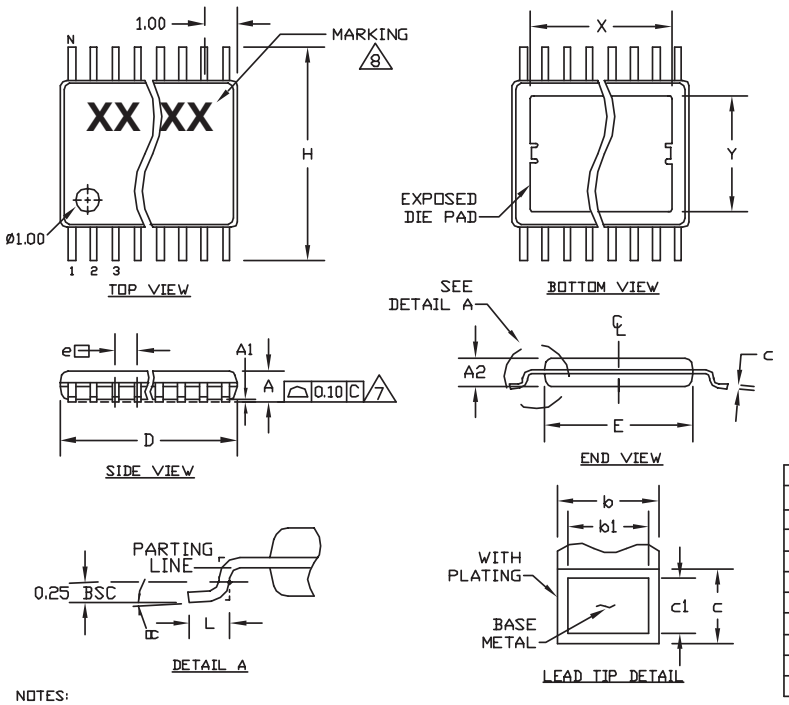
TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0140	REV. K	2/2

Buffered, Fast-Settling, Quad, 12-/10-/8-Bit, Voltage-Output DACs

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP 4.4mm BODY.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	--	1.10	--	0.043
A1	0.00	0.15	0.000	0.006
A2	0.85	0.95	0.033	0.037
b	0.19	0.30	0.007	0.012
b1	0.19	0.25	0.007	0.010
c	0.090	0.20	0.004	0.008
c1	0.090	0.135	0.004	0.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	0.112	0.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
ABT-1	14	D	4.90	5.10	0.193	0.201
		X	2.95	3.25	0.116	0.128
ABT	16	D	4.90	5.10	0.193	0.201
		X	2.85	3.15	0.112	0.124
ACT	20	D	6.40	6.60	0.252	0.260
		X	4.00	4.34	0.157	0.171
AET	28	D	9.60	9.80	0.378	0.386
		X	5.35	5.65	0.211	0.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0108	E	1/1

Revision History

Pages changed at Rev 3: 1, 6–9, 34, 35, 36

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