Features

- **Comprehensive Library of Standard Logic and I/O Cells**
- **ATC18RHA Core pads Designed to Operate with V_{DD} = 1.8V +/- 0.15V as Main Condition**
- **IO33 Pad Libraries Provide Interfaces to 3.3+/-0.3V and 2.5 +/- 0.25V Environments**
- **Memory Cells Compiled or synthesized to the Requirements of the Design**
- **EDAC Library**
- **Cold Sparing Buffers**
- **High Speed LVDS Buffers (655Mbps)**
- **PCI Buffers**
- **Predefined Die Sizes to Accommodate Standardized Packages and ESA (European Space Agency) Multi-project Wafer Services**
- **MQFP Package Up to 352 Pins (336 Signal Pins)**
- **MCGA Packages Up to 625 Pins (575 Signal Pins)**
- **ESD better than 2000V for IO33 and better than 1000V for PLL**
- **No single event latch-up below a LET threshold of 80 Mev/mg/cm² at ambient temperature**
- **SEU hardened flip-flops**
- **Tested up to a total dose of 300 krads (Si) according to Mil Std 883 Test Method 1019**
- **Quality Grades: QML-Q and QML-V with 5962-06B02, ESCC 9000**

Description

The ATC18RHA is fabricated on a proprietary 0.18 µm, five-metal-layers CMOS process intended for use with a supply voltage of 1.8V ± 0.15V.

The Atmel cell libraries and memory compilers have been designed and or characterized in order to be compatible with each other. Simulation representations exist for three types of operating conditions. They correspond to three characterization condition sets defined as follows:

- MIN conditions:
  - – T_J = -55°C
  - – V_{DD} (cell) = 1.95V
  - – Process = fast (0.95)
- TYP conditions:
  - – T_J = +25°C
  - – V_{DD} (cell) = 1.8V
  - – Process = typical (1)
- MAX conditions:
  - – T_J = +125°C
  - – V_{DD} (cell) = 1.65V
  - – Process = slow (1.1)

Rad. Hard 0.18 µm CMOS Cell-based ASIC for Space Use

ATC18RHA

4261F–AERO–08/08

Overview

Introduction

The ASIC ATC18RHA Design Manual presents all the required information and flows for 0.18µm designs for aerospace applications, allowing users to view Atmel specific or standard commercial tool kits and methodological details for actual implementations.

This offering is a 0.18µm CMOS technology based, using 5 Metal layers, and specified with the 3.3V or 2.5V range for the periphery, and with the 1.8V range for the core. The technology parameters and some extra features are described here after.

Periphery

Buffers Description

The peripheral buffer (also called pad) is the electrical interface between the external signals (voltage range from 0 to 3.3V) and the internal core signals (from 0 to 1.8V).

Several Power Supply rails are used inside the chip.

The ATC18RHA buffer family is called I033 family:

• VCCB = 3.3V *(3V to 3.6V) and 2.5V (2.25V to 2.75V)*

IO33 family contains:

• Bidirectional pads

• Tristate Output pads

• Output Only pads

• Input Only pads *(Inverting,Non-Inverting,Schmitt Trigger)*

Furthermore the Bidirectional, Tristate Ouputs and Input Only pads are available with or without **Pull-Up** or **Pull-Down** structures.

Specific pads have been developed in 3.3V and 2.5V:

• **LVDS** transmitter and Receiver differential pads

• **LVPECL** Receiver differential pads

And, in 3.3V only:

• **PCI** Bidirectional, Tristate Output and Output Only pads

Standard pads Input level compatibility

• IO33: CMOS,LVTTL compatible

Tolerance and Cold Sparing Features

All IO33 pads are **Cold Sparing**. This means that when VCCB is “off” these pads have a negligible leakage current.

Furthermore standard IO33 pads (PCI,LVDS,LVPECL excepted) are **tolerant**. This means that when

- the pad is configured as an input
- VCCB is < 3.3V (ex 2.5V)
- The external signal can go up to 3.3V (max 3.6V) with negligible leakage current.

Clusters

The periphery of the chip (pad ring) can be split into several I/O segments *(I/O clusters)* which can be supplied at different voltages (ie “n” clusters at 2.5V and “m” clusters at 3.3V). Some clusters can be unpowered while others are active.

A specific Power control line is distributed inside the cluster to be able to force all the I/Os of the cluster in tristate mode whatever their initial state is (ie: an output only buffer will also be turned to HiZ mode).

This Power Control line can be driven in two ways:

- **Cold Sparing** mode: the Power control line is active when VCCB is “off” (case of VCCB Power Supply Pad including a Power Control feature).
- **Hot Swap** mode: a specific pad in the cluster is dedicated to Power Control. When this pad is left open (driven to “0” by an internal pull-down) the Power Control line is activated.

ESD Protection

The introduction of a multiple supply architecture increases the sensitivity to Electro-Static Discharges. In ATC18RHA periphery, the VCCB,VSSB supplies are isolated from VCC, VSS supplies and furthermore when making clusters, the VCCB supply rail is split into several segments.

A solution to improve ESD immunity consists in adding discharge conduction paths between supply rails. To implement this solution some specific cells must be inserted in the Pad Ring.

Two kinds of cells are used:

- *Back to Back Diodes* between VSSB and VSS
- *Grounded N-Gates* between two VCCB segments

Some ESD cells are “pad count” transparent (implemented in the Die Corners) but others must be taken into account in the Pad Ring definition (each ESD cell has the size of a standard pad).

Double Pad Ring

In the double pad ring configuration, all core power supply pads must be moved to the inner ring and PV18IxxZ pads must be replaced by PV18IDxxZ pads. Therefore, there must be no PV18ID00Z or PV18ID18Z pads left on the outer ring .

The number of pads on the inner ring will be tailored to the actual need of each design.

These core supplies are automatically routed to the inner ring. As long as the double pad ring configuration is used only for core supply pads, the designs are produceable to space quality levels.

During the detailed feasibility study, an investigation will be conducted to evaluate if additional pads, and how many, can be added to the inner ring to be used as pure CMOS IO and their power supplies, and still be produced to space quality. Anyhow, the resulting total number of pads on the inner ring must not go above the maximum number given in the table 4.

Warning: there is no means to have any LVDS IO and their power supplies moved to the inner ring.

Pad Site and Pad Pitch

In the ATC18RHA95 family the minimum Pad Width and Pad Pitch are 95µm.

Case of Differential Pads

- LVDS transmitter: width= 3x95µm and pitch= 190µm
- LVDS Receiver and LVPECL Receiver : width= 2x95µm and pitch=95µm

PCI Buffers

The PCI buffers are based on the 3.3V PCI standard where Inputs are required to be clamped to both ground and VCCB (3.3V) rails. To be also Cold Sparing these buffers are:

• Cold sparing when VCCB=0V (clamped to VSSB only)

• clamped to VCCB and VSSB when VCCB=3.3V

The PCI family includes 3 buffer types:

• **PP33B01Z** : Bidirectional

• **PP33T01Z** : 3-state Output

• **PP33O01Z** : Output only

The PCI drive strength is almost equivalent to the standard IO33 Drive 08. The main differences are:

• the non tolerance

• the input trigger levels which are slightly lower (VIH min = 0.5 x VCCB V)

LVDS Buffers

The LVDS family is based on the ANSI/TIA/EIA-644 Standard. It is composed of:

- a Voltage /Current Reference (**PL33REFZ or PL25REFZ**).
- a transmitter buffer (**PL33TXZ or PL25TXZ**) with Outp and Outn differential outputs.
- a receiver buffer (**PL33RXZ or PL25RXZ**) with Inp and Inn differential inputs.

The 3 pads are Cold Sparing (high impedance when VCCB=0V) but they are tolerant only when they are disabled (ien = “1” or oen = “1”).

The LVDS standard transmission levels are +/- 350mV differential around 1.25V common mode. As these levels are tight to achieve in military temperature range the PL33REFZ/PL25REFZ pad provides 2 references to the other LVDS pads of the same cluster:

- the external Ref voltage which is used by transmitter only to force the common mode voltage *(Vref)*
- a current reference which is used by both transmitter and receiver *(Iref).*

The LVDS Tx takes the place of three standard I/O pads and the LVDS Rx takes the room of two.

LVPECL Buffer

The PE33RXZ/PE25RXZ PECL buffer is a simplified version of PL33RXZ/PL25RXZ LVDS buffer. It is a differential input with LVPECL levels and it does not need Ref. So it can be implemented inside a standard IO33 cluster.

The PECL RX occupies two standard I/O places.

Power “On/Off” Sequence

In a multiple Power Supplies application the discrepancy between various supply rise/fall times may induce high currents through the ESD protection clamping diodes during Power on/off sequences.

The typical case is when an external signal is applied on an input with Vih > VCCB + 400mV. The input current is mainly limited by the external signal generator impedance.

If many inputs are in that configuration the resulting current may damage the circuit.

Tolerant inputs are not clamped to VCCB (ATC18RHA standard IO33 family) so this potential problem is present only on non tolerant inputs which is the case for specific pads (PCI, LVDS, LVPECL).

In fact for all these pads when VCC is off (whatever VCCB state) the clamping diodes present on inputs are disconnected (inputs are turned to tolerant mode).

So when all the ATC18RHA circuit must be powered on/off while other circuits in the application are still powered on, the recommended sequences are:

• **power-up**: VCCB on -> VCC(vdd!) on

• **power-down**: VCC(vdd!) off -> VCCB off

It is also recommended to stop all activity during these phases as I/O could be in an undetermined state (Input or Output) and create bus contention.

If the ATC18RHA circuit must be partially activated (some clusters on while the others are off) two cases must be considered:

• all the circuit is powered on/off while a particular cluster is always off : as all pads are Cold Sparing there is no problem

• a particular cluster must be power on/off while the rest of the circuit is still on. For tolerant input there is no problem but for not tolerant inputs (PCI) the Hot Swap mode must be used (see Power Control pads in clusters). For LVDS family and LVPECL the disable mode is enough to disconnect input clamping diodes (ien,oen=”1”).

If two ATC18RHA circuits are in parallel (spare configuration) with one circuit powered on/off while the other is always off there is no problem as all pads are Cold Sparing.

PLL

The PLL includes the Loop Filter so the block only needs a specific VCCPLL,VSSPLL 1.8V supply pair.

Core

Core Array

All the cells of the ATC18RHA library are a multiple of a site, each site being 0.56µm width and 5.6µm height. For example, a NAND2 / Drive 2 cell will need 6 sites resulting in a cell size of 3.36µm x 5.6µm or 18.816µm².

Standard cell library

The Atmel Standard Cell Library, SClib, contains a comprehensive set of a combination of logic and storage cells. The SClib library includes cells that belong to the following categories:

• Buffers and Gates

• Multiplexers

• Standard and SEU Hardened Flip-flops

• Standard and SEU Hardened Scan Flip-flops

• Latches

• Adders and Subtractors

Synthesized Memory Blocks

The ATC18RHA Synthesized Memory flow is based on *GENESYS*, an Atmel GATEAID Software.

GENESYS is a software that has been developed to generate synthesizable VHDL blocks and associated scripts for synthesis tools and then produce gate level net-lists in the chosen technology.

Figure 1. Genesys memory synthesis flow

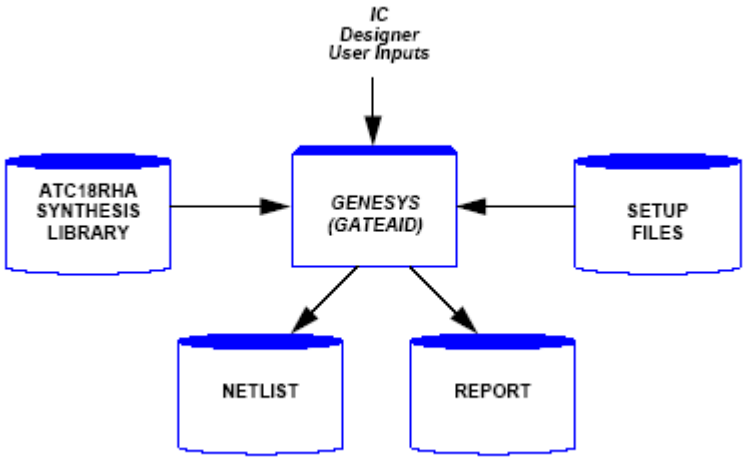


Table 1. Genesys memories size limits

Type	Maximum authorized size
RAM	4K
TPRAM	4K
DPRAM	2K

Memory Hard Blocks

The ATC18RHA memory libraries are developed from Virage memory compilers. All these memories are synchronous.

It can compile single-port synchronous SRAM, dual port (2RW) synchronous SRAM and Two-port (1W,1R) synchronous Register-File.

Recommendations are made in the design manual to help the designer to minimize multiple SEU induced errors per word.

For maximum block sizes, see the design manual.

Array Organization

Though ATC18RHA is a standard cell library, pre-defined matrix sizes and pad frames have been set so as to ease the assembly of every individual ASIC design by sticking to presently available package cavity sizes and layouts. These are close in size to MH1RT matrix sizes.

The following tables demonstrate, for each matrix, for a single or a double pad ring configuration, the maximum number of pads on the outer ring, the maximum number of pads implementable on the inner ring, and the resulting typical gate count capability of each matrix.

Table 2. Single Pad Ring Standard Arrays Dimensions and Integration Capabilities

Name	MH1 Equivalence	Size (mm)	Pads (+power only)	Usable Gates (typ)
ATC18RHA95_216	NA	6.19x6.19	216 (+8)	1M
ATC18RHA95_324	MH1099E	8.76x8.76	324 (+8)	2.2M
ATC18RHA95_404	MH1156E	10.66x10.66	404 (+8)	3.5M
ATC18RHA95_504	MH1242E	13.03x13.03	504 (+8)	5.5M

Table 3. Double Pad Ring: Number of Pads and Integration Capabilities

Name	Outer Ring Programmable Pad	Inner Ring Max Number of Pads	Buffer Power Supply Pads	Usable Gates (typ)
ATC18RHA95_216D	216	88	Corners	0.725M
ATC18RHA95_324D	324	140	8	1.8M
ATC18RHA95_404D	404	180	8	2.97M
ATC18RHA95_504D	504	232	8	4.83M

Design Management

Introduction

Atmel used to propose different design modes, where each mode indicated the designer responsibilities, the design location and the design tools. With designs becoming more complex, timing and power constraints more severe, and design behaviour more technology dependent, Atmel believes that any design must be a close cooperation between the customer and the manufacturer. Therefore, only one design scenario is retained: the ASIC chip is designed by the customer, at his site with a set of design tools supported by Atmel.

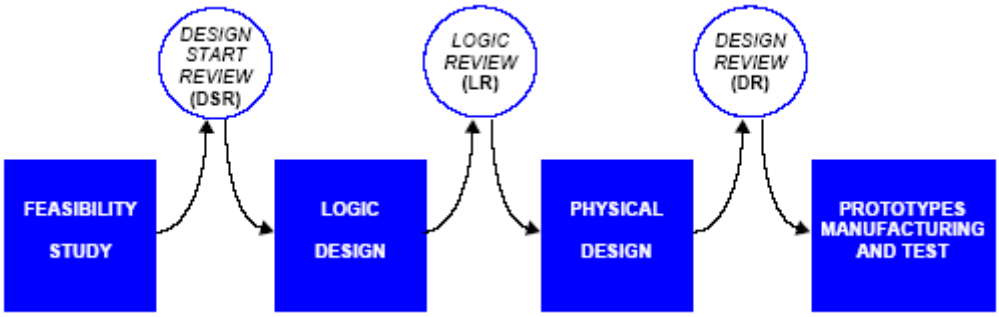
Customers now have the possibility to embark on a Multi Project Wafer (**MPW**). This has no technical impact on the flow which will be described below. There will be some additional planning constraints and new milestones. This is also explained in this section.

Design Phases

The development of an ASIC chip can be split into 4 main phases.

A meeting is set between each phase.

Figure 2. *Design Management Phases*



- Phase 1: Feasibility study
  Meeting: Design Start Review (**DSR**)
- Phase 2: Logic design
  Meeting: Logic Review (**LR**)
- Phase 3: Physical design
  Meeting: Design Review (**DR**)
- Phase 4: Prototypes manufacturing and test

During the review meetings, the conformity of the design to Atmel rules is checked and acknowledged in formal documents, and the data is transferred to the next phase. The content of each phase is described in the following sections. The responsibility of each step is dependent on the design flow. The flows will be described later on.

Phase 1

Feasibility Study

At this step, the customer is asked to provide:

• the project identification (name, type)

• an overall description of the functions of the ASIC

• an estimation of the number of logic gates

• an estimation of the number, size and type of the memory blocks

• other hard/compiled blocks

• macro-cells (PLL)

• the number of I/Os without supply (number of LVDS buffers if requested)

• the number of expected supply buffers for periphery (according drive, simultaneous switching, load...)

• number of simultaneous switching scan FF to determine supply buffers for the core

• preliminary net-list (*)

- preliminary pin-out and floor-plan (*)
- max clock and data rates
- expected a.c. and d.c. characteristics
- expected static and dynamic consumption
- list of design tools at customer's site
- package type
- logic review and design review dates
- prototypes availability date

(*) The availability of a preliminary net-list, pin-out and floor-plan will allow to run a detailed feasibility study. It will consist of making some placement and routing trials with different tools in order to determine the final flow and to anticipate as much tasks as possible prior to the reception of the final net-list.

Depending on the available information, 2 types of feasibility study can be run: First level or detailed feasibility study.

First level feasibility study will consist of estimating:

- design and support time
- die size
- package (type and cavity)

Detailed feasibility study will consist of:

- die size choice
- package (type and cavity) choice
- pin-out description
- first layout prototyping (**)
- placement
- clock tree generation
- routing
- static timing analysis (Atmel/Customer)
- choice of final flow
- design and support time

(**) This is performed in case of high timing criticality. It consists of running a fast place and route to early evaluate the parasitic effects.

Placement, Clock Tree Generation (CTG) and routing may be performed with different tools (for example, CTG could be made using CTPKS, FE/CTS or CTGen).

During the feasibility phase, several meetings and reviews can be set up if some technical details have not yet been defined and agreed.

The results of the feasibility study are gathered in a report provided to the customer and reviewed during the Feasibility Study Review (FSR). The FSR can be either a conference call or a meeting. From the FSR onwards, a firm quotation can be issued.

DSR Meeting

As soon as the NRE order is placed, a Design Start Review (DSR) is organized.

The DSR is a kick off meeting of the ASIC development between the customer and Atmel (under the responsibility of the Marketing) and involving the Technical Center, the Product Engineering, Sales and any other necessary resources.

Phase 2:

Logic Design

This phase consists of building the project database at the logic level, using a selected set of CAD tools. It consists of creating a first net-list (interconnection of Atmel ASIC cells) describing the behaviour and the structure of the circuit.

LR Meeting

Once the logic design is completed and checked at the logic level, a formal meeting is set up involving the customer and Atmel, for the official freezing of the data and the start of the physical design.

Phase 3:

Physical Design

After the customer's design data has been transferred to the Atmel Technical Centre, the layout is performed.

Then, post layout simulations are run and back annotations given to the customer. Changes can be made on the layout until the best trade off is found between Atmel and the customer, provided it has been approved before.

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DR Meeting

Once the design layout is completed, the entire circuit database is reviewed by the customer and Atmel in order to validate the physical design.

The main criteria to be checked are:

- Simulation results with post-layout back-annotation timings.
- Layout organization with bonding diagrams and package features.
- Test program in compliance with Atmel tester rules.

The final agreement for processing the parts is mentioned in a formal document which is signed by both sides, and includes all the reference file names and technical comments, with a check list.

Phase 4: Prototypes

Once the Design Review meeting has been held, the project database is transferred to the Atmel factory in Nantes (France). This database is then followed step by step by the Product Engineering (PE) group.

The masks and test devices are created and used to process and test the samples before and after the assembly steps.

The test program generated during the development phase is applied either onto the wafer or after the dice are packaged. The Credence Octet test equipment is used for this operation. The samples are then shipped to the customer for functional acceptance.

Deliverables

Table 4. Deliverables at the end of each phase

DESIGN PHASE	DELIVERABLE	WHO
FEASIBILITY STUDY	ASIC feasibility study report (APF-tc-FSR-project code). Design start review document (APF-tc-DSR-project code).	Atmel
LOGIC DESIGN	ASIC logic review document (APF-tc-LR-project code) + Files as required in the document.	CUSTOMER
	Updated DSR document	Atmel
PHYSICAL DESIGN	ASIC design review document (APF-tc-DR-project code) + Files as required in the document.	CUSTOMER
	Updated DSR document	Atmel
PROTOTYPES MANUFACTURING & TEST	Packaged parts and associated documents	Atmel

MPW new Milestones

Though a large increase in performance is reached using 0.18µm process, many designs would not be able to benefit from the advanced technology due to the high costs involved. Therefore, Atmel proposes, in cooperation with the European Space Agency who manages the eligible designs and launch dates, a Multi Project Wafer service called SMPW (*Space Multi Project Wafer*) to its customers.

It is a way to decrease the cost of the reticules and silicon by sharing them over a number of designs.

Specific milestones have been created to coordinate, manage the activities and guarantee that there will be no interaction between any customer design and the others.

The main milestones are the *Logic Review Closing Date* (**LRCD**) and the *Design Review Closing Date* (**DRCD**).

The LR meeting must be held prior to the LRCD. The DR meeting must be held prior to the DRCD. For this reason, Pre Logic and Pre Design Reviews are strongly recommended.

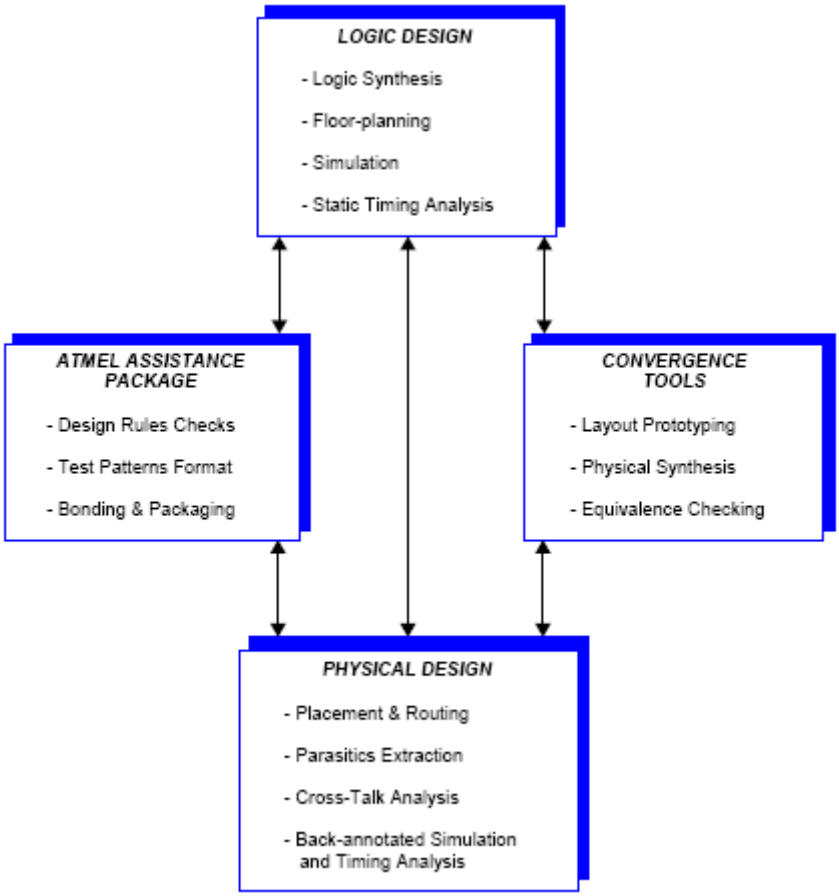
For each SMPW run, those dates are known in advance. A procedure has been defined to embark on a run. In summary, a request to embark has to be made and the reservation on a run occurs once the LRCD is passed. Any question related to the SMPW service can be addressed to the hotline, at the following email address: smpw-atc18@nto.atmel.com.

Design Flows

Introduction

This chapter summarizes the design flow with reference to different platforms used for Cell based chip design. For further details, refer to the ATC18RHA design manual.

Figure 3. Global design flow



Atmel Package Assistant is running on SUN stations under SOLARIS and on LINUX PC (RedHat distribution from version 7.0). Design Kits are compatible with both platforms depending on third party tools availability. Disk space for software and kits is checked by the installation tool. Hardware platform memory requirement is design dependant.

Design Kit

The use of both external and internal IC CAD tools requires the modelization of each library element. The set of required files for all the supported CAD tools relevant to the ATC18RHA family is called the *ATC18RHA Design Kit*. These files describe the functionality, including or not timings and other attributes, with respect to each targeted tools modelization features and methods.

The design kit contains relevant descriptions of standard cells and peripheral cells, given for different pre-defined ranges of temperature, voltage and process.

Table 5. ATC18RHA design kit supported CAD tools

Tools	Supplier	Purpose
GATEAID2	Atmel	Atmel support tools
MODELSIM (1)	MENTOR	VHDL/VITAL RTL + VERILOG RTL + gate level simulation
NCSIM (1)	CADENCE	
DESIGNCOMPILER	SYNOPSYS	HDL synthesis
BUILDGATES	CADENCE	HDL synthesis
POWERCOMPILER, PRIMEPOWER	SYNOPSYS	Synthesis power optimization & analysis
DFT SUITE	MENTOR	Scan + ATPG (FastScan), JTAG (BSD-Architect), BIST (MBIST-Architect)
FE-ULTRA, PKS	CADENCE	Floor-planning, layout prototyping, physical synthesis
PRIMETIME	SYNOPSYS	Static timing analysis
FORMALITY	SYNOPSYS	Equivalence checking, formal proof

Note: (1) Golden simulators

Design flow

The Design flow can be described in two sections.

The front-end done at the customer's premises

The following table lists the activities and tools that will be used during the front-end design.

Function	Tool	Supplier
RTL simulation	MODELSIM	MENTOR
	NC-SIM	CADENCE
Code coverage	VHDL-COVER	TRANSEDA
RTL to gate synthesis	DESIGN-COMPILER	SYNOPSYS
	BUILD-GATES	CADENCE
Power optimization	POWER-COMPILER	SYNOPSYS
Power analysis	PRIME-POWER	SYNOPSYS
Test insertion + ATPG	DFT-SUITE	MENTOR
Gate level simulation	MODELSIM	MENTOR
	NC-SIM	CADENCE
Net-list translation	NETCVT	Atmel
Design rules check	STAR	Atmel

The back-end at Atmel Technical Centers

Provided that the front-end activity has been validated and accepted by Atmel during the Logic Review (LR) meeting, the following table lists the activities and the tools that will be used during the back-end design:

Activities	Function	Tool	Supplier
Bonding diagram	Array Definition	Mgtechgen	Atmel
	Bonding diagram	Pimtool	Atmel
	Pads pre-placement	P2def	Atmel
	Periphery check	COP	Atmel
	IBIS model	Genibis	Atmel
Physical implementation	Blocks Preplacement	Silver	Atmel
	Virtual Layout Prototyping	First Encounter	CADENCE
	Physical Knowledgeable Synthesis	FE OPT.	CADENCE
	Power routing	Snow	Atmel
	Placement	FE Place	CADENCE
	Scan chains ordering	FE Place	CADENCE
	Clock tree synthesis	FE CTS	CADENCE
	Routing	Nanoroute	CADENCE
	Final violation fix	FE OPT.	CADENCE
	Eco Place and route	FE	CADENCE
	Layout edition	Silver	Atmel
	3D extraction	Star-RCXT + F & I	SYNOPSYS
Final verifications	Static timing analysis	Prime time	SYNOPSYS
	Equivalence checking	Formality	SYNOPSYS
	Back-annotated simulation	Modelsim	MENTOR
		Nc-sim	CADENCE
	Consumption analysis	Prime Power	Atmel
	Power scheme check	Voltagestorm	CADENCE
	Cross talk analysis	Celtic	CADENCE
	Cross talk errors fix	Nano Route	CADENCE
	Final analysis	Celtic-NDC	CADENCE
	Test patterns	PATFORM	Atmel
	GDSII generation	SE2GDS	Atmel

Electrical Characteristics

Absolute Maximum Ratings

Core Supply Voltage.....-0.3V to +2V Buffer Supply Voltage .....-0.3V to +4V Buffer Input Voltage..... -0.3V to +4.0V Storage Temperature..... -65°C to +150°C ESD for I/O33 .....>2000V ESD for PLL .....>1000V	*NOTICE: This absolute maximum ratings voltage is the maximum voltage that guarantees that the device will not be burned if those maximum voltages are applied during a very limited period of time. This is not a guarantee of functionality or reliability. The users must be warned that if a voltage exceeding the maximum voltage (nominal +10%) and below this absolute maximum rating voltages, is applied to their devices, the reliability of their devices will be affected.

Recommended Operating Conditions

Core Supply Voltage	1.65V to 1.95V
3.3V Buffer Supply Voltage	3.0V to 3.6V
2.5V Buffer Supply Voltage	2.25V to 2.75V
Buffer Input Voltage	0V to Vccb
Storage Temperature	-65°C to +150°C

Consumption

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Ta	Operating Temperature	-55	25	125	°C	
Vcc	Supply Voltage	1.65	1.8	1.95	V	core
ICCSBA	Leakage current per Kgate		145	5500	nA	
ICCOPA	Dynamic current per Kgate			44	nA/MHz	

IO33 DC at 3.3V Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Ta	Operating Temperature	-55	25	125	°C	
Vcc	Supply Voltage	1.65	1.8	1.95	V	core
Vccb	Buffer Supply voltage	3.0	3.3	3.6	V	IOs
IIL	Low Level Input Current	-1		1	µA	Vin=Vss
	Pull-up resistor	110	220	400	µA	
	Pull-down resistor	-5		5	µA	
IIH	High Level Input Current	-1		1	µA	Vin=Vccb
	Pull-up resistor	-5		5	µA	
	Pull-down resistor	140	320	600	µA	
IOZ	High Impedance State Output Current	-1		1	µA	Vin=Vccb or Vss no pull resistor
VIL	Low-Level Input Voltage	-0.3		0.8	V	
VIH	High- Level Input Voltage	2		Vccb+0.3	V	
Vhyst	Hysteresis		400		mV	
IICS	Cold Sparing leakage input current	-1		1	µA	Vccb=Vss=0V Vin=0 to Vccb
IOCS	Cold Sparing leakage output current	-1		1	µA	Vccb=Vss=0V Vout=0 to Vccb
VCSTH	Supply threshold of cold sparing buffers			0.5	V	IICS < 4µA
VOL	Low level output voltage			0.4	V	IOL=2,4,8,12,16mA
VOH	High level output voltage	vccb-0.4			V	IOH=2,4,8,12,16mA
IOS (1)	Output Short circuit current IOSN (nn=1) IOSP (nn=1)			23 23	mA mA	Vout=Vccb Vout=Vss

(1) Supplied as a design limit but not guaranteed or tested. No more than one output may be shorted at a time for a maximum duration of 10 seconds.

IOSmax = 23,46,92,138,184 mA for nn=1,2,4 ,6,8

IO33 DC at 2.5V Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Ta	Operating Temperature	-55	25	125	°C	
Vcc	Supply Voltage	1.65	1.8	1.95	V	core
Vccb	Buffer Supply voltage	2.25	2.5	2.75	V	IOs
IIL	Low Level Input Current	-1		1	µA	Vin=Vss
	Pull-up resistor	60	130	260	µA	
	Pull-down resistor	-5		5	µA	
IIH	High Level Input Current	-1		1	µA	Vin=Vccb
	Pull-up resistor	-5		5	µA	
	Pull-down resistor	75	180	360	µA	
IOZ	High Impedance State Output Current	-1		1	µA	Vin=Vccb or Vss no pull resistor
VIL	Low-Level Input Voltage	-0.3		0.7	V	
VIH	High- Level Input Voltage	2		Vccb+0.3	V	
Vhyst	Hysteresis		350		mV	
IICS	Cold Sparing leakage input current	-1		1	µA	Vccb=Vss=0V Vin=0 to Vccb
IOCS	Cold Sparing leakage output current	-1		1	µA	Vccb=Vss=0V Vout=0 to Vccb
VCSTH	Supply threshold of cold sparing buffers			0.5	V	IICS < 4µA
VOL	Low level output voltage			0.4	V	IOL=1.5,3,6,9,12mA
VOH	High level output voltage	vccb-0.4			V	IOH=1.5,3,6,9,12mA
IOS (1)	Output Short circuit current IOSN (nn=1) IOSP (nn=1)			14 14	mA mA	Vout=Vccb Vout=Vss

(1) Supplied as a design limit but not guaranteed or tested. No more than one output may be shorted at a time for a maximum duration of 10 seconds.

IOSmax = 14,28,56,84,112 mA for nn=1,2,4 ,6,8

PCI Characteristics

DC specifications

Symbol	Parameter	Min	Typ	Max	Unit	Tests conditions
Vccb	Buffer Supply voltage	3.0	3.3	3.6	V	
VIH	High Input Level	0.5 Vccb		Vccb + 0.3	V	
VIL	Low Input Level	-0.3		0.3 Vccb	V	
IOH	High Level Current	16	32		mA	VOH=Vccb - 0.4V
IOL	Low Level Current	16	32		mA	VOL=0.4V
IOHCC	Output Short Current		112	184	mA	VOH=0
IOLCC	Output Short Current		112	184	mA	VOL=Vccb
VCSTH	Supply threshold of cold sparing buffers			0.5	V	IICS < 4µA

LVPECL Receiver (PE33RXZ/PE25RXZ) characteristics

DC specifications

Symbol	Parameter	Min	Typ	Max	Unit	Tests conditions
Vccb	Buffer Supply voltage	3.0	3.3	3.6	V	PE33RXZ
Vccb	Buffer Supply voltage	2.25	2.5	2.75	V	PE25RXZ
VIH	High Input Level	Vccb -1165		Vccb-880	mV	
VIL	Low Input Level	Vccb-1610		Vccb-1475	mV	
IIA,IIB	Input Leakage	-10		10	µA	
ICCstat	Static Consumption(ien=0)		2.5	4	mA	PE33RXZ
ICCstdby	Static Consumption(ien=1)			10	µA	PE33RXZ
ICCstat	Static Consumption(ien=0)		1.5	2.3	mA	PE25RXZ
ICCstdby	Static Consumption(ien=1)			5.8	µA	PE25RXZ

LVDS Transmitter (PL33TXZ/PL25TXZ) characteristics

DC specifications

Symbol	Parameter	MIN	TYP	MAX	Unit	Tests conditions
Vccb	Buffer Supply voltage	3.0	3.3	3.6	V	PL33TXZ
Vccb	Buffer Supply voltage	2.25	2.5	2.75	V	PL25TXZ
|VOD|	Differential Output Voltage	247	350	454	mV	
VOH	Output Voltage Low	1088	1775	1775	mV	

VOL	Output Voltage High	828	1358	1358	mV	
VOS	Common Mode Output Voltage	1.125	1.25	1.375	V	
ISA, ISB	Output short current to GND		7	24	mA	
ISAB	short current between Output		4.5	12	mA	
ICCstat	Static Consumption (ien=”0”)		4	6	mA	PL33TXZ
ICCsdby	Static Consumption (ien=”1”)			10	µA	PL33TXZ
ICCstat	Static Consumption (ien=”0”)		2.3	3.5	mA	PL25TXZ
ICCsdby	Static Consumption (ien=”1”)			5.8	µA	PL25TXZ

LVDS Receiver (PL33RXZ/PL25RXZ) characteristics

DC specifications

Symbol	Parameter	MIN	TYP	MAX	Unit	Tests conditions
Vccb	Buffer Supply voltage	3.0	3.3	3.6	V	PL33RXZ
Vccb	Buffer Supply voltage	2.25	2.5	2.75	V	PL25RXZ
VID	Differential Input Voltage	200		600	mV	
VCM	Common Mode Input Voltage	0.05		2.35	V	
IIA,IIB	Input Leakage	-10		10	µA	
ICCstat	Static Consumption (ien=”0”)		3.5	6	mA	PL33RXZ
ICCsdby	Static Consumption (ien=”1”)			10	µA	PL33RXZ
ICCstat	Static Consumption (ien=”0”)		2	3.5	mA	PL25RXZ
ICCsdby	Static Consumption (ien=”1”)			5.8	µA	PL25RXZ

LVDS Reference (PL33REFZ/PL25REFZ) characteristics

DC specifications

Symbol	Parameter	MIN	TYP	MAX	Unit	Tests conditions
Vccb	Buffer Supply voltage	3.0	3.3	3.6	V	PL33REFZ
Vccb	Buffer Supply voltage	2.25	2.5	2.75	V	PL25REFZ
Vref	Input Voltage		1.25		V	
Rpd	Pull Down with Vin=1.25V	140	200	260	KOhm	
ICCstat	Static Consumption (ien=”0”)		260	320	µA	PL33REFZ
ICCsdby	Static Consumption (ien=”1”)			2	µA	PL33REFZ
ICCstat	Static Consumption (ien=”0”)		150	184	µA	PL25REFZ
ICCsdby	Static Consumption (ien=”1”)			1.2	µA	PL25REFZ

Testability Techniques

For complex designs, involving blocks of memory and/or cores, careful attention must be given to design-for-test techniques. The sheer size of complex designs and the number of functional vectors that would need to be created to exercise them fully, strongly suggests the use of more efficient techniques. Combinations of SCAN paths, multiplexed access to memory and/or core blocks, and built-in-self-test logic must be employed, in addition to functional test patterns, to provide both the user and Atmel the ability to test the finished product.

An example of a highly complex design could include a PLL for clock management or synthesis, a microcontroller or DSP engine or both, SRAM to support the microcontroller or DSP engine, and glue logic to support the interconnectivity of each of these blocks. The design of each of these blocks must take into consideration the fact that the manufactured device will be tested on a high performance digital tester. Combinations of parametric, functional, and structural tests, defined for digital testers, should be employed to create a suite of manufacturing tests.

The type of block dictates the type of testability technique to be employed. The PLL will, by construction, provide access to key nodes so that functional and/or parametric testing can be performed. Since a digital tester must control all the clocks during the testing of chip, provision must be made for the VCO to be bypassed. Atmel's PLLs include a multiplexing capability for just this purpose. The addition of a few pins will allow other portions of the PLL to be isolated for test, without impinging upon the normal functionality.

In a similar vein, access to microcontroller, DSP, and SRAM blocks must be provided so that controllability and observability of the inputs and outputs to the blocks are achieved with the minimum amount of preconditioning. SRAM blocks need to provide access to both address and data ports so that comprehensive memory tests can be performed. Multiplexing I/O pins provides a method for providing this accessibility.

The glue logic can be designed using full SCAN techniques to enhance its testability.

It should be noted that, in almost all of these cases, the purpose of the testability technique is to provide Atmel a means to assess the structural integrity of the chip, i.e., sort devices with manufacturing-induced defects. All of the techniques described above should be considered supplemental to a set of patterns which exercise the functionality of the design in its anticipated operating modes.

Advanced Packaging

The ATC18RHA Series are offered in ceramic packages: multi layers quad flat packs (MQFP) with up to 352 pins and a BGA based on ceramic land grid arrays, so called multi layer column grid array (MCGA) with up to 625 pins.

The following table provides the matrix / package combination in single ring configuration.

	ATC18RHA95 _216	**ATC18RHA95 _324**	**ATC18RHA95 _404**	**ATC18RHA95 _504**
MQFPT352		X	X	X
MQFPF256		X	X	X
MQFPF196	X	X		
MQFPF160	X			

	ATC18RHA95 _216	ATC18RHA95 _324	ATC18RHA95 _404	ATC18RHA95 _504
MCGA625[1]				X
MCGA472			X	X
MCGA349		X	X	X

Note: 1. Under qualification.

Document Revision History

Changes from Rev. 4261B - 06/05 to 4261C - 04/06

1. Added double pad ring configuration.
2. Clarification of paragraphs concerning, ESD and Array Organization.
3. Tools update, (moved from HyperExtract to Star-RCXT).

Changes from Rev. 4261C - 04/06 to 4261D - 07/07

1. Removed 1.8V I/O offering.

Changes from Rev. 4261D - 07/07 to 4261E - 10/07

1. Added I/O33 supplied at 2.5V offering and LVDS/LVPECL 2.5V.

Changes from Rev. 4261E - 10/07 to 4261F - 05/08

1. Added note to MCGA625 product offering.

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