Radiation Hardened 9A, Non-Inverting Power MOSFET Drivers

ISL74422ARH

The Radiation Hardened ISL74422ARH is a non-inverting, monolithic high-speed MOSFET driver designed to convert a CMOS level input signal into a high current output at voltages up to 18V. Its fast rise times and high current output allow very quick control of even the largest power MOSFETs in high frequency applications.

The input of the ISL74422ARH can be directly driven by our HS-1825ARH and IS-1845ASRH PWM devices. The 9A high current output minimizes power losses in MOSFETs by rapidly charging and discharging high gate capacitances.

Constructed with the Intersil dielectrically isolated Rad Hard Silicon Gate (RSG) BiCMOS process, these devices are immune to Single Event Latch-up and have been specifically designed to provide highly reliable performance in harsh radiation environments.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-01521. A link is provided on our website for downloading.

Features

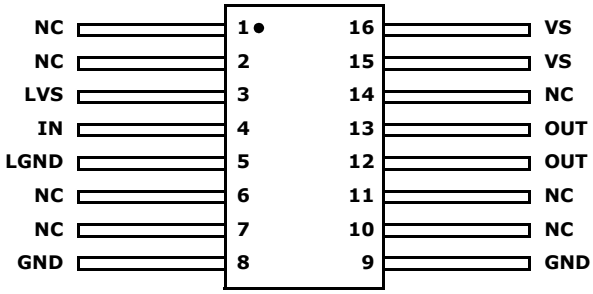
- QML Qualified per MIL-PRF-38535 Requirements
- Electrically Screened to DSCC SMD # 5962-01521
- Radiation Environment
  - Total Dose (Max) . . . . . .300krad(SI)
  - Latch-Up Immune
- I_{PEAK} . . . . . .9A(Min)
- T_F (C_L = 10,000pF) . . . . . 70ns(Typ); 90ns(Max)
- T_R (C_L = 10,000pF) . . . . .90ns(Typ); 105ns(Max)
- Prop Delay High-Low (C_L = 10,000pF) . . . . . .75ns(Max), 55ns(Typ)
- Prop Delay Low-High (C_L = 10,000pF) . . . . . .50ns(Max), 30ns(Typ)
- Consistent Delay Times with V_{CC} Changes
- Wide Supply Voltage Range . . . . . 7V to 18V
- Low Stand-by Power Consumption
  - Input Low . . . . . <2mW(Max)
  - Inputs High. . . . . <18mW(Max)
- ESD Protected . . . . . .>1750V

Applications

- Switching Power Supplies
- DC/DC Converters
- Motor Controllers

Pin Configuration

ISL74422ARH-F
(FLATPACK CDFP4-F16)
TOP VIEW



Pin Descriptions

PIN(s)	SYMBOL	DESCRIPTION
1, 2, 6, 7, 10, 11, 14	NC	NO Connect.
3	LVS	Provides the supply voltage for the control logic. It is not internally connected to Pins 15 and 16 for noise immunity purposes, but may be connected externally.
4	IN	Input voltage to the driver.
5	LGND	Control logic return. It is not internally connected to Pins 8 and 9 for noise immunity purposes, but may be connected externally.
8, 9	GND	Pins must be connected to GND.
12, 13	OUT	Pins must be connected to output.
15, 16	VS	Pins must be connected to VS.

Ordering Information

ORDERING NUMBER	PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS COMPLIANT)
5962F0152101VXC	ISL74422ARHVF	Q5962F01 52101VXC	-55 to +125	16 LD Flatpack
5962F0152101QXC	ISL74422ARHQF	Q5962F01 52101QXC	-55 to +125	16 LD Flatpack
5962F0152101V9A	ISL74422ARHVX		-55 to +125	DIE
ISL74422ARHF/PROTO	ISL74422ARHF/PROTO	ISL7 4422ARHF /PROTO	-55 to +125	16 LD Flatpack
ISL74422ARHY/SAMPLE	ISL74422ARHY/SAMPLE		-55 to +125	DIE SAMPLE

NOTE: These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Die Characteristics

DIE DIMENSIONS:

3838µm x 4829µm (151.1 mils x 190.1mils)
Thickness: 483µm ± 25.4µm (19 mils ± 1 mil)

INTERFACE MATERIALS:

Glassivation:

Type: PSG (Phosphorous Silicon Glass)
Thickness: 8.0kÅ ± 1.0kÅ

Top Metallization:

Type: AlSiCu
Thickness: 16.0kÅ ± 2kÅ

Substrate:

Radiation Hardened Silicon Gate,
Dielectric Isolation

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Unbiased (DI)

ADDITIONAL INFORMATION:

Worst Case Current Density:

$<2.0 \times 10^5$ A/cm^2

Transistor Count:

30

Metallization Mask Layout

ISL74422ARH