

BLF4G10LS-160

UHF power LDMOS transistor

Rev. 01 — 19 June 2007

Product data sheet

1. Product profile

1.1 General description

160 W LDMOS power transistor for base station applications at frequencies from 800 MHz to 1000 MHz.

Table 1. Typical performance

RF performance at $T_{case} = 25\text{ °C}$ in a common source class-AB test circuit.

Mode of operation	f (MHz)	V _{DS} (V)	P _L (W)	P _{L(AV)} (W)	G _p (dB)	η _D (%)	ACPR ₄₀₀ (dBc)	ACPR ₆₀₀ (dBc)	EVM _{rms} (%)	IMD3 (dBc)
CW	894	28	200	-	19.0	59	-	-	-	-
2-tone	894	28	-	80	19.7	42.5	-	-	-	-30
GSM EDGE	894	28	-	80	19.7	41.5	-61 ^[1]	-72 ^[1]	2.6	-

[1] ACPR₄₀₀ and ACPR₆₀₀ at 30 kHz resolution bandwidth.

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

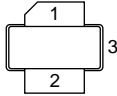
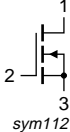
- Typical GSM EDGE performance at $f = 894\text{ MHz}$, $V_{DS} = 28\text{ V}$ and $I_{Dq} = 900\text{ mA}$:
 - ◆ Average output power = 80 W
 - ◆ Gain = 19.7 dB
 - ◆ Efficiency = 41.5 %
 - ◆ ACPR₄₀₀ = -61 dBc
 - ◆ ACPR₆₀₀ = -72 dBc
 - ◆ EVM_{rms} = 2.6 %
- Easy power control
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (800 MHz to 1000 MHz)
- Internally matched for ease of use

1.3 Applications

- RF power amplifiers for GSM, GSM EDGE and CDMA base stations and multi carrier applications in the 800 MHz to 1000 MHz frequency range.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Symbol
1	drain		 sym112
2	gate		
3	source		

[1] Connected to flange

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF4G10LS-160	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+15	V
I_D	drain current		-	15	A
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$			
		$P_L = 50\text{ W}$	0.49	0.58	K/W
		$P_L = 130\text{ W}$	0.38	0.47	K/W

6. Characteristics

Table 6. Characteristics

$T_j = 25\text{ }^\circ\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 2.1\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 230\text{ mA}$	2.5	2.9	3.5	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}$; $I_D = 900\text{ mA}$	2.65	3.15	3.65	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$	-	-	5	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 6\text{ V}$; $V_{DS} = 10\text{ V}$	35	42	-	A
I_{GSS}	gate leakage current	$V_{GS} = 15\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	420	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 7.5\text{ A}$	-	11	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 6\text{ V}$; $I_D = 7.5\text{ A}$	-	0.065	-	Ω
C_{rs}	feedback capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$; $f = 1\text{ MHz}$	-	3.0	-	pF

7. Application information

Table 7. Application information

Mode of operation: 2-tone; $f_1 = 894\text{ MHz}$; $f_2 = 894.2\text{ MHz}$; RF performance at $V_{DS} = 28\text{ V}$;
 $I_{Dq} = 900\text{ mA}$; $T_{case} = 25\text{ }^\circ\text{C}$; unless otherwise specified; in a class-AB test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(PEP)} = 160\text{ W}$	18.5	19.7	21	dB
RL_{in}	input return loss	$P_{L(PEP)} = 160\text{ W}$	-	-10	-6	dB
η_D	drain efficiency	$P_{L(PEP)} = 160\text{ W}$	40	42.5	-	%
IMD3	third order intermodulation distortion	$P_{L(PEP)} = 160\text{ W}$	-	-30	-27	dBc
IMD5	fifth order intermodulation distortion	$P_{L(PEP)} = 160\text{ W}$	-	-39	-36	dBc
IMD7	seventh order intermodulation distortion	$P_{L(PEP)} = 160\text{ W}$	-	-59	-55	dBc

7.1 Ruggedness in class-AB operation

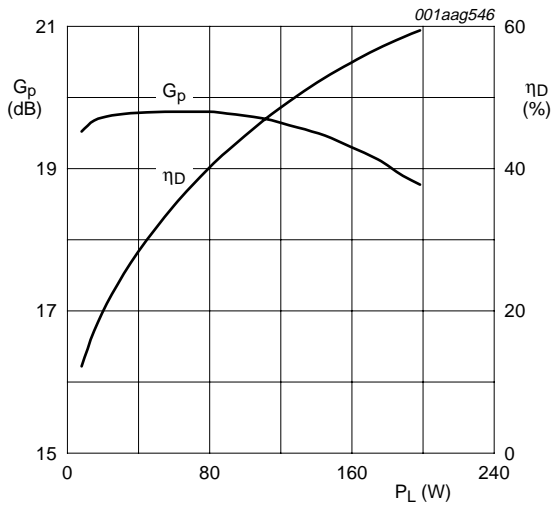
The BLF4G10LS-160 is capable of withstanding a load mismatch corresponding to $VSWR = 10 : 1$ through all phases under the following conditions: $V_{DS} = 28\text{ V}$;
 $I_{Dq} = 900\text{ mA}$; $P_L = 160\text{ W (CW)}$; $f = 894\text{ MHz}$.

Table 8. RF gain grouping

$f_1 = 894 \text{ MHz}$; $f_2 = 894.2 \text{ MHz}$

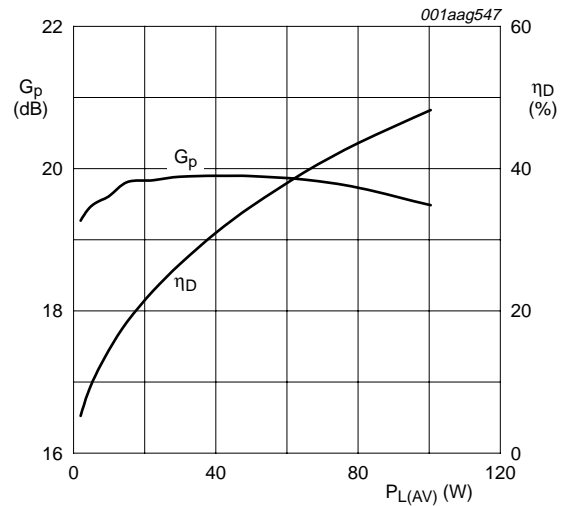
Code ^[1]	Gain (dB) for two-tone	
	Min	Max
C	18.5	19
D	19	19.5
E	19.5	20
F	20	20.5
G	20.5	21

[1] 0.2 overlap is allowed for measurement reproducibility.



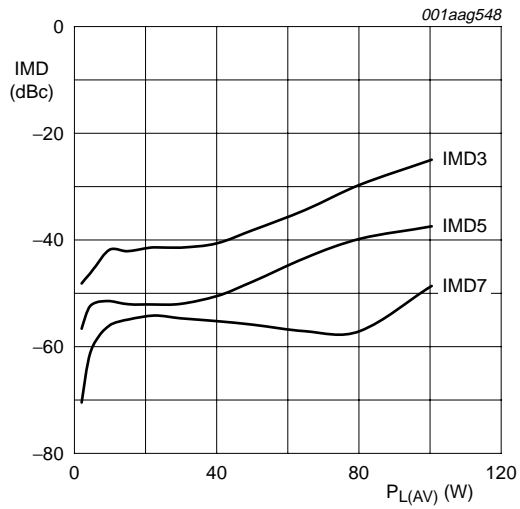
$V_{DS} = 28 \text{ V}$; $I_{Dq} = 900 \text{ mA}$; $T_{case} = 25 \text{ }^\circ\text{C}$;
 $f = 894 \text{ MHz}$.

Fig 1. One-tone CW power gain and drain efficiency as functions of load power; typical values



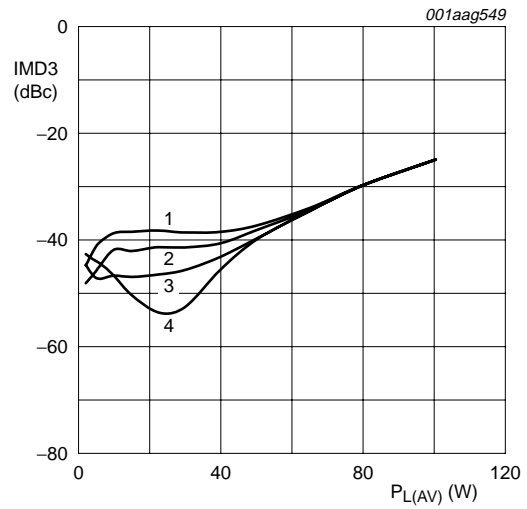
$V_{DS} = 28 \text{ V}$; $I_{Dq} = 900 \text{ mA}$; $T_{case} = 25 \text{ }^\circ\text{C}$;
 $f = 894 \text{ MHz}$.

Fig 2. Two-tone power gain and drain efficiency as functions of average load power; typical values



$V_{DS} = 28\text{ V}$; $I_{Dq} = 900\text{ mA}$; $T_{case} = 25\text{ }^{\circ}\text{C}$;
 $f = 894\text{ MHz}$.

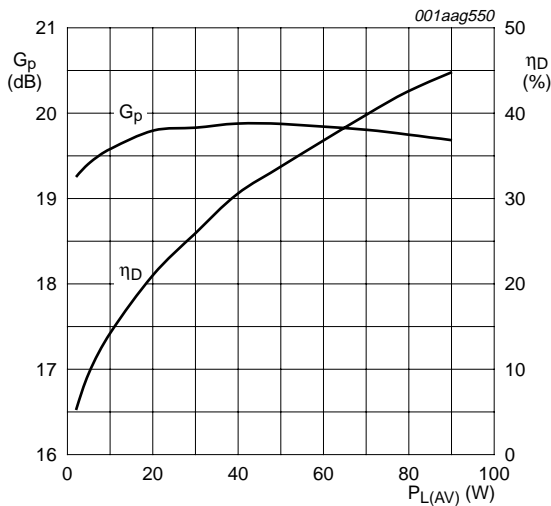
Fig 3. Intermodulation distortion a function of average load power; typical values



$V_{DS} = 28\text{ V}$; $T_{case} = 25\text{ }^{\circ}\text{C}$; $f = 894\text{ MHz}$.

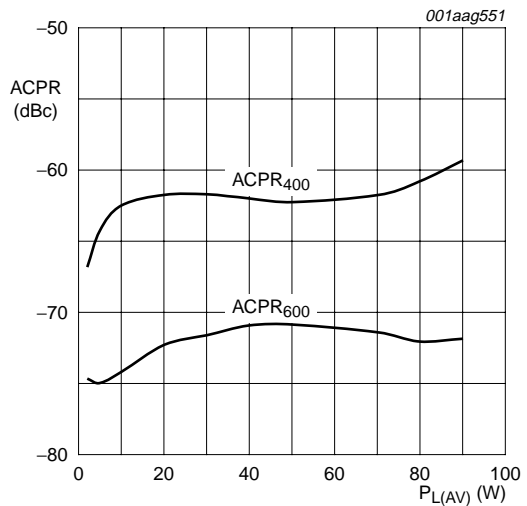
- (1) $I_{Dq} = 800\text{ mA}$.
- (2) $I_{Dq} = 900\text{ mA}$.
- (3) $I_{Dq} = 1000\text{ mA}$.
- (4) $I_{Dq} = 1100\text{ mA}$.

Fig 4. IMD3 as a function of average load power; typical values



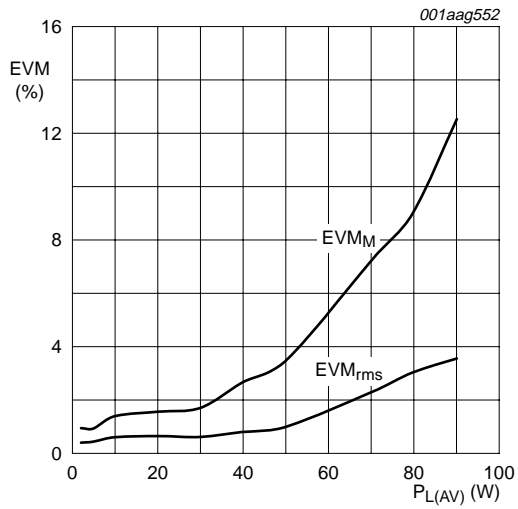
$V_{DS} = 28\text{ V}$; $I_{Dq} = 900\text{ mA}$; $T_{case} = 25\text{ }^{\circ}\text{C}$;
 $f = 894\text{ MHz}$.

Fig 5. GSM EDGE power gain and drain efficiency as functions of average load power; typical values



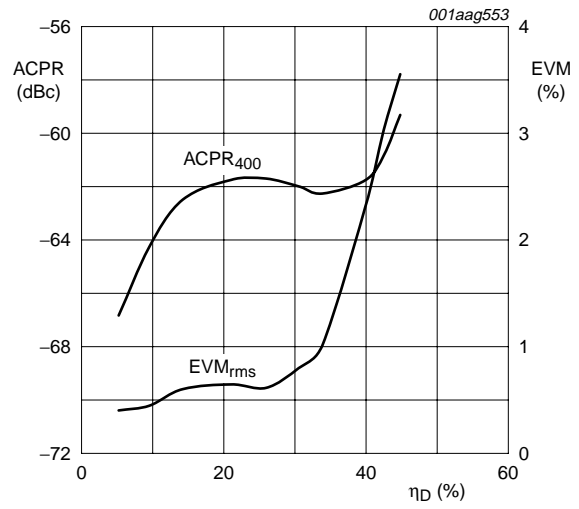
$V_{DS} = 28\text{ V}$; $I_{Dq} = 900\text{ mA}$; $T_{case} = 25\text{ }^{\circ}\text{C}$;
 $f = 894\text{ MHz}$.

Fig 6. GSM EDGE ACPR at 400 kHz and at 600 kHz as a function of average load power; typical values



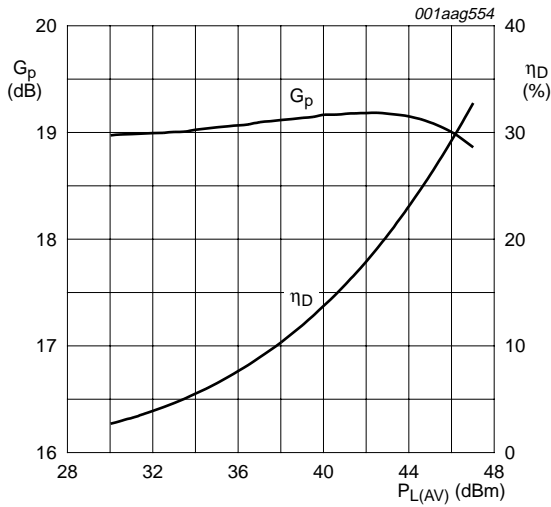
$V_{DS} = 28\text{ V}$; $I_{Dq} = 900\text{ mA}$; $T_{case} = 25\text{ }^\circ\text{C}$;
 $f = 894\text{ MHz}$.

Fig 7. GSM EDGE rms EVM and peak EVM as functions of average load power; typical values



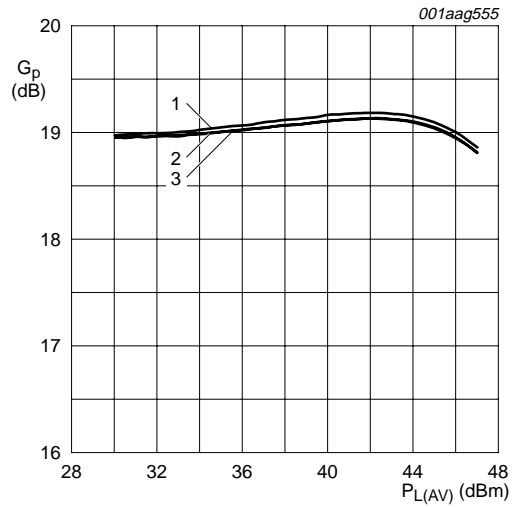
$V_{DS} = 28\text{ V}$; $I_{Dq} = 900\text{ mA}$; $T_{case} = 25\text{ }^\circ\text{C}$;
 $f = 894\text{ MHz}$.

Fig 8. GSM EDGE ACPR and rms EVM as functions of drain efficiency; typical values



$V_{DS} = 28\text{ V}$; $I_{Dq} = 1100\text{ mA}$; $f = 881.5\text{ MHz}$.
 Test signal: IS-95 with PAR = 9.9 dB at 0.01 % probability.

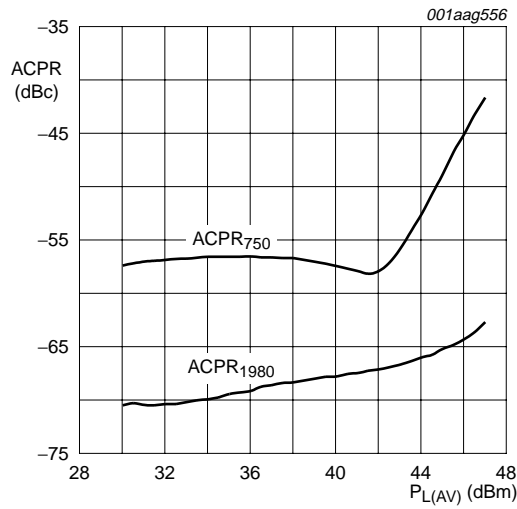
Fig 9. CDMA power gain and drain efficiency as functions of average load power; typical values, measured in a CDMA demo test circuit



$V_{DS} = 28\text{ V}$; $I_{Dq} = 1100\text{ mA}$.

- (1) $f = 869\text{ MHz}$.
- (2) $f = 881.5\text{ MHz}$.
- (3) $f = 894\text{ MHz}$.

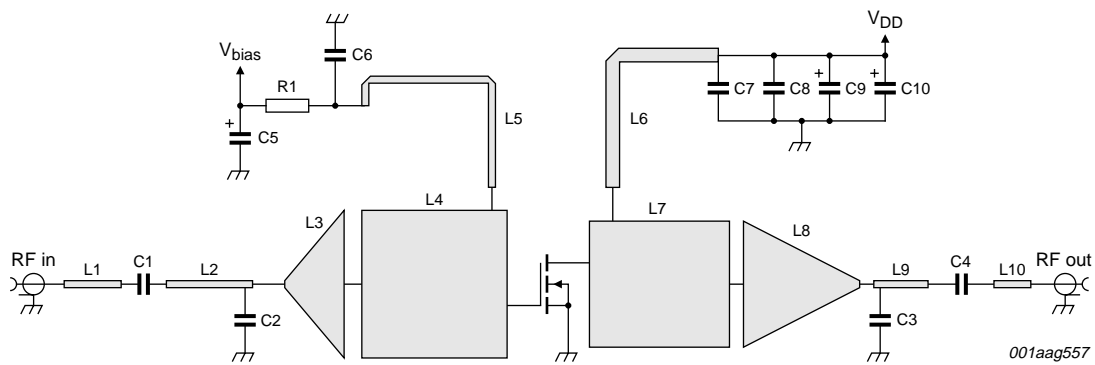
Fig 10. CDMA power gain as a function of average load power at various frequencies; typical values, measured in a CDMA demo test circuit



$V_{DS} = 28\text{ V}$; $I_{DQ} = 1100\text{ mA}$; $T_{case} = 25\text{ }^{\circ}\text{C}$; $f = 881.5\text{ MHz}$.

Fig 11. CDMA ACPR at 750 kHz and at 1980 kHz as functions of average load power; typical values, measured in a CDMA demo test circuit

8. Test information



See [Table 9](#) for a list of components

Fig 12. Circuit schematic for 894 MHz production test circuit

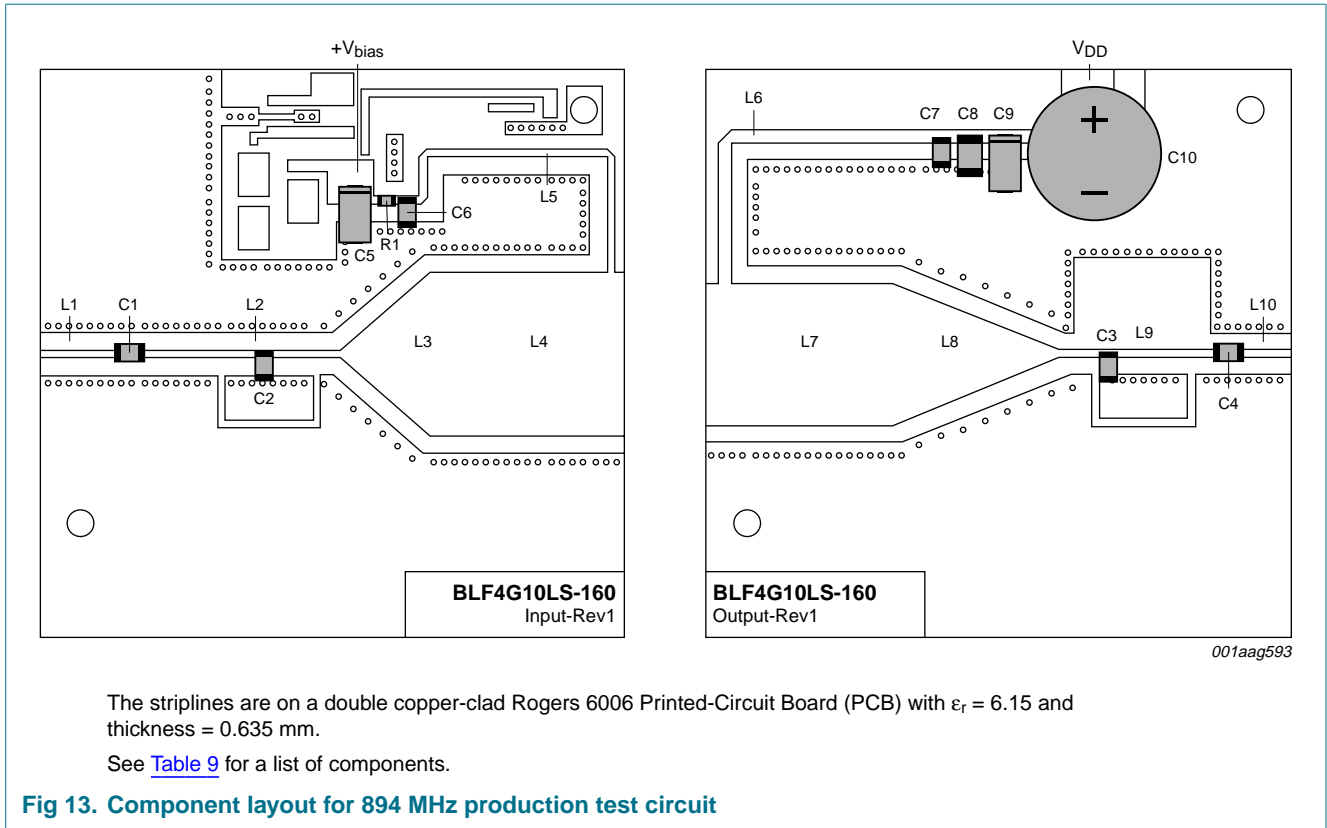


Fig 13. Component layout for 894 MHz production test circuit

Table 9. List of components (see Figure 12 and Figure 13).

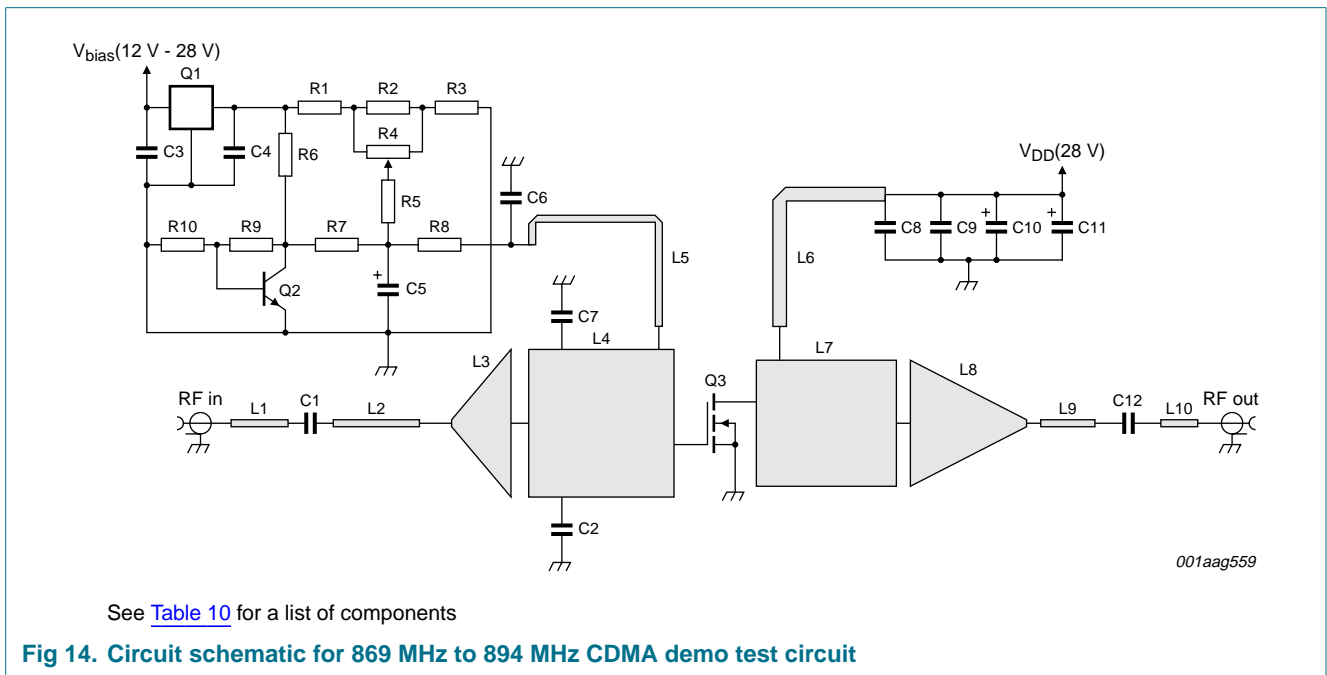
Component	Description	Value	Remarks
C1, C4, C6, C7	multilayer ceramic chip capacitor	68 pF	[1]
C2	multilayer ceramic chip capacitor	1.5 pF	[1]
C3	multilayer ceramic chip capacitor	1.4 pF	[1]
C5, C9	tantalum capacitor	10 μF	
C8	ceramic capacitor	1 μF	1812X7R105KL2AB
C10	electrolytic capacitor	220 μF	
L1	stripline		[2] (W × L) 0.914 mm × 10.160 mm
L2	stripline		[2] (W × L) 0.914 mm × 24.384 mm
L3	tapered stripline		[2] (W1 × W2 × L) 0.914 mm × 19.812 mm × 11.024 mm
L4	stripline		[2] (W × L) 19.812 mm × 21.438 mm
L5	stripline		[2] (W × L) 0.914 mm × 42.342 mm
L6	stripline		[2] (W × L) 1.524 mm × 42.418 mm
L7	stripline		[2] (W × L) 17.221 mm × 22.479 mm
L8	tapered stripline		[2] (W1 × W2 × L) 17.221 mm × 0.914 mm × 20.625 mm

Table 9. List of components (see [Figure 12](#) and [Figure 13](#)). ...continued

Component	Description	Value	Remarks
L9	stripline		[2] (W × L) 0.914 mm × 19.126 mm
L10	stripline		[2] (W × L) 0.914 mm × 6.858 mm
R1	SMD resistor	5.1 Ω	

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] The striplines are on a double copper-clad Rogers 6006 Printed-Circuit Board (PCB) with $\epsilon_r = 6.15$ and thickness = 0.635 mm.



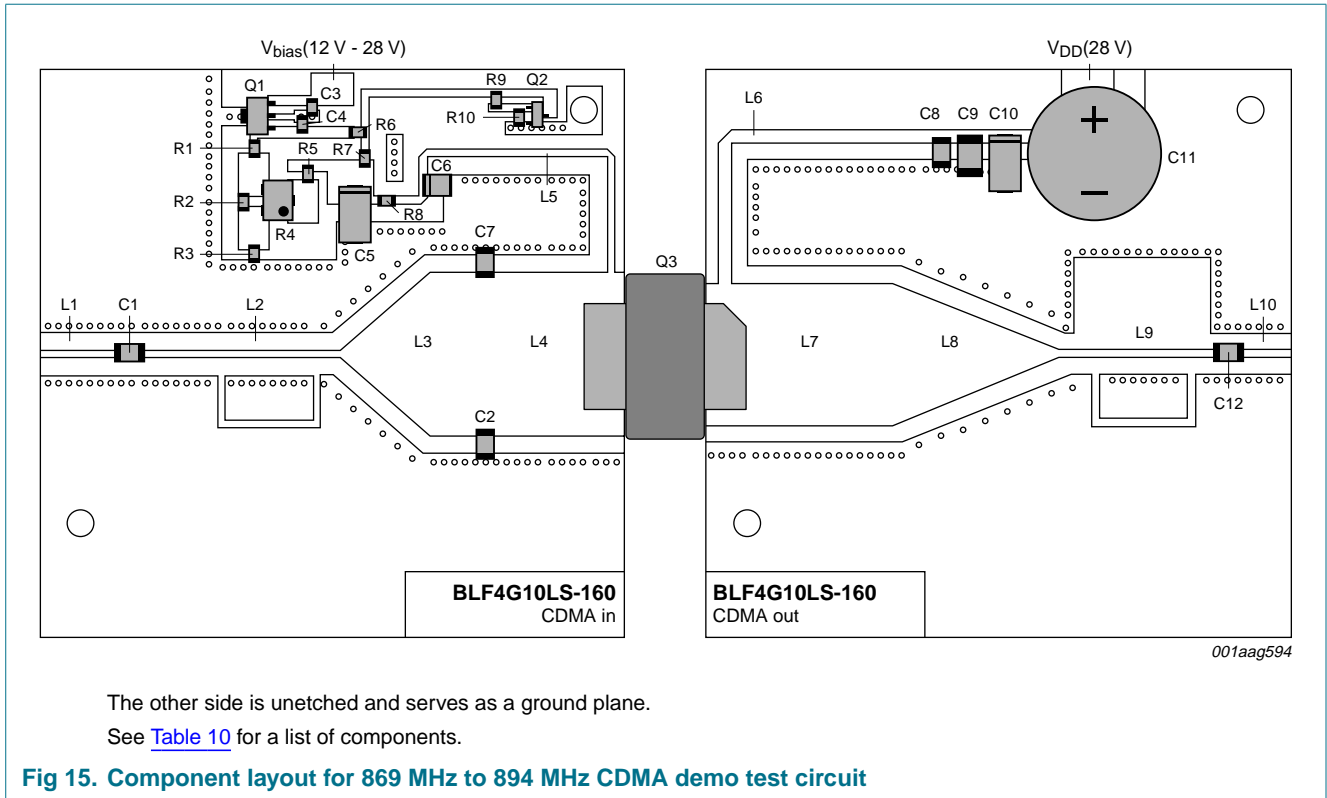


Fig 15. Component layout for 869 MHz to 894 MHz CDMA demo test circuit

Table 10. List of components (see Figure 14 and Figure 15).

Component	Description	Value	Remarks
C1, C6, C8	multilayer ceramic chip capacitor	68 pF	[1]
C2, C7	multilayer ceramic chip capacitor	1.3 pF	[1]
C3, C4	ceramic capacitor	100 nF	
C5, C10	tantalum capacitor	10 µF	
C9	ceramic capacitor	1 µF	
C11	electrolytic capacitor	2200 µF	
C12	multilayer ceramic chip capacitor	18 pF	[1]
L1	stripline		[2] (W × L) 0.914 mm × 10.160 mm
L2	stripline		[2] (W × L) 0.914 mm × 24.384 mm
L3	tapered stripline		[2] (W1 × W2 × L) 0.914 mm × 19.812 mm × 11.024 mm
L4	stripline		[2] (W × L) 19.812 mm × 21.438 mm
L5	stripline		[2] (W × L) 0.914 mm × 42.342 mm
L6	stripline		[2] (W × L) 1.524 mm × 42.418 mm
L7	stripline		[2] (W × L) 17.221 mm × 22.479 mm
L8	tapered stripline		[2] (W1 × W2 × L) 17.221 mm × 0.914 mm × 20.625 mm
L9	stripline		[2] (W × L) 0.914 mm × 19.126 mm

Table 10. List of components (see [Figure 14](#) and [Figure 15](#)). ...continued

Component	Description	Value	Remarks
L10	stripline		[2] (W × L) 0.914 mm × 6.858 mm
R1, R2	SMD resistor	430 Ω	
R3	SMD resistor	300 Ω	
R4	potentiometer	200 Ω	
R5	SMD resistor	2 kΩ	
R6	SMD resistor	1.1 kΩ	
R7	SMD resistor	11 kΩ	
R8	SMD resistor	5.1 Ω	
R9	SMD resistor	5.1 kΩ	
R10	SMD resistor	910 Ω	
Q1	voltage regulator		78L08
Q2	transistor		2N2222
Q3	BLF4G10-160		

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] The striplines are on a double copper-clad Rogers 6006 Printed-Circuit Board (PCB) with $\epsilon_r = 6.15$ and thickness = 0.635 mm.

9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A

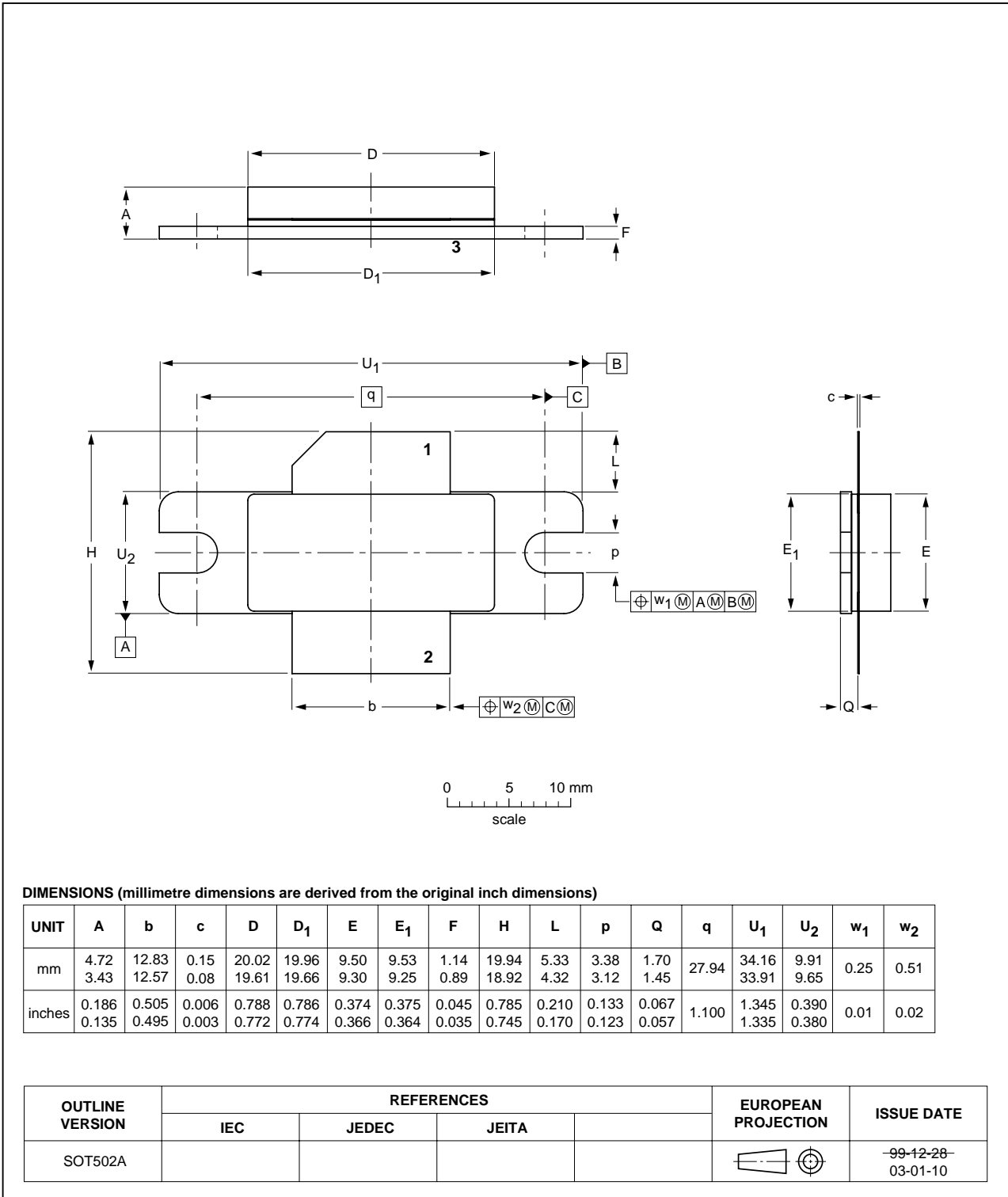


Fig 16. Package outline SOT502A

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
ACPR	Adjacent Channel Power Ratio
CDMA	Code Division Multiple Access
CW	Continuous Waveform
EDGE	Enhanced Data GSM Environment
EVM	Error Vector Magnitude
GSM	Global System for Mobile communications
IS-95	CDMA Interim Standard 95
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
RMS	Root Mean Square
SMD	Surface-Mount Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF4G10LS-160_1	20070619	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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