BLS6G3135-20; BLS6G3135S-20

LDMOS S-Band radar power transistor

Rev. 03 — 3 March 2009 Product data sheet

1. Product profile

1.1 General description

20 W LDMOS power transistor intended for radar applications in the 3.1 GHz to 3.5 GHz range.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C; t_p = 300 μs; δ = 10 %; I_{Dq} = 50 mA; in a class-AB production test circuit.

Mode of operation	f (GHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	t_r (ns)	t_f (ns)
Pulsed RF	3.1 to 3.5	32	20	15.5	45	20	10

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

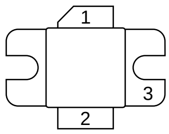
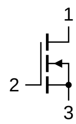
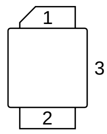
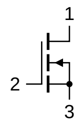
- Typical pulsed RF performance at a frequency of 3.1 GHz to 3.5 GHz, a supply voltage of 32 V, an I_{Dq} of 50 mA, a t_p of 300 μs and a δ of 10 %:
  - Output power = 20 W
  - Power gain = 15.5 dB
  - Efficiency = 45 %
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (3.1 GHz to 3.5 GHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- S-Band power amplifiers for radar applications in the 3.1 GHz to 3.5 GHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLS6G3135-20 (SOT608A)				
1	drain			
2	gate			 sym112
3	source	[1]		
BLS6G3135S-20 (SOT608B)				
1	drain			
2	gate			 sym112
3	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLS6G3135-20	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT608A
BLS6G3135S-20	-	ceramic earless flanged package; 2 leads	SOT608B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	60	V
V_{GS}	gate-source voltage		–0.5	+13	V
I_D	drain current		-	2.1	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 20 W			
		t_p = 100 μs; δ = 20 %	0.76	0.92	K/W
		t_p = 300 μs; δ = 10 %	0.79	0.95	K/W

6. Characteristics

Table 6. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.5 mA	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 40 mA	1.4	2	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.5	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	6	8.2	-	A
I_{GSS}	gate leakage current	V_{GS} = 8.3 V; V_{DS} = 0 V	-	-	150	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 1.4 A	-	2.8	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)}$ + 3.75 V; I_D = 1.4 A	-	0.37	0.58	Ω

7. Application information

Table 7. Application information

Mode of operation: pulsed RF; t_p = 300 μs; δ = 10 %; RF performance at V_{DS} = 32 V; I_{Dq} = 50 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_L	output power		-	20	-	W
V_{CC}	supply voltage	P_L = 20 W	-	-	32	V
G_p	power gain	P_L = 20 W	12	15.5	-	dB
η_D	drain efficiency	P_L = 20 W	40	45	-	%
t_r	rise time	P_L = 20 W	-	20	50	ns
t_f	fall time	P_L = 20 W	-	10	50	ns

7.1 Impedance information

Table 8. Typical impedance

f	Z_S	Z_L (optimized for η_D)	Z_L (optimized for G_p)	$G_{p(opt)}$	η_D [1]
GHz	Ω	Ω	Ω	dB	%
3.1	31.24 – j31.07	6.99 + j12.9	13.01 + j14.75	18.08	48.34
3.2	50.56 – j12.48	5.82 + j8.77	11.47 + j11.17	17.97	45.60
3.3	43.66 + j17.27	2.32 + j6.17	10.05 + j10.55	17.75	47.01
3.4	24.13 + j28.47	5.52 + j6.10	9.93 + j8.48	17.91	47.03
3.5	10.56 + j22.21	5.79 + j3.19	9.37 + j5.73	17.68	46.54

[1] Measured with Z_L optimized for G_p.

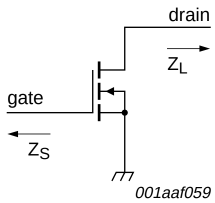
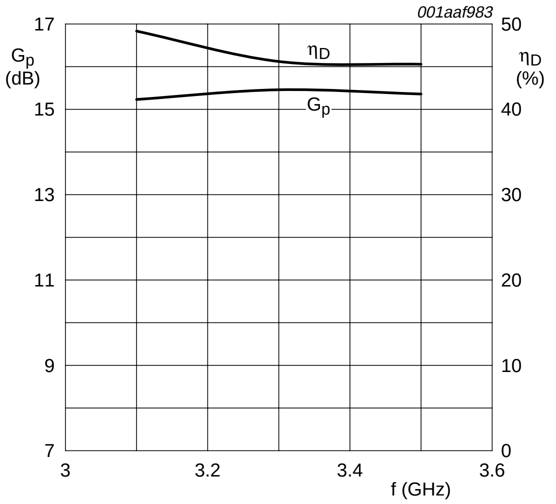


Fig 1. Definition of transistor impedance

7.2 Ruggedness in class-AB operation

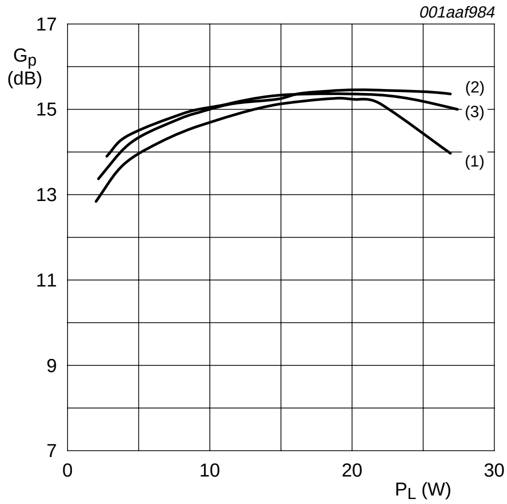
The BLS6G3135-20 and BLS6G3135S-20 are capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 50 mA; P_L = 20 W; t_p = 300 μs; δ = 10 %.

7.3 Graphs



V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %;
P_L = 20 W.

Fig 2. Power gain and drain efficiency as functions of frequency; typical values



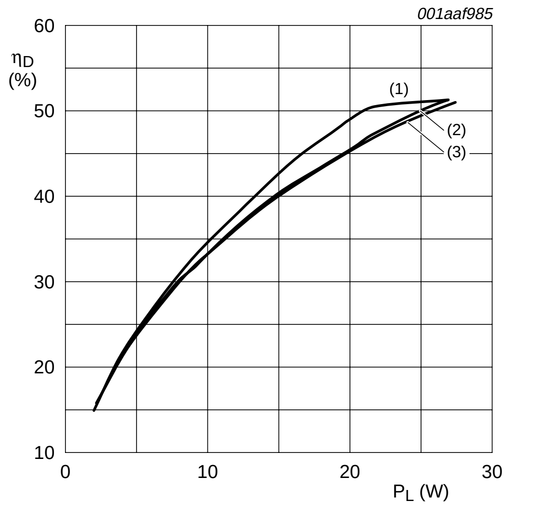
V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %.

(1) f = 3.1 GHz

(2) f = 3.3 GHz

(3) f = 3.5 GHz

Fig 3. Power gain as a function of load power; typical values



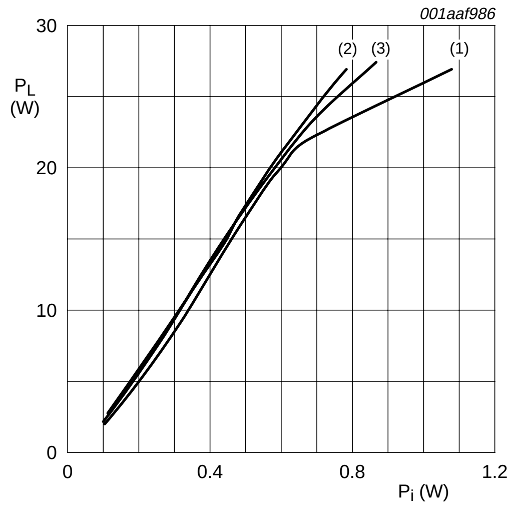
V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %.

(1) f = 3.1 GHz

(2) f = 3.3 GHz

(3) f = 3.5 GHz

Fig 4. Efficiency as a function of load power; typical values



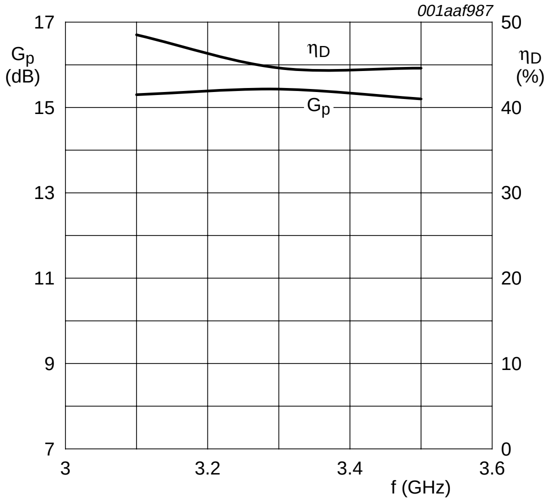
V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %.

(1) f = 3.1 GHz

(2) f = 3.3 GHz

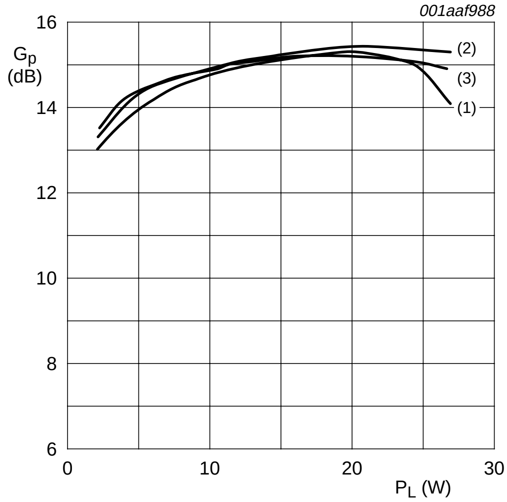
(3) f = 3.5 GHz

Fig 5. Load power as a function of input power; typical values



V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 50 μs; δ = 20 %; P_L = 20 W.

Fig 6. Power gain and drain efficiency as functions of frequency; typical values



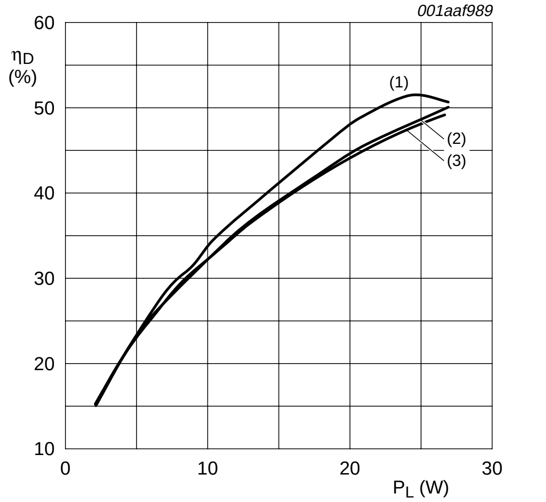
V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 100 μs; δ = 20 %.

(1) f = 3.1 GHz

(2) f = 3.3 GHz

(3) f = 3.5 GHz

Fig 7. Power gain as a function of load power; typical values



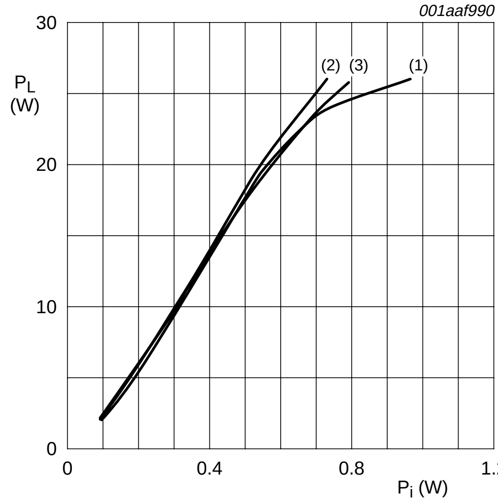
V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 100 μs; δ = 20 %.

(1) f = 3.1 GHz

(2) f = 3.3 GHz

(3) f = 3.5 GHz

Fig 8. Efficiency as a function of load power; typical values



V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 100 μs; δ = 20 %.

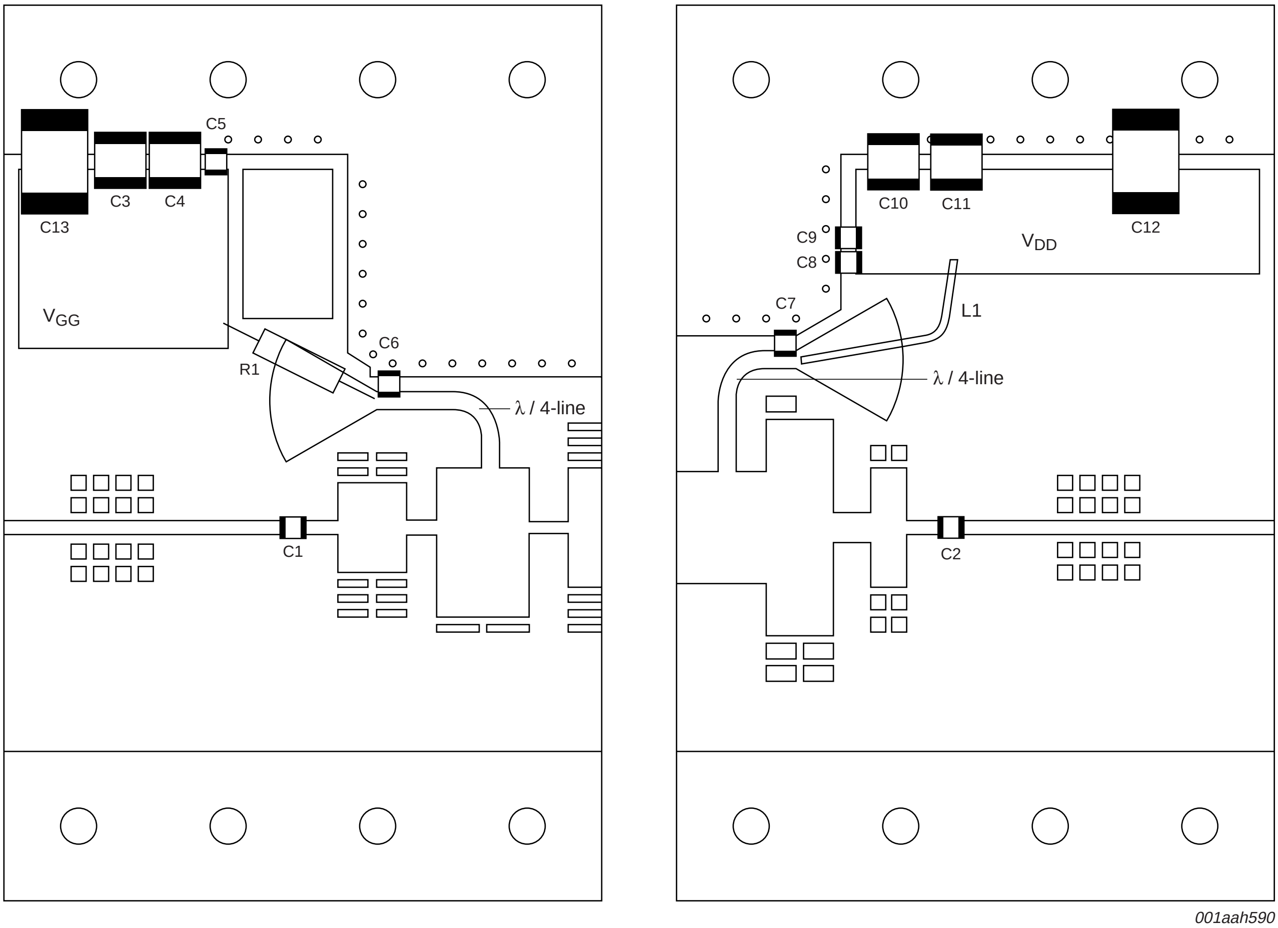
(1) f = 3.1 GHz

(2) f = 3.3 GHz

(3) f = 3.5 GHz

Fig 9. Load power as a function of input power; typical values

8. Test information



Striplines are on a double copper-clad Rogers Duroid 6006 Printed-Circuit Board (PCB) with ε_r = 6.2 and thickness = 0.64 mm.

See Table 9 for list of components.

Fig 10. Component layout for 3.1 GHz to 3.5 GHz test circuit

Table 9. List of components

See Figure 10.

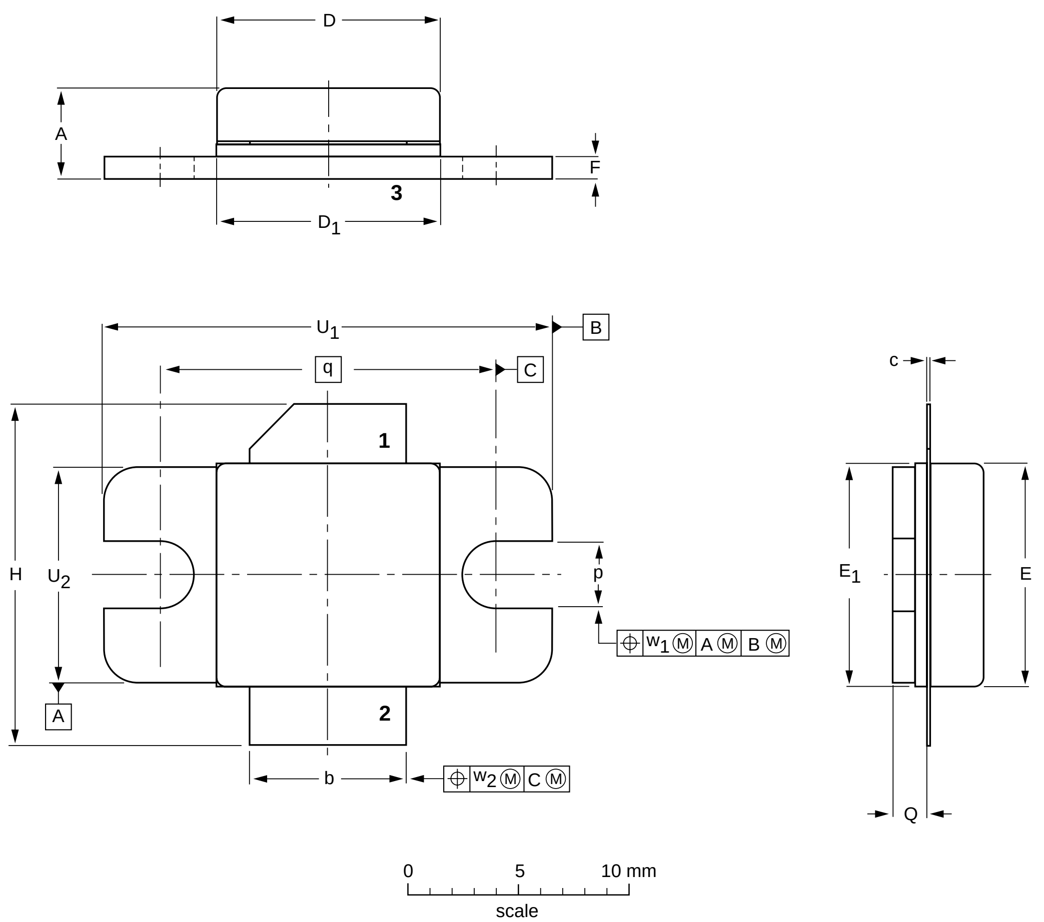
Component	Description	Value	Remarks
C1, C2, C5, C6, C7, C8, C9	multilayer ceramic chip capacitor	33 pF	[1]
C3, C4, C10, C11	multilayer ceramic chip capacitor	470 pF	[2]
C12	electrolytic capacitor	47 µF; 63 V	
C13	electrolytic capacitor	10 µF; 35 V	
L1	copper wire	-	
R1	resistor	49.9 Ω	

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

9. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT608A**



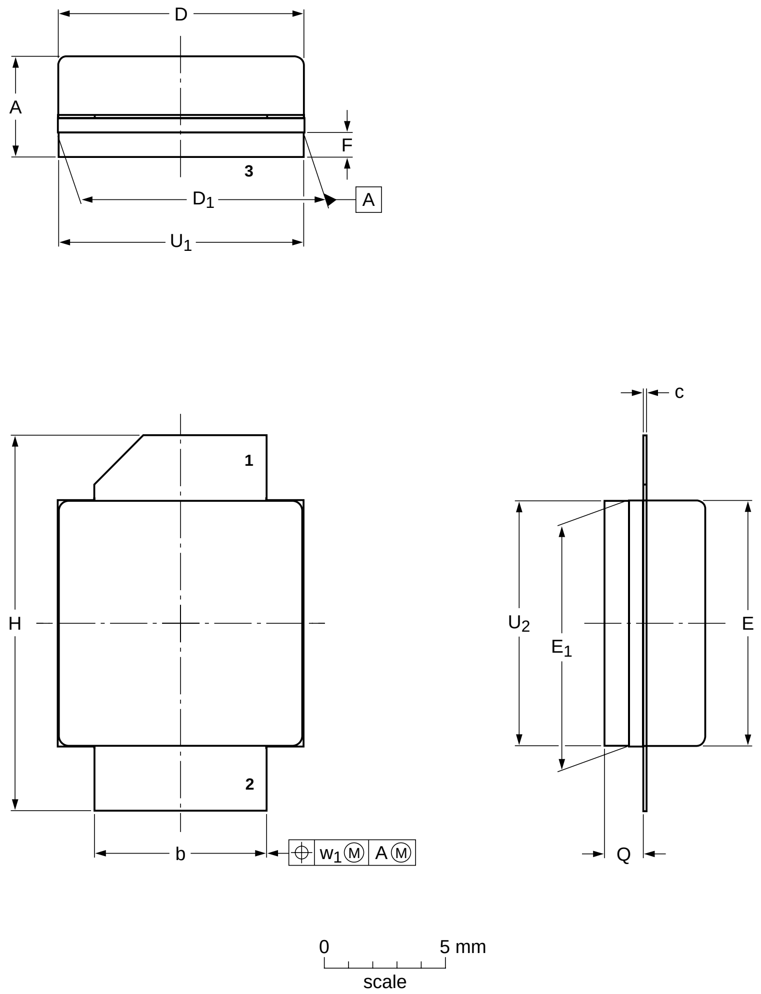
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.62 3.76	7.24 6.99	0.15 0.10	10.21 10.01	10.29 10.03	10.21 10.01	10.29 10.03	1.14 0.89	15.75 14.73	3.30 2.92	1.70 1.35	15.24	20.45 20.19	9.91 9.65	0.25	0.51
inches	0.182 0.148	0.285 0.275	0.006 0.004	0.402 0.394	0.405 0.395	0.402 0.394	0.405 0.395	0.045 0.035	0.620 0.580	0.130 0.115	0.067 0.053	0.600	0.805 0.795	0.390 0.380	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT608A						~~01-02-22~~ 02-02-11

Fig 11. Package outline SOT608A

Ceramic earless flanged package; 2 leads **SOT608B**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	Q	U_1	U_2	w_1
mm	4.62 3.76	7.24 6.99	0.15 0.10	10.21 10.01	10.29 10.03	10.21 10.01	10.29 10.03	1.14 0.89	15.75 14.73	1.70 1.35	10.24 9.98	10.24 9.98	0.51
inch	0.182 0.148	0.285 0.275	0.006 0.004	0.402 0.394	0.405 0.395	0.402 0.394	0.405 0.395	0.045 0.035	0.620 0.580	0.067 0.053	0.403 0.393	0.403 0.393	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT608B						~~06-11-27~~ 06-12-06

Fig 12. Package outline SOT608B

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
LDMOS	Laterally Diffused Metal Oxide Semiconductor
RF	Radio Frequency
S-Band	Short wave Band
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLS6G3135-20_6G3135S-20_3	20090303	Product data sheet	-	BLS6G3135-20_6G3135S-20_2
Modifications:	• Section 7.1 on page 4: Impedance information added			
BLS6G3135-20_6G3135S-20_2	20081217	Product data sheet	-	BLS6G3135-20_6G3135S-20_1
BLS6G3135-20_6G3135S-20_1	20070307	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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