DESCRIPTION

PT2462 is remote control transmitter utilizing CMOS Technology specially designed for infrared applications. It is compatible with LC7462M and is capable of controlling 32 function keys and 3 double keys. PT2462 is available in 20 pins, SOP or DIP Package and provides 8 bits of Custom Code.

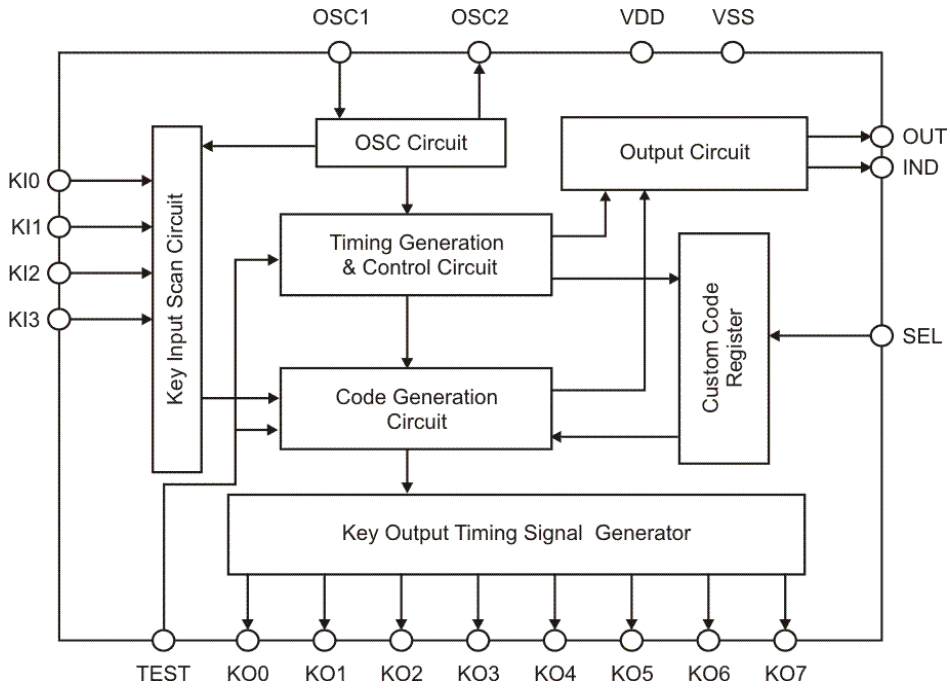
FEATURES

- CMOS technology
- Low power consumption
- Least external components
- 32 ⊕ 3 function keys
- Wide range of operating voltage: VDD=1.8 ~ 5.5V
- Double key operation (No order of priority given)
- On-chip oscillator can be constructed using an externally connected ceramic resonator
- Using SEL pin, PT2462 provides 2 custom code options.

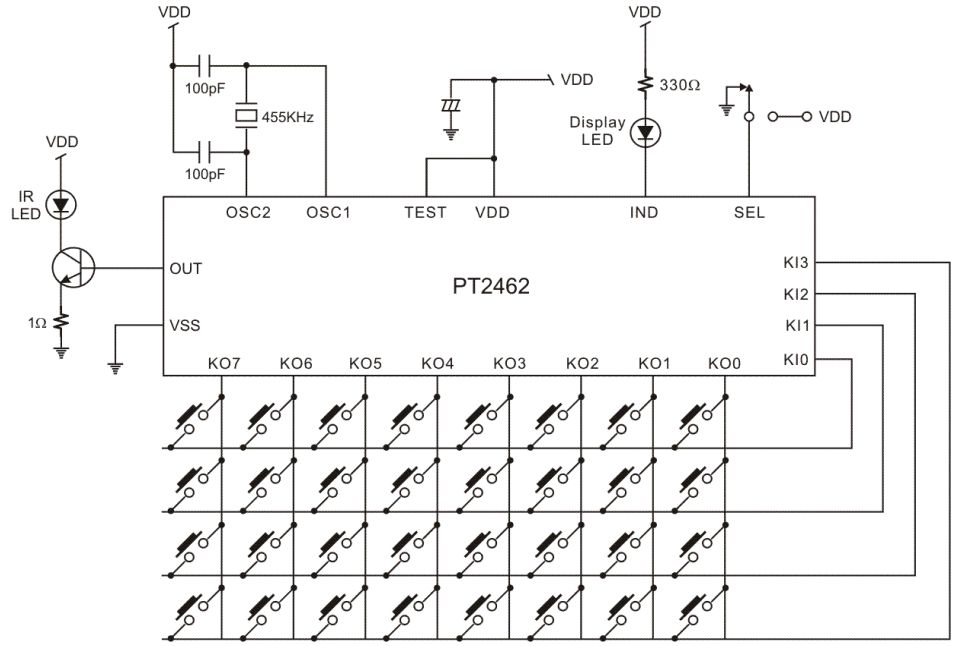
APPLICATIONS

- Multi-media DVD player
- Moniputer
- Audio equipment
- Televisions (TVs)
- Video cassette recorders (VCRs)
- Audio cassette decks
- Air conditioners

BLOCK DIAGRAM



APPLICATION CIRCUIT



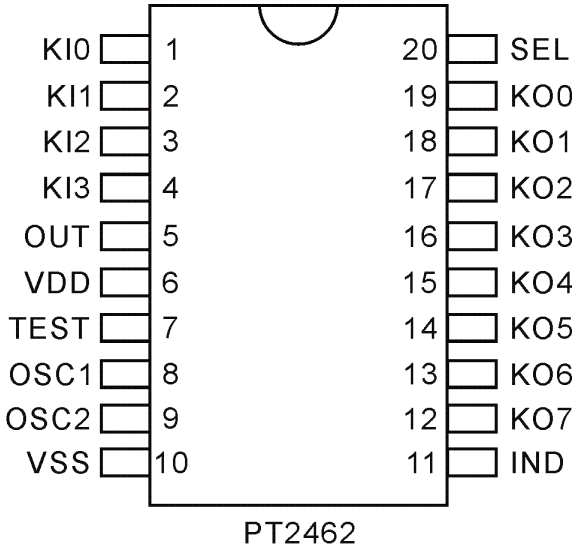
ORDER INFORMATION

Valid Order Number	Package Type	Top Code
PT2462	20 Pins, DIP, 300mil	PT2462-D-167
PT2462-S	20 Pins, SOP, 300mil	PT2462-167

Notes:
1. PT2462 Custom Code ID: (000~FFF)
2. 167: Custom Code 8167

0	0	0	C3	1	1	0	0

PIN CONFIGURATION



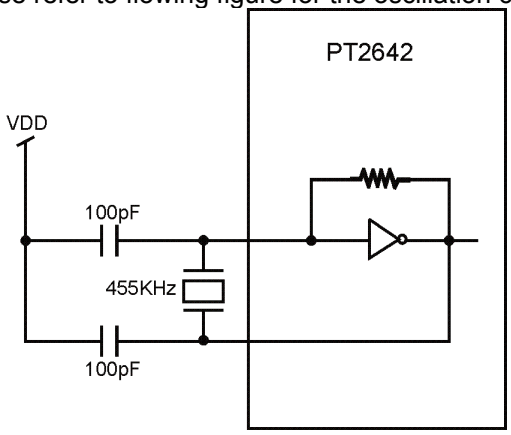
PIN DESCRIPTION

Pin Name	I/O	Description	Pin No
KI0 ~ KI3	I	Key Input Pins	1 ~ 4
OUT	O	Output Pins for Transit LED Drive	5
VDD	-	Power Supply	6
TEST	I	LSI Test Pin This pin is normally set to high state or floating	7
OSC1	I	Oscillator Pin No. 1	8
OSC2	O	Oscillator Pin No. 2	9
VSS	-	Power Supply VSS=GND	10
IND	O	LED Indicator Output Pin	11
KO7 ~ KO0	O	Key Scan Timing Signal Output Pins	12 ~ 19
SEL	I	Select Pin Option 1 -- 2 Custom code selections by SEL “H” or “L” Option 2 -- 1 Custom code selection by not connecting SEL.	20

FUNCTION DESCRIPTION

OSCILLATION CIRCUIT

A self-biased type amplifier is housed by a CMOS Inverter Method. Thus, an oscillation circuit can be constructed by connecting a ceramic resonator. Please refer to flowing figure for the oscillation circuit diagram.



Unless the keys are being operated, the oscillation is normally stopped. Thus, power consumption is considerably reduced.

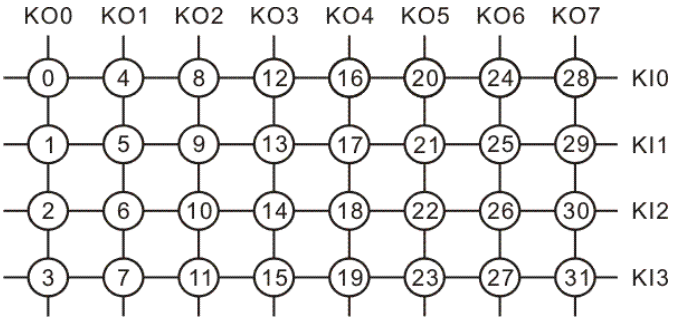
KEY INPUT

A total of 32 keys can be connected by Key Inputs-- KI0 ~ KI3 and Timing Signals -- KO0 ~ KO7. Double Key Operation is possible for only Key No. 20 in combination with the other keys connected to the KO5 line, namely: Key No. 21, 22 or 23. Thus, only the following key combinations may be used for the double key operation:

- Key No. 20 and 21
- Key No. 20 and 22
- Key No. 20 and 23

There is no order of priority given in key input. This means that keys designated for the double keying operation may be pressed in any sequence. When two keys (designated for the double key operation) are pressed simultaneously, a series of pulse is outputted according to each key input. Pressing other keys that are NOT intended for the double key operation do NOT generate any output.

The Key Matrix is given in the following diagram.



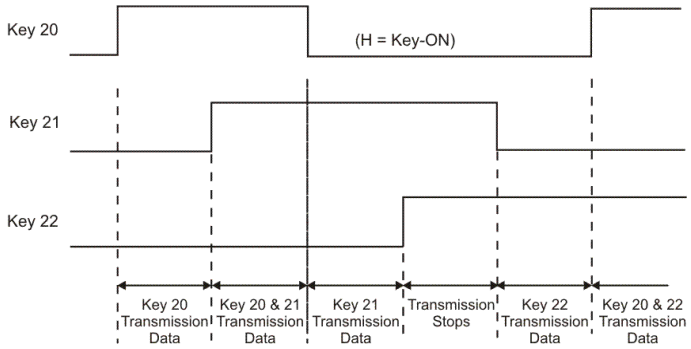
DOUBLE KEY OPERATION

Double Key Operation is useful for tape deck recording operation. The following table shows the Key Data corresponding to the double keys pressed. Also refer to the Key Input Section.

Key No.	D0	D1	D2	D3	D4	D5	D6	D7
20 & 21	1	0	1	0	1	1	0	0
20 & 22	0	1	1	0	1	1	0	0
20 & 23	1	1	1	0	1	1	0	0

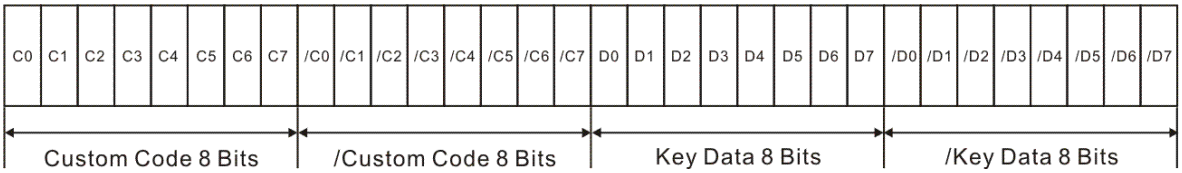
* Key Data -- D6 and D7 may be preset to “0”, “1” by mask option.
When any of the double key combinations (Key No. 20 & 21, Key No. 20 & 22, and Key No. 20 & 23) are pressed.

- D5 is set to “1”
- No Key Input Sequence is needed to perform the Double Key Operation



DATA FRAME

A PT2462 Data Frame consists of 32-bit, namely: 8-bit Custom Code (C0 ~ C7), 8-bit Key Data (D0 ~ D8) and their respective Inverse Codes. Please refer to the diagram below.



CUSTOM CODE

The Custom Code consists of 8-bit, namely C0 ~ C7. Eight (8) Bits-- C0 ~ C7 are internally fixed by the mask ROM. Thus, it is impossible to externally set these bits. Please refer to the diagram below.

C0	C1	C2	C3	C4	C5	C6	C7

However, PTC has made available two (2) Custom Code Options that may be externally selected by using the SEL (Select) Pin. These options are enumerated below:

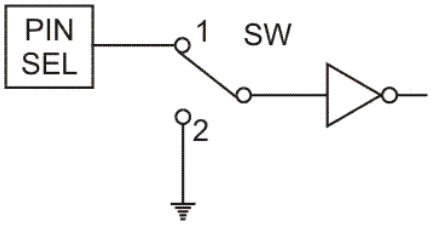
CUSTOM CODE OPTIONS

Option No. 1 (PT2462 Default Option)

There are two (2) Custom Code Selections that could be set internally. Using the SEL Pin, the two custom code choices are either:

- Select SEL "H" or,
- Select SEL "L"

Please refer to the diagram below when SW Position 1 is ON.



Option No. 2 (Customer Option)

There is only one Custom Code Selection that could be set internally. In this case, the SEL Pin is not connected. Please refer to the above figure when the SW position 2 is ON.

KEY DATA

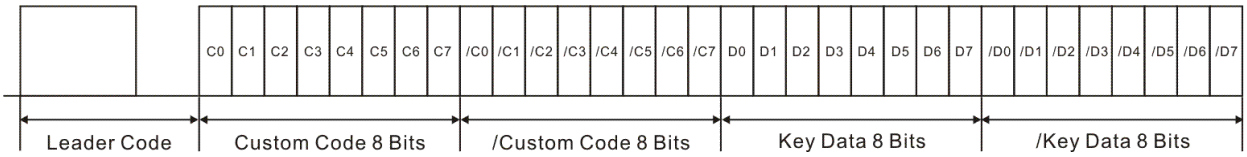
The key data has 7 bits (D0 ~ D7) and has the following key data codes.

Key No.	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
2	0	1	0	0	0	0	0	0
3	1	1	0	0	0	0	0	0
4	0	0	1	0	0	0	0	0
5	1	0	1	0	0	0	0	0
6	0	1	1	0	0	0	0	0
7	1	1	1	0	0	0	0	0
8	0	0	0	1	0	0	0	0
9	1	0	0	1	0	0	0	0
10	0	1	0	1	0	0	0	0
11	1	1	0	1	0	0	0	0
12	0	0	1	1	0	0	0	0
13	1	0	1	1	0	0	0	0
14	0	1	1	1	0	0	0	0
15	1	1	1	1	0	0	0	0
16	0	0	0	0	1	0	0	0
17	1	0	0	0	1	0	0	0
18	0	1	0	0	1	0	0	0
19	1	1	0	0	1	0	0	0
20	0	0	1	0	1	0	0	0
21	1	0	1	0	1	0	0	0
22	0	1	1	0	1	0	0	0
23	1	1	1	0	1	0	0	0
24	0	0	0	1	1	0	0	0
25	1	0	0	1	1	0	0	0
26	0	1	0	1	1	0	0	0
27	1	1	0	1	1	0	0	0
28	0	0	1	1	1	0	0	0
29	1	0	1	1	1	0	0	0
30	0	1	1	1	1	0	0	0
31	1	1	1	1	1	0	0	0

* D6 and D7 may be preset to “0”, “1”.

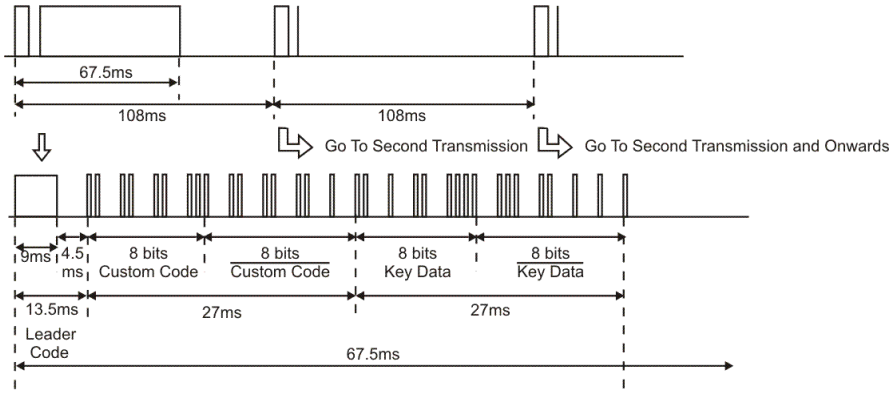
TRANSMISSION CODE

The PT2462 transmission code consists of a leader code, 8 bits custom codes and 8 bits key data codes. The inverse code of both the custom and key data codes are also sent simultaneously; thus, allowing an extremely low error rate in the system configuration. Please refer to the following diagram.

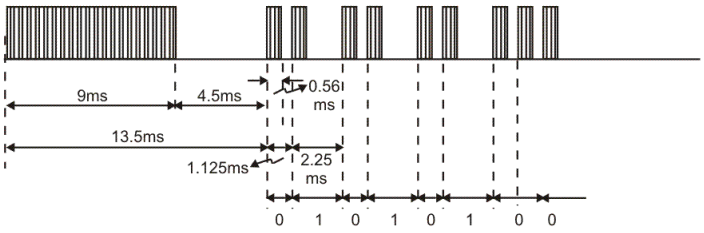


The leader code consists of a 9 ms carrier waveform followed by a 4.5ms OFF waveform. It is used as the leader for the following codes (Custom, Data and their respective inverse codes.) Thus, when the reception is configured by a microcomputer, the time relationship between the reception detection and other processes can be managed efficiently. The code uses the PPM (Pulse Position Modulation) Method, with "1" and "0" differentiated by the time between pulses.

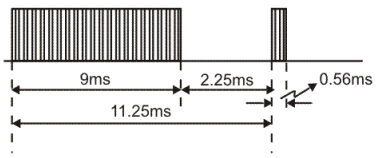
TRANSMISSION WAVEFORM



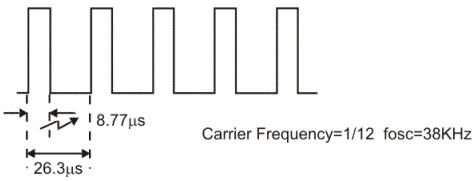
First Transmission ⇩



Second Transmission Onwards (Transmission is available only when key input continues)



Carrier Waveform



ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

Parameter	Symbol	Pin Name	Rating	Unit
Maximum supply voltage	VDD MAX	VDD	Vss-0.3 to 10	V
Input voltage	VIN	Each Input pin	VSS-0.3 to VDD+0.3	V
Output voltage	VOUT		Vss-0.3 to VDD+0.3	V
Output current	IOUT	OUT	-35	mA
Allowable power dissipation	Pd max	Ta< 85℃	150	mW
Operating temperature	Topr		-40 to +85	℃
Storage temperature	Tstg		-65 to +150	℃

ALLOWABLE OPERATING CONDITIONS

(Ta=25℃)

Parameter	Symbol	Pin Name	Condition	Min.	Typ.	Max.	Unit
Supply voltage	VDD	VDD	fosc=455KHz	1.8	3.0	5.5	V
High level input voltage	VIH	KI0 to KI3 C0 TO C5		0.7VDD		VDD	V
Low level input voltage	VIL	KI0 to KI3 C0 to C5		VSS		0.3VDD	V
Oscillation frequency	fosc			400	455	500	KHz

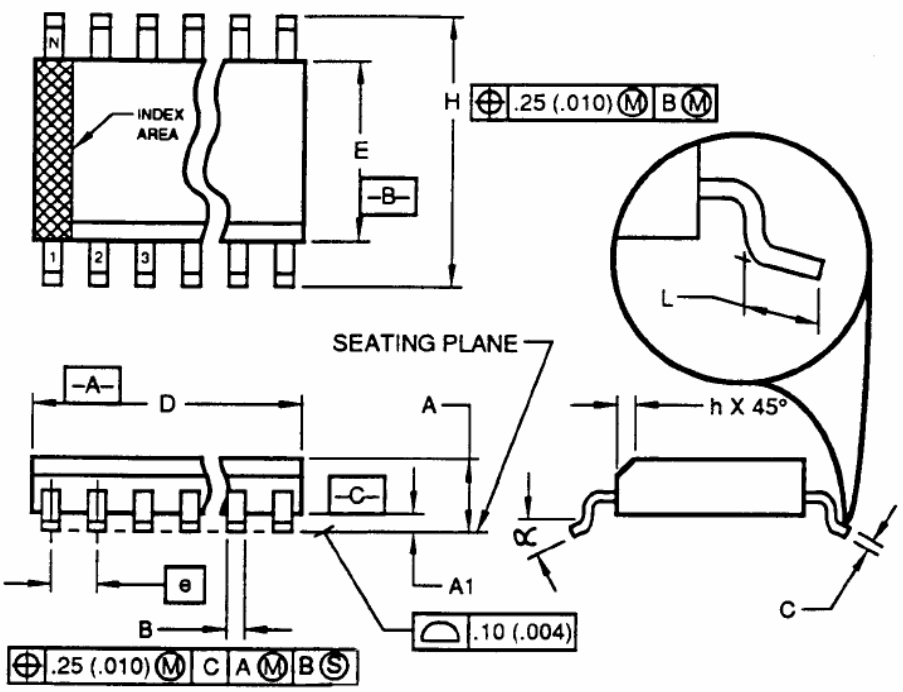
ELECTRICAL CHARACTERISTICS

(Ta=25℃, VDD=3.0V)

Parameter	Symbol	Pin Name	Conditions	Min.	Typ.	Max.	Unit
Operating supply current	IDD	VDD	Key ON, Output: no load			1	mA
Quiescent supply current	IDS	VDD	All keys OFF, OSC stops			1	μA
High level output current	IOH1	OUT	VDD=1.8V, VOH=1.0 V		-8		mA
	IOH2	OUT	VDD=3.0V, VOH=1.0V		-25		mA
High level output voltage	VOH	KO0 to KO7	IOH=-1mA	2.4			V
Low level output voltage	VOL	OUT	IOL=1mA			0.2	V
Output OFF-state leakage current	IOFF	KO0 to KO7				1	μA
High level input current	IIH	C0 to C5	VIN=VDD			1	μA
Low level input current	IIL	C0 to C5	VIN=VSS	-1			μA
Input floating voltage	VIF	KI0 to KI3			0.1VDD		V
Input pull-down resistance	RIN	KI0 to KI3		75	100	125	KΩ

PACKAGE INFORMATION

24 PINS, SOP, 300 MIL



Symbols	Min.	Nom.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	15.20		15.60
E	7.40		7.60
e	1.27 bsc.		
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
α	0°		8°

Notes:
1. Dimensioning and tolerancing per ANSI Y 14.5-1982.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15mm (0.006 in)per side.
3. Dimension “E” does not include interlead flash protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. “L” is the length of the terminal for soldering to a substrate.
6. “N” is the number of terminal position. (N=24)
7. The lead width “B” as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.24 in).
8. Controlling dimension: MILLIMETER.
9. Refer to JEDEC MS-013, Variation AD.

JEDEC is the trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION.

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.
PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

Princeton Technology Corp.
2F, 233-1, Baociao Road,
Sindian, Taipei 23145, Taiwan
Tel: 886-2-66296288
Fax: 886-2-29174598
http://www.princeton.com.tw