## FEATURES

- Extended Data Out operation
- $\overline{RAS}$ access time: 35, 40, 50, 60
- 2 $\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$ - before – $\overline{RAS}$ refresh capability
- $\overline{RAS}$ only and Hidden refresh capability
- Early write or output enable controlled write
- Package : 40pin 400mil SOJ packages
  40 pin 400mil TSOP-Ⅱ
- Single +5V±10% power supply
- TTL compatible inputs and outputs
- 256 refresh cycles /8ms

| Speed | -35 | -40 | -50 | -60 |
|---|---|---|---|---|
| $t_{RAC}$ | 35ns | 40ns | 50ns | 60ns |
| $t_{CAA}$ | 18ns | 20ns | 24ns | 30ns |
| $t_{PC}$ | 14ns | 15ns | 19ns | 27ns |
| $t_{CAC}$ | 11ns | 12ns | 14ns | 15ns |
| $t_{RC}$ | 70ns | 75ns | 90ns | 110ns |

## PIN DESCRIPTION

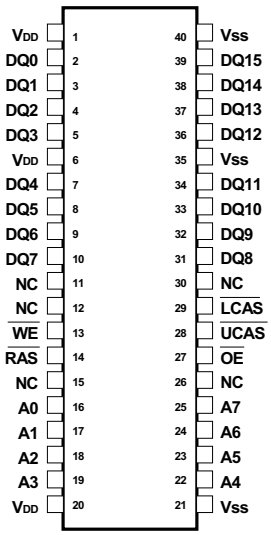
| SYMBOL | DESCRIPTION |
|---|---|
| A0-A7 | Address Inputs |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{UCAS}$ | Column Address Strobe/Upper Byte Control |
| $\overline{LCAS}$ | Column Address Strobe/Lower Byte Control |
| $\overline{WE}$ | Write enable |
| $\overline{OE}$ | Output enable |
| DQ0-DQ15 | Data Input, Data Output |
| $V_{DD}$ | +5V Supply |
| Vss | 0V Supply |
| NC | No Connect |

## GENERAL DESCRIPTION

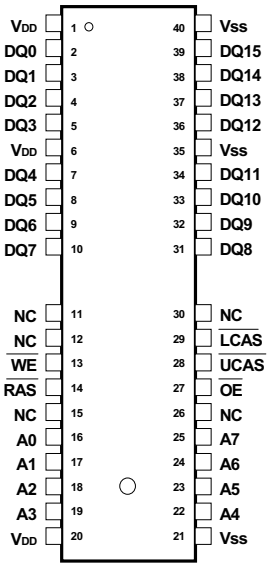
The UT51C161 is high speed 5 Volt EDO DRAMs organized as 64K bit X 16 I/O and fabricated with the CMOS process. The UT51C161 offers a combination of unique features including: EDO Page Mode operation for higher bandwidth with Page Mode cycle time as short as 14ns. All inputs are TTL compatible. Input and output capacitance is significantly lowered to increase performance and minimize loading. These features make the UT51C161 suited for wide variety of high performance computer systems and peripheral applications

## PIN ARRANGEMENT

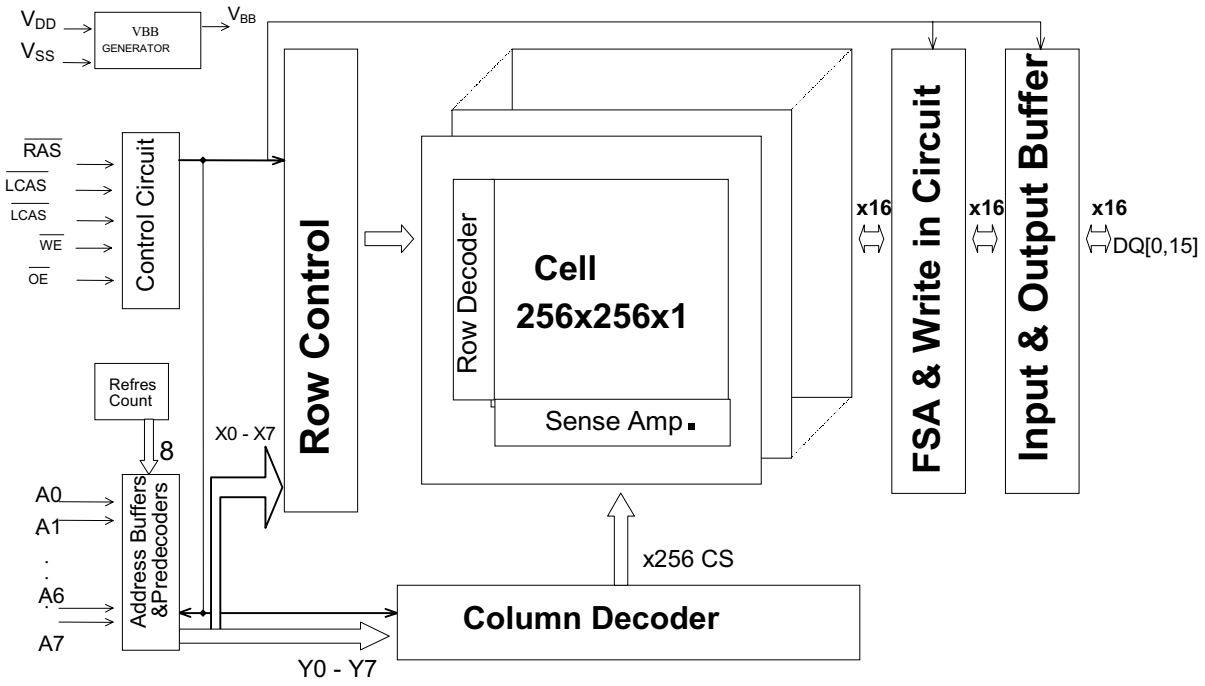
**UT51C161**
**40-pin SOJ**




**UT51C161**
**40- pin TSOP-Ⅱ**



## FUNCTION BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | VALUE | UNIT | NOTES |
|---|---|---|---|---|
| Voltage on any pin relative to Vss | $V_T$ | -1.0 to +7V | V | |
| Supply voltage relative to $V_{SS}$ | $V_{DD}$ | -1.0 to +7V | V | |
| Short circuit output current | $I_{OUT}$ | 50 | mA | |
| Power dissipation | $P_T$ | 1.0 | W | |
| Operating temperature | $T_{OPR}$ | 0 to + 70 | ºC | |
| Storage temperature | $T_{STG}$ | -55 to +125 | ºC | |

Notes: Permanent device damage may occur if absolute maximum ratings are exceed.

## RECOMMENDED DC OPERATING CONDITIONS (TA = 0℃ TO +70ºC)

| PARAMETER | SYMBOL | MIN | MAX | UNIT | NOTES |
|---|---|---|---|---|---|
| Supply voltage | VDD | 4.5 | 5.5 | V | 1 |
| | Vss | 0 | 0 | V | |
| Input high voltage | $V_{IH}$ | 2.4 | VDD +1V | V | 1,2 |
| Input low voltage | $V_{IL}$ | -0.3 | 0.8 | V | 1,3 |

Notes: 1. All Voltage referred to Vss
2. VIH(MAX)= 7 V for pulse width ≦ 20ns
3. VIL (MIN)= -1.0V for pulse width ≦ 20ns

## CAPACITANCE($T_A$ = 25ºC, $V_{DD}$=5V±10%, f=1MHz)

| | SYMBOL | TYP | MAX | UNIT |
|---|---|---|---|---|
| Input capacitance(A0-A7) | $C_{IN}1$ | 3 | 4 | pF |
| Input Capacitance ($\overline{RAS}$ , $\overline{UCAS}$ , $\overline{LCAS}$ , $\overline{WE}$ , $\overline{OE}$ ) | $C_{IN}2$ | 4 | 5 | pF |
| Output capacitance(DQ0-DQ15) | $C_{DQ}$ | 5 | 7 | pF |

## DC CHARACTERISTICS ($T_A$ = 0℃ to 70ºC, $V_{DD}$ = 5.0 V ± 0.5 V, Vss = 0 V)

| SYMBOL | PARAMETER | SPEED ($t_{RAC}$) | UT51C161 Min | UT51C161 Max | UNIT | TEST CONDITION |
|---|---|---|---|---|---|---|
| $I_{DD1}$ | Operating current, Vdd supply | -35 | | 150 | mA | $t_{RC} = t_{RC}$ (min.) |
| | | -40 | | 140 | | |
| | | -50 | | 130 | | |
| | | -60 | | 120 | | |
| $I_{DD2}$ | Standby current (TTL input) | | | 3 | mA | $\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{IH}$ |
| $I_{DD3}$ | $\overline{RAS}$ only refresh current | -35 | | 150 | mA | $t_{RC} = t_{RC}$ (min.) |
| | | -40 | | 140 | | |
| | | -50 | | 130 | | |
| | | -60 | | 120 | | |
| $I_{DD4}$ | EDO page mode current | -35 | | 180 | mA | $t_{PC} = t_{PC}$ (min.) |
| | | -40 | | 160 | | |
| | | -50 | | 150 | | |
| | | -60 | | 140 | | |
| $I_{DD5}$ | CBR refresh current | -35 | | 150 | mA | $t_{RC} = t_{RC}$ (min.) |
| | | -40 | | 140 | | |
| | | -50 | | 130 | | |
| | | -60 | | 120 | | |
| $I_{DD6}$ | Standby current (CMOS input) | | | 2 | mA | $\overline{RAS} \geqq V_{DD}$-0.2V<br>$\overline{CAS} \geqq V_{DD}$-0.2V<br>All other inputs>= $V_{SS}$ |
| $V_{DD}$ | Power Supply | | 4.5 | 5.5 | V | |
| $I_{LI}$ | Input Leakage Current | | -10 | 10 | uA | $V_{SS} \leqq V_{IN} \leqq V_{DD}$ |
| $I_{LO}$ | Output Leakage Current | | -10 | 10 | uA | $V_{SS} \leqq V_{OUT} \leqq V_{DD}$<br>$\overline{RAS} = \overline{CAS} = V_{IH}$ |
| $V_{IL}$ | Input Low Voltage | | -1 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | | 2.4 | $V_{DD}$ +1 | V | |
| $V_{OL}$ | Output Low Voltage | | | 0.4 | V | $I_{OI}$ =2mA |
| $V_{OH}$ | Output High Voltage | | 2.4 | | V | $I_{OH}$ = 2mA |

Notes: $I_{DD}1$, $I_{DD}3$, $I_{DD}4$, $I_{DD}5$ are dependent on output loading and cycle rates. Specified values are obtained with the output open. IDD is specified as an average current. In $I_{DD}1$, $I_{DD}3$, and $I_{DD}5$ address can be changed maximum once while $\overline{RAS} = V_{IL}$. In $I_{DD}4$, address can be changed maximum once within one EDO page cycle time, $t_{PC}$.

## AC CHARACTERISTICS ($T_A$ = 0℃ to 70°C, $V_{DD}$ = 5V ± 10%, Vss = 0 V)

Test condition: $V_{DD}$ = 5.0V±10%, $V_{IH}/V_{IL}$=3V/0V, $V_{OH}/V_{OL}$=2.0/0.8)

| | SYMBOL | PARAMETER | 35 | | 40 | | 50 | | 60 | | UNIT | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max | Min. | Max | Min. | Max | Min. | Max | | |
| 1 | $t_{RAS}$ | $\overline{RAS}$ Pulse Width | 35 | 75K | 40 | 75K | 50 | 75K | 60 | 75K | ns | |
| 2 | $t_{RC}$ | Read or Write Cycle Time | 70 | | 75 | | 90 | | 110 | | ns | |
| 3 | $t_{RP}$ | $\overline{RAS}$ Precharge Time | 25 | | 25 | | 30 | | 40 | | ns | |
| 4 | $t_{CSH}$ | $\overline{CAS}$ Hold Time | 35 | | 40 | | 50 | | 60 | | ns | |
| 5 | $t_{CAS}$ | $\overline{CAS}$ Pulse Width | 8 | | 8 | | 10 | | 10 | | ns | |
| 6 | $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ Delay | 13 | 24 | 17 | 28 | 19 | 36 | 20 | 45 | ns | |
| 7 | $t_{RCS}$ | Read Command Setup Time | 0 | | 0 | | 0 | | 0 | | ns | *1 |
| 8 | $t_{ASR}$ | Row Address Setup Time | 0 | | 0 | | 0 | | 0 | | Ns | |
| 9 | $t_{RAH}$ | Row Address hold Time | 6 | | 7 | | 9 | | 10 | | ns | |
| 10 | $t_{ASC}$ | Column Address Setup Time | 0 | | 0 | | 0 | | 0 | | ns | |
| 11 | $t_{CAH}$ | Column Address Hold Time | 6 | | 7 | | 9 | | 10 | | ns | |
| 12 | $t_{RSH}$ | $\overline{RAS}$ to $\overline{CAS}$ Hold Time | 10 | | 12 | | 14 | | 15 | | ns | |
| 13 | $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 5 | | 5 | | 5 | | 5 | | ns | |
| 14 | $t_{RCH}$ | Read Command Hold Time Reference $\overline{CAS}$ | 0 | | 0 | | 0 | | 0 | | ns | *2 |
| 15 | $t_{RRH}$ | Read Command Hold Time Reference $\overline{RAS}$ | 0 | | 0 | | 0 | | 0 | | ns | *2 |
| 16 | $t_{ROH}$ | $\overline{RAS}$ Hold Time Referenced to $\overline{OE}$ | 7 | | 8 | | 10 | | 10 | | ns | |
| 17 | $t_{OAC}$ | Access Time from $\overline{OE}$ | | 11 | | 12 | | 14 | | 15 | ns | *9 |
| 18 | $t_{CAC}$ | Access Time from $\overline{CAS}$ | | 11 | | 12 | | 14 | | 15 | ns | *3,4, 11 |
| 19 | $t_{RAC}$ | Access Time from $\overline{RAS}$ | | 35 | | 40 | | 50 | | 60 | ns | *3,5, 6 |
| 20 | $t_{CAA}$ | Access Time From Column Address | | 18 | | 20 | | 24 | | 30 | ns | *3,4, 7 |
| 21 | $t_{LZ}$ | $\overline{OE}$ or $\overline{CAS}$ to Low-Z Output | 0 | | 0 | | 0 | | 0 | | ns | *13 |
| 22 | $t_{HZ}$ | $\overline{OE}$ or $\overline{CAS}$ to High-Z Output | 0 | 5 | 0 | 6 | 0 | 8 | 0 | 10 | ns | *13 |
| 23 | $t_{AR}$ | Column Address Hold Time from $\overline{RAS}$ | 25 | | 30 | | 40 | | 50 | | ns | |
| 24 | $t_{RAD}$ | $\overline{RAS}$ to Column Address Delay Time | 10 | 17 | 12 | 20 | 14 | 26 | 15 | 30 | ns | *8 |
| 25 | $t_T$ | Transition Time | 1.5 | 50 | 1.5 | 50 | 1.5 | 50 | 1.5 | 50 | ns | *12 |
| 26 | $t_{CWL}$ | Write Command to $\overline{CAS}$ Lead Time | 8 | | 10 | | 10 | | 10 | | ns | |
| 27 | $t_{WCS}$ | Write Command Setup Time | 0 | | 0 | | 0 | | 0 | | ns | *9,10 |
| 28 | $t_{WCH}$ | Write Command Hold time | 5 | | 6 | | 7 | | 10 | | ns | |

## AC CHARACTERISTICS ($T_A$ = 0℃ to 70°C, $V_{DD}$ = 5V ± 10%, Vss = 0 V)

| | SYMBOL | PARAMETER | 35 | | 40 | | 50 | | 60 | | unit | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max | Min. | Max | Min. | Max | Min. | Max | | |
| 29 | $t_{WP}$ | Write Pulse Width | 5 | | 6 | | 7 | | 10 | | ns | |
| 30 | $t_{WCR}$ | Write Command Hold Time from $\overline{RAS}$ | 25 | | 30 | | 40 | | 50 | | ns | |
| 31 | $t_{RWL}$ | Write Command to $\overline{RAS}$ Lead Time | 11 | | 12 | | 14 | | 15 | | ns | |
| 32 | $t_{DS}$ | Data in Setup Time | 0 | | 0 | | 0 | | 0 | | ns | *11 |
| 33 | $t_{DH}$ | Data in Hold Time | 5 | | 6 | | 7 | | 10 | | ns | *11 |
| 34 | $t_{WOH}$ | Write to $\overline{OE}$ Hold time | 5 | | 6 | | 8 | | 10 | | ns | *11 |
| 35 | $t_{OED}$ | $\overline{OE}$ to Data Delay Time | 5 | | 6 | | 8 | | 10 | | ns | *11 |
| 36 | $t_{RWC}$ | Read-Modify-Write Cycle Time | 105 | | 110 | | 130 | | 170 | | Ns | |
| 37 | $t_{RRW}$ | Read-Modify-Write Cycle Time $\overline{RAS}$ Pulse Width | 70 | | 75 | | 85 | | 105 | | ns | |
| 38 | $t_{CWD}$ | $\overline{CAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle | 28 | | 30 | | 34 | | 40 | | ns | *9 |
| 39 | $t_{RWD}$ | $\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle | 54 | | 58 | | 68 | | 85 | | ns | *9 |
| 40 | $t_{CRW}$ | $\overline{CAS}$ pulse Width in RMW | 46 | | 48 | | 52 | | 65 | | ns | |
| 41 | $t_{AWD}$ | Column Address to $\overline{WE}$ Delay Time | 35 | | 38 | | 42 | | 58 | | ns | *9 |
| 42 | $t_{PC}$ | EDO Page Mode Read or Write Cycle Time | 14 | | 15 | | 19 | | 27 | | ns | |
| 43 | $t_{CP}$ | $\overline{CAS}$ Precharge Time | 4 | | 5 | | 7 | | 10 | | ns | |
| 44 | $t_{CAR}$ | Column Address to $\overline{RAS}$ Setup Time | 18 | | 20 | | 24 | | 30 | | ns | |
| 45 | $t_{CAP}$ | Access Time from Column Precharge | | 20 | | 23 | | 27 | | 34 | ns | *4 |
| 46 | $t_{DHR}$ | Data in Hold Time Referenced to $\overline{RAS}$ | 25 | | 30 | | 40 | | 50 | | ns | |
| 47 | $t_{CSR}$ | $\overline{CAS}$ Setup Time in CBR Refresh | 8 | | 10 | | 10 | | 10 | | ns | |
| 48 | $t_{RPC}$ | $\overline{RAS}$ to $\overline{CAS}$ Precharge Time | 0 | | 0 | | 0 | | 0 | | ns | |
| 49 | $t_{CHR}$ | $\overline{CAS}$ Hold Time in CBR Refresh | 8 | | 9 | | 12 | | 15 | | ns | |
| 50 | $t_{PCM}$ | EDO Page Mode Cycle Time in RMW | 55 | | 60 | | 70 | | 85 | | ns | |
| 51 | $t_{COH}$ | Output Hold After $\overline{CAS}$ Low | 3 | | 3 | | 3 | | 3 | | ns | |
| 52 | $t_{OES}$ | $\overline{OE}$ Low to $\overline{CAS}$ High Setup Time | 3 | | 4 | | 6 | | 8 | | ns | |
| 53 | $t_{OEH}$ | $\overline{OE}$ Hold Time from $\overline{WE}$ in RMW Cycle | 5 | | 6 | | 8 | | 10 | | ns | |
| 54 | $t_{OEP}$ | $\overline{OE}$ Pulse Width | 8 | | 10 | | 14 | | 18 | | ns | |
| 55 | $t_{REF}$ | Refresh Interval (512 Cycles) | | 8 | | 8 | | 8 | | 8 | ms | *14 |

Notes:

1. $t_{RCD}$ (Max.) is specified for reference only. Operation within $t_{RCD}$ (Max.) limits insures that $t_{RAC}$ (Max.) and $t_{CAA}$ (Max.) can be met. If $t_{RCD}$ is greater than the specified $t_{RCD}$ (Max.), the access time is controlled by $t_{CAA}$ and $t_{CAC.}$

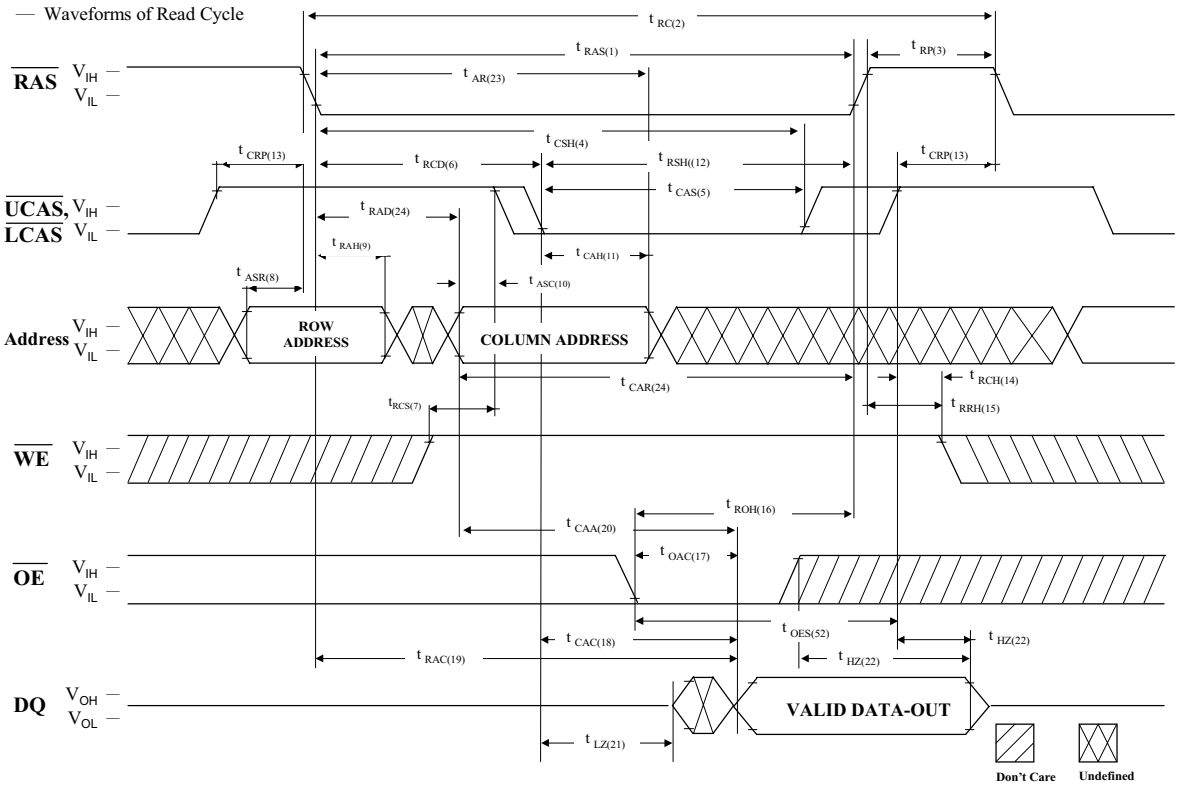
2. Either $t_{RRH}$ or $t_{RCH}$ must be satisfied for Read Cycle to occur.
3. Measured with a load equivalent to one TTL input and 50pF.
4. Access time is determined by the longest of $t_{CAA}$ , $t_{CAC}$ and $t_{CAP}$ .
5. Assumes that $t_{RAD} \leqq t_{RAD}$ (Max.). If $t_{RCD}$ is greater than $t_{RCD}$ (Max.), $t_{RAC}$ will increase by the amount that $t_{RCD}$ exceeds $t_{RCD}$ (Max.)
6. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If $t_{RCD}$ is greater than $t_{RCD}$ (Max.), $t_{RAC}$ will increase by the amount that $t_{RAD}$ exceeds $t_{RAD}$ (Max.)
7. Assumes that $t_{RAD} \geqq t_{RAD}$ (Max.).
8. Operation within the $t_{RAD}$ (Max.) limits ensures that $t_{RA}$ can be met. $t_{RAD}$ (Max.) is specified as a reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD}$ (Max.), the access time is controlled by $t_{CAA}$ and $t_{CAC.}$
9. $t_{WCS}$ , $t_{RWD}$ , $t_{AWD}$ and $t_{CWD}$ are not restrictive operating parameters.
10. $t_{WCS}$ (min.) must be satisfied in an Early Write Cycle.
11. $t_{DS}$ and $t_{DH}$ are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$ .
12. $t_T$ is measured between $V_{IH}$ (min.) and $V_{IL}$ (max.). AC-measurements assume $t_T$ = 3Ns.
13. Assumes a tri-state test load (5pF and a 500Ohm Thevenin equivalent).
14. An initial pause of 200us is required after power-up followed by any 8 CBR or ROR cycles before device operation is achieved.

## TRUTH TABLE

| FUNCTION | $\overline{RAS}$ | $\overline{LCAS}$ | $\overline{UCAS}$ | $\overline{WE}$ | $\overline{OE}$ | ADDRESS | DQ0-7 | DQ8-15 | |
|---|---|---|---|---|---|---|---|---|---|
| Standby | H | H | H | X | X | X | High-Z | High-Z | |
| Read:Word | L | L | L | H | L | ROW/COL | DQ-OUT | | |
| Read: Lower Byte | L | L | H | H | L | ROW/COL | DQ-OUT | High-Z | |
| Read: Upper Byte | L | H | L | H | L | ROW/COL | High-Z | DQ-OUT | |
| Write: Word (Early-Write) | L | L | L | L | X | ROW/COL | DQ-IN | | |
| Write: Lower Byte (Early-Write) | L | L | H | L | X | ROW/COL | DQ-IN | High-Z | |
| Write: Upper Byte (Early-Write) | L | H | L | L | X | ROW/COL | High-Z | DQ-IN | |
| Read-Write | L | L | L | H→L | L→H | ROW/COL | DQ-OUT,DQ-IN | | *1,2 |
| EDO Page-Mode Read | L | H→L | H→L | H | L | COL | DQ-OUT | | *2 |
| EDO Page-Mode Write | L | H→L | H→L | L | X | COL | DQ-IN | | *2 |
| EDO Page –Mode Read-Write | L | H→L | H→L | H→L | L→H | COL | DQ-OUT,DQ-IN | | *1,2 |
| Hidden Refresh Read | L→H→L | L | L | H | L | ROW/COL | DQ-OUT | | *2 |
| $\overline{RAS}$ Only Refresh | L | H | H | X | X | ROW | High-Z | | |
| CBR Refresh | H→L | L | L | X | X | X | High-Z | | |

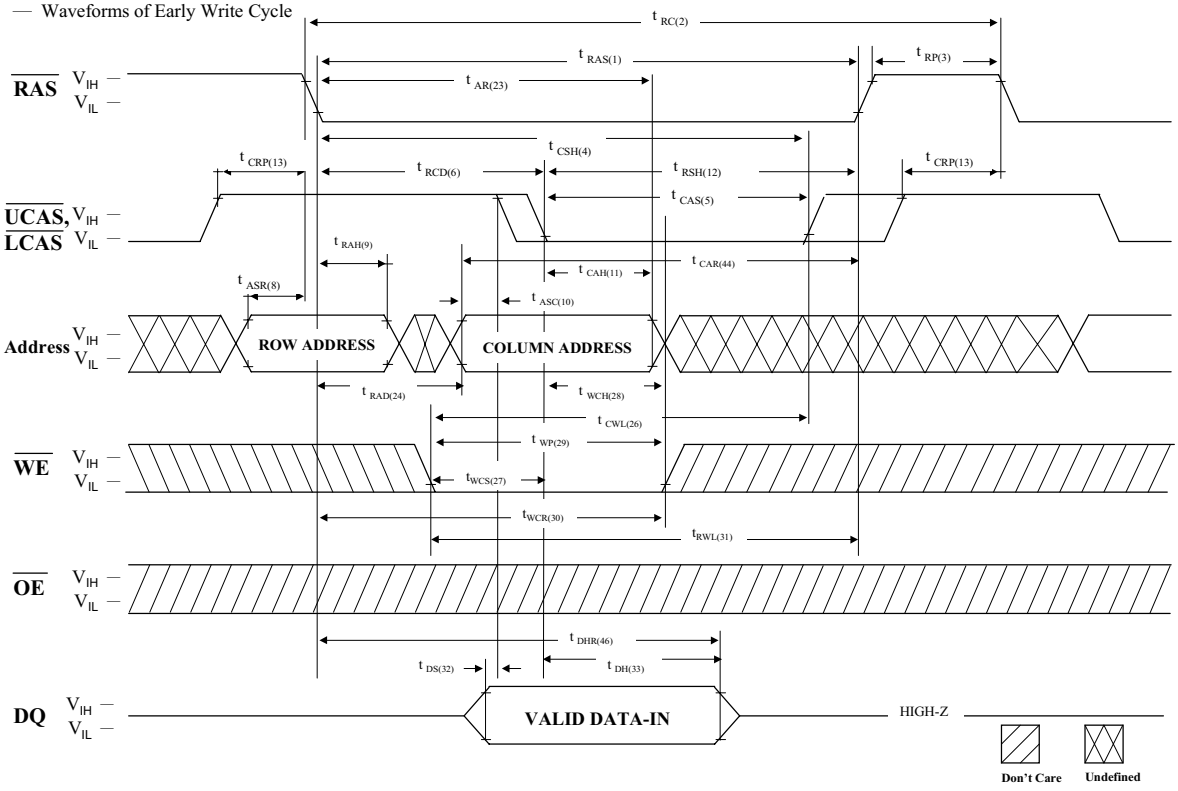
Notes:
1. Byte Write cycles $\overline{LCAS}$ or $\overline{UCAS}$ active.
2. Byte Read cycles $\overline{LCAS}$ or $\overline{UCAS}$ active.

***UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram***

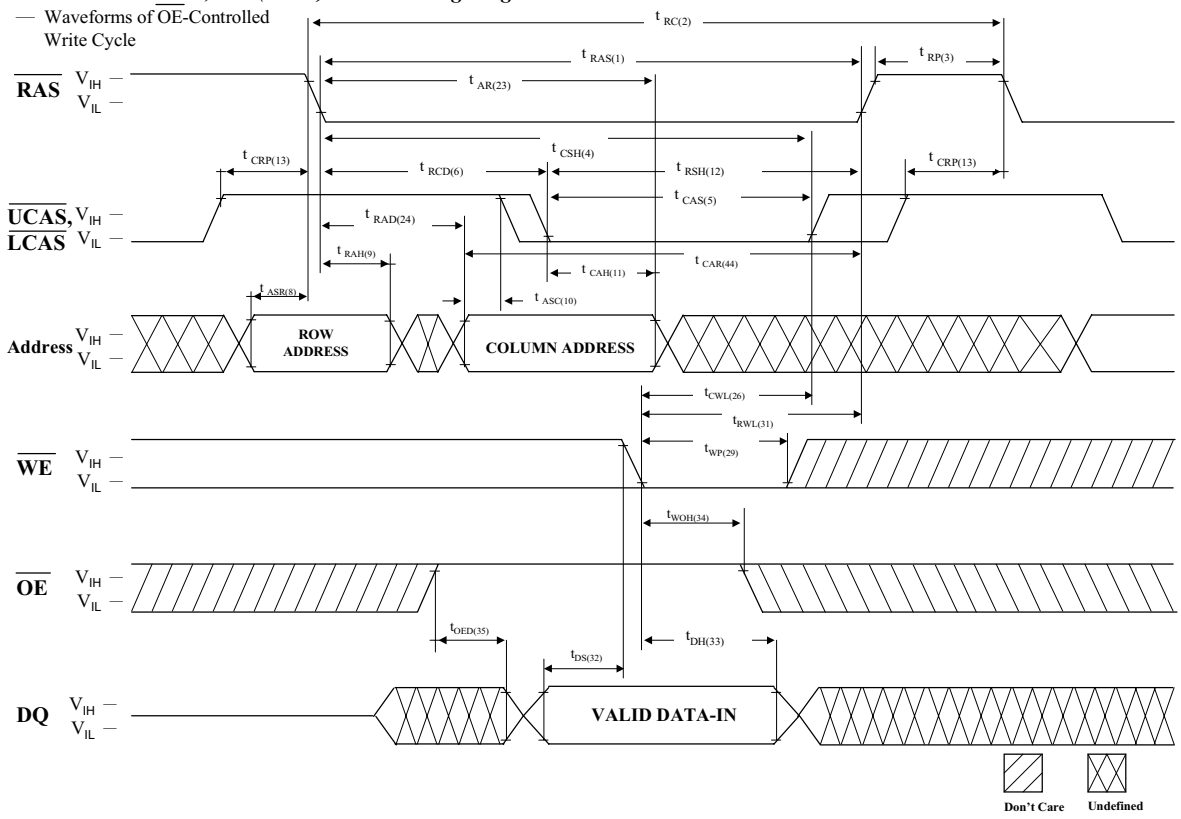


***UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram***

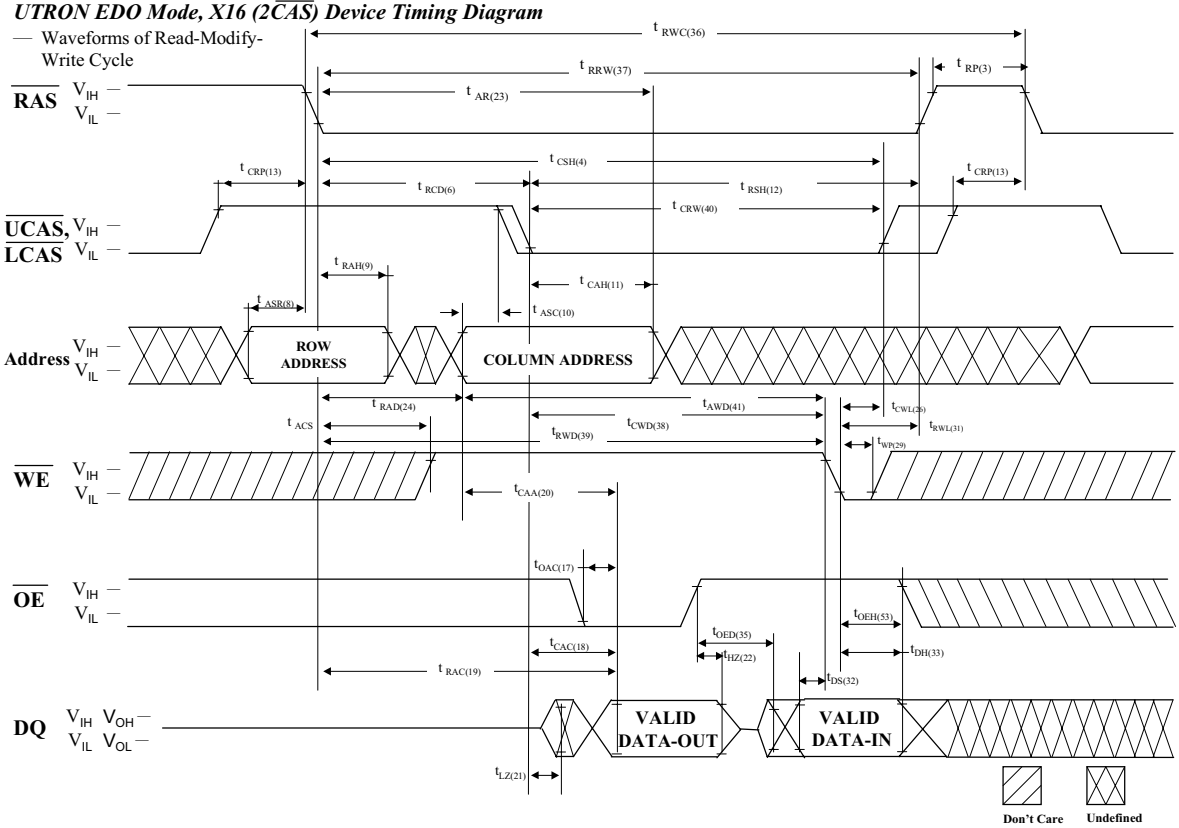
— Waveforms of Early Write Cycle



***UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram***

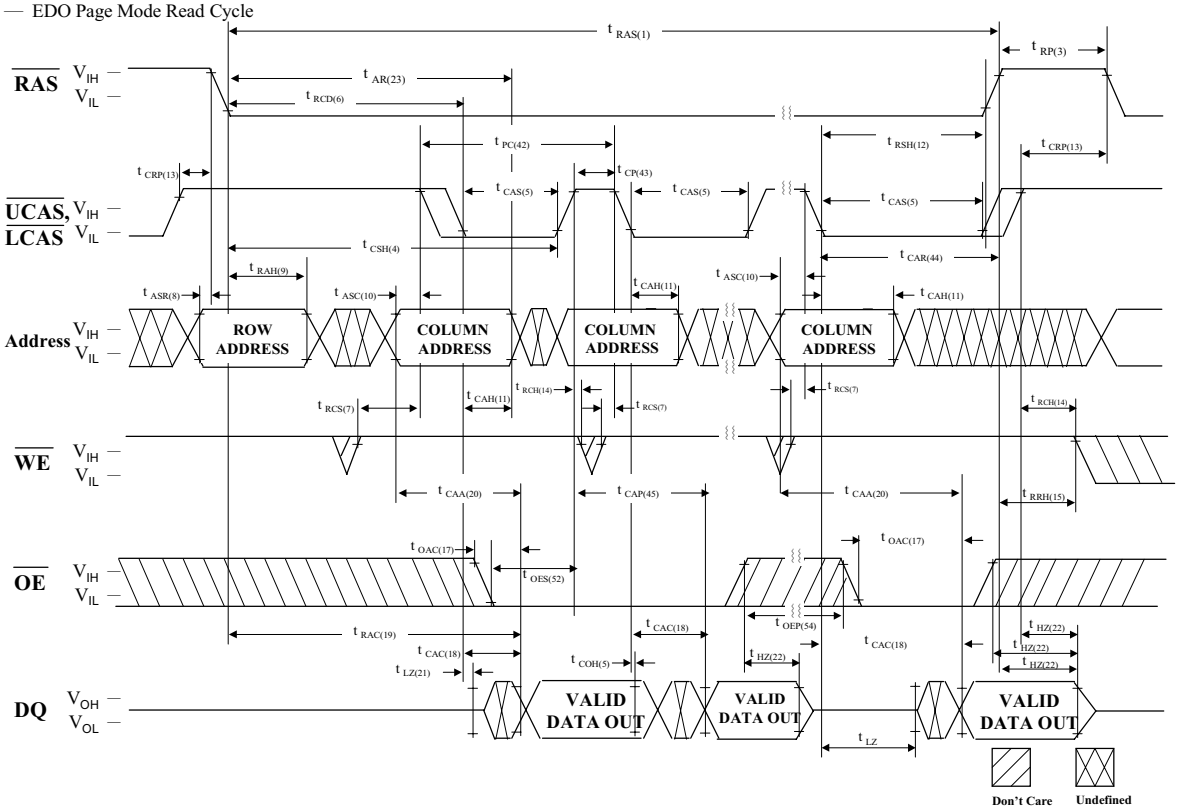


***UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram***

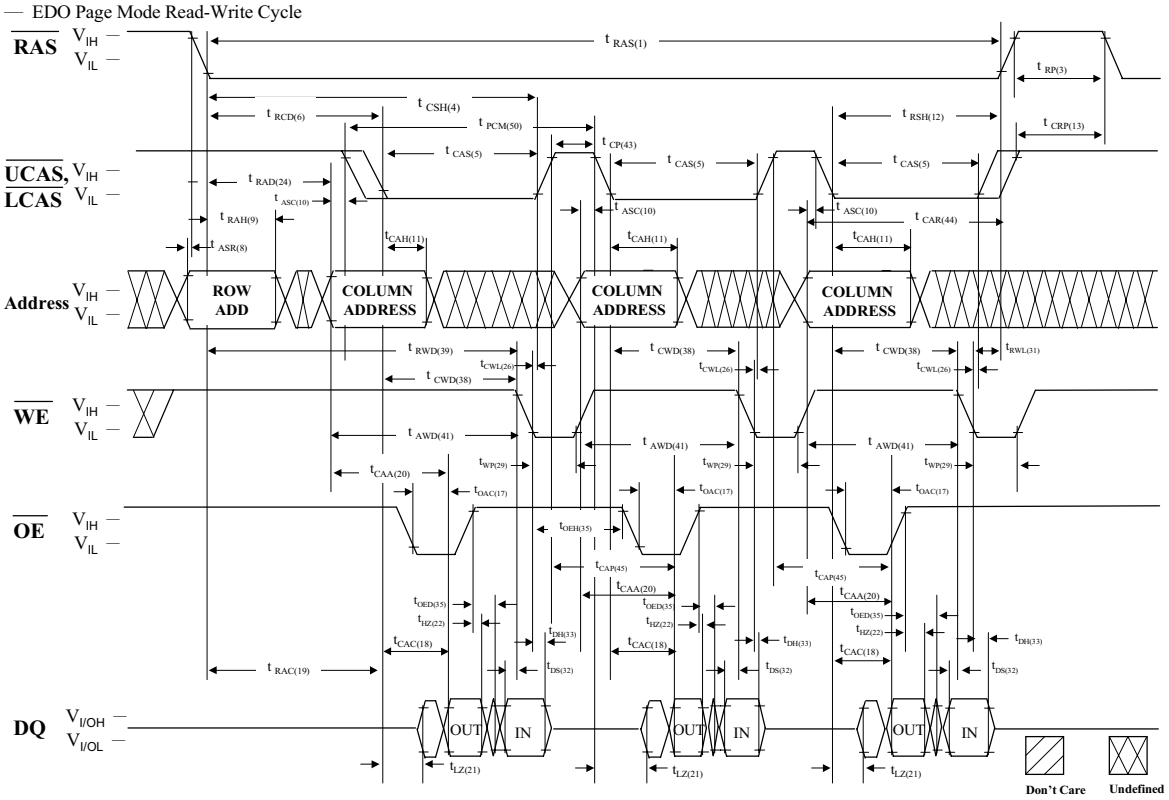


***UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram***

— EDO Page Mode Read Cycle

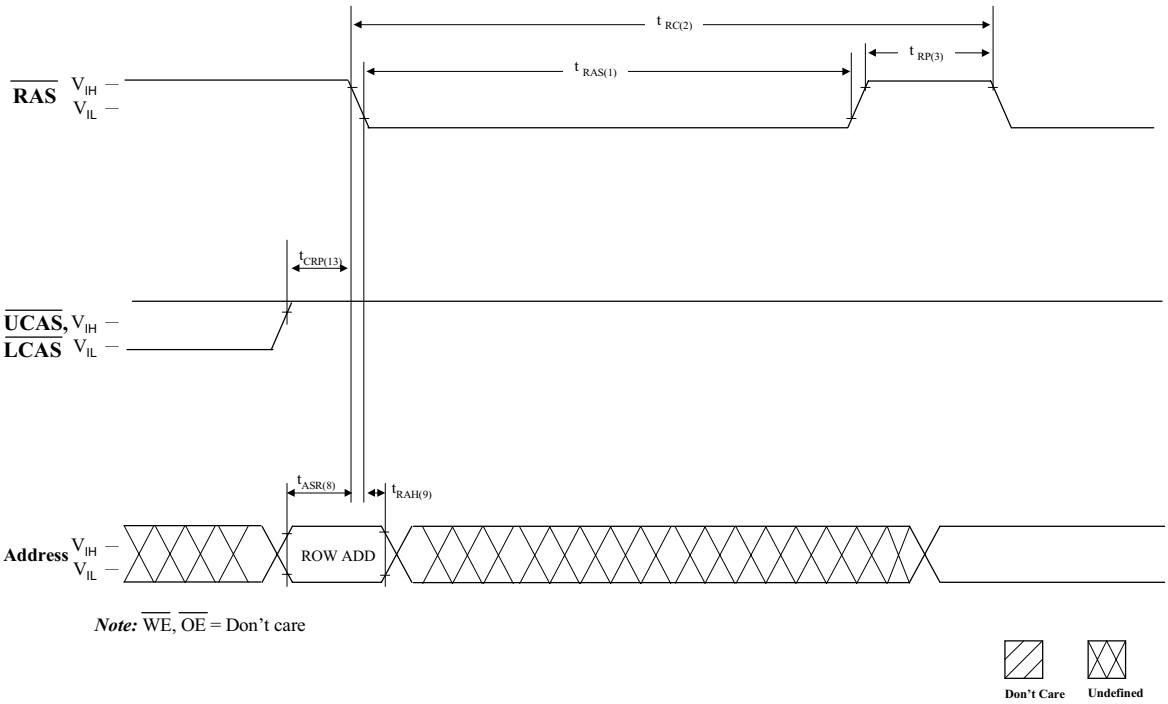


***UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram***



***UTRON EDO Mode, X16 (2CAS) Device Timing Diagram***

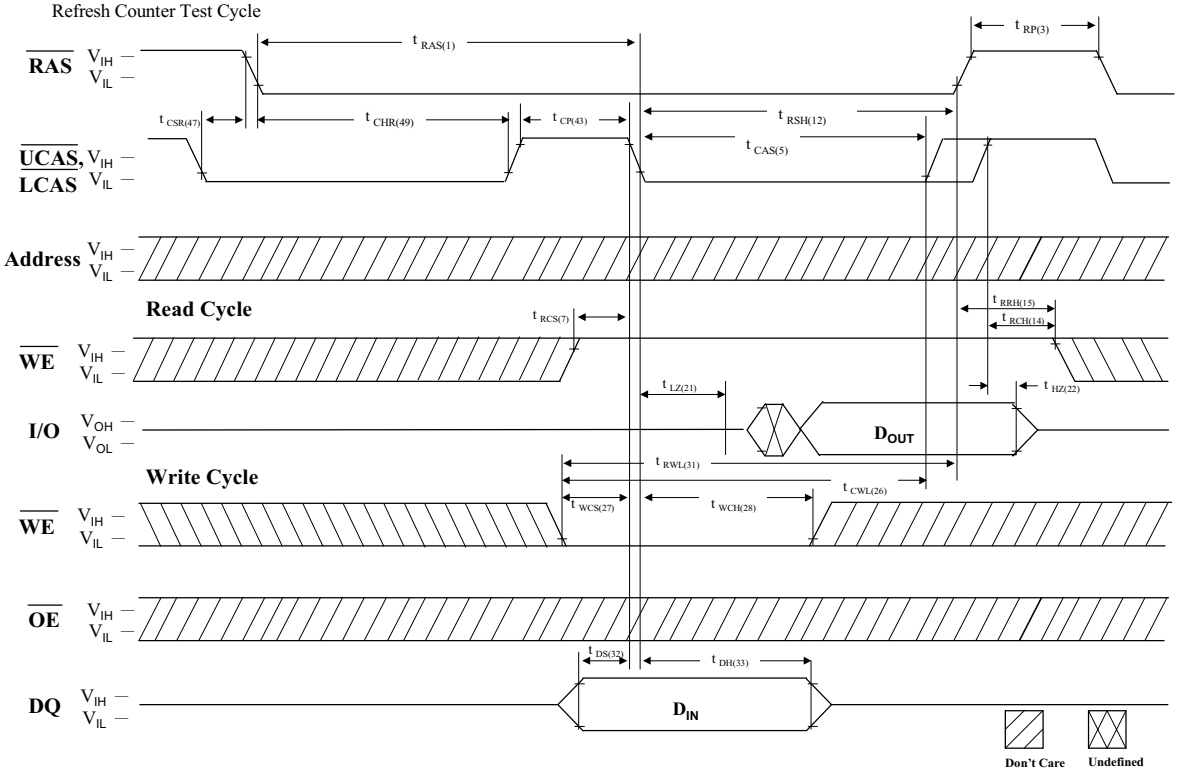
— Waveforms of $\overline{RAS}$-Only Refresh Cycle




***Note:*** $\overline{WE}$, $\overline{OE}$ = Don't care

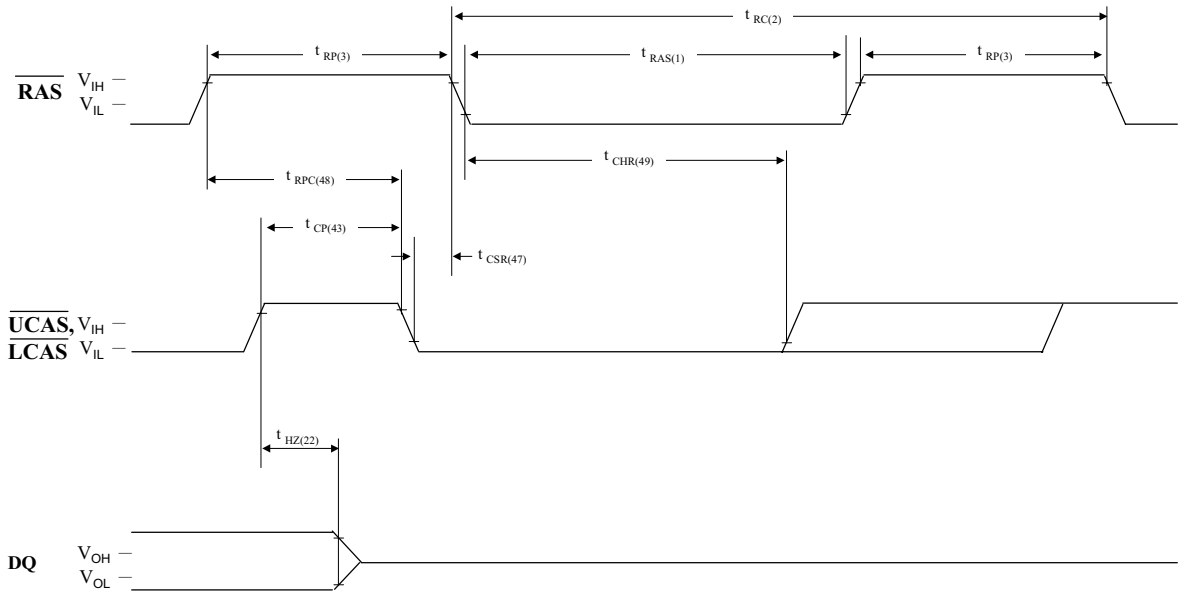
***UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram***

— Waveforms of $\overline{CAS}$-before-$\overline{RAS}$
Refresh Counter Test Cycle



***UTRON EDO Mode, X16 (2CAS) Device Timing Diagram***

— Waveforms of CAS-before-RAS Refresh Cycle

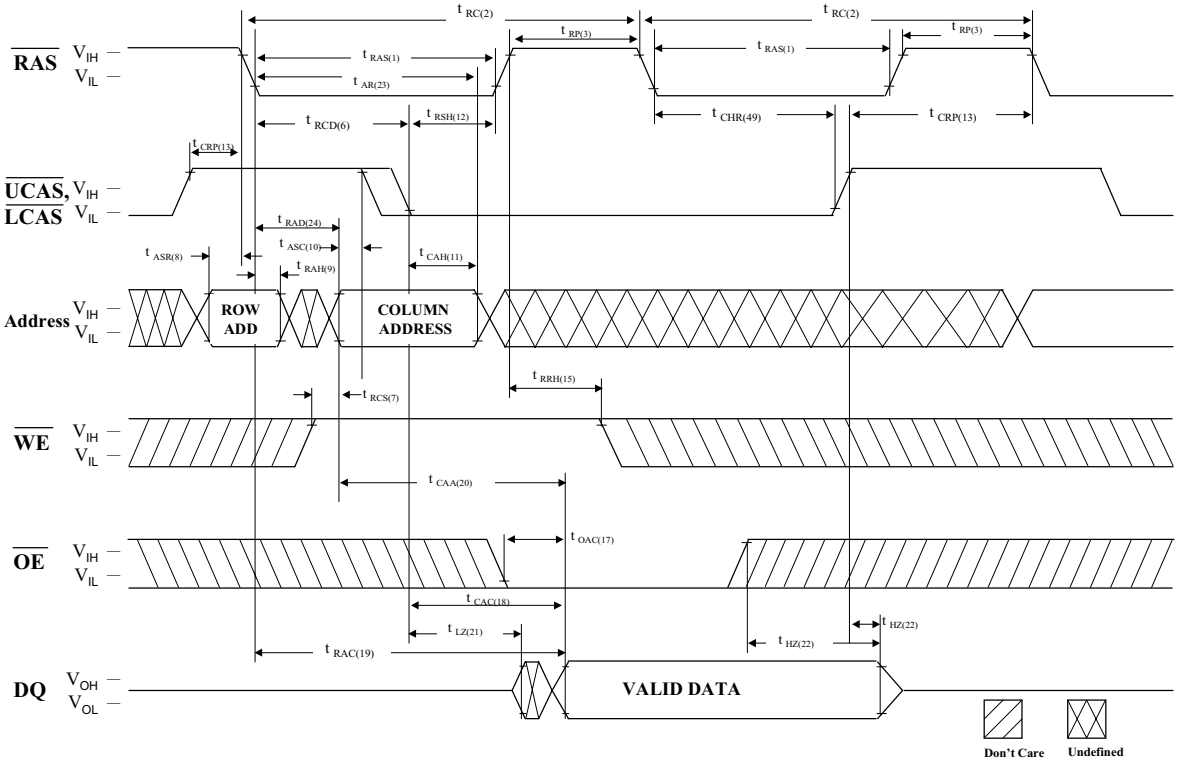



***Note:*** WE, OE = $A_0$ - $A_8$ = Don't care

Don't Care Undefined

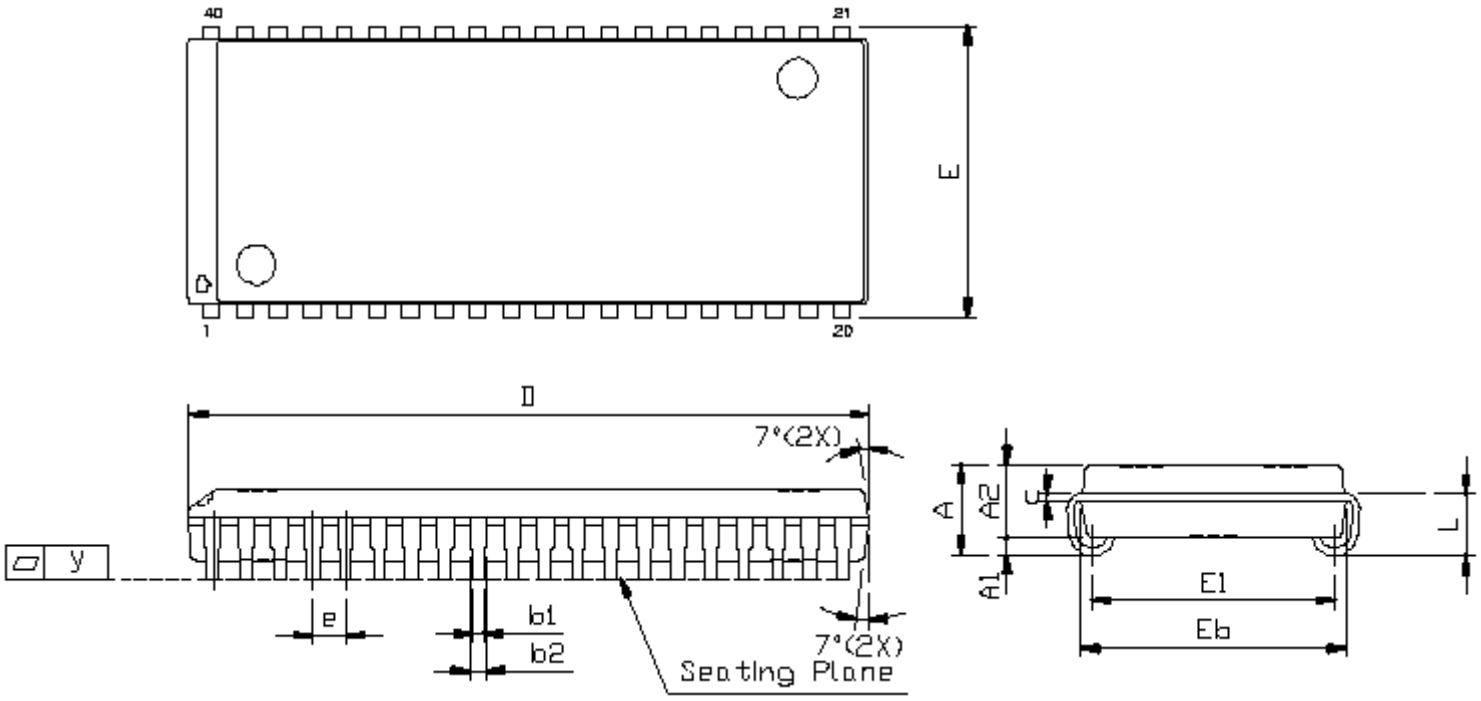
***UTRON EDO Mode, X16 (2$\overline{CAS}$) Device Timing Diagram***

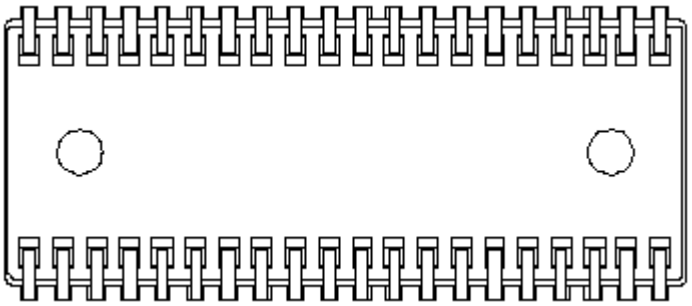
— Waveforms of Hidden Refresh Cycle (Read)



## PACKAGE OUTLINE DIMENSION

### 40 pin 400mil SOJ PACKAGE OUTLINE DIMENSION

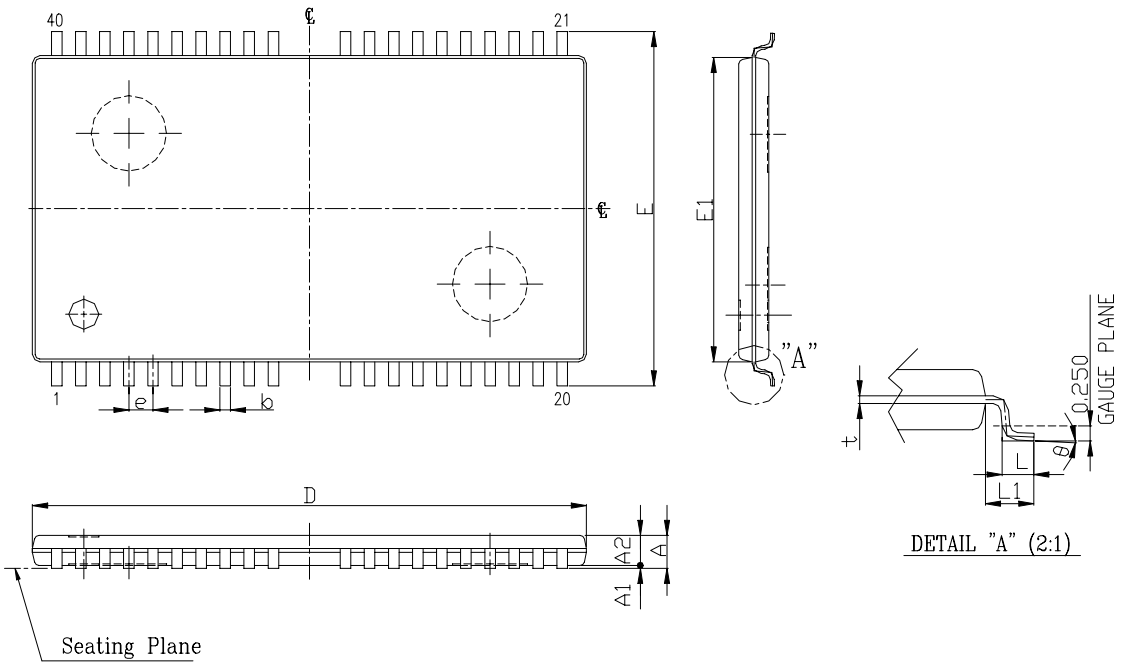


| UNIT / SYMBOL | INCH(BASE) | MM(REF) |
|---|---|---|
| A | 0.148 (MA) | 3.759 (MAX) |
| A1 | 0.024(MIN) | 0.061(MIN) |
| A2 | 0.115(MAX) | 2.921(MAX) |
| b1 | 0.018 (TYP) | 0.457(TYP) |
| b2 | 0.025 (TYP) | 0.635(TYP) |
| c | 0.010 (TYP) | 0.254 (TYP) |
| D | 1.025± 0.004 | 26.238± 0.102 |
| E | 0.440± 0.010 | 11.176± 0.254 |
| E1 | 0.38 (MAX) | 9.652 (MAX) |
| Eb | 0.400± 0.004 | 10.16± 0.102 |
| e | 0.050 (TYP) | 1.27 (TYP) |
| L | 0.093± 0.006 | 2.362± 0.152 |
| △c y | 0.004(MAX) | 0.101 (MAX) |

Material: Plastics

**40 pin 400mil TSOP-Ⅱ PACKAGE OUTLINE DIMENSION**




| UNIT / SYMBOL | MM(BASE) |
|---|---|
| A | 1.20(MAX) |
| A1 | 0.10± 0.05 |
| A2 | 1.00± 0.05 |
| b | 0.30~0.45 |
| t | 0.13(TYP) |
| D | 18.41± 0.10 |
| E1 | 10.16± 0.10 |
| E | 11.76± 0.20 |
| e | 0.80(TYP) |
| L | 0.50± 0.10 |
| L1 | 0.80(REF) |
| $\theta$ | 0° ~8° |

## ORDERING INFORMATION

| PART NO. | ACCESS TIME (ns) | PACKAGE |
|---|---|---|
| UT51C161JC-35 | 35 | 40-PIN SOJ |
| UT51C161JC-40 | 40 | 40-PIN SOJ |
| UT51C161JC-50 | 50 | 40-PIN SOJ |
| UT51C161JC-60 | 60 | 40-PIN SOJ |
| UT51C161MC-35 | 35 | 40-PIN TSOP-Ⅱ |
| UT51C161MC-40 | 40 | 40-PIN TSOP-Ⅱ |
| UT51C161MC-50 | 50 | 40-PIN TSOP-Ⅱ |
| UT51C161MC-60 | 60 | 40-PIN TSOP-Ⅱ |

## REVISION HISTORY

| REVISION | DESCRIPTION | DATE |
|---|---|---|
| Preliminary Rev. 0.9 | Original. | Oct 20,1999 |
| Preliminary Rev. 1.0 | | |
| Rev. 2.0 | Add TSOP-Ⅱ package | Aug 3,2001 |