NTVS3141P

Power MOSFET

–20 V, –3.7 A, 85 mΩ, Single P–Channel, CSP 1.0x1.5x0.65 mm

Features

- Low $R_{DS(on)}$ at Low Gate Voltage
- Chip Scale Packaging
- High Power Density (A/mm^2)
- This is a Pb–Free Device

Applications

- Load Switch in Cell Phone, DSC, PMP, GPS, PC's
- Battery Charging Switch

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating			Symbol	Value	Unit
Drain–to–Source Voltage			V_{DSS}	–20	V
Gate–to–Source Voltage			V_{GS}	±8	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	–3.7	A
Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	–2.9	A
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.5	W
Power Dissipation (Note 2)	Steady State	T_A = 25°C	P_D	0.9	W
Pulsed Drain Current		t_p = 10 μs	I_{DM}	–15	A
Operating Junction and Storage Temperature			T_J, T_{STG}	–55 to 150	°C
Source Current (Body Diode)			I_S	–1.1	A
Lead Temperature for Soldering Purposes (IR/Convection)			T_L	250	°C

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction–to–Ambient – Steady State (Note 1)	$R_{\theta JA}$	83	°C/W
Junction–to–Ambient – Steady State (Note 2)	$R_{\theta JA}$	133	°C/W

1. Surface–mounted on FR4 board using 1 inch sq pad size (Cu area = 1 in sq [2 oz] including traces)
2. Surface–mounted on FR4 board using 77.3 sq mm min pad, 2 oz Cu.

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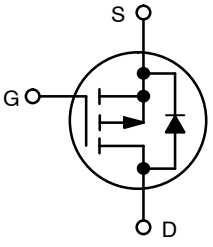
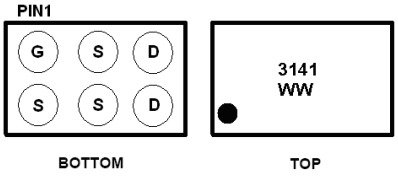
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX (Note 1)
–20 V	85 mΩ @ –4.5 V	–3.7 A
	123 mΩ @ –2.5 V	
	150 mΩ @ –1.8 V	
	200 mΩ @ –1.5 V	



P–Channel MOSFET

6 PIN FLIP–CHIP
1.0 x 1.5
CASE 499BC

PIN CONNECTION AND MARKING DIAGRAM



3141 = Specific Device Code
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NTVS3141PT2G	CSP–6 (Pb–Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA	−20			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = −250 μA, ref to 25°C		−9.0		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −20 V			−1.0	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±0.1	μA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA	−0.4	−0.7	−1.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			3.0		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V, I_D = −1.0 A		73	85	mΩ
		V_{GS} = −2.5 V, I_D = −1.0 A		87	123	
		V_{GS} = −1.8 V, I_D = −1.0 A		107	150	
		V_{GS} = −1.5 V, I_D = −1.0 A		134	200	
On to State Drain Current	$I_{D(on)}$	V_{GS} = −4.5 V, V_{DS} = −5.0 V	−10			A
Forward Transconductance	g_{FS}	V_{DS} = −5.0 V, I_D = −1.0 A		6.0		S
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −10 V		840		pF
Output Capacitance	C_{OSS}			155		
Reverse Transfer Capacitance	C_{RSS}			120		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −1.0 A		9.0	13	nC
Gate−to−Source Charge	Q_{GS}			1.0		
Gate−to−Drain Charge	Q_{GD}			3.0		
Gate Resistance	R_G	f = 1 MHz		9.0		Ω
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 3)						
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −1.0 A, R_G = 6.0 Ω		7.5	20	ns
Rise Time	t_r			9.5	20	
Turn−Off Delay Time	$t_{d(OFF)}$			35	65	
Fall Time	t_f			50	80	
DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −1.1 A		−0.7	−1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, di/dt = 100 A/μs, I_S = −1.1 A		37		ns
Reverse Recovery Charge	Q_{RR}			23		nC

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%

TYPICAL PERFORMANCE CURVES

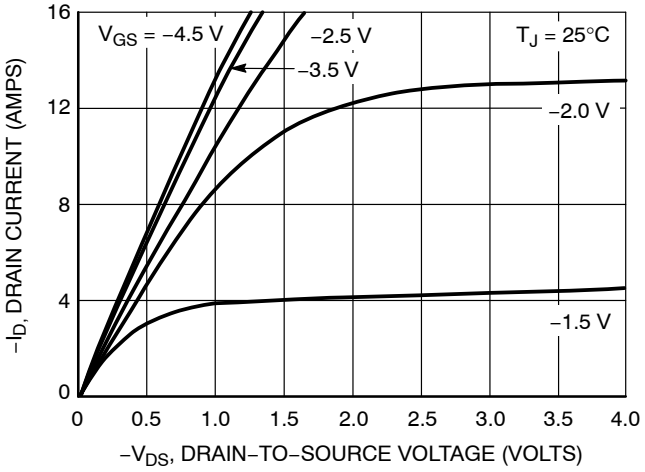


Figure 1. On−Region Characteristics

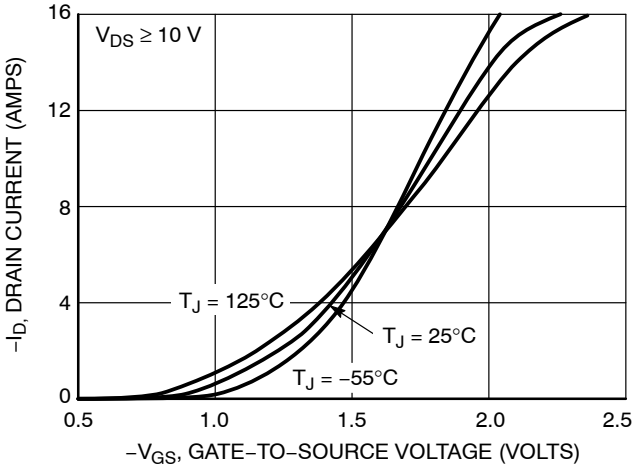


Figure 2. Transfer Characteristics

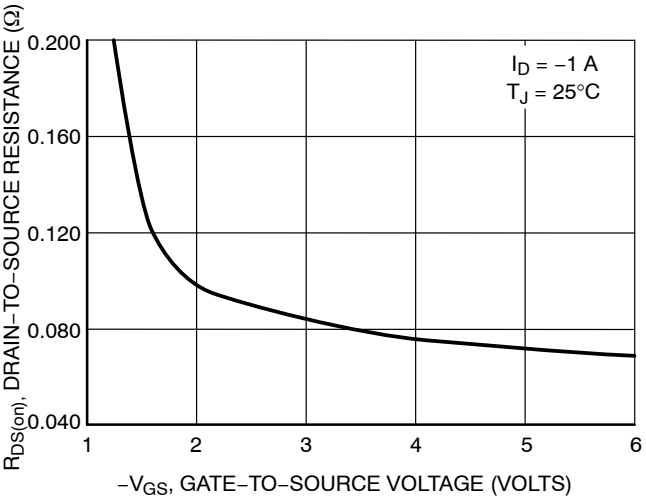


Figure 3. On−Resistance vs. Gate Voltage

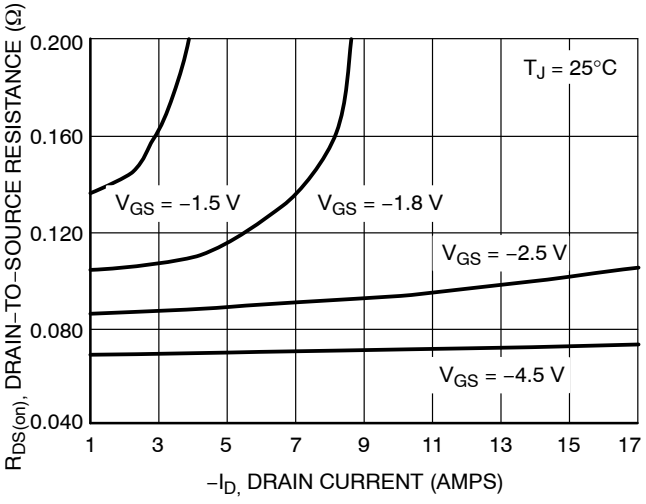


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

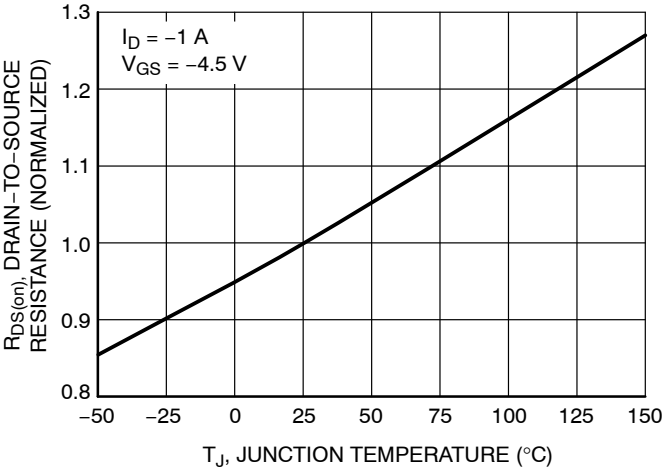


Figure 5. On−Resistance Variation with Temperature

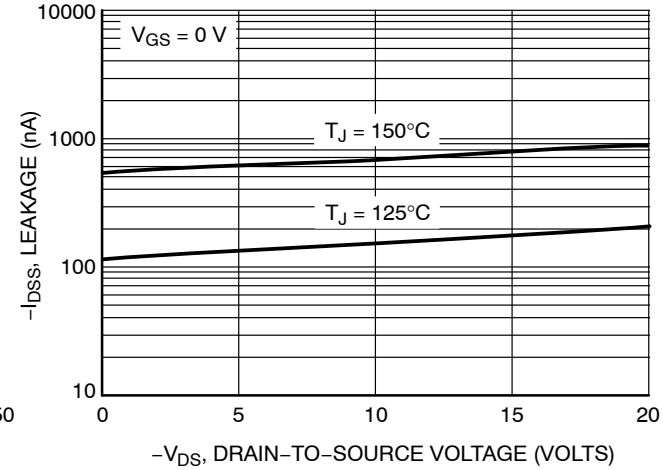


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

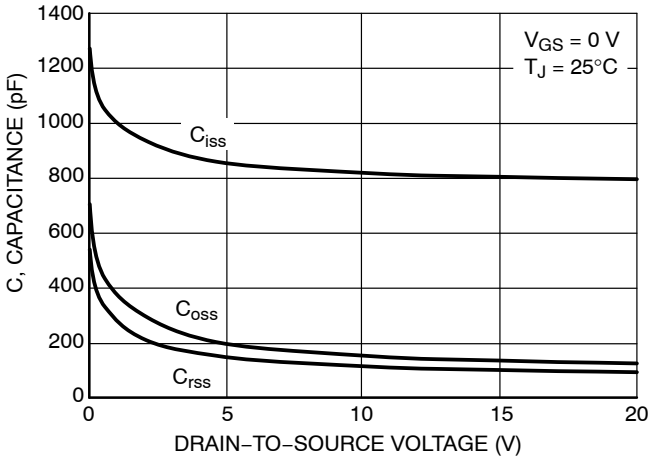


Figure 7. Capacitance Variation

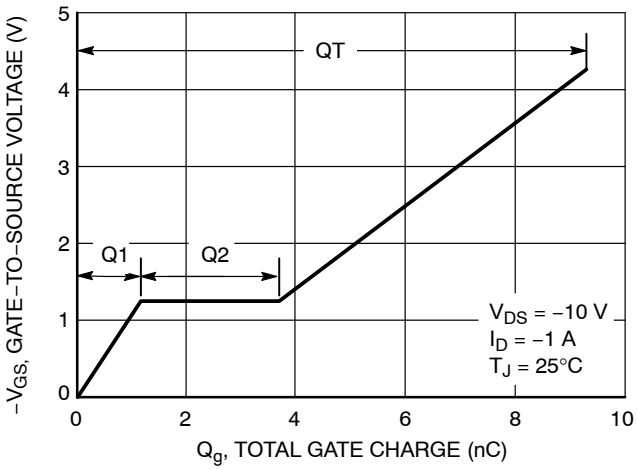


Figure 8. Gate−to−Source Voltage vs. Total Gate Charge

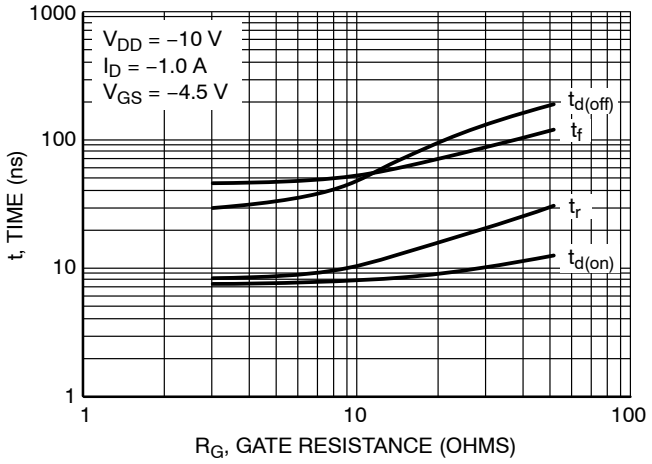


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

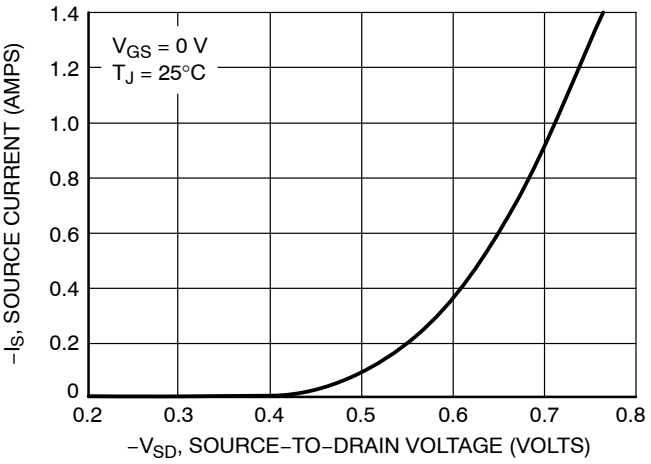


Figure 10. Diode Forward Voltage vs. Current

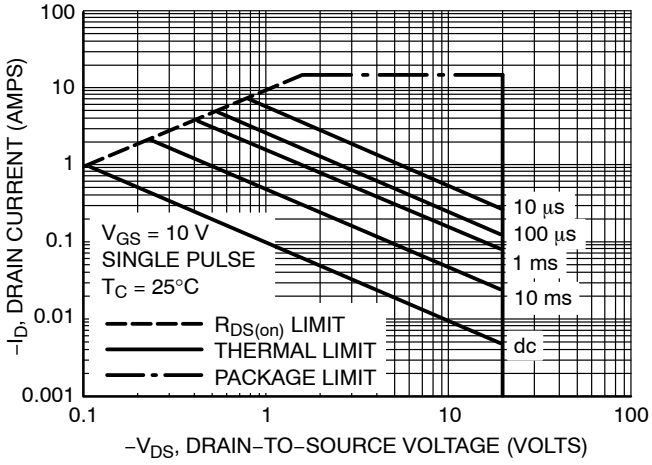


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL PERFORMANCE CURVES

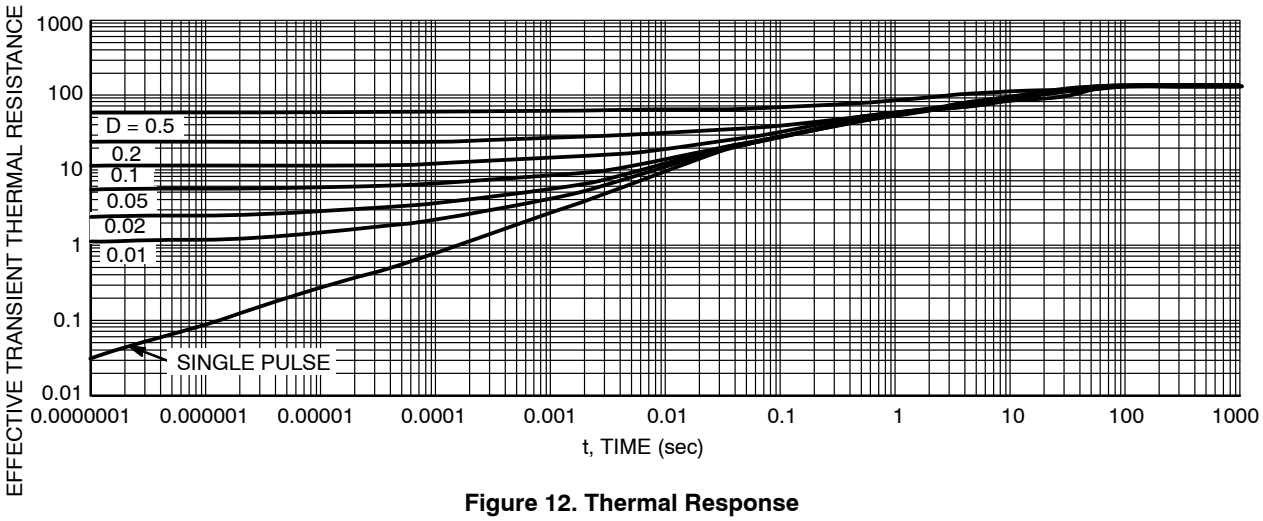
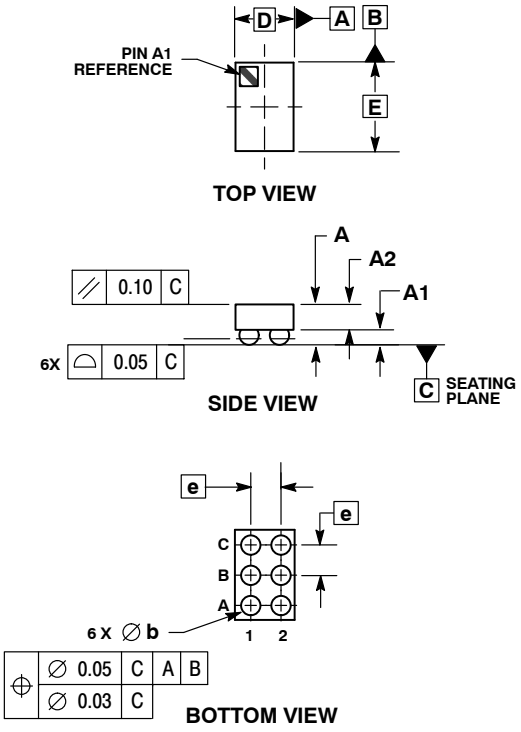


Figure 12. Thermal Response

PACKAGE DIMENSIONS

6 PIN FLIP−CHIP, 1.0x1.5
CASE 499BC
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.64
A1	0.22	0.28
A2	0.34	0.36
b	0.29	0.34
D	0.92	1.00
E	1.42	1.50
e	0.50 BSC	

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