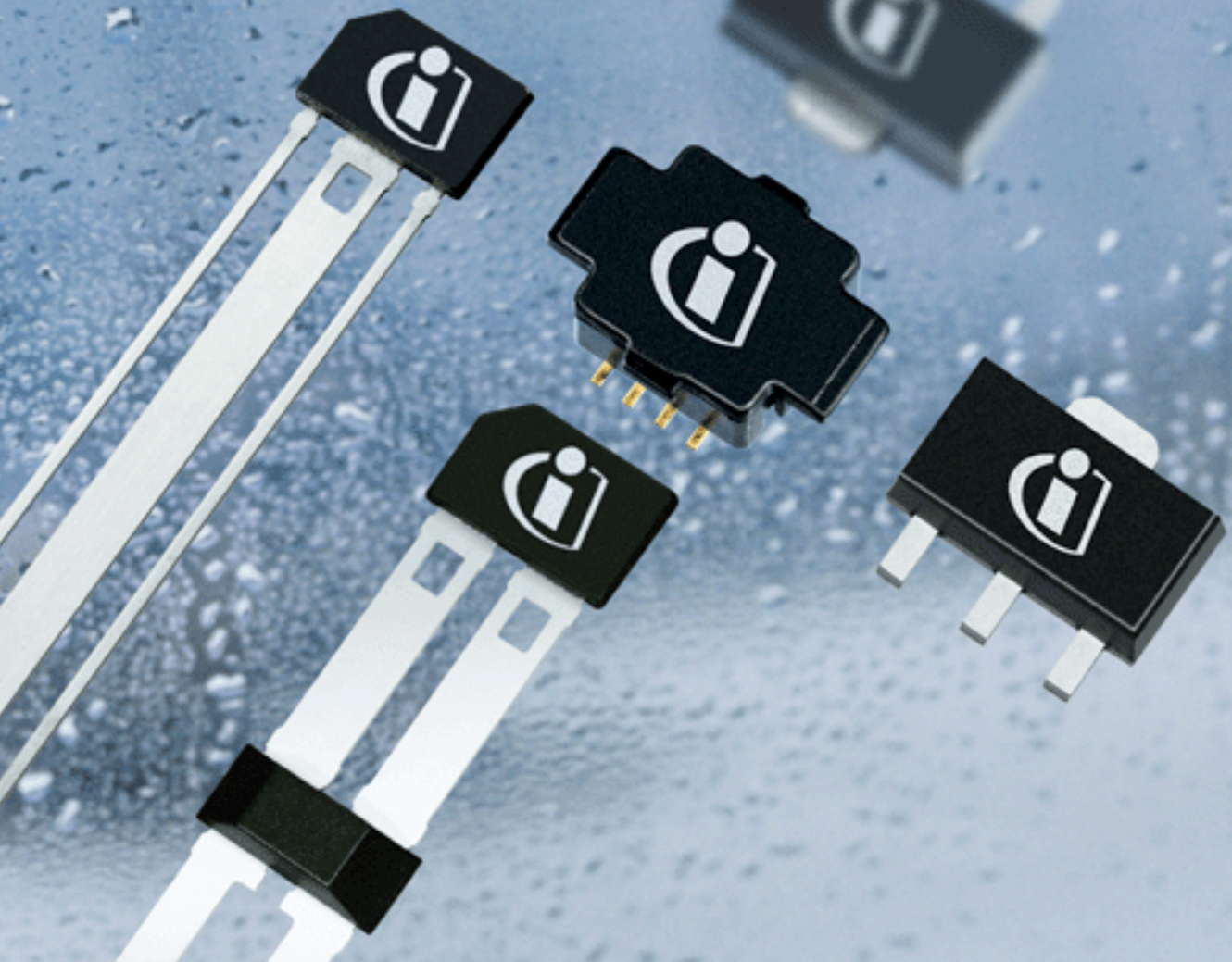


# TLE4997I

Programmable Linear Hall Sensor  
for Industrial Use



Sensors



Never stop thinking.

**Edition 2007-06**

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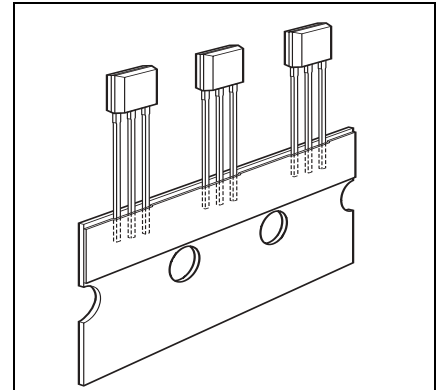
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## 1 Overview

### 1.1 Features

- High linear and ratiometric push-pull rail-to-rail output signal
- 20-bit Digital Signal Processing
- Digital temperature compensation
- 12-bit overall resolution
- Operates from -40°C up to 120°C
- Low drift of output signal over temperature and lifetime
- Programmable parameters stored in redundant EEPROM (single bit error correction):
  - magnetic range and magnetic sensitivity (gain)
  - zero field voltage (offset)
  - bandwidth
  - polarity of the output slope
  - clamping option
  - temperature coefficient for all common magnets
  - memory lock
- Re-programmable until memory lock
- Single supply voltage 4.5 - 5.5 V (4 - 7 V in extended range)
- Continuous measurement ranges between -200 mT and +200 mT
- Slim 3-pin package (Green)
- Reverse polarity and overvoltage protection for all pins
- Output short circuit protection
- On-board diagnostics (wire breakage detection, undervoltage, overvoltage)
- Digital readout of internal temperature and magnetic field values in calibration mode.
- Individual programming and operation of multiple sensors with common power supply
- Two-point calibration of magnetic transfer function
- Precise calibration without iteration steps
- High immunity against mechanical stress, EMC, ESD



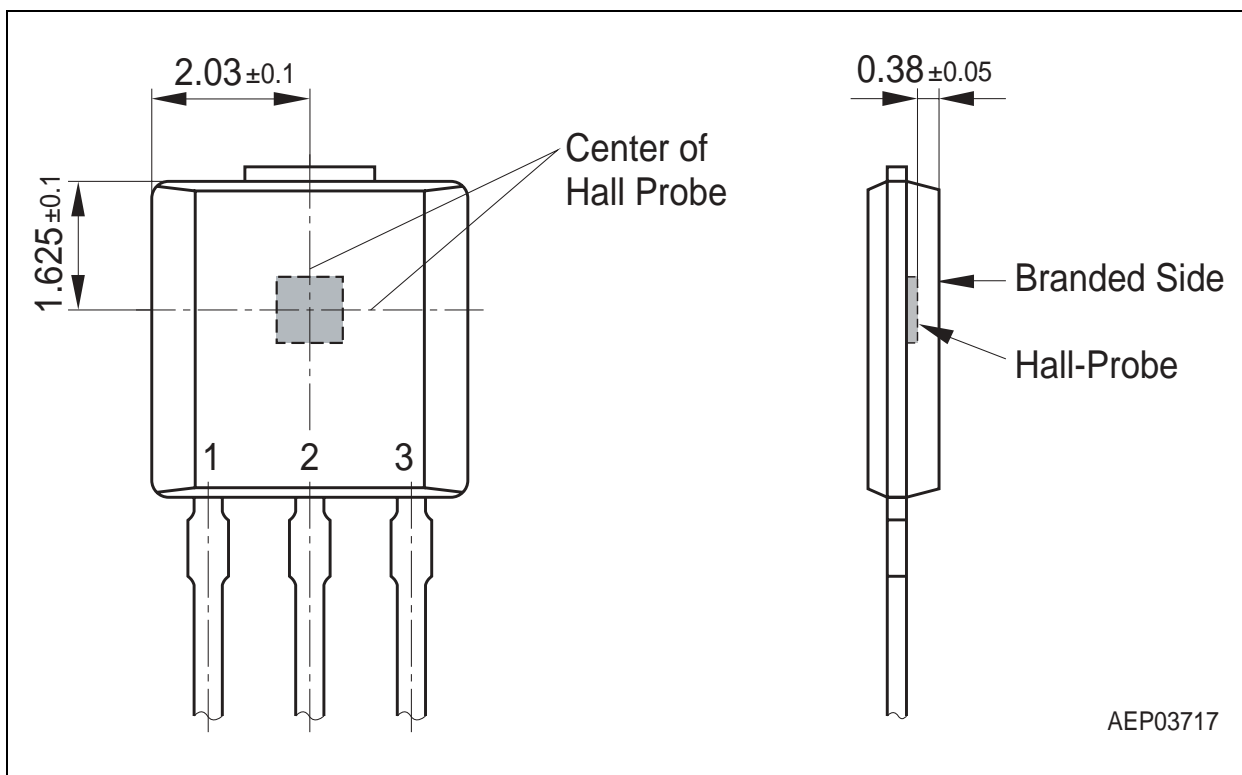
Type	Marking	Ordering Code	Package
TLE4997I	4997I2	SP000248475	PG-SSO-3-10

## 1.2 Target Applications

- Robust replacement of potentiometers
  - No mechanical abrasion
  - Resistant to humidity, temperature, pollution and vibration
- Linear and angular position sensing
- High current sensing

## 1.3 Pin Configuration

**Figure 1** shows the location of the Hall element in the chip and the distance between the Hall probe and the surface of the package.



**Figure 1 Pin Configuration and Hall Cell Location**

**Table 1 Pin Definitions and Functions**

Pin No.	Symbol	Function
1	$V_{DD}$	Supply voltage / programming interface
2	$GND$	Ground
3	$OUT$	Output voltage / programming interface



## 2 General

### 2.1 Block Diagram

Figure 2 shows a simplified block diagram.

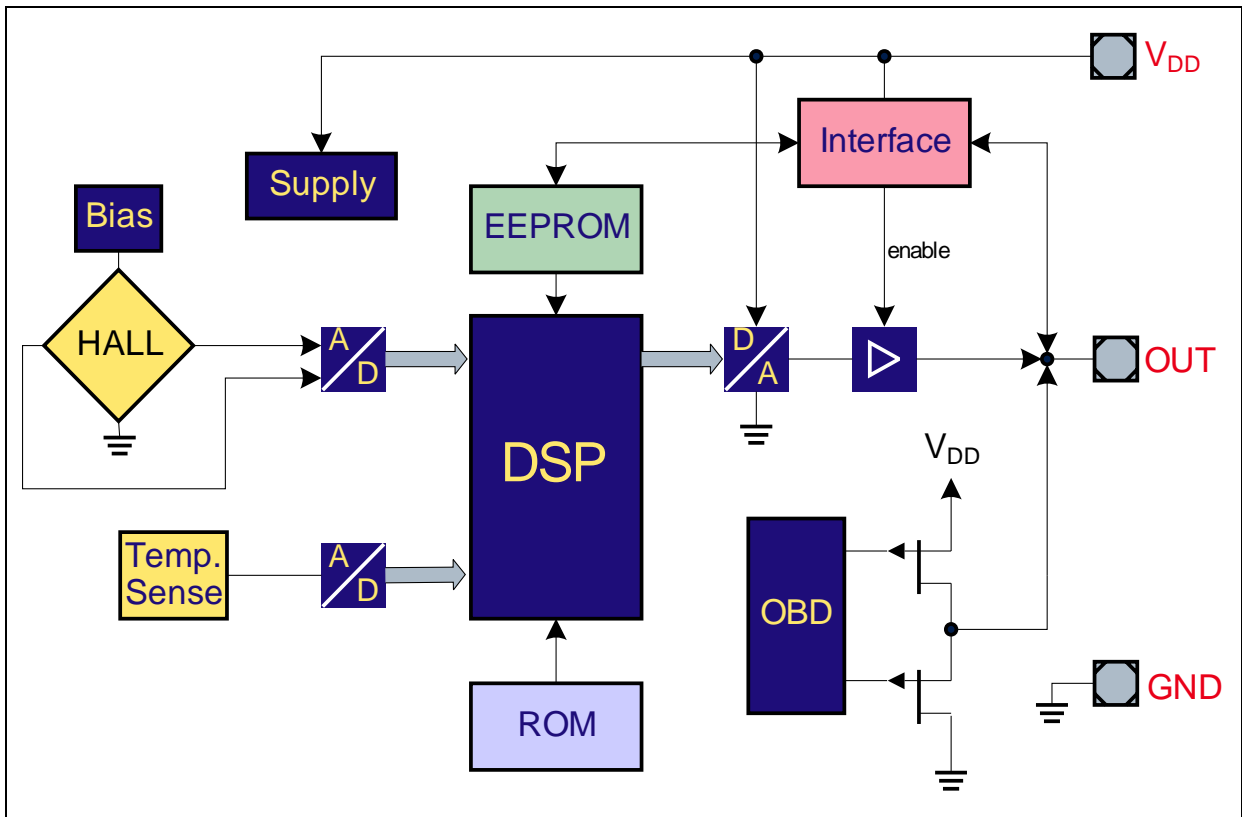


Figure 2 Block Diagram

### 2.2 Functional Description

The linear Hall IC TLE4997I has been designed specifically to meet the demands of highly accurate rotation and position detection, as well as for current measurement applications.

The sensor provides a ratiometric analog output voltage, which is ideally suited to Analog-to-Digital (A/D) conversion with the supply voltage as a reference.

The IC is produced in BiCMOS technology with high voltage capability and also provides reverse polarity protection.

Digital signal processing using a 16-bit DSP architecture and digital temperature compensation guarantees excellent stability over a long period of time.

The minimum overall resolution is 12 bits. Nevertheless, some internal stages work with resolutions up to 20 bits.

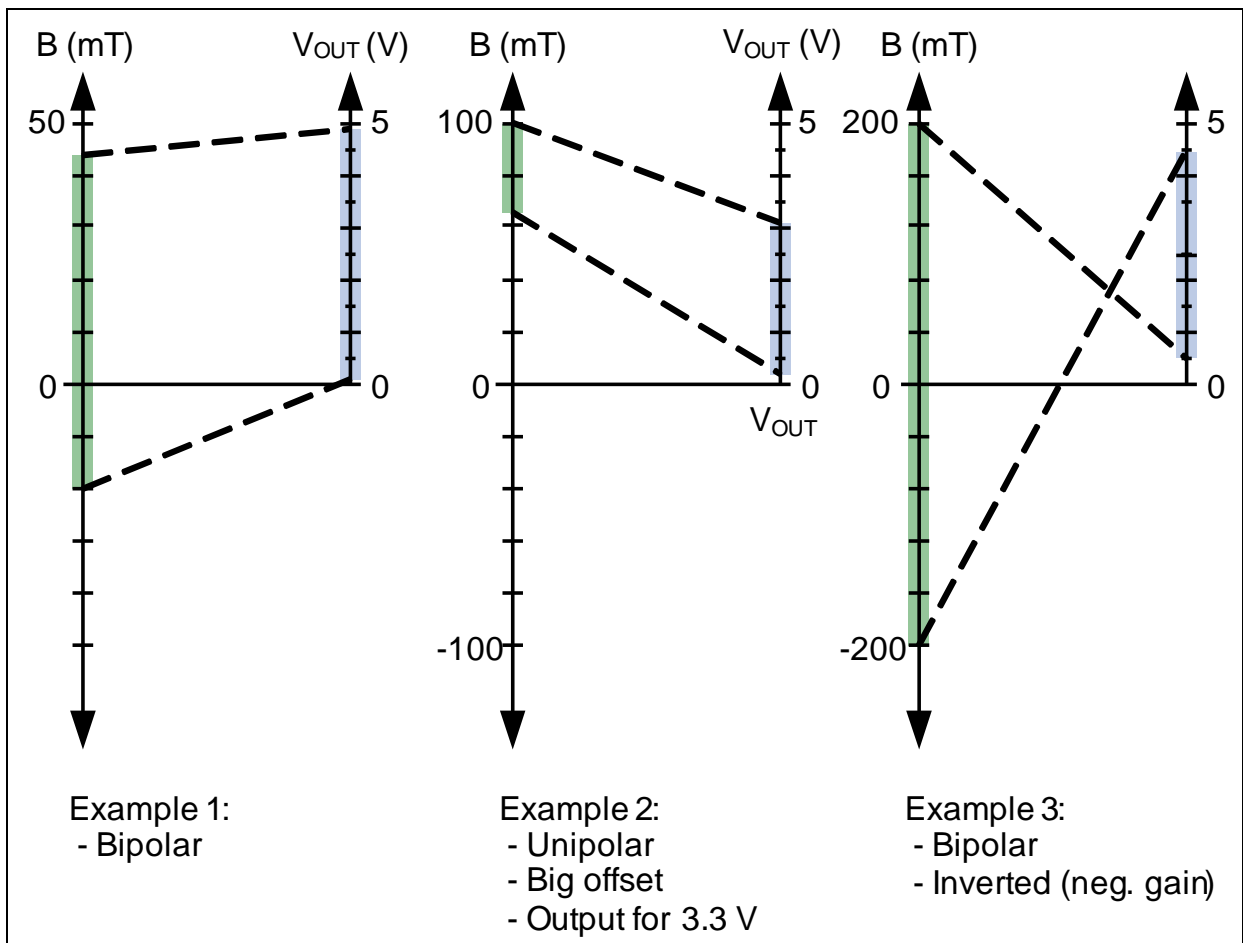
## 2.3 Principle of Operation

- A magnetic flux is measured by a Hall-Effect cell.
- The output signal from the Hall-Effect cell is converted from Analog to Digital signals.
- The chopped Hall-effect cell and continuous-time A to D conversion provide very low and stable magnetic offset.
- A programmable Low-Pass filter reduces the noise.
- The temperature is measured and A to D converted.
- Temperature compensation is processed digitally using a second order function.
- Digital processing of output voltage is based on zero field and sensitivity value.
- The output voltage range can be clamped by digital limiters.
- The final output value is D to A converted.
- The output voltage is proportional to the supply voltage (ratiometric DAC).
- An On-Board-Diagnostics (OBD) circuit connects the output to  $V_{DD}$  or GND in case of errors.

## 2.4 Transfer Functions

The examples in **Figure 3** show how easily different magnetic field ranges can be mapped to the output voltage.

- Polarity Mode:
  - **Unipolar:** Only North- or South-oriented magnetic fields are measured.
  - **Bipolar:** Magnetic fields can be measured in both orientations. The limit points must not be symmetric to the zero field point.
- Inversion: The gain values can be set positive or negative.



**Figure 3** Examples of Operation

*Note: Due to the ratiometry, voltage drops at the  $V_{DD}$  line are imaged in the output signal.*

### 3 Maximum Ratings

**Table 2 Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	$T_{ST}$	-40	150	°C	1)
Junction temperature	$T_J$	-40	150	°C	1)
Voltage on $V_{DD}$ pins with respect to ground ( $V_{SS}$ )	$V_{DD}$	-16 <sup>2)</sup>	16 <sup>3)</sup>	V	$R_{THja} \leq 150$ K/W
Supply current @ overvoltage	$I_{DDov}$	-	52	mA	
Supply current @ reverse voltage	$I_{DDrev}$	- 75	-	mA	
Voltage on output pin with respect to ground ( $V_{SS}$ )	$V_{OUTov}$	-16 <sup>4)</sup>	16 <sup>3)</sup>	V	$R_{THja} \leq 150$ K/W $V_{out}$ may be $> V_{DD}$
Magnetic field	$B_{MAX}$	-	unlimited	T	
ESD protection	$V_{ESD}$	-	2.0	kV	According HBM JESD22-A114-B <sup>5)</sup>

1) For limited time only. Depends on customer temperature lifetime cycles. Please ask for support by Infineon.

2) max 24 h @  $-40^{\circ}\text{C} \leq T_J < 30^{\circ}\text{C}$   
max 10 min. @  $30^{\circ}\text{C} \leq T_J < 80^{\circ}\text{C}$   
max 30 sec. @  $80^{\circ}\text{C} \leq T_J < 120^{\circ}\text{C}$

3) max. 24 h @  $T_J < 80^{\circ}\text{C}$ .

4) Max. 1 ms @  $T_J < 30^{\circ}\text{C}$ ; -8.5 V for 100 h @  $T_J < 80^{\circ}\text{C}$ .

5) 100 pF and 1.5 k $\Omega$

*Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Furthermore, only single error cases are assumed. More than one stress/error case may also damage the device.*

*Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ( $V_{IN} > V_{DD}$  or  $V_{IN} < V_{SS}$ ) the voltage on  $V_{DD}$  pins with respect to ground ( $V_{SS}$ ) must not exceed the values defined by the absolute maximum ratings.*

## 4 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE4997I. All parameters specified in the following sections of this document refer to these operating conditions, unless otherwise indicated.

**Table 3 Operating Range**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	$V_{DD}$	4.5	5.5	V	
		4	7	V	Extended range <sup>1)</sup>
Load resistance	$R_L$	10	-	k $\Omega$	Pull-down to GND Pull-up to $V_{DD}$
		50	-		
Load capacitance	$C_L$	0	210	nF	
Junction temperature <sup>2)</sup>	$T_J$	-40	120	$^{\circ}\text{C}$	For 5000 h

<sup>1)</sup> For reduced output accuracy.

<sup>2)</sup>  $R_{THja} \leq 150 \text{ K/W}$ .

*Note: Keeping signal levels within the limits specified in this table ensures operation without overload conditions*

## 5 Electrical and Magnetic Parameters

**Table 4 Electrical Characteristics**

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Output voltage range	$V_{OUT}$	5	-	95	% $V_{DD}$	
Supply current	$I_{DD}$	3	7.5	10	mA	Also in extended $V_{DD}$ range <sup>1)</sup> , $I_{OUT}=0mA$
Output current @ OUT shorted to supply lines	$I_{OUTsh}$	-30	-	30	mA	For operating supply voltage range only
Zero field voltage	$V_{ZERO}$	-100		100	%	Of $V_{DD}$ <sup>2)</sup>
Zero field voltage drift	$\Delta V_{ZERO}$	-0.5	-	0.5	% $V_{DD}$	In lifetime <sup>3)</sup>
		-0.5	-	0.5	% $V_{DD}$	Over temperature <sup>3)</sup>
Ratiometry error	$E_{RAT}$	-0.25	-	+0.25	%	Of $V_{DD}$ <sup>4)5)</sup>
Thermal resistance	$R_{thJA}$	-	-	219	K/W	Junction to air
	$R_{thJC}$	-	-	47	K/W	Junction to case
Power on time	$t_{Pon}$	-	-	1	ms	$\Delta V_{OUT} \leq \pm 5\%$ of $V_{DD}$ $\Delta V_{OUT} \leq \pm 1\%$ of $V_{DD}$
		-	-	10		
Power On Reset level	$V_{DDpon}$	2	-	4	V	
Output DAC quantization	$\Delta V_{OUT}$	1.22			mV	@ $V_{DD} = 5V$
Output DAC resolution	-	12			bit	
Output DAC bandwidth	$f_{DAC}$	-	3.2	-	kHz	Interpolation filter <sup>6)</sup>
Output noise	$V_{noise}$	-	-	4.68	mV <sub>pp</sub>	5% exceeded <sup>7)8)</sup>
Differential non-linearity	$DNL$	-1	-	1	LSB	Of output DAC
Signal delay	$t_{DS}$	-	-	250	$\mu s$	@ 100 Hz <sup>9)</sup>

1) For  $V_{OUT}$  within the range of 5%... 95% of  $V_{DD}$

2) Programmable in steps of 1.22 mV ( @  $V_{DD} = 5V$  ).

3) For small sensitivity settings. For higher sensitivities, the magnetic offset drift is dominant. This means that, for an example with a calibrated 60mV/mT sensitivity, the typical output drift might be given due to the allowed magnetic offset tolerance up to  $\pm 0.5 mT \times 60 mV/mT = \pm 30 mV$  @ 5 V  $V_{DD}$ .

4) For  $4.5 V \leq V_{DD} \leq 5.5 V$  and within nominal  $V_{OUT}$  range; see **“Ratiometry” on Page 15** for details on  $E_{RAT}$ .

5) For the maximum error in the extended voltage range, see **“Ratiometry” on Page 15**.

6) More information, see **“DAC Input Interpolation Filter” on Page 22**.

7) 100 mT range, sensitivity 60 mV/mT, LP-filter 244 Hz, 160 Hz external RC low pass filter as application circuit.

8) '5% exceeded' means that 5 of 100 continuously measured  $V_{OUT}$  samples are out of limit.

9) A sinusoidal magnetic field is applied,  $V_{OUT}$  shows amplitude of 20% of  $V_{DD}$ , no LP filter is selected.

### Ratiometry

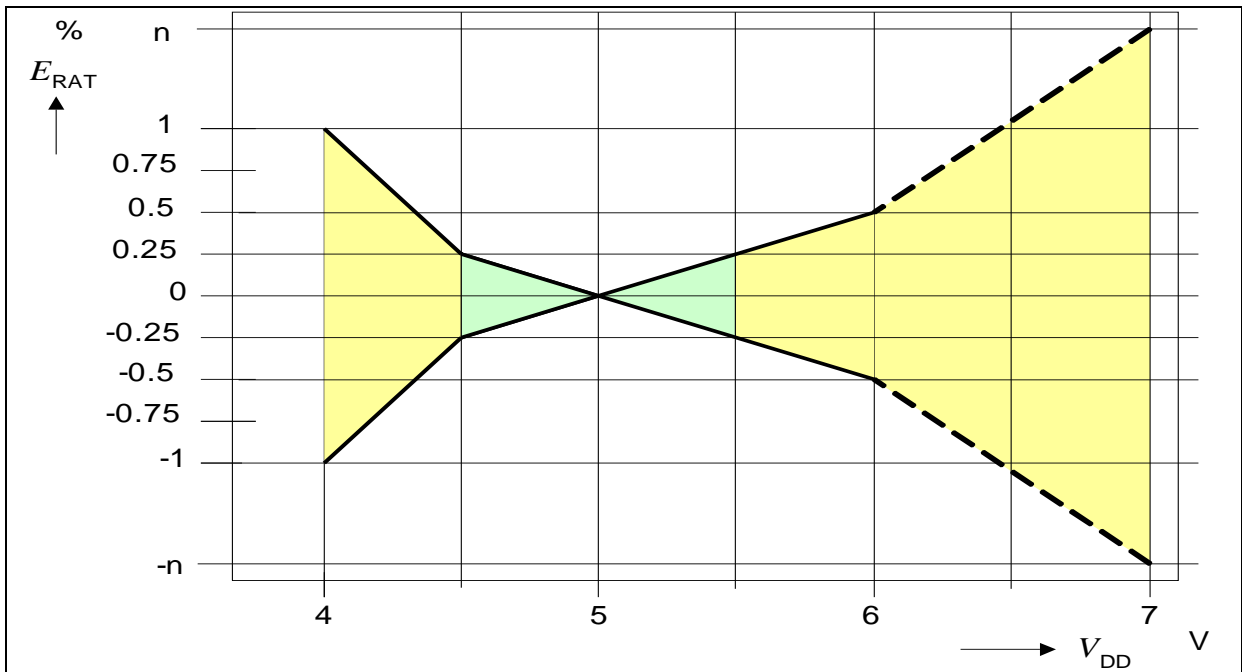
The linear Hall sensor works like a potentiometer. The output voltage is proportional to the supply voltage. The division factor depends on the magnetic field strength. This behavior is called “ratiometric”.

The supply voltage  $V_{DD}$  should be used as the reference for the A/D Converter of the microcontroller. In this case, variations of  $V_{DD}$  are compensated.

The ratiometry error is defined as follows:

$$E_{RAT} = \left( \frac{V_{OUT}(V_{DD})}{V_{DD}} - \frac{V_{OUT}(5V)}{5V} \right) \times 100 \%$$

The ratiometry error band displays as a “Butterfly Curve”.



**Figure 4 Ratiometry Error Band**

The error band in the extended  $V_{DD}$  range below 4.5 V and above 5.5 V is defined as shown in [Figure 4](#). In the range from 6 to 7 Volts, the error band depends on the output signal. For  $V_{OUT}$  lower than 20% of  $V_{DD}$ , the value for  $n$  is 2%. For  $V_{OUT}$  higher than 80% of  $V_{DD}$ , the value for  $n$  is 5%. And if  $V_{OUT}$  is kept (clamped) in between, the value for  $n$  is 1%.

*Note: Take care of possible voltage drops on the  $V_{DD}$  and  $V_{OUT}$  line degrading the result. Ideally, both values are acquired and their ratio is calculated to gain the highest accuracy. This method should be used especially during calibration.*

**Electrical and Magnetic Parameters**
**Calculation of the Junction Temperature**

The total power dissipation  $P_{TOT}$  of the chip increases its temperature above the ambient temperature.

The power multiplied with the total thermal resistance  $R_{thJA}$  (Junction to Ambient) leads to the final junction temperature.  $R_{thJA}$  is the sum of the addition of the values of the two components *Junction to Case* and *Case to Ambient*.

$$R_{thJA} = R_{thJC} + R_{thCA}$$

$$T_J = T_A + \Delta T$$

$$\Delta T = R_{thJA} \times P_{TOT} = R_{thJA} \times (V_{DD} \times I_{DD} + V_{OUT} \times I_{OUT}) \quad I_{DD}, I_{OUT} > 0, \text{ if direction is into IC}$$

Example (assuming no noticeable load on  $V_{out}$ ):

- $V_{DD} = 5 \text{ V}$
- $I_{DD} = 10 \text{ mA}$
- $\Delta T = 219 \text{ [K/W]} \times (5 \text{ [V]} \times 0.01 \text{ [A]} + 0 \text{ [VA]}) = 11 \text{ K}$

For moulded sensors, the calculation with  $R_{thJC}$  is more adequate.

**Magnetic Parameters**
**Table 5 Magnetic Characteristics**

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Sensitivity	$S$	$\pm 12.5$	-	$\pm 300$	mV/mT	1) 2)
Magnetic field range	$MFR$	$\pm 50$	$\pm 100$ <sup>3)</sup>	$\pm 200$	mT	Programmable <sup>4)</sup>
Integral nonlinearity	$Inl$	-15	-	15	mV	= $\pm 0.3\%$ of $V_{DD}$ <sup>5)</sup>
Magnetic offset	$B_{OS}$	-500	-	500	$\mu\text{T}$	6) 7) 8)
Magnetic offset drift	$\Delta B_{OS}$	- 5	-	5	$\mu\text{T} / ^\circ\text{C}$	Error band <sup>7)</sup>

1) Programmable in steps of 0.024%.

2) @  $V_{DD} = 5 \text{ V}$  and  $T_J = 25^\circ\text{C}$

3) This range is also used for temperature and offset pre-calibration of the IC.

4) Depending on the Offset and Gain settings, the output may saturate at lower fields.

5)  $Inl = V_{out} - V_{out,lse}$  with  $V_{out,lse}$  = least square error fit of  $V_{out}$ .  
Valid in the range  $(5\% \text{ of } V_{DD}) < V_{OUT} < (95\% \text{ of } V_{DD})$

6) In operating temperature range. More information, see **“Operating Range” on Page 13**.

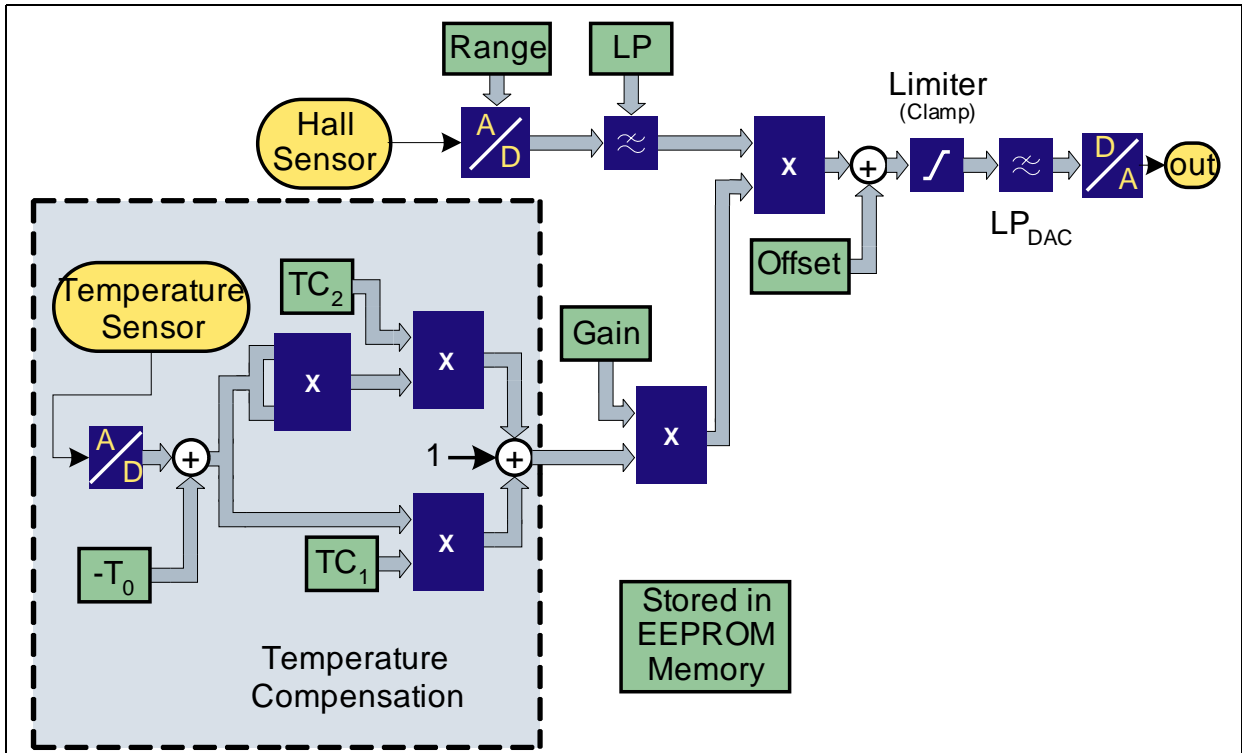
7) For Sensitivity  $S > 25 \text{ mV} / \text{mT}$ . For lower sensitivities, the zero field voltage drift is dominant.

8) Measured at  $\pm 100 \text{ mT}$  range.



## 6 Signal Processing

The flow diagram in **Figure 5** shows the data processing algorithm.



**Figure 5** Signal Processing Flow

### Magnetic Field Path

- The analog output signal of the chopped Hall cell is converted in the continuous-time A/D Converter. The range of the chopped A/D Converter can be set in several steps (see **Table 6**). This assures a suitable level for the A/D Converter.
- After the A/D conversion, a digital low pass filter reduces the bandwidth (**Table 10**).
- A multiplier amplifies the value according to the gain setting (see **Table 8**) plus temperature compensation.
- The offset value is added (see **Table 9**).
- A limiter reduces the resulting signal to 12 bits and feeds the D/A converter.

### Temperature Compensation

(Details are listed in **Chapter 8**)

- The output signal of the temperature cell is also A/D converted.
- The temperature is normalized by subtraction of the  $T_0$  value (zero point of the quadratic function).
- The linear path is multiplied with the  $TC_1$  value.

**Signal Processing**

- In the quadratic path, the difference temperature is squared and multiplied with the  $TC_2$  value.
- Both path outputs are added together and multiplied with the gain value from the EEPROM.

### 6.1 Magnetic Field Ranges

The working range of the magnetic field defines the input range of the A/D Converter. It is always symmetric to the zero field point. Any two points in the magnetic range can be selected to be the end points of the output curve. The output voltage represents the range between the two points.

In the case of fields higher than the range values, the output signal may be distorted. The range must be set before the calibration of offset and gain.

**Table 6 Range Setting**

Range	Range in mT	Parameter R
Low	$\pm 50$	3
Mid	$\pm 100$	1
High	$\pm 200$	0

**Table 7 Range**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Register size	<i>R</i>	2		bit	<sup>1)</sup>

<sup>1)</sup> Ranges do not have a guaranteed absolute accuracy. The temperature pre-calibration is performed in the mid range (100 mT).

## 6.2 Gain Setting

The sensitivity is defined by the range and the gain setting. The output of the A/D Converter is multiplied with the gain value.

**Table 8 Gain**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Register size	<i>G</i>	15		bit	Unsigned integer value
Gain range	<i>Gain</i>	- 4.0	3.9998	-	1)2)
Gain quantization steps	$\Delta Gain$	244.14		ppm	Corresponds to 1/4096

1) For gain values between - 0.5 and + 0.5, the numeric accuracy decreases.

To obtain a flatter output curve, it is recommended to select a higher range setting.

2) A gain value of +1.0 corresponds to a typical 40 mV/mT sensitivity (100 mT range, not guaranteed). It is crucial to do a final calibration of each IC within the application using the Gain/ $V_{OS}$  value.

The gain value can be calculated by

$$Gain = \frac{(G - 16384)}{4096}$$

## 6.3 Offset Setting

The offset voltage corresponds to an output voltage with zero field at the sensor.

**Table 9 Offset**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Register size	<i>OS</i>	15		bit	Unsigned integer value
Offset range	$V_{OS}$	-400	399	% $V_{DD}$	1)
Offset quantization steps	$\Delta V_{OS}$	1.22		mV	@ $V_{DD} = 5\text{ V}$ generally $V_{DD} / 4095$

1) It is crucial to do a final calibration of each IC within the application using the Gain/ $V_{OS}$  value.

The offset value can be calculated by:

$$V_{OS} = \frac{(OS - 16384)}{4096} \times V_{DD}$$

## 6.4 DSP Input Low Pass Filter

A digital Low Pass Filter is placed between the Hall A/D Converter and the DSP to reduce the noise level. The Low Pass filter has a constant DC amplification of 0 dB (this is exactly a gain of 1), which means that its setting has no influence on the internal Hall A/D Converter value.

The bandwidth can be set in 8 steps.

**Table 10 Low Pass Filter Setting**

Parameter LP	0	1	2	3	4	5	6	7
Cutoff Frequency in Hz (at 3dB attenuation) <sup>1)</sup>	78	244	421	615	826	1060	1320	off <sup>2)</sup>

1) As this is a digital filter running with an RC-based oscillator, the cutoff frequency may vary within  $\pm 30\%$ .

2) The output low pass-interpolation filter behavior remains as a main component in the signal path.

**Table 11 Range**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Register size	<i>LP</i>	3		bit	
Corner frequency variation	$\Delta f$	- 30	+ 30	%	

*Note: In Range 7 (filter off), the output noise increases. Because of higher DSP load, the current consumption also rises slightly.*

Signal Processing

Figure 6 shows the characteristic of the filter as a magnitude plot (the highest setting is marked). The “off” position would be a flat 0 dB line. In this case, the output decimation filter limits the bandwidth of the sensor. The update rate after the Low Pass filter is 16 kHz.

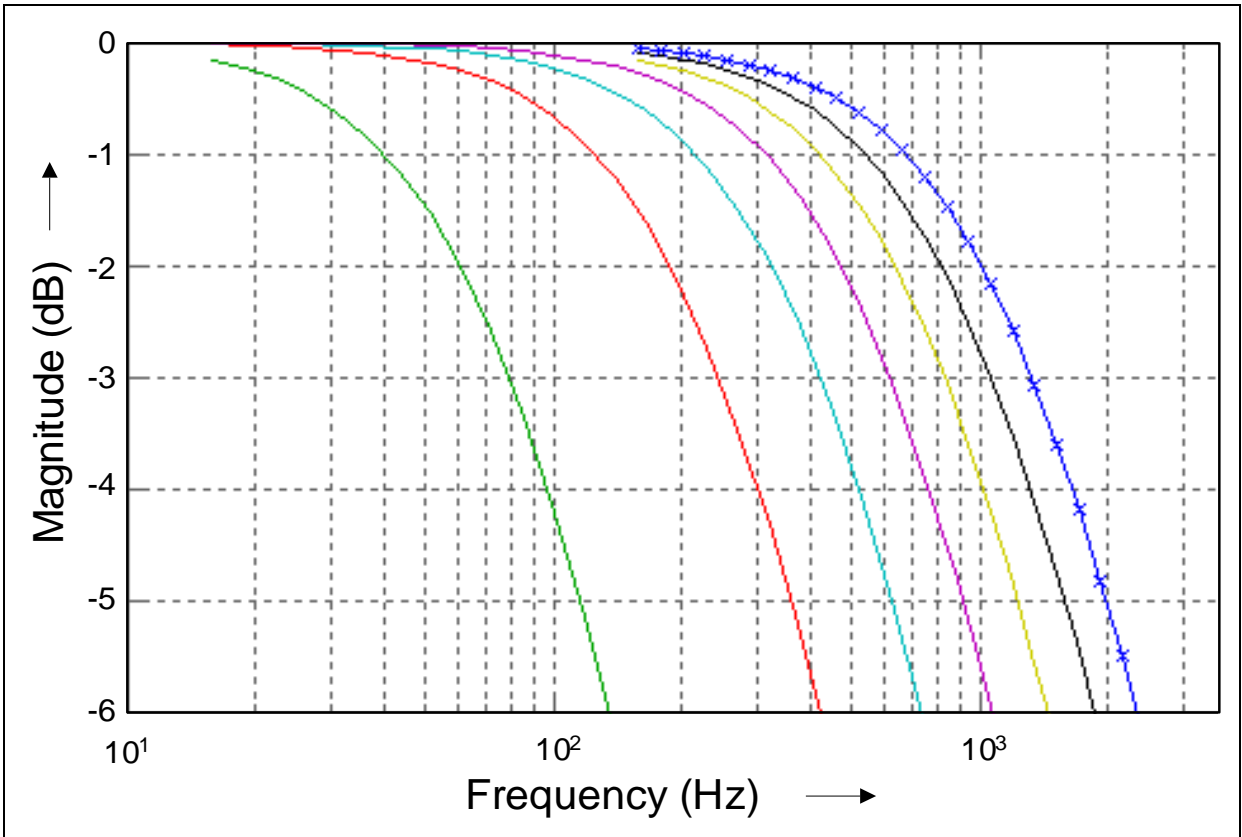
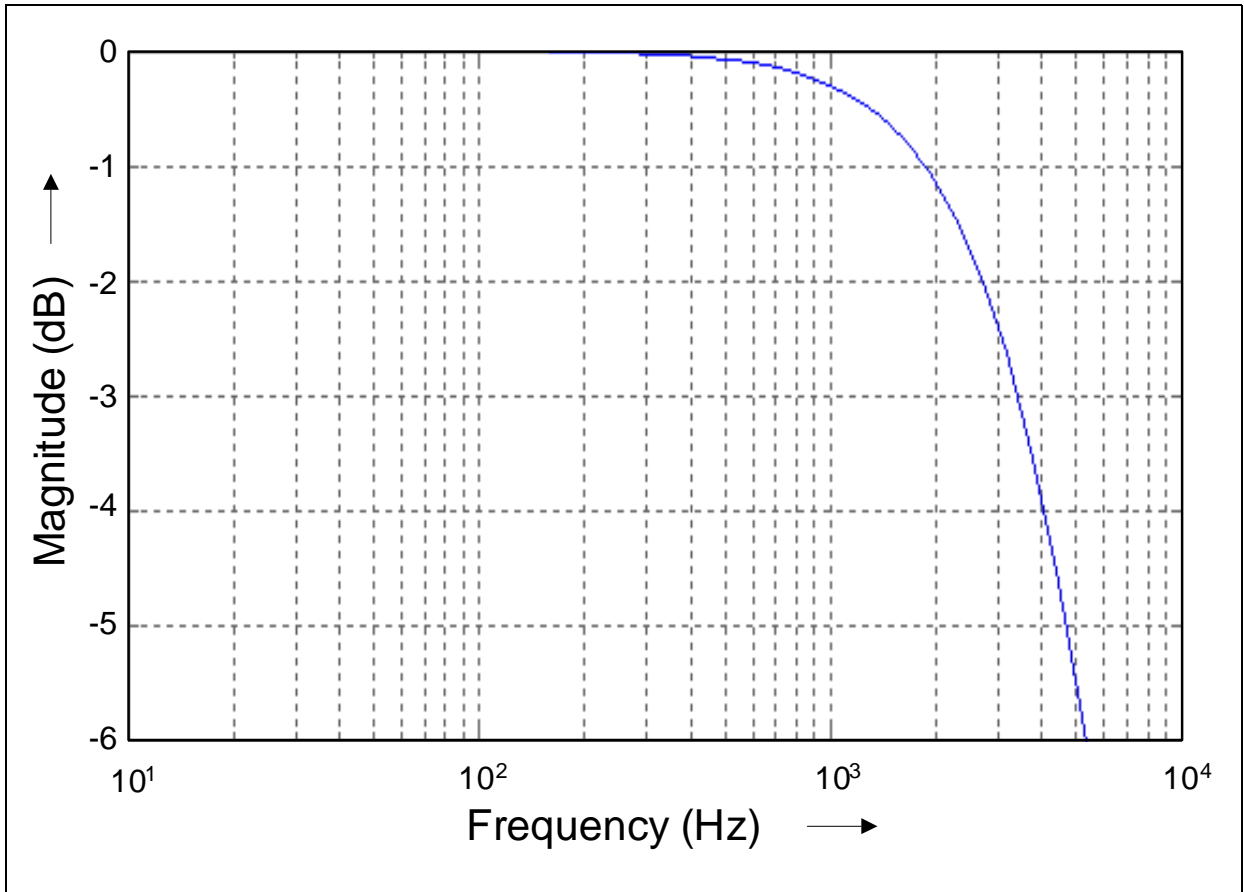


Figure 6 DSP Input Filter (Magnitude Plot)

### 6.5 DAC Input Interpolation Filter

An interpolation filter is placed between the DSP and the output DAC. It cannot be switched off. This filter limits the frequency behavior of the complete system if the DSP input filter is disabled. The update rate after the interpolation filter is 256 kHz.



**Figure 7 DAC Input Filter (Magnitude Plot)**

*Note: As this is a digital filter running with an RC-based oscillator, the cutoff frequency may vary within ±30%.*

## 6.6 Clamping

The clamping function is useful for splitting the output voltage into the operating range and error ranges. If the magnetic field is outside the selected measurement range, the output voltage  $V_{out}$  is limited to the clamping values.

**Table 12 Clamping**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Register size	$CL, CH$	2 x 12		bit	
Clamping voltage low	$V_{CLL}$	0	100	% $V_{DD}$	1)
Clamping voltage high	$V_{CLH}$	0	100	% $V_{DD}$	1)
Clamping quantization steps	$\Delta V_{CLQ}$	1.22		mV	@ $V_{DD} = 5\text{ V}$
Clamping voltage drift	$\Delta V_{CL}$	-0.5	0.5	% $V_{DD}$	In lifetime <sup>2)</sup>
		-0.5	0.5		Over temperature <sup>2)</sup>

1) If clamping is set, it must be within the allowed output voltage range to be effective.

2) Valid in the range (5% of  $V_{DD}$ ) <  $V_{OUT}$  < (95% of  $V_{DD}$ )

The clamping values are calculated by:

Clamping low voltage:

$$V_{CLL} = \frac{CL}{4096} \times V_{DD}$$

Clamping high voltage:

$$V_{CLH} = \frac{CH}{4096} \times V_{DD}$$

*Note: For an exact setup, the register value may be re-adjusted due to the actual output voltage in the clamping condition. The output voltage range itself has electrical limits. See the [Electrical Characteristics](#) of  $V_{out}$ .*

Figure 8 shows an example in which the magnetic field range between  $B_{\min}$  and  $B_{\max}$  is mapped to voltages between 0.8 V and 4.2 V.

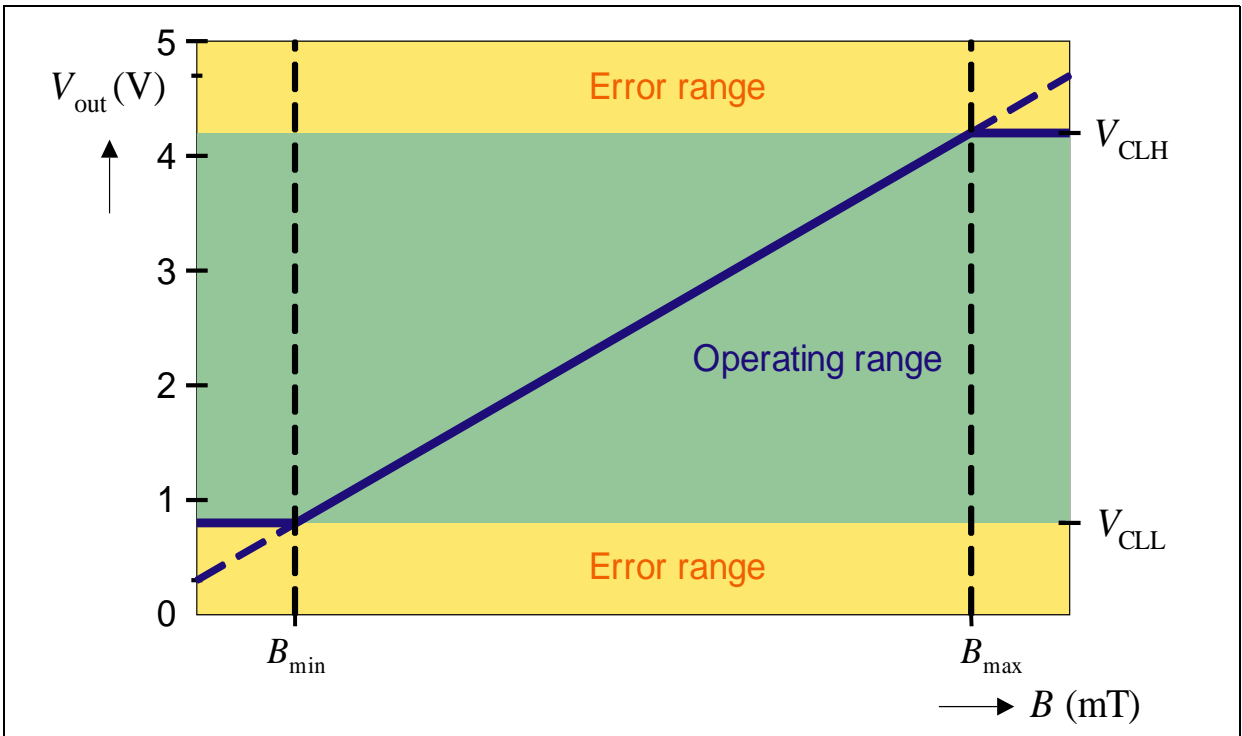


Figure 8 Clamping Example

Note: The high value must be above the low value.



## 7 Error Detection

Different error cases can be detected by the On-Board-Diagnostics (OBD) and reported to the microcontroller. The OBD is useful only when the clamping function is enabled. It is important to set the clamping threshold values inside the error voltage values shown in [Table 13](#) and [Table 14](#) to ensure that it is possible to distinguish between correct output voltages and error signals.

### 7.1 Voltages Outside the Operating Range

The output signals error conditions, if  $V_{DD}$  lies

- inside the ratings specified in [Table 2 "Absolute Maximum Ratings" on Page 12](#)
- outside the range specified in [Table 3 "Operating Range" on Page 13](#).

**Table 13 Undervoltage and Overvoltage**

( $R_{LOAD} \geq 10k$  pull down or  $50k$  pull up)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Undervoltage threshold	$V_{DDuv}$	3	4	V	
Overvoltage threshold	$V_{DDov}$	7	8.3	V	
Output voltage @ overvoltage	$V_{OUTov}$	$0.96 \times V_{DD}$	-	V	$V_{DDov} < V_{DD} \leq 16 \text{ V}$
Supply current <sup>1)</sup>	$I_{DDuv}$	-	10	mA	@ undervoltage

<sup>1)</sup> For overvoltage and reverse voltage, see [Table 2 "Absolute Maximum Ratings" on Page 12](#).

### 7.2 Open Circuit of Supply Lines

In the case of interrupted supply lines, the data acquisition device can alert the user.

**Table 14 Open Circuit (OBD Parameters) <sup>1)</sup>**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Output voltage @ open $V_{DD}$ line	$V_{OUT}$	0	0.2	V	
Output voltage @ open $V_{SS}$ line	$V_{OUT}$	4.8	5	V	

<sup>1)</sup> With  $V_{DD} = 5 \text{ V}$  and  $R_L \geq 10 \text{ k}\Omega$  pull-down or  $R_L \geq 50 \text{ k}\Omega$  pull-up.

### 7.3 Not Correctable EEPROM Errors

The parity method is able to correct one single bit in one EEPROM line. One other single bit error in another line can also be detected. As this situation is not correctable, this status is signalled at the output pin by clamping the output value to  $V_{DD}$ .

**Table 15 EEPROM Error Signalling**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Output voltage @ EEPROM error	$V_{OUT}$	$0.96 \times V_{DD}$	$V_{DD}$	V	

## 8 Temperature Compensation

The magnetic field strength of a magnet depends on the temperature. This material constant is specific to different magnet types. Therefore, the TLE4997I offers a second order temperature compensation polynomial, by which the Hall signal output is multiplied in the DSP.

There are three parameters for the compensation:

- Reference temperature  $T_0$
- A linear part (1<sup>st</sup> order)  $TC_1$
- A quadratic part (2<sup>nd</sup> order)  $TC_2$

The following formula describes the sensitivity dependent on the temperature in relation to the sensitivity at the reference temperature  $T_0$ :

$$S_{TC}(T) = 1 + TC_1 \times (T - T_0) + TC_2 \times (T - T_0)^2$$

For more information, see also the signal processing flow in [Figure 5](#).

The full temperature compensation of the complete system is done in three steps:

### 1. Pre-calibration in the Infineon final test.

The parameters  $TC_1$ ,  $TC_2$ ,  $T_0$  are set to maximally flat temperature characteristics regarding the Hall probe and internal analog processing parts in the 100 mT range.

### 2. Overall System calibration.

The typical coefficients  $TC_1$ ,  $TC_2$ ,  $T_0$  of the magnetic circuitry are programmed. This can be done deterministically, as the algorithm of the DSP is fully reproducible. The final settings of the  $TC_1$ ,  $TC_2$ ,  $T_0$  values are relative to the pre-calibrated values.

**Table 16 Temperature Compensation**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Register size $TC_1$	$TL$	-	9	bit	Unsigned integer values
1 <sup>st</sup> order coefficient $TC_1$	$TC_1$	-1000	2500	ppm/ °C	
Quantization steps of $TC_1$	$\Delta TC_1$	15.26		ppm/ °C	
Register size $TC_2$	$TQ$	-	8	bit	Unsigned integer values
2 <sup>nd</sup> order coefficient $TC_2$	$TC_2$	- 4	4	ppm/ °C <sup>2</sup>	
Quantization steps of $TC_2$	$\Delta TC_2$	0.119		ppm/ °C <sup>2</sup>	
Register size $T_0$	$TR$	-	3	bit	Unsigned integer values
Reference temperature	$T_0$	- 48	64	°C	
Quantization steps of $T_0$	$\Delta T_0$	16		°C	1)

1) A quantization step of 1°C is handled by algorithm (See Application Note).

## 8.1 Parameter Calculation

The parameters  $TC_1$ ,  $TC_2$  and  $T_0$  may be calculated by:

$$TC_1 = \frac{TL - 160}{65536} \times 1000000$$

$$TC_2 = \frac{TQ - 128}{8388608} \times 1000000$$

$$T_0 = 16TR - 48$$

Now the output  $V_{OUT}$  for a given field  $B_{IN}$  at a specific temperature can be roughly calculated by:

$$V_{OUT} = \left( \frac{B_{IN}}{B_{FSR}} \times S_{TC} \times S_{TCHall} \times S_O \times V_{DD} \right) + V_{OS}$$

$B_{FSR}$  is the full range magnetic field. It is dependent on the range setting (e.g 100 mT).

$S_O$  is the nominal sensitivity of the Hall probe times the Gain factor set in the EEPROM.

$S_{TC}$  is the temperature-dependent sensitivity factor calculated by the DSP.

$S_{TCHall}$  is the temperature behavior of the Hall probe.

The pre-calibration at Infineon is performed such that the following condition is met:

$$S_{TC}(T_J - T_0) \times S_{TCHall}(T_J) \approx 1$$

Within the application, an additional factor  $B_{IN}(T) / B_{IN}(T_0)$  will be given due to the magnetic system.  $S_{TC}$  needs now to be modified to  $S_{TCnew}$  so that the following condition is satisfied:

$$\frac{B_{IN}(T)}{B_{IN}(T_0)} \times S_{TCnew}(T) \times S_{TCHall}(T) \approx S_{TC}(T) \times S_{TCHall}(T) \approx 1$$

Therefore, the new sensitivity parameters  $S_{TCnew}$  can be calculated from the pre-calibrated setup  $S_{TC}$  using the relation:

$$\frac{B_{IN}(T)}{B_{IN}(T_0)} \times S_{TCnew}(T) \approx S_{TC}(T)$$

## 9 Calibration

A special hardware interface to an external computing system and measurement equipment is required for calibration of the sensor. All calibration and setup bits can be written into a random access memory (RAM). This allows the EEPROM to remain untouched during the entire calibration process. Therefore, this temporary setup (using the RAM only) does not stress the EEPROM—and even allows a pre-verification<sup>1)</sup> of the setup before programming—as the number of EEPROM programming cycles is limited to provide a high data endurance.

The digital signal processing is completely deterministic. This allows a two point calibration in one step without iterations. The two magnetic fields (here described as two “positions” of an external magnetic circuitry) need to be applied only once. Furthermore, a complete setup and calibration procedure can be performed requiring only one EEPROM programming cycle at the end<sup>2)</sup>.

After setting up the temperature coefficients, the calibrated Hall A/D Converter values of both positions need to be read and the sensor output signals (using a DAC test mode) need to be acquired for the corresponding end points. Using this data, the signal processing parameters can be immediately calculated with a program running on the external computing system.

**Note: The calibration and programming process must be performed only at the start of life of the device.**

**Table 17 Calibration Characteristics**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Temperature of sensor at 2 point calibration and programming	$t_{CAL}$	10	30	°C	
2 point calibration accuracy <sup>1)</sup>	$\Delta V_{CAL1}$	-0.5	0.5	% of VDD	In both positions

<sup>1)</sup> Setup and validation performed at start of life.

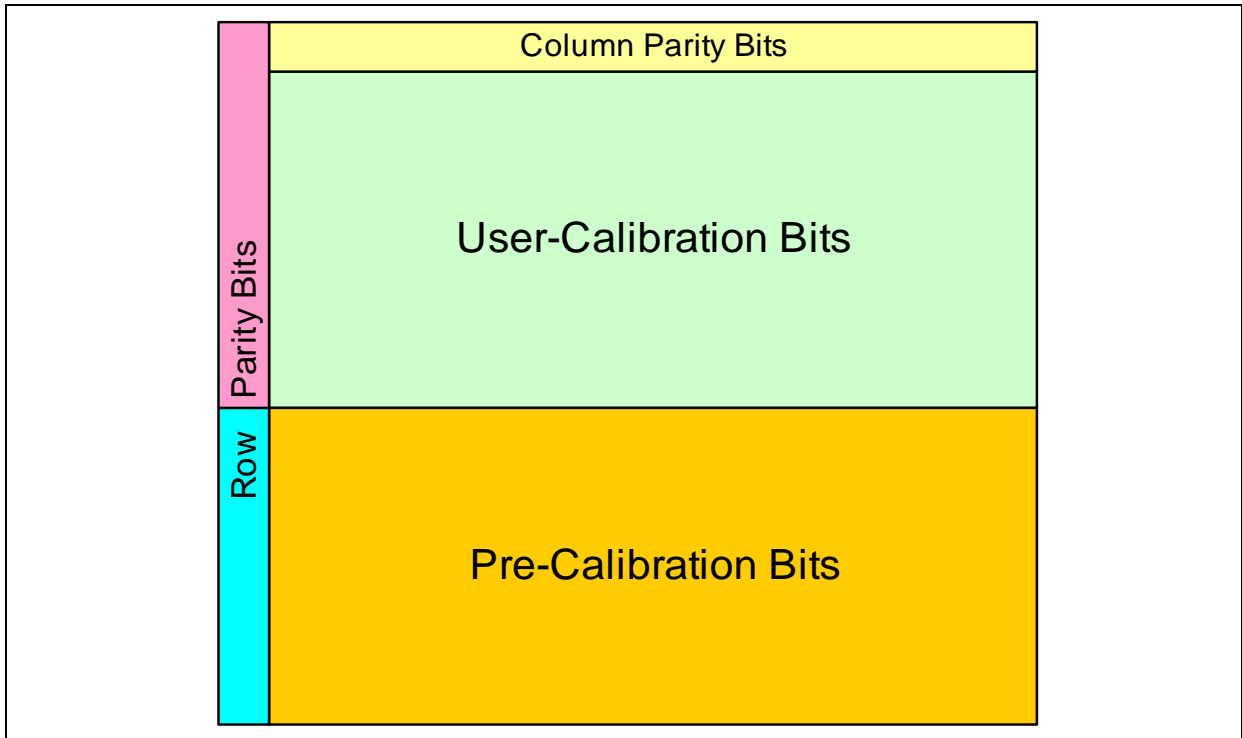
*Note: Depending on the application and external instrumentation setup, the accuracy of the 2 point calibration can be improved.*

<sup>1)</sup> This feature is not required for a deterministic two-point setup to fulfill the specification.

<sup>2)</sup> Details and basic algorithms for this step are available on request.

## 9.1 Calibration Data Memory

When the MEMLOCK bits are programmed (two redundant bits), the memory contents are frozen and may no longer be changed. Furthermore, the programming interface is locked out and the chip remains in Application Mode only. This prevents accidental programming due to environmental influences.



**Figure 9 EEPROM Map**

A matrix parity architecture allows the automatic correction of any single bit error. Each row is protected by a row parity bit. The sum of bits set including this bit must be an odd number (ODD PARITY). Each column is additionally protected by a column parity bit. The sum of all the bits in the even positions (0, 2, etc.) of all lines must be an even number (EVEN PARITY); the sum of all the bits in the odd positions (1,3, etc.) must be an odd number (ODD PARITY). This mechanism of different parity calculations protects against many block errors (such as erasing a full line or even the entire EEPROM).

When modifying the application bits (such as Gain, Offset, TC, etc.) the parity bits must be updated. For the column bits, the pre-calibration area must be also read out and considered for correct parity generation.

*Note: A specific programming algorithm must be followed to ensure the data retention. A separate detailed programming specification is available on request.*

**Table 18 Programming Characteristics**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Number of EEPROM programming cycles	$N_{PRG}$	-	8	Cycles 1)	Programming allowed only at start of lifetime
Ambient temperature at programming	$T_{PRG}$	10	30	°C	
Programming time	$t_{PRG}$	100	-	ms	For complete memory 2)
Calibration memory	-	135		Bit	All active EEPROM bits
Error correction	-	25		Bit	All parity EEPROM bits

1) 1 cycle is the simultaneous change of  $\geq 1$  bit. For experimental and evaluation purposes, the device may be programmed more often, but then data retention is no longer guaranteed.

2) Depends on the clock frequency at  $V_{DD}$ .

## 9.2 Programming Interface

The supply pin and the output pin are used as two-wire interface to transmit the EEPROM data to and from the sensor.

This allows

- communication with high data reliability
- bus-type connection of several sensors

In many applications, two sensors are used to measure the same parameter. This redundancy allows the operation to continue in an emergency mode. If both sensors use the same power supply lines, they can be programmed together in parallel.

The data transfer protocol and programming is described in a separate document. A laboratory evaluation programmer for programming of the evaluation samples and qualified samples is available on request.

## 10 Application Circuit

Figure 10 shows the connection of multiple sensors to a microcontroller.

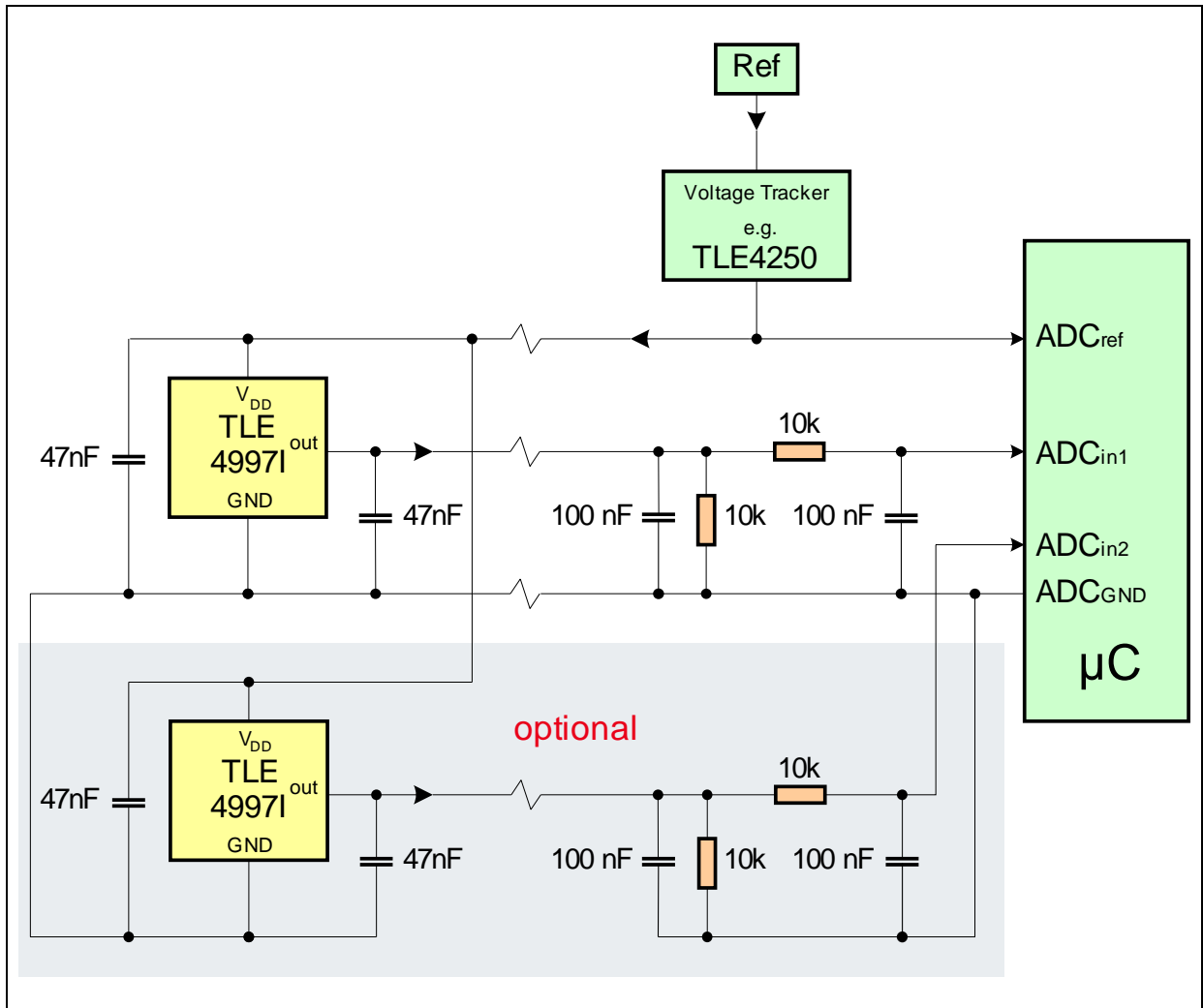


Figure 10 Application Circuit

Note: For calibration and programming, the interface must be connected directly to the output pin.

The given application circuit must be regarded as only an example. It needs to be adapted according to the requirements of the specific application.





## **12 Life Support Applications**

This product is not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Infineon Technologies AG customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify Infineon Technologies AG for any damages resulting from such improper use or sale.



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