Hi-performance Regulator IC Series for PCs

Main Power Supply IC for Note PC (Linear Regulator Integrated)

BD9524MUV

No.10030ECT06

●Description

BD9524MUV is a switching regulator controller with high output current which can achieve low output voltage (2.0V～5.5V) from a wide input voltage range (7V~25V). High efficiency for the switching regulator can be realized by utilizing an external N-MOSFET power transistor. A new technology called H^{3}Reg^{TM} is a Rohm proprietary control method to realize ultra high transient response against load change. SLLM (Simple Light Load Mode) technology is also integrated to improve efficiency in light load mode, providing high efficiency over a wide load range. For protection and ease of use, the soft start function, variable frequency function, short circuit protection function with timer latch, over voltage protection with timer latch, and Power good function are all built in. This switching regulator is specially designed for Main Power Supply.

●Features

1) 2ch H^{3}Reg^{TM} Switching Regulator Controller
2) Adjustable Simple Light Load Mode (SLLM), Quiet Light Load Mode (QLLM) and Forced continuous Mode
3) Thermal Shut Down (TSD), Under Voltage Lock Out (UVLO), Over Current Protection (OCP), Over Voltage Protection (OVP), Short circuit protection with timer-latch (SCP)
4) Soft start function to minimize rush current during startup
5) Switching Frequency Variable (f=200KHz～500KHz)
6) Power good circuit
7) 2ch Linear regulator
8) VQFN032V5050 package

●Applications

Laptop PC, Desktop PC, LCD-TV, Digital Components

●Maximum Absolute Ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Terminal voltage	VIN, CTL	30 *1*2	V
	EXTVCC, PGOOD1, PGOOD2FB1, FB2, Is+1, Is+2, MCTL	7 *1*2	V
	FS1, FS2, REF1, REF2, SS1, SS2, LG1, LG2	REG1+0.3 *1*2	V
	BOOT1, BOOT2	35 *1*2	V
	BOOT1-SW1, BOOT2-SW2, HG1-SW1, HG2-SW2	7 *1*2	V
	HG1	BOOT1+0.3 *1*2	V
	HG2	BOOT2+0.3 *1*2	V
	EN1, EN2	6 *1*2	V
	DGND, PGND1, PGND2	AGND±0.3 *1*2	V
Power dissipation 1	Pd1	0.38 *3	W
Power dissipation 2	Pd2	0.88 *4	W
Power dissipation 3	Pd3	2.06 *5	W
Power dissipation 4	Pd4	4.56 *6	W
Operating temperature range	Topr	-10 ~ +100	℃
Storage temperature range	Tstg	-55 ~ +150	℃
Junction Temperature	Tjmax	+150	℃

*1 Do not however exceed Pd.
*2 Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.
*3 Reduced by 3.0mW for each increase in Ta of 1℃ over 25℃ (when don't mounted on a heat radiation board)
*4 Reduced by 7.0mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm × 70mm × 1.6mm Glass-epoxy PCB which has 1 layer. (Copper foil area : 0mm^2))
*5 Reduced by 16.5mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm × 70mm × 1.6mm Glass-epoxy PCB which has 4 layers. (1st and 4th copper foil area : 20.2mm^2, 2nd and 3rd copper foil area : 5505mm^2))
*6 Reduced by 36.5mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm × 70mm × 1.6mm Glass-epoxy PCB which has 4 layers. (All copper foil area : 5505mm^2))

●Operating Conditions (Ta=25℃)

Parameter	Symbol	MIN.	MAX.	Unit
Terminal voltage	VIN	7	25	V
	EXTVCC	4.5	5.5	V
	CTL	-0.3	25	V
	EN1, EN2	-0.3	5.5	V
	BOOT1, BOOT2	4.5	30	V
	BOOT1-SW1, BOOT2-SW2, HG1-SW1, HG2-SW2	-0.3	5.5	V
	PGOOD1, PGOOD2	-0.3	5.5	V
	FS1, FS2	0.09	1.25	V
	REF1, REF2	1	2.75	V
	Is+1, Is+ 2, FB1, FB2	1.9	5.6	V
	MCTL	-0.3	REG1+0.3	V

*This product should not be used in a radioactive environment.

●Electrical characteristics

(unless otherwise noted, Ta=25℃ VIN=12V, CTL=5V, EN1=EN2=5V, REF1=2.5V, REF2=1.65V, FS1=FS2=0.582V)

Parameter	Symbol	Standard Value			Unit	Conditions
		MIN.	TYP.	MAX.		
VIN standby current	ISTB	70	150	250	μA	CTL=5V, EN1=EN2=0V
VIN bias current	IIN	0	45	130	μA	EXTVCC=5V
Shut down mode current	ISHD	-10	0	10	μA	CTL=0V
CTL Low voltage	VCTLL	-0.3	-	0.8	V	
CTL High voltage	VCTLH	2.3	-	25	V	
CTL bias current	ICTL	-	1	3	μA	VCTL=5V
EN Low voltage	VENL	-0.3	-	0.8	V	
EN High voltage	VENH	2.3	-	5.5	V	
EN bias current	IEN	-	1	3	μA	VEN=3V
[5V linear regulator]						
REG1 output voltage	VREG1	4.90	5.00	5.10	V	IREG1=1mA
Maximum current	IREG1	200	-	-	mA	IREG2=0mA
Line Regulation	REG1I	-	90	180	mV	VIN=7.5 to 25V
Load Regulation	REG1L	-	30	50	mV	IREG1=0 to 30mA
[3.3V linear regulator]						
REG2 output voltage	VREG2	3.27	3.30	3.33	V	IREG2=1mA
Maximum current	IREG2	100	-	-	mA	
Line regulation	REG2I	-	-	20	mV	VIN=7.5 to 25V
Load regulation	REG2L	-	-	30	mV	IREG2=0 to 100mA
[5V switch block]						
EXTVCC input threshold voltage	VCC_UVLO	4.2	4.4	4.6	V	EXTVCC: Sweep up
EXTVCC input delay time	TVCC	2	4	8	ms	
Switch Resistance	RVCC		1.0	2.0	Ω	
[Under voltage lock out block for DC/DC]						
REG1 threshold voltage	REG1_UVLO	4.0	4.2	4.4	V	REG1: Sweep up
REG2 threshold voltage	REG2_UVLO	2.45	2.65	2.85	V	REG2: Sweep up
Hysteresis voltage	dV_UVLO	50	100	200	mV	REG1, REG2: Sweep down
[Error amplifier block]						
Feedback voltage 1	VFB1	REF1×2 -25m	REF1×2	REF1×2 +25m	V	
FB1 bias current	IFB1	20	45	90	μA	FB1=5V
Output discharge resistance 1	RDISOUT1	0.5	1	3	kΩ	
Feedback voltage 2	VFB2	REF2×2 -25m	REF2×2	REF2×2 +25m	V	
FB2 bias current	IFB2	10	30	60	μA	FB2=3.3V
Output discharge resistance 2	RDISOUT2	0.5	1	3	kΩ	
REF1, REF2 bias current	IREF1, IREF2	-10	-	10	μA	

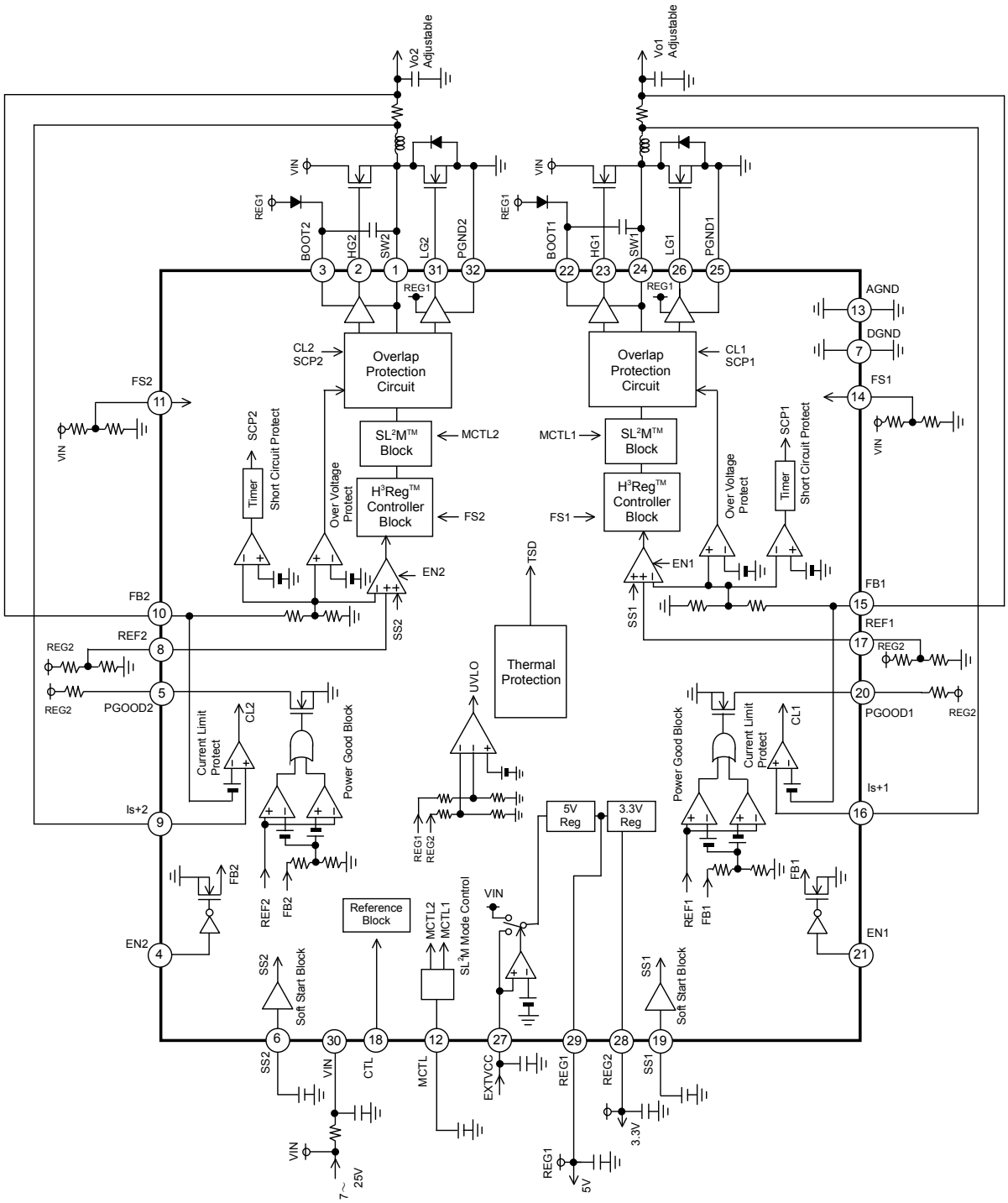
●Electrical characteristics - Continued
(unless otherwise noted, Ta=25℃ VIN=12V, CTL=5V, EN1=EN2=5V, REF1=2.5V, REF2=1.65V, FS1=FS2=0.582V)

Parameter	Symbol	Standard Value			Unit	Conditions
		MIN.	TYP.	MAX.		
[H^3Reg^{TM} block]						
On Time 1	TON1	0.810	0.960	1.110	μs	REF=2.5V
On Time 2	TON2	0.520	0.670	0.820	μs	REF=1.65V
Maximum On Time	TONMAX	3.5	7	14	μs	
Minimum Off Time	TOFFMIN	-	0.2	0.4	μs	
FS1, FS2 bias current	IFS	-10	0	10	μA	
[FET driver block]						
HG higher side ON resistor	HGHON	-	3.0	6.0	Ω	
HG lower side ON resistor	HGLON	-	2.0	4.0	Ω	
LG higher side ON resistor	LGHON	-	2.0	4.0	Ω	
LG lower side ON resistor	LGLON	-	0.5	1.0	Ω	
[Over Voltage Protection block]						
Latch Type OVP Threshold voltage	VLOVP	REF × 2 × 1.15	REF × 2 × 1.175	REF × 2 × 1.20	V	
Latch Type OVP delay time	TLOVP	50	150	300	μs	
[Short circuit protection block]						
SCP Threshold voltage	VSCP	REF × 2 × 0.66	REF × 2 × 0.7	REF × 2 × 0.74	V	
Delay time	TSCP	0.5	1	2	ms	
[Current limit protection block]						
Maximum offset voltage	dVSMAX	50	65	80	mV	
Is+1 bias current	IISP1	-	2.5	10	μA	
Is+2 bias current	IISP2	-	2.5	10	μA	
[Power good block]						
Power good low threshold	VPGTHL	REF × 2 × 0.87	REF × 2 × 0.90	REF × 2 × 0.93	V	
Power good high threshold	VPGTHH	REF × 2 × 1.07	REF × 2 × 1.10	REF × 2 × 1.13	V	
Power good low voltage	VPGL	-	0.1	0.2	V	IPGOOD=1mA
Power good leakage current	ILEAKPG	-2	0	2	μA	VPGOOD=5V
[Soft Start block]						
Charge current	ISS	1.8	2.5	3.2	μA	
Standby voltage	VSS_STB	-	-	50	mV	
[SLLM mode control block]						
MCTL terminal voltage 1	VCONT	-0.3	-	0.3	V	Continuous mode
MCTL terminal voltage 2	VQLLM	1.5	-	3.0	V	QL^2M mode (Maximum LG off time : 50μs)
MCTL terminal voltage 3	VSLLM	4.5	-	REG1+0.3	V	SL^2M mode (Maximum LG off time : ∞)
MCTL float level	VMCTL	1.5	-	3.0	V	

●Output condition table

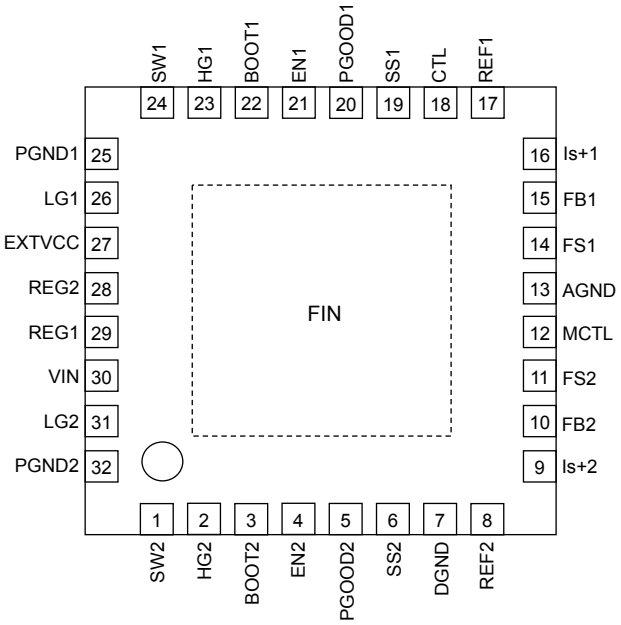
Input			Output			
CTL	EN1	EN2	REG1(5V)	REG2(3.3V)	DC/DC1	DC/DC2
Low	Low	Low	OFF	OFF	OFF	OFF
Low	Low	High	OFF	OFF	OFF	OFF
Low	High	Low	OFF	OFF	OFF	OFF
Low	High	High	OFF	OFF	OFF	OFF
High	Low	Low	ON	ON	OFF	OFF
High	Low	High	ON	ON	OFF	ON
High	High	Low	ON	ON	ON	OFF
High	High	High	ON	ON	ON	ON

●Block Diagram, Application circuit



*Apply the supply voltage EXTVCC pin after REG1 pin is operated.

●Pin Configuration



●Pin Function Table

PIN No.	PIN name	PIN Function
1	SW2	Highside FET source pin 2
2	HG2	Highside FET gate drive pin 2
3	BOOT2	HG Driver power supply pin 2
4	EN2	Vo2 ON/OFF pin (High=ON, Low=OFF)
5	PGOOD2	Vo2 Power Good Open Drain Output pin
6	SS2	Vo2 soft start pin
7	DGND	Ground
8	REF2	Vo2 output voltage setting pin
9	Is+2	Current sense pin +2
10	FB2	Vo2 output voltage sense pin, current sense pin -2
11	FS2	Input pin for setting Vo2 frequency
12	MCTL	Mode shift pin (Low=continuous, Middle=QLLM, High=SLLM)
13	AGND	Input pin Ground
14	FS1	Input pin for setting Vo1 frequency
15	FB1	Vo2 output voltage sense pin, current sense pin -1
16	Is+1	Current sense pin +1
17	REF1	Vo1 output voltage setting pin
18	CTL	Linear regulator ON/OFF pin (High=ON, Low=OFF)
19	SS1	Vo1 soft start pin
20	PGOOD1	Vo1 Power Good Open Drain Output pin
21	EN1	Vo1 ON/OFF pin (High=ON, Low=OFF)
22	BOOT1	HG Driver power supply pin 1
23	HG1	Highside FET gate drive pin 1
24	SW1	Highside FET source pin 1
25	PGND1	Lowside FET source pin 1
26	LG1	Lowside FET gate drive pin 1
27	EXTVCC	Outside power supply input pin
28	REG2	3.3V linear regulator output pin
29	REG1	5V linear regulator output pin
30	VIN	Power supply input pin
31	LG2	Lowside FET gate drive pin 2
32	PGND2	Lowside FET source pin 2
Reverse	FIN	Exposed Pad, Connect to GND

●Reference data

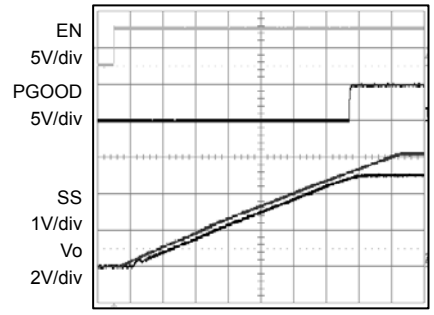


Fig.1 wake up (Vo=5.0V)

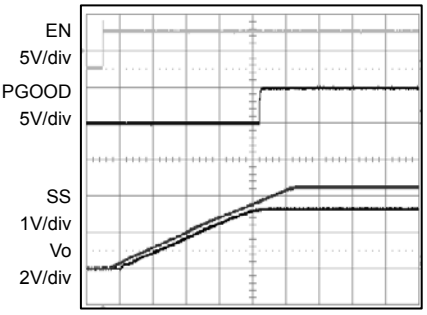


Fig.2 wake up (Vo=3.3V)

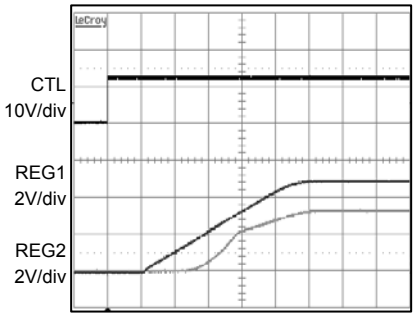


Fig.3 wake up (REG1, REG2)

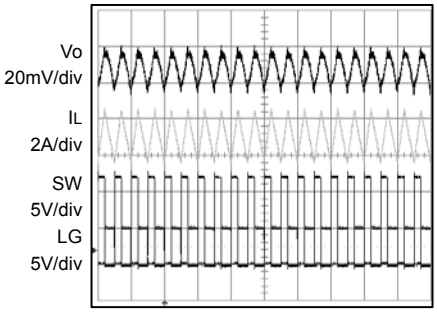


Fig.4 CONT Mode (Io=0A)

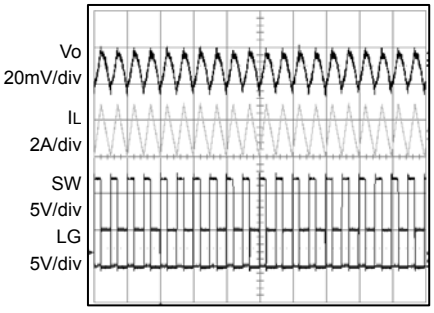


Fig.5 CONT Mode (Io=0.4A)

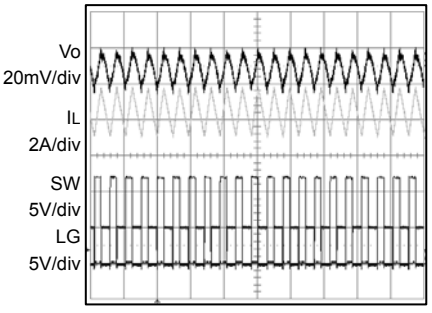


Fig.6 CONT Mode (Io=1.4A)

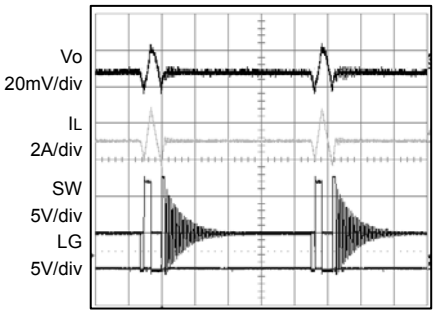


Fig.7 QLLM (Io=0A)

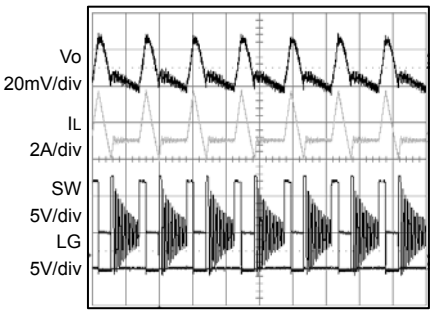


Fig.8 QLLM (Io=0.4A)

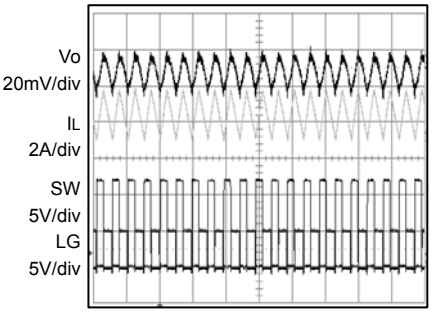


Fig.9 QLLM (Io=1.4A)

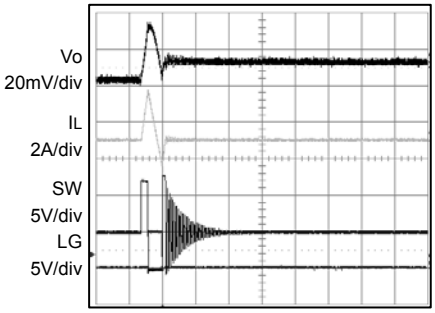


Fig.10 SLLM (Io=0A)

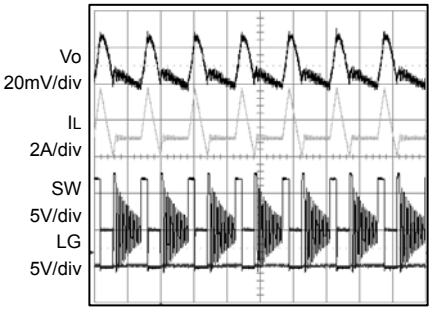


Fig.11 SLLM (Io=0.4A)

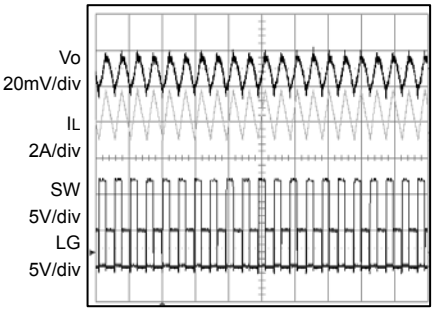


Fig.12 SLLM (Io=1.4A)

●Reference data

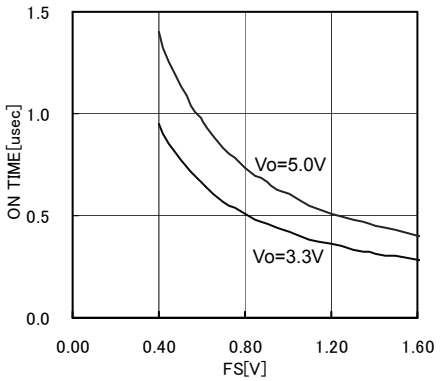


Fig.13 FS-ON TIME

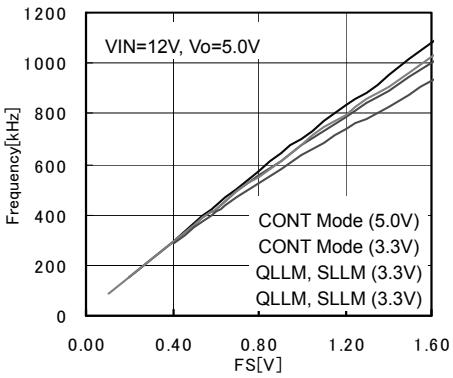


Fig.14 FS-frequency

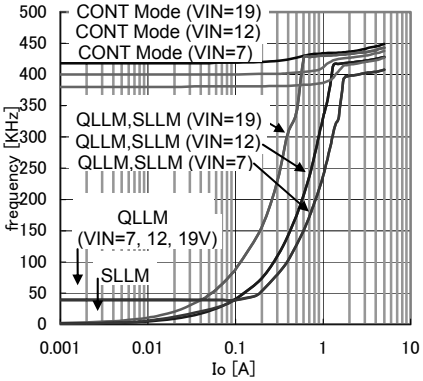


Fig.15 Io-frequency (Vo1=5.0V)

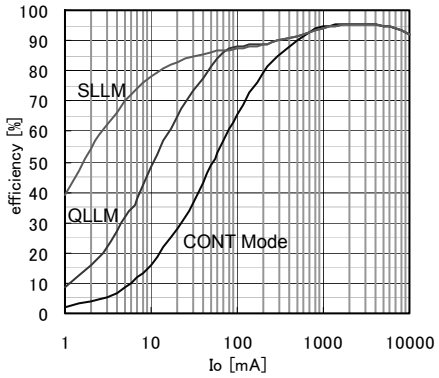


Fig.16 Io-efficiency (VIN=12V, Vo1=5.0V)

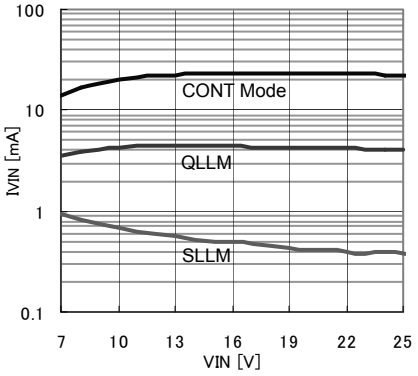


Fig.17 VIN-IVIN (Io=0A, Vo1=5.0V)

●Pin Descriptions

・VIN
This is the main power supply pin. The input supply voltage range is 7V to 25V. The duty cycle of BD9524MUV is determined by input voltage and control output voltage. Therefore, when VIN voltage fluctuated, the output voltage also becomes unstable. Since VIN line is also the input voltage of switching regulator, stability depends on the impedance of the voltage supply. It is recommended to establish bypass capacitor and CR filter suitable for the actual application.

・CTL
When CTL pin voltage is at least 2.3V the status of the linear regulator output becomes active (REG1=5V, REG2=3.3V). Conversely, the status switches off when CTL pin voltage goes lower than 0.8V. The switching regulator doesn't become active when the status of CTL pin is low, if the status of EN pin is high.

・EN
When EN pin voltage is at least 2.3V, the status of the switching regulator becomes active. Conversely, the status switches off when EN pin voltage goes lower than 0.8V.

・REG1
This is the output pin for 5V linear regulator and also active in power supply for driver and control circuit of the inside. The standby function for REG1 is determined by CTL pin. The voltage is 5V, with 100mA current ability. It is recommended that a 10uF capacitor (X5R or X7R) be established between REG1 and GND.

・REG2
This is the output pin for 3.3V linear regulator. The standby function for REG2 is determined by CTL. The voltage is 3.3V, with 100mA current ability. It is recommended that a 10uF capacitor (X5R or X7R) be established between REG2 and GND. It is available to set REF and SS by the resistance division value from REG2 in case REF are not set from an external power supply.

・EXTVCC
This is the external input pin to REG1. When EXTVCC is beyond 4.4V, it supplies REG1 as EXTVCC is the power supply.

・REF
This is the setting pin for output voltage of switching regulator. It is so convenient to be synchronized to outside power supply. This IC controls the voltage in the status of 2×REF≒FB.

・FB
This is the feedback pin from the output of switching regulator. This IC controls the voltage in the status of 2×REF≒FB.

・SS
This is the setting pin for soft start. The rising time is determined by the capacitor connected between SS and GND, and the fixed current inside IC after it is the status of low in standby mode. It controls the output voltage till SS voltage catch up the REF pin to become the double of the SS terminal voltage.

・FS
This is the input pin for setting the frequency. It is available to set it in frequency range is 200KHz to 500kHz.

・Is+
This is the sense pin for output current. In case it is connected to side of the coil resistance for sense current and the voltage is set 65mV(typ) or more higher than FB pin voltage, the switching operation turns OFF.

・PGOOD
This is the open drain pin for deciding the output of switching regulator.

・MCTL
This is the switching shift pin for SLLM (Simple Light Load Mode). The efficiency in SLLM mode improves in setting MCTL pin to 1.5V or more. In case MCTL terminal voltage range is from 1.5 to 3.0V, LG maximum OFF time is 40usec, from 4.5V to REG1+0.3V, LG maximum OFF time is to infinity. It is in continuous mode that MCTL pin voltage is set 0.3V or less.

・AGND,DGND
This is the ground pin.

・BOOT
This is the power supply pin for high side FET driver. The maximum voltage range to GND pin is to 35V, to SW pin is to 7V. In switching operations, the voltage swings from (VIN+REG1) to REG1 by BOOT pin operation.

・HG
This is the highside FET gate drive pin. It is operated in switching between BOOT to SW. In case the output MOS is 3ohm /the status of Hi, 2ohm/the status of Low, it is operated hi-side FET gate in high speed.

・SW
This is the ground pin for high side FET drive. The maximum voltage range to GND pin is to 30V. Switching operation swings from the status of BOOT to the status of GND.

・LG
This is the lowside FET gate drive pin. It is operated in switching between REG1 to PGND. In case the output MOS is 2ohm /the status of Hi, 0.5ohm/the status of Low, it is operated low-side FET gate in high speed.

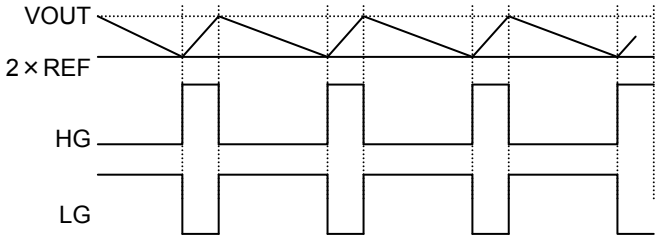
・PGND
This is the ground pin for low side FET drive.

● Explanation of Operation

The BD9524MUV is a 2ch synchronous buck regulator controller incorporating ROHM's proprietary H^3Reg^{TM} CONTROLLA control system. When VOUT drops due to a rapid load change, the system quickly restores VOUT by extending the TON time interval. Thus, it serves to improve the regulator's transient response. Activating the Light Load Mode will also exercise Simple Light Load Mode (SLLM) control when the load is light, to further increase efficiency.

H^3Reg^{TM} control

(Normal operation)

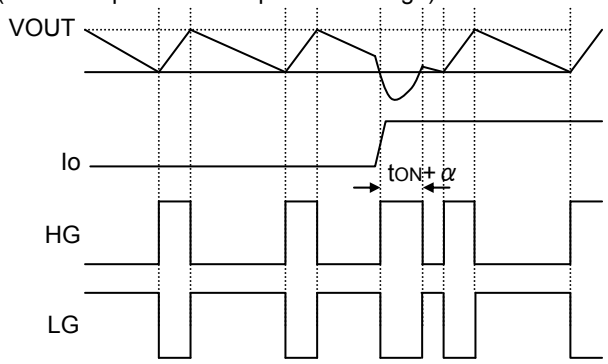


When VOUT falls to a reference voltage (2×REF), the drop is detected, activating the H^3Reg^{TM} CONTROLLA system.

$$t_{ON} = \frac{2 \times REF}{VIN} \times \frac{1}{f} \text{ [sec]} \cdot \cdot \cdot (1)$$

HG output is determined by the formula above.

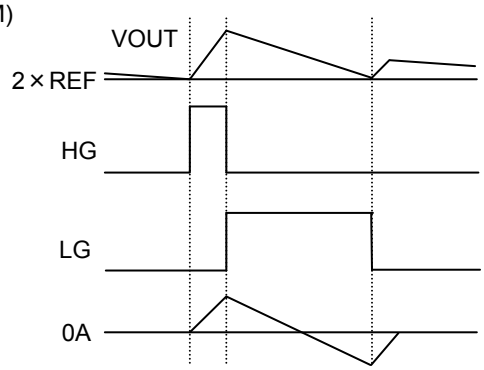
(VOUT drops due to a rapid load change)



When V_{OUT} drops due to a rapid load change, and the voltage remains below reference voltage after the programmed t_{ON} time interval has elapsed, the system quickly restores V_{OUT} by extending the t_{ON} time, improving the transient response.

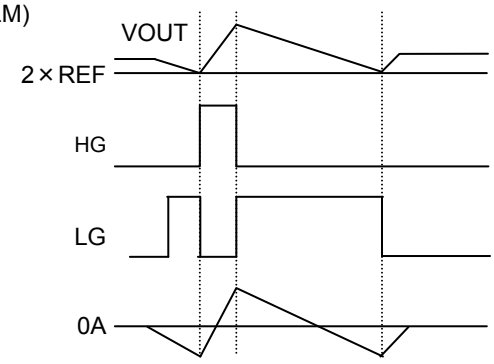
Light Load Control

(SLLM)



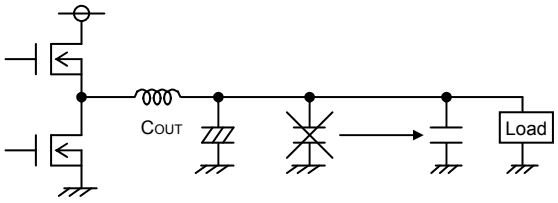
In SLLM (MCTL="High voltage"), when the status of LG is OFF and the coil current is within 0A (it flows to SW from VOUT.), SLLM function is operated to prevent output next HG. The status of HG is ON, when VOUT falls below reference voltage again.

(QLLM)



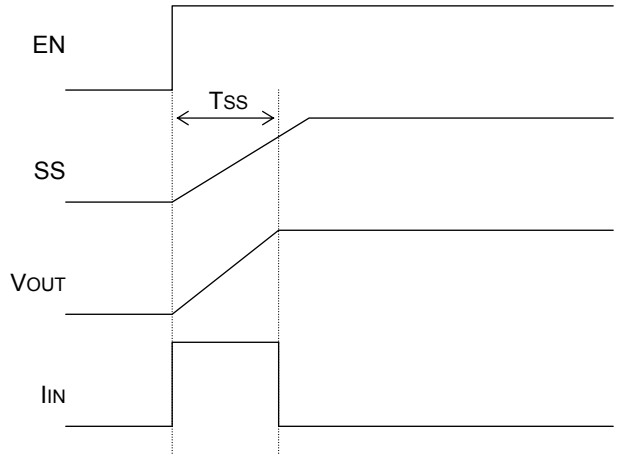
In QLLM (MCTL="Hiz or Middle voltage"), when the status of LG is OFF and the coil current is within 0A (it flows to SW from VOUT.), QLLM function is operated to prevent output next HG.
Then, VOUT falls below the output programmed voltage within the programmed time (typ=40μs), the status of HG is ON. In case VOUT doesn't fall in the programmed time, the status of LG is ON forcedly and VOUT falls. As a result, he status of next HG is ON.

*Attention: H^3Reg^{TM} CONTROLLA monitors the supplying current from capacitor to load, using the ESR of output capacitor, and realize the rapid response. Bypass capacitor used at each load (Ex. Ceramic capacitor) exercise the effect with connecting to each load side. Do not put a ceramic capacitor on C_{OUT} side of power supply.



● Timing Chart

• Soft Start Function



Soft start is exercised with the EN pin set high. Current control takes effect at startup, enabling a moderate output voltage “ramping start.” Soft start timing and incoming current are calculated with formulas (2) and (3) below.

Soft start time

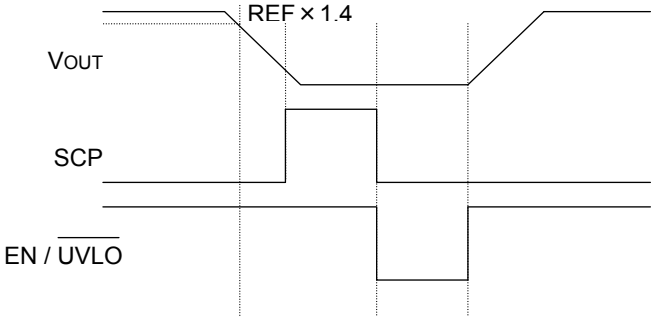
$$Tss = \frac{REF \times Css}{2\mu A(typ)} \text{ [sec]} \quad \cdot\cdot\cdot (2)$$

Incoming current

$$I_{IN} = \frac{Co \times V_{OUT}}{Tss} \text{ [A]} \quad \cdot\cdot\cdot (3)$$

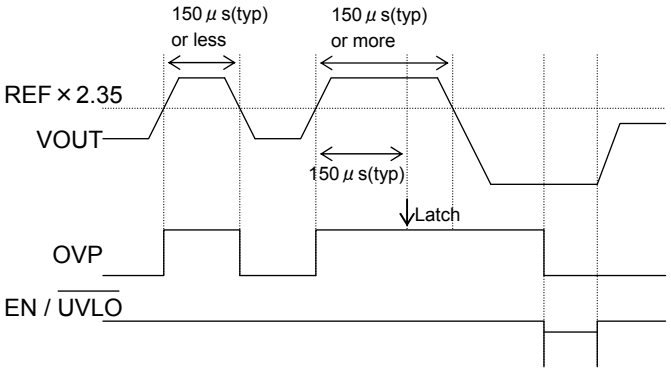
(Css: Soft start capacitor; Co: Output capacitor)

・Timer Latch Type Short Circuit Protection



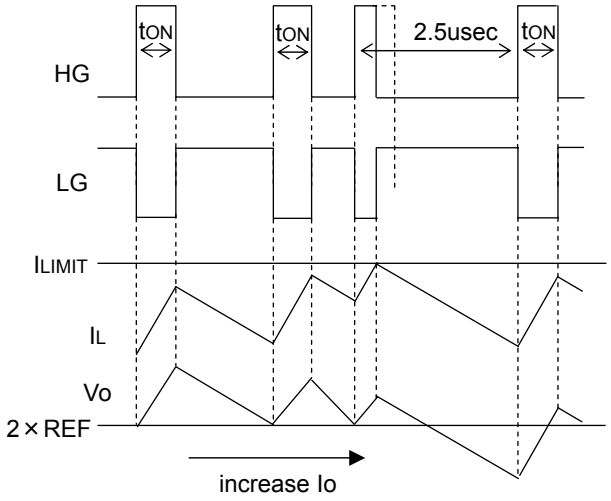
Short protection kicks in when output falls to or below REF × 1.4 (setting voltage × 0.7).
When the programmed time period elapses, output is latched OFF to prevent destruction of the IC. Output voltage can be restored either by reconnecting the EN pin or disabling UVLO.

・Over Voltage Protection



When output rise to or above REF × 2.35 (output setting voltage × 1.175), output over voltage protection is exercised, and low side FET goes up maximum for reducing output.（LG=High, HG=Low）. When output falls within the programmed time (typ=150μs), it returns to the standard mode. When the programmed time period elapses, output is latched OFF to prevent destruction of the IC. Output voltage can be restored either by reconnecting the EN pin or disabling UVLO.

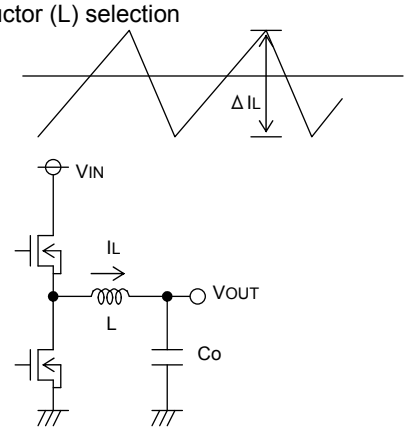
・Over current protection circuit



During the normal operation, when VOUT becomes less than reference voltage, HG becomes High during the time tON . However, when inductor current exceeds ILIMIT threshold, HG becomes OFF.
After 2.5μsec(typ), HG becomes ON again if the output voltage is lower than the specific voltage level and IL is lower than ILIMIT level.

● External Component Selection

1. Inductor (L) selection



Output ripple current

The inductor value is a major influence on the output ripple current. As formula (4) below indicates, the greater the inductor or the switching frequency, the lower the ripple current.

$$\Delta I_L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f} \quad [A] \cdot \cdot \cdot (4)$$

The proper output ripple current setting is about 30% of maximum output current.

$$\Delta I_L = 0.3 \times I_{OUT}max. \quad [A] \cdot \cdot \cdot (5)$$

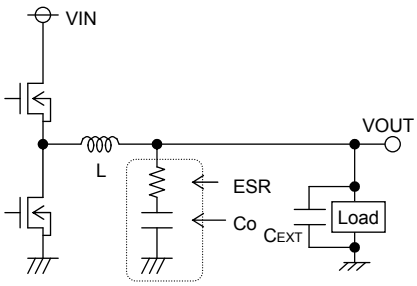
$$L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{IN} \times f} \quad [H] \cdot \cdot \cdot (6)$$

(ΔI_L: output ripple current; f: switch frequency)

※Passing a current larger than the inductor's rated current will cause magnetic saturation in the inductor and decrease system efficiency. In selecting the inductor, be sure to allow enough margin to assure that peak current does not exceed the inductor rated current value.

※To minimize possible inductor damage and maximize efficiency, choose a inductor with a low (DCR, ACR) resistance.

2.Output Capacitor (C_O) Selection



Output Capacitor

When determining the proper output capacitor, be sure to factor in the equivalent series resistance required to smooth out ripple volume and maintain a stable output voltage range.

Output ripple voltage is determined as in formula (7) below.

$$\Delta V_{OUT} = \Delta I_L \times ESR \quad [V] \cdot \cdot \cdot (7)$$

(ΔI_L: Output ripple current; ESR: C_O equivalent series resistance)

※ In selecting a capacitor, make sure the capacitor rating allows sufficient margin relative to output voltage. Note that a lower ESR can minimize output ripple voltage.

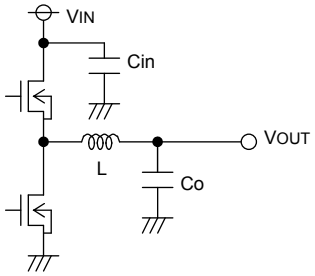
Please give due consideration to the conditions in formula (8) below for output capacity, bear in mind that output rise time must be established within the soft start time frame.

$$Co+C_{EXT} \leqq \frac{T_{SS} \times (Limit-I_{OUT})}{V_{OUT}} \quad \cdot \cdot \cdot (8)$$

Tss: Soft start time
Limit: Over current detection 2A(Typ)

Note: Improper capacitor may cause startup malfunctions.

3. Input Capacitor (Cin) Selection



Input Capacitor

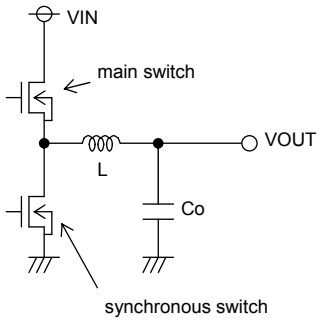
The input capacitor selected must have low enough ESR resistance to fully support large ripple output, in order to prevent extreme over current. The formula for ripple current IRMS is given in (9) below.

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{IN}(V_{IN}-V_{OUT})}}{V_{IN}} \quad [A] \cdot \cdot \cdot (9)$$

Where $V_{IN} = 2 \times V_{OUT}$, $I_{RMS} = \frac{I_{OUT}}{2}$

A low ESR capacitor is recommended to reduce ESR loss and maximize efficiency.

4. MOSFET Selection



Loss on the main MOSFET

$P_{main}=P_{RON}+P_{GATE}+P_{TRAN}$

$$= \frac{V_{OUT}}{V_{IN}} \times R_{ON} \times I_{OUT}^2 + Ciss \times f \times V_{DD} + \frac{V_{IN}^2 \times Crss \times I_{OUT} \times f}{I_{DRIVE}} \quad \cdot\cdot\cdot (10)$$

(Ron: On-resistance of FET; Ciss: FET gate capacitance;
f: Switching frequency Crss: FET inverse transfer function;
I_{DRIVE}: Gate peak current)

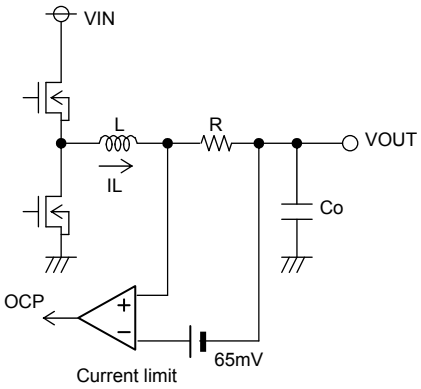
Loss on the synchronous MOSFET

$P_{syn}=P_{RON}+P_{GATE}$

$$= \frac{V_{IN}-V_{OUT}}{V_{IN}} \times R_{ON} \times I_{OUT}^2 + Ciss \times f \times V_{DD} \quad \cdot\cdot\cdot (11)$$

5. Setting Detection Resistance (Detect ILIMIT at the peak current)

(A) High accuracy current detective circuit (use the low resistance)

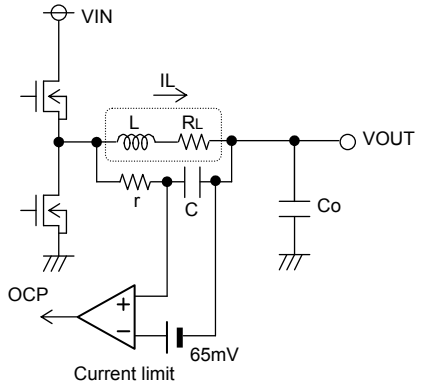


The over current protection function detects the output ripple current peak value. This parameter (setting value) is determined as in formula (13) below.

$$I_{LMIT}= \frac{65mV(typ)}{R} \text{ [A]} \cdot\cdot\cdot (12)$$

(R: Detection resistance)

(B) Low loss current detective circuit (use the DCR value of inductor)



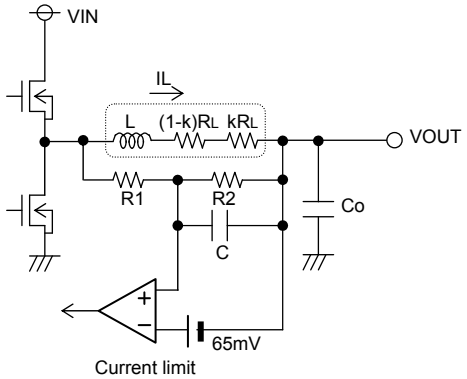
When the over current protection is detected by DCR of inductor L, this parameter (setting value) is determined as in formula (13) below.
(Application circuit:P18)

$$I_{LMIT}=65mV(typ) \times \frac{r \times C}{L} \text{ [A]} \cdot\cdot\cdot (13)$$

$$(R_L= \frac{L}{r \times C})$$

(R_L: the DCR value of inductor)

(C) Low loss current detective circuit (the DCR value of inductor : high)

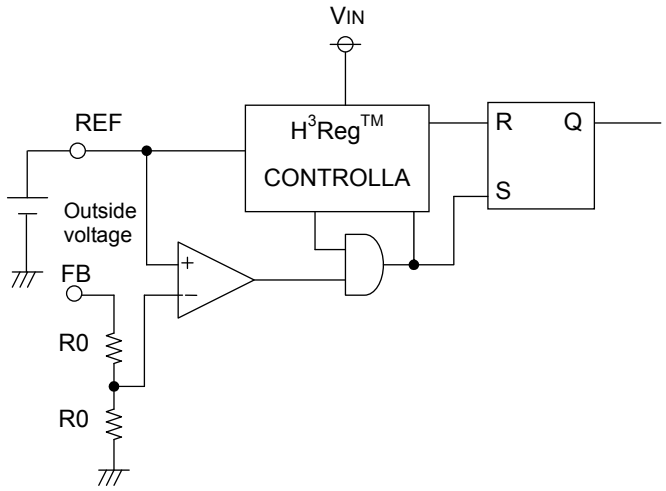


$$I_{LIMIT}= \frac{65mV(typ)}{k \times R_L} \text{ [A]} \cdot\cdot\cdot (14)$$

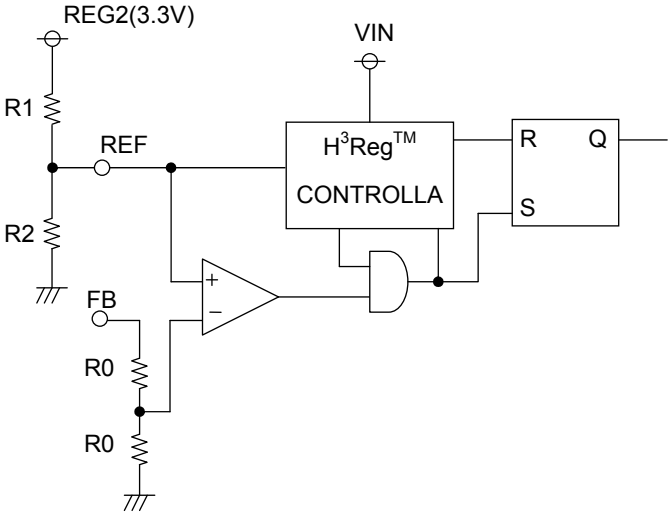
$$\left(k= \frac{R_2}{R_1+R_2}, \frac{L}{R_L} = kR_1C \right)$$

(R_L: the DCR value of inductor)

6. Setting standard voltage (REF)



It is available to set the reference voltage (REF) with outside supply voltage ×2 [V] by using outside power supply voltage.

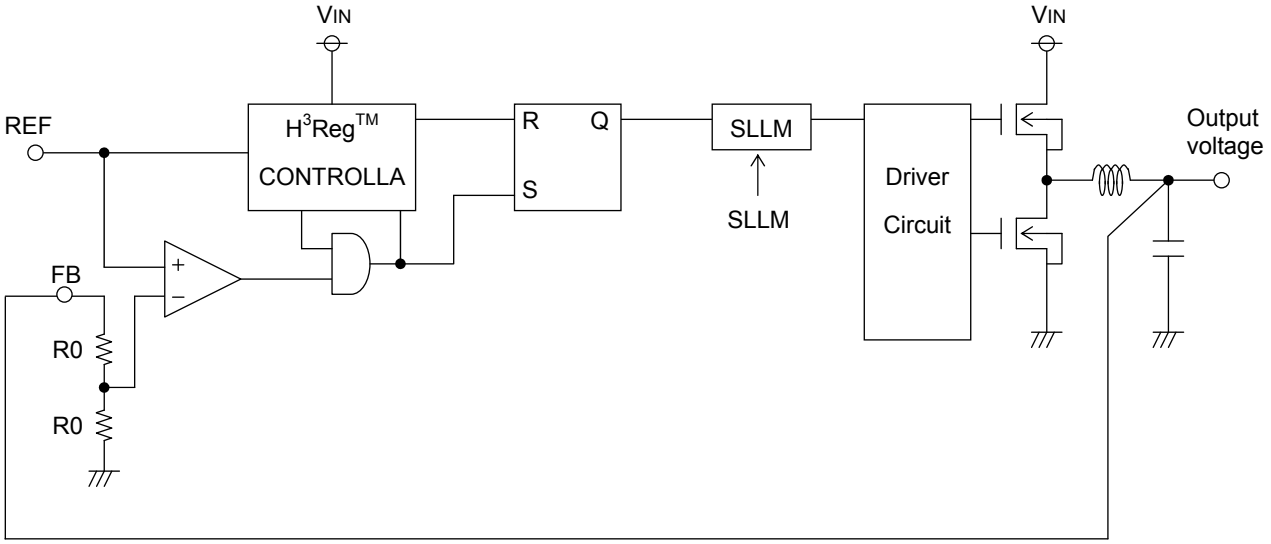


It is available to set the reference voltage (REF) by the resistance division value from REG2 in case REF is not set from an external power supply.

$$REF = \frac{R2}{R1+R2} \times REG2\ [V] \cdots (15)$$

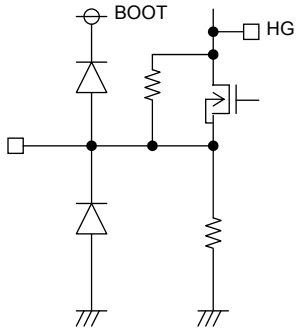
7. Setting output voltage

This IC is operated that output voltage is REF×2≒FB.
And it is operated that output voltage is feed back to FB pin.

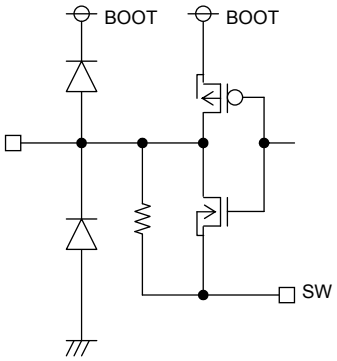


●I/O Equivalent Circuit

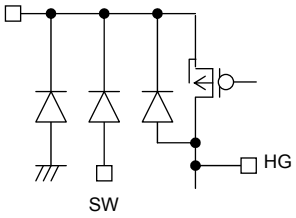
1, 24pin (SW2, SW1)



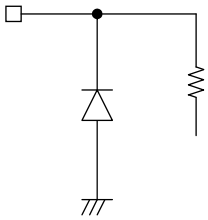
2, 23pin (HG2, HG1)



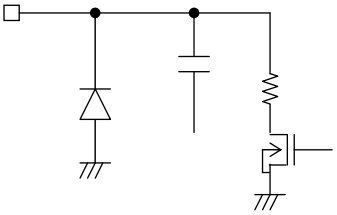
3, 22pin (BOOT2, BOOT1)



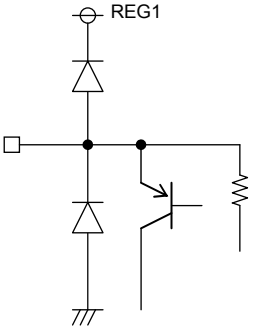
4, 21pin (EN2, EN1)



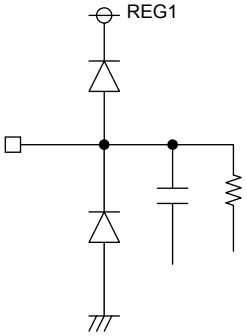
5, 20pin (PGOOD2, PGOOD1)



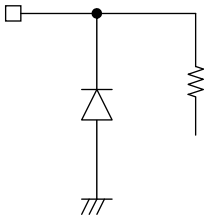
6, 19pin (SS2, SS1)



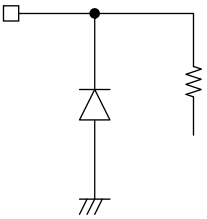
8, 17pin (REF2, REF1)



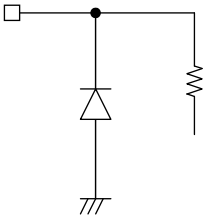
9, 16pin (Is+2, Is+1)



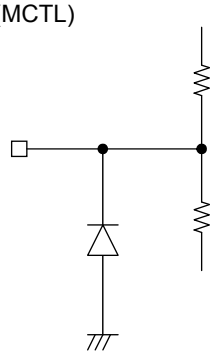
10, 15pin (FB2, FB1)



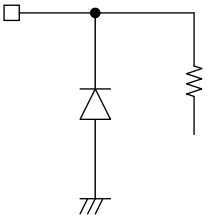
11, 14pin (FS2, FS1)



12pin (MCTL)

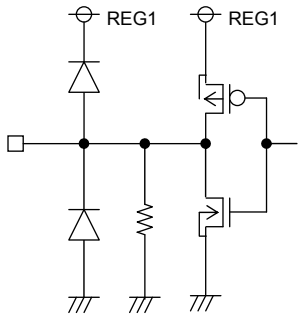


18pin (CTL)

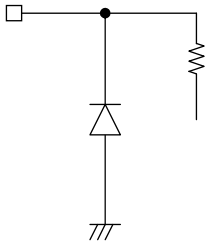


●I/O Equivalent Circuit

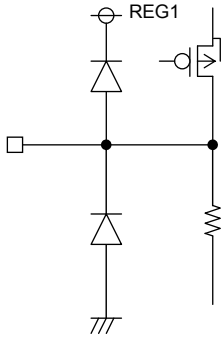
26, 31pin (LG1, LG2)



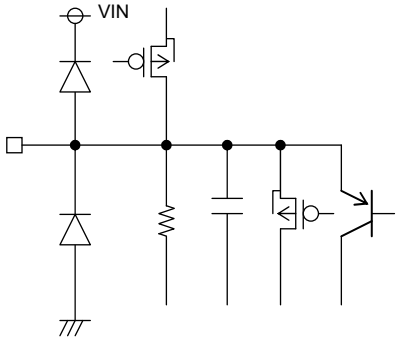
27pin (EXTVCC)



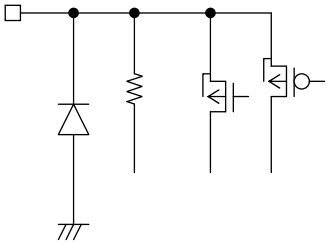
28pin (REG2)



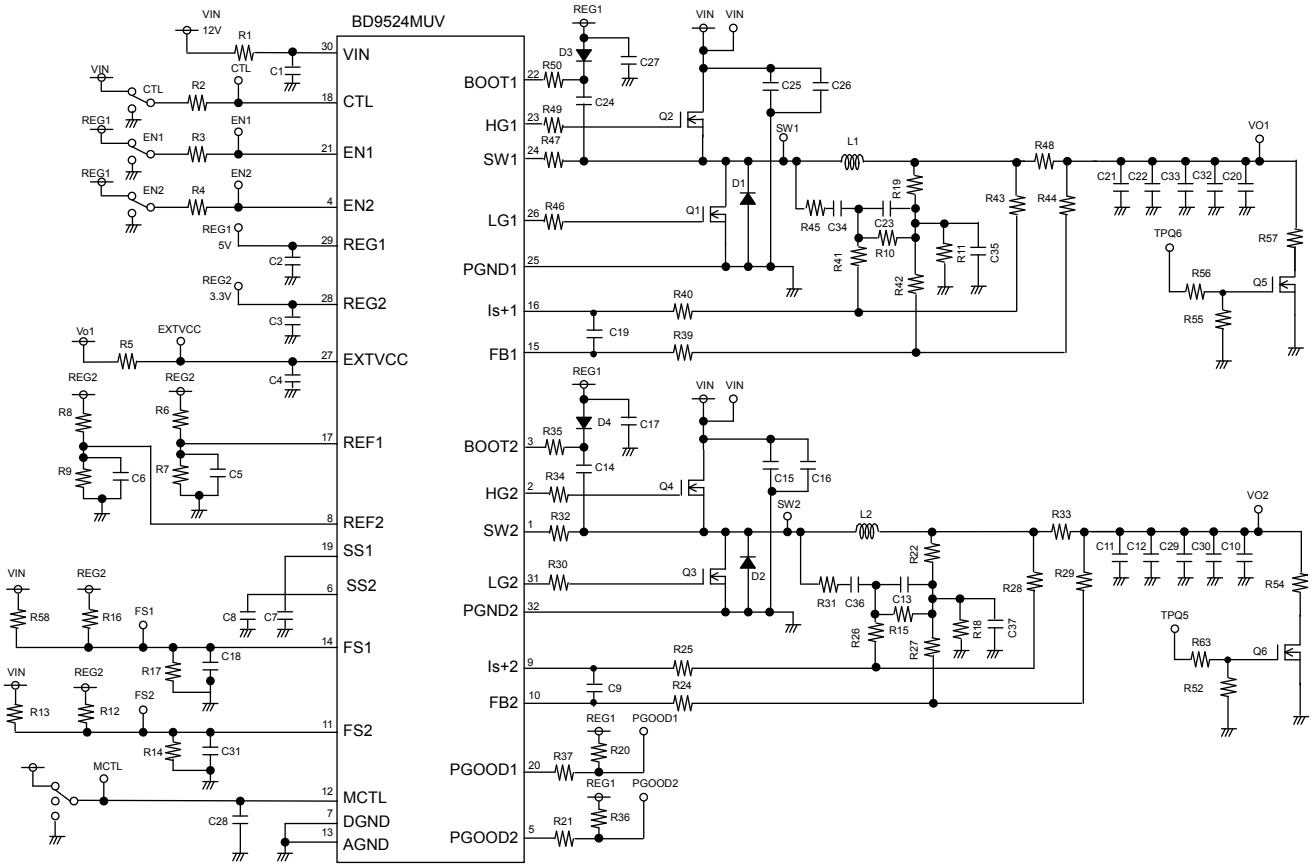
29pin (REG1)



30pin (VIN)



●Evaluation Board Circuit (Vo1=5V f1=300kHz Vo2=3.3V f2=400kHz)



DESIGNATION	RATING	PART No.	COMPANY
R1	0Ω	MCR03EZHJ000	ROHM
R2	0Ω	MCR03EZHJ000	ROHM
R3	0Ω	MCR03EZHJ000	ROHM
R4	0Ω	MCR03EZHJ000	ROHM
R5	0Ω	MCR03EZHJ000	ROHM
R6	15kΩ	MCR03PZHZF1502	ROHM
R7	47kΩ	MCR03PZHZF4702	ROHM
R8	30kΩ	MCR03PZHZF3002	ROHM
R9	30kΩ	MCR03PZHZF3002	ROHM
R10 *	-	-	-
R11 *	-	-	-
R12	-	-	-
R13	1MΩ	MCR03PZHZF1004	ROHM
R14	51kΩ	MCR03PZHZF5102	ROHM
R15 *	-	-	-
R16	-	-	-
R17	36kΩ	MCR03PZHZF3602	ROHM
R18 *	-	-	-
R19 *	-	-	-
R20	100kΩ	MCR03PZHZF1003	ROHM
R21	0Ω	MCR03EZHJ000	ROHM
R22 *	-	-	-
R24	0Ω	MCR03EZHJ000	ROHM
R25	0Ω	MCR03EZHJ000	ROHM
R26 *	-	-	-
R27 *	-	-	-
R28	0Ω	MCR03EZHJ000	ROHM
R29	0Ω	MCR03EZHJ000	ROHM
R30	0Ω	MCR03EZHJ000	ROHM
R31 *	-	-	-
R32	0Ω	MCR03EZHJ000	ROHM
R33	5mΩ	PMR100HZPFU5L00	ROHM
R34	0Ω	MCR03EZHJ000	ROHM
R35	0Ω	MCR03EZHJ000	ROHM
R36	100kΩ	MCR03PZHZF1003	ROHM
R37	0Ω	MCR03EZHJ000	ROHM
R39	0Ω	MCR03EZHJ000	ROHM
R40	0Ω	MCR03EZHJ000	ROHM
R41 *	-	-	-
R42 *	-	-	-
R43	0Ω	MCR03EZHJ000	ROHM
R44	0Ω	MCR03EZHJ000	ROHM
R45 *	-	-	-
R46	0Ω	MCR03EZHJ000	ROHM
R47	0Ω	MCR03EZHJ000	ROHM
R48	5mΩ	PMR100HZPFU5L00	ROHM
R49	0Ω	MCR03EZHJ000	ROHM
R50	0Ω	MCR03EZHJ000	ROHM
R52	-	-	-
R54	-	-	-
R55	-	-	-
R56	-	-	-
R57	-	-	-

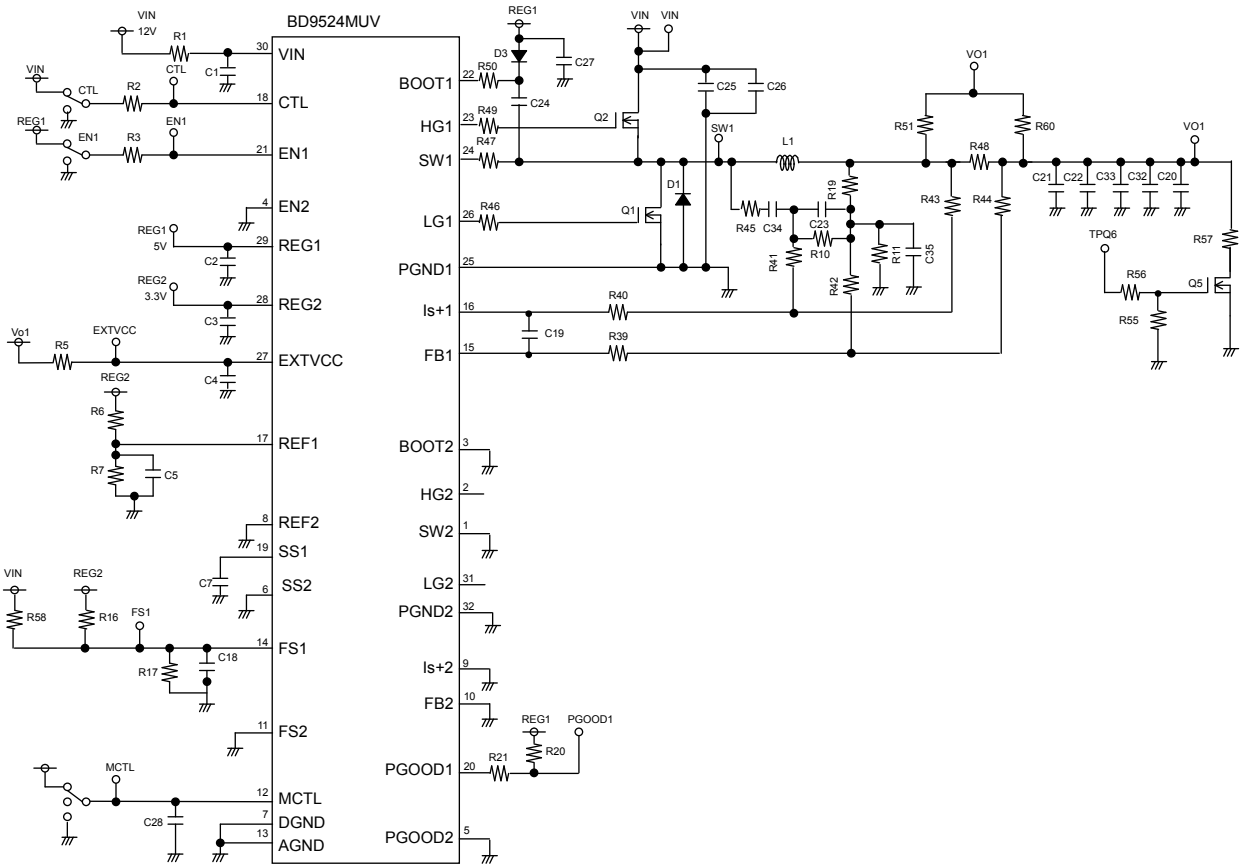
DESIGNATION	RATING	PART No.	COMPANY
R58	1MΩ	MCR03PZHZF1004	ROHM
R63	-	-	-
C1	10uF(25V)	CM32X7R106M25A	KYOCERA
C2	10uF(6.3V)	GRM21BB10J106KD	MURATA
C3	10uF(6.3V)	GRM21BB10J106KD	MURATA
C4	10uF(6.3V)	GRM21BB10J106KD	MURATA
C5	0.01uF(50V)	GRM188B11H103KD	MURATA
C6	0.01uF(50V)	GRM188B11H103KD	MURATA
C7	1000pF(50 V)	GRM188B11H102KD	MURATA
C8	1000pF(50V)	GRM188B11H102KD	MURATA
C9	-	-	-
C10	-	-	-
C11	220uF	6TPE220MI	SANYO
C12	-	-	-
C13 *	-	-	-
C14	0.47uF(10V)	GRM188B11A474KD	MURATA
C15	10uF(25V)	CM32XR7106M25A	KYOCERA
C16	10uF(25V)	CM32XR7106M25A	KYOCERA
C17	10uF(6.3V)	GRM21BB10J106KD	MURATA
C18	-	-	-
C19	-	-	-
C20	-	-	-
C21	220uF	6TPE220MI	SANYO
C22	-	-	-
C23 *	-	-	-
C24	0.47uF(10V)	GRM188B11A474KD	MURATA
C25	10uF(25V)	CM32XR7106M25A	KYOCERA
C26	10uF(25V)	CM32XR7106M25A	KYOCERA
C27	10uF(6.3V)	GRM21BB10J106KD	MURATA
C28	-	-	-
C29	-	-	-
C30	-	-	-
C31	-	-	-
C32	-	-	-
C33	-	-	-
C34 *	-	-	-
C35 *	-	-	-
C36 *	-	-	-
C37 *	-	-	-
D1	Diode	RSX501L-20	ROHM
D2	Diode	RSX501L-20	ROHM
D3	Diode	RB520S-30	ROHM
D4	Diode	RB520S-30	ROHM
L1	2.5uH	CDEP105NP-2R5MC-32	Sumida
L2	2.5uH	CDEP105NP-2R5MC-32	Sumida
Q1	FET	uPA2702	NEC
Q2	FET	uPA2702	NEC
Q3	FET	uPA2702	NEC
Q4	FET	uPA2702	NEC
Q5	-	-	-
Q6	-	-	-
U1	-	BD9524MUV	ROHM

* Patterns for over current detection used DCR.

●Handling method of unused pin during using only 1ch DC/DC.

If using only 1ch DC/DC and 2ch pin is set to be off at all times, please manage the unused pin as diagram below.

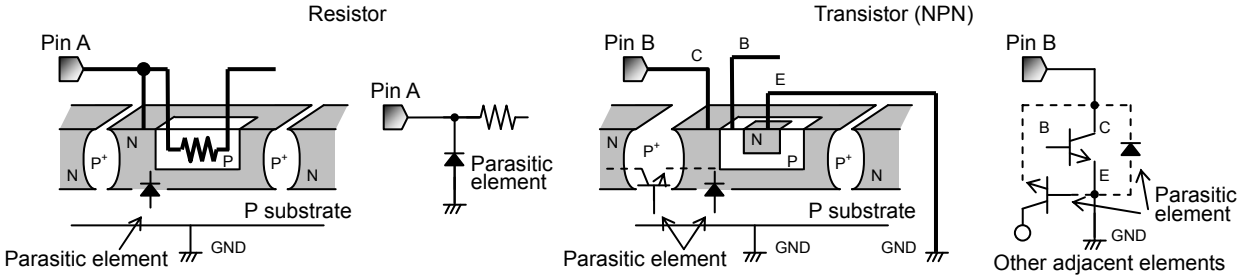
PIN No,	PIN Name	Management
1	SW2	GND
2	HG2	OPEN
3	BOOT2	GND
4	EN2	GND
5	PGOOD2	GND
6	SS2	GND
8	REF2	GND
9	Is+2	GND
10	FB2	GND
11	FS2	GND
31	LG2	OPEN



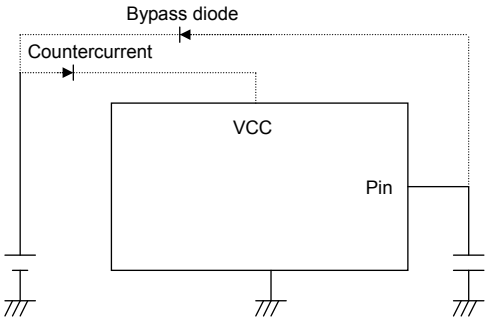
●Notes for use

1. This integrated circuit is a monolithic IC, which (as shown in the figure below), has P isolation in the P substrate and between the various pins. A P-N junction is formed from this P layer and N layer of each pin, with the type of junction depending on the relation between each potential, as follows:
   - When GND> element A> element B, the P-N junction is a diode.
   - When element B>GND element A, the P-N junction operates as a parasitic transistor.

   Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, as well as operating malfunctions and physical damage. Therefore, be careful to avoid methods by which parasitic diodes operate, such as applying a voltage lower than the GND (P substrate) voltage to an input pin.



2. In some modes of operation, power supply voltage and pin voltage are reversed, giving rise to possible internal circuit damage. For example, when the external capacitor is charged, the electric charge can cause a VCC short circuit to the GND. In order to avoid these problems, inserting a VCC series countercurrent prevention diode or bypass diode between the various pins and the VCC is recommended.



3. Absolute maximum rating

   Although the quality of this IC is rigorously controlled, the IC may be destroyed when applied voltage or operating temperature exceeds its absolute maximum rating. Because short mode or open mode cannot be specified when the IC is destroyed, it is important to take physical safety measures such as fusing if a special mode in excess of absolute rating limits is to be implemented.

4.GND potential

   Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode.

5. Thermal design

   In order to build sufficient margin into the thermal design, give proper consideration to the allowable loss (Power Dissipation) in actual operation.

6. Short-circuits between pins and incorrect mounting position

   When mounting the IC onto the circuit board, be extremely careful about the orientation and position of the IC. The IC may be destroyed if it is incorrectly positioned for mounting. Do not short-circuit between any output pin and supply pin or ground, or between the output pins themselves. Accidental attachment of small objects on these pins will cause shorts and may damage the IC.

7. Operation in strong electromagnetic fields
   Use in strong electromagnetic fields may cause malfunctions. Use extreme caution with electromagnetic fields.

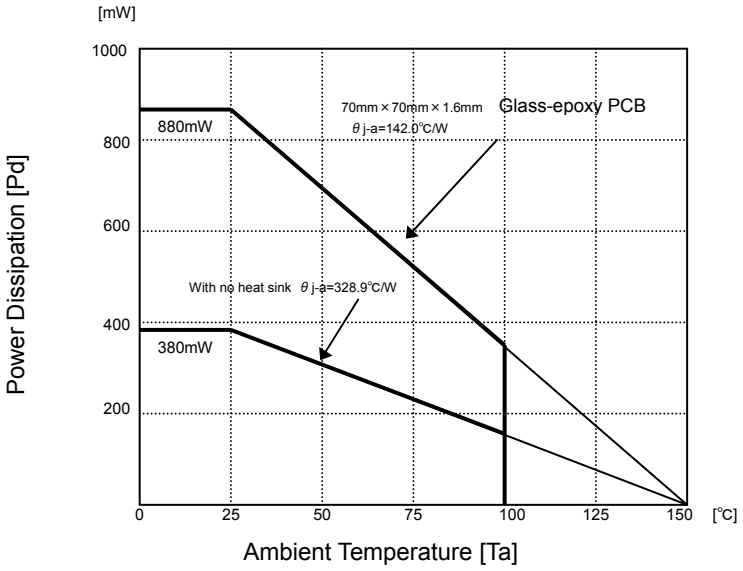
8. Thermal shutdown circuit
   This IC is provided with a built-in thermal shutdown (TSD) circuit, which is activated when the operating temperature reaches 175℃ (standard value), and has a hysteresis range of 15℃ (standard). When the IC chip temperature rises to the threshold, all the inputs automatically turn OFF. Note that the TSD circuit is provided for the exclusive purpose shutting down the IC in the presence of extreme heat, and is not designed to protect the IC per se or guarantee performance when or after extreme heat conditions occur. Therefore, do not operate the IC with the expectation of continued use or subsequent operation once the TSD is activated.

9. Capacitor between output and GND
   When a larger capacitor is connected between the output and GND, Vcc or VIN shorted with the GND or 0V line – for any reason – may cause the charged capacitor current to flow to the output, possibly destroying the IC. Do not connect a capacitor larger than 1000uF between the output and GND.

10. Precautions for board inspection
    Connecting low-impedance capacitors to run inspections with the board may produce stress on the IC. Therefore, be certain to use proper discharge procedure before each process of the operation. To prevent electrostatic accumulation and discharge in the assembly process, thoroughly ground yourself and any equipment that could sustain ESD damage, and continue observing ESD-prevention procedures in all handling, transfer and storage operations. Before attempting to connect components to the test setup, make certain that the power supply is OFF. Likewise, be sure the power supply is OFF before removing any component connected to the test setup.

11. GND wiring pattern
    When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

●Power Dissipation

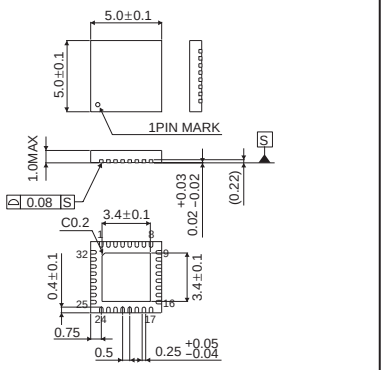


●Ordering part number

B	D	9	5	2	4	M	U	V	-	E	2

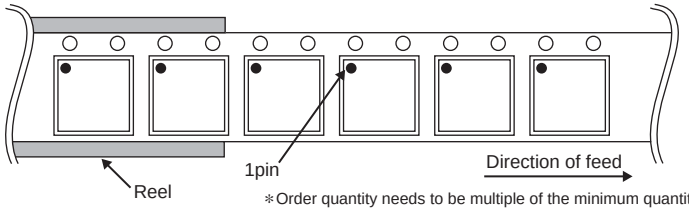
Part No. (BD) | Part No. (9524) | Package MUV : VQFN032V5050 | Packaging and forming specification E2: Embossed tape and reel

VQFN032V5050



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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