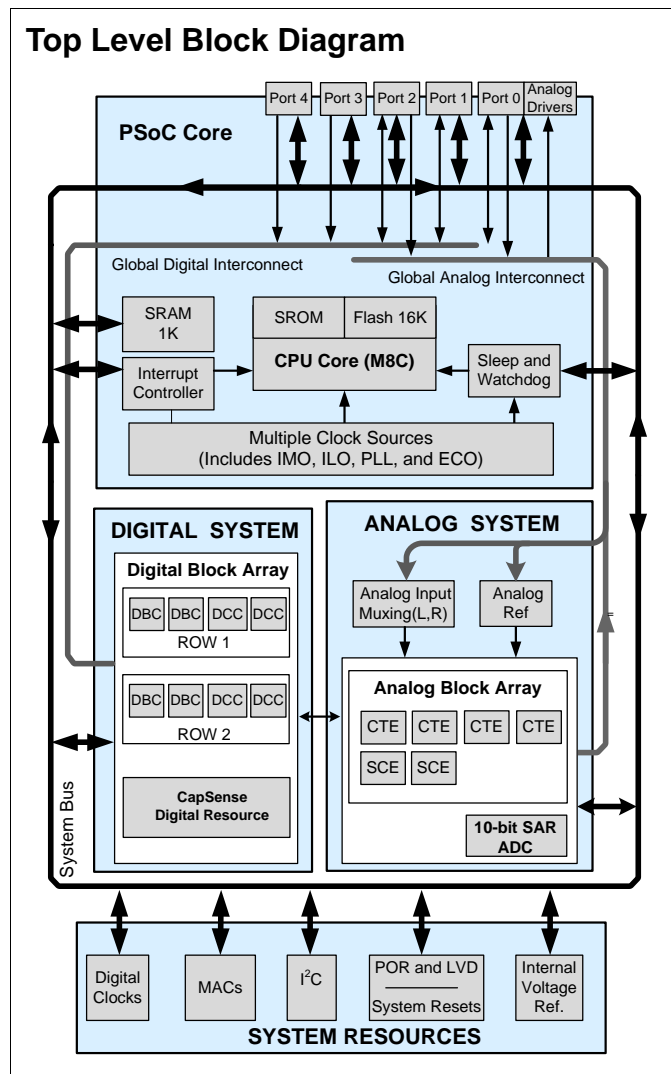# PSoC® Programmable System-on-Chip™

Features

- Powerful Harvard Architecture Processor:
  - ❐ M8C Processor Speeds up to 24 MHz
  - ❐ 8x8 Multiply, 32-Bit Accumulate
  - ❐ Low Power at High Speed
  - ❐ 3.0V to 5.25V Operating Voltage
  - ❐ Industrial Temperature Range: -40°C to +85°C

- Advanced Peripherals (PSoC Blocks)
  - ❐ Six Analog Type "E" PSoC Blocks provide:
    - • Single or Dual 8-Bit ADC
    - • Comparators (up to Four)
  - ❐ Up to Eight Digital PSoC Blocks provide:
    - • 8 to 32-Bit Timers, Counters, and PWMs
    - • One Shot, Multi Shot Mode Support in Timers and PWMs
    - • PWM with Deadband Support in One Digital Block
    - • Shift Register, CRC, and PRS Modules
    - • Full Duplex UART
    - • Multiple SPI™ Masters or Slaves, Variable Data Length Support: 8, 9, ...,16-bit
    - • Can be Connected to all GPIO Pins
  - ❐ Complex Peripherals by Combining Blocks
  - ❐ Shift Function Support for FSK Detection
  - ❐ Powerful Synchronize Feature Support. Analog Module Operations can be Synchronized by Digital Blocks or External Signals.

- High Speed 10-Bit SAR ADC with Sample and Hold Optimized for Embedded Control

- Precision, Programmable Clocking:
  - ❐ Internal ± 5% 24/48 MHz Oscillator across the Industrial Temperature Range
  - ❐ High Accuracy 24 MHz with Optional 32 kHz Crystal and PLL
  - ❐ Optional External Oscillator, up to 24 MHz
  - ❐ Internal/External Oscillator for Watchdog and Sleep

- Flexible On-Chip Memory:
  - ❐ Up to 16K Bytes Flash Program Storage 50,000 Erase/Write Cycles
  - ❐ Up to 1K Byte SRAM Data Storage
  - ❐ In-System Serial Programming (ISSP™)
  - ❐ Partial Flash Updates
  - ❐ Flexible Protection Modes
  - ❐ EEPROM Emulation in Flash

- Optimized CapSense Resource:
  - ❐ Two IDAC Support up to 640 µA Source Current to Replace External Resistor
  - ❐ Two Dedicated Clock Resources for CapSense:
    - • CSD_CLK: 1/2/4/8/16/32/128/256 Derive from SYSCLK
    - • CNT_CLK: 1/2/4/8 Derive from CSD_CLK
  - ❐ Dedicated 16-Bit Timers/Counters for CapSense Scanning
  - ❐ Support Dual CSD Channels Simultaneous Scanning

- Programmable Pin Configurations:
  - ❐ 25 mA Sink on all GPIO
  - ❐ Pull up, Pull down, High Z, Strong, or Open Drain Drive Modes on all GPIO
  - ❐ Up to 38 Analog Inputs on GPIO
  - ❐ Configurable Interrupt on all GPIO

- Additional System Resources:
  - ❐ I^{2}C™ Slave, Master, and MultiMaster to 400 kHz, Supports Hardware Addressing Feature
  - ❐ Watchdog and Sleep Timers
  - ❐ User Configurable Low Voltage Detection
  - ❐ Integrated Supervisory Circuit
  - ❐ On-Chip Precision Voltage Reference
  - ❐ Supports RTC Block into Digital Peripheral Logic

Top Level Block Diagram

Cypress Semiconductor Corporation • 198 Champion Court • San Jose, CA 95134-1709 • 408-943-2600
Document Number: 001-43084 Rev. *H
Revised March 16, 2009

[+] Feedback

PSoC® Functional Overview

The PSoC® family consists of many On-Chip Controller devices. These devices are designed to replace multiple traditional MCU-based system components with one low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts and packages.

The PSoC architecture, shown in Figure 1, consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing allows the combining of all the device resources into a complete custom system. The PSoC family can have up to five IO ports connecting to the global digital and analog interconnects, providing access to eight digital blocks and six analog blocks.

PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with 21 vectors, to simplify the programming of real time embedded events.

Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory encompasses 16 KB of Flash for program storage, 1K bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator). The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. If crystal accuracy is required, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC), and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin can also generate a system interrupt on high level, low level, and change from last read.

Digital System

The Digital System is composed of eight digital PSoC blocks. Each block is an 8-bit resource that may be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram
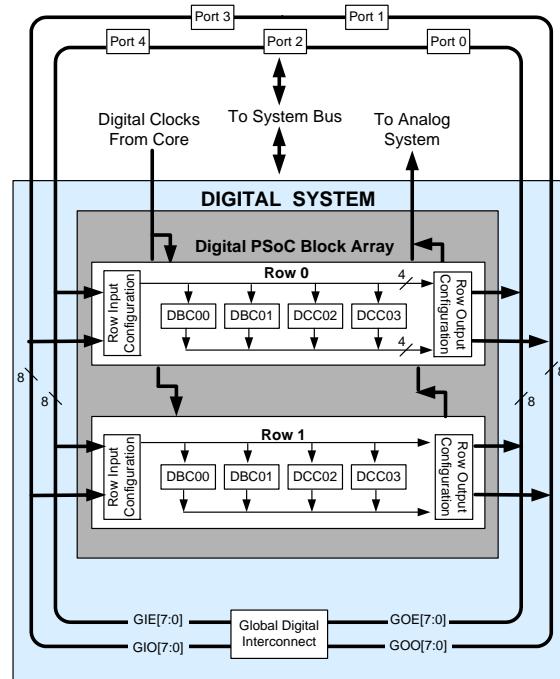
Digital peripheral configurations are:

- PWMs (8 to 32-Bit)

- PWMs with Dead band (8 to 32-Bit)

- Counters (8 to 32-Bit)

- Timers (8 to 32-Bit)

- UART 8 Bit with Selectable Parity (Up to Two)

- SPI Master and Slave (Up to Two)

- Shift Register (1 to 32-Bit)

- I2C Slave and Master (One Available as a System Resource)

- Cyclical Redundancy Checker/Generator (8 to 32-Bit)

- IrDA (Up to Two)

- Pseudo Random Sequence Generators (8 to 32-Bit)

The digital blocks may be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This provides a choice of system resources for your application. Family resources are shown in Table 1 on page 3.

[+] Feedback

Analog System

The Analog System consists of a 10-bit SAR ADC and six configurable blocks.

The programmable 10-bit SAR ADC is an optimized ADC that could be run up to 200 ksps with ± 1.5 LSB DNL and ± 2.5 LSB INL (true for $V_{DD} \geq 3.0V$ and Vref $\geq 3.0V$). External filters are required on ADC input channels for antialiasing. This ensures that any out-of-band content is not folded into the input signal band.

Reconfigurable analog resources allow creating complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-Digital converters (Single or Dual, with 8-bit resolution)

- Pin-to-pin Comparator

- Single ended comparators with absolute (1.3V) reference or 5-bit DAC reference

- 1.3V reference (as a System Resource)

Analog blocks are provided in columns of four, which include CT-E (Continuous Time) and SC-E (Switched Capacitor) blocks. These devices provide limited functionality Type "E" analog blocks.

Figure 2. Analog System Block Diagram
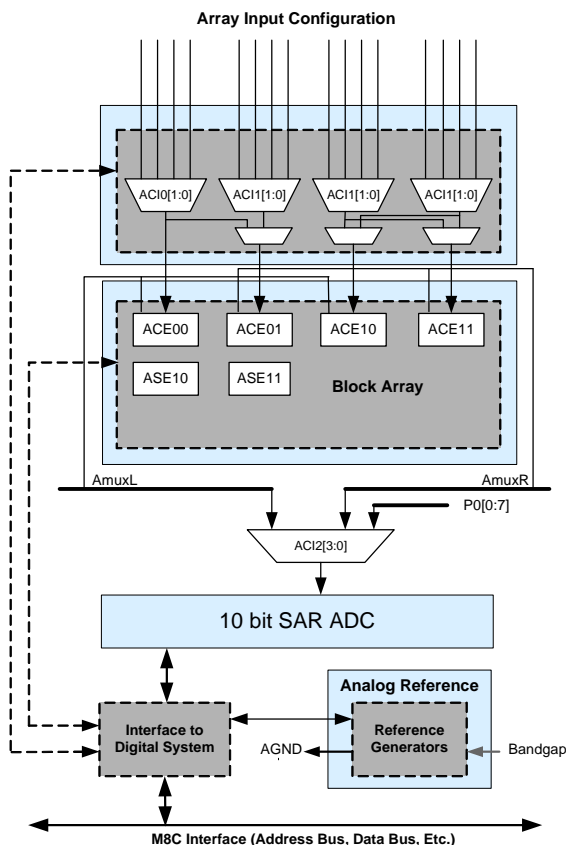
Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a MAC, low voltage detection, and power on reset. The merits of each system resource are:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks may be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.

- Additional Digital resources and clocks optimized for CSD.

- Support "RTC" block into digital peripheral logic.

- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math and digital filters.

- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.

- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.

- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital IO	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks
CY8C29x66	up to 64	4	16	12	4	4	12
CY8C27x66	up to 44	2	8	12	4	4	12
CY8C27x43	up to 44	2	8	12	4	4	12
CY8C22x45	**up to 38**	**2**	**8**	**10**	**0**	**4**	**6[a]**
CY8C21x34	up to 28	1	4	28	0	2	4[a]
CY8C21345	up to 24	1	4	10	0	4	6[a]
CY8C24x23	up to 24	1	4	12	2	2	6
CY8C24x33	up to 26	1	4	12	2	2	4

a. Limited analog functionality.

[+] Feedback

Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the *PSoC Programmable System-on-Chip Technical Reference Manual* for CY8C28xxx PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at www.cypress.com/psoc.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: www.cypress.com/psoc. Select Application Notes under the Documentation tab.

Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

Solutions Library

Visit our growing library of solution focused designs at www.cypress.com/solutions. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

PSoC Designer Software Subsystems

System-Level View

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC programmable system-on-chip controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.4. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select components
2. Configure components
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

Both the system-level and chip-level views provide a library of prebuilt, pretested hardware peripheral components. In the system-level view, these components are called "drivers" and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I^2C-bus, for example), and the logic to control how they interact with one another (called valuators).

In the chip-level view, the components are called "user modules". User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and programmable system-on-chip varieties.

Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in the PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

[+] Feedback

Organize and Connect

You can build signal chains at the chip level by interconnecting user modules to each other and the IO pins, or connect system level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view, selecting a potentiometer driver to control a variable speed fan driver and setting up the valuators to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog to digital converter (ADC) to convert the potentiometer's output to a digital signal, and a PWM to control the fan.

In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the "Generate Application" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

The system-level design also generates a C main() program that completely controls the chosen application and contains place-holders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside the PSoC Designer's Debugger subsystem. The Debugger downloads the HEX image to the In-Circuit Emulator (ICE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this data sheet.

Table 2. Acronyms

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose IO
ICE	in-circuit emulator
IDE	integrated development environment
IO	input/output
IPOR	imprecise power on reset
LSb	least significant bit
LVD	low voltage detect
MSb	most significant bit
PC	program counter
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip
PWM	pulse width modulator
RAM	random access memory
ROM	read only memory
SC	switched capacitor
SMP	switch mode pump

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 5 on page 9 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, 01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimal.
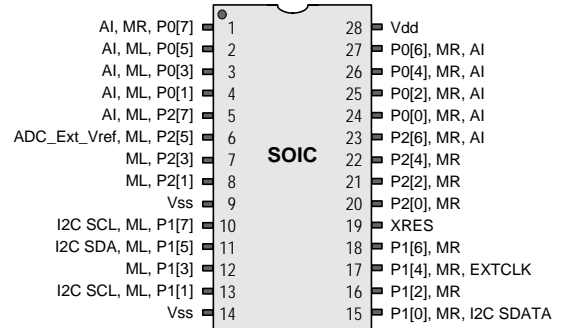
Pinouts

This PSoC device family is available in a variety of packages that are listed in the following tables. Every port pin (labeled with a "P") is capable of Digital IO. However, Vss, Vdd, and XRES are not capable of Digital IO.

CY8C22345, CY8C21345 28-Pin SOIC

Table 3. Pin Definitions

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I, MR	P0[7]	Integration Capacitor for MR
2	IO	I, ML	P0[5]	Integration Capacitor for ML
3	IO	I, ML	P0[3]	
4	IO	I, ML	P0[1]	
5	IO	I, ML	P2[7]	To Compare Column 0
6	IO	ML	P2[5]	Optional ADC External Vref
7	IO	ML	P2[3]	
8	IO	ML	P2[1]	
9	Power		Vss	Ground Connection
10	IO	ML	P1[7]	I2C Serial Clock (SCL)
11	IO	ML	P1[5]	I2C Serial Data (SDA)
12	IO	ML	P1[3]	
13	IO	ML	P1[1]*	I2C Serial Clock (SCL), ISSP-SCLK
14	Power		Vss	Ground Connection
15	IO	MR	P1[0]*	I2C Serial Clock (SCL), ISSP-SDATA
16	IO	MR	P1[2]	
17	IO	MR	P1[4]	Optional External Clock Input (EXT-CLK)
18	IO	MR	P1[6]	
19	Input		XRES	Active High Pin Reset with Internal Pull Down
20	IO	MR	P2[0]	
21	IO	MR	P2[2]	
22	IO	MR	P2[4]	
23	IO	I, MR	P2[6]	To Compare Column 1
24	IO	I, MR	P0[0]	
25	IO	I, MR	P0[2]	
26	IO	I, MR	P0[4]	
27	IO	I, MR	P0[6]	
28	Power		Vdd	Supply Voltage

Figure 3. Pin Diagram


```
AI, MR, P0[7] ─┤ 1         28 ├─ Vdd
AI, ML, P0[5] ─┤ 2         27 ├─ P0[6], MR, AI
AI, ML, P0[3] ─┤ 3         26 ├─ P0[4], MR, AI
AI, ML, P0[1] ─┤ 4         25 ├─ P0[2], MR, AI
AI, ML, P2[7] ─┤ 5         24 ├─ P0[0], MR, AI
ADC_Ext_Vref, ML, P2[5] ─┤ 6   23 ├─ P2[6], MR, AI
ML, P2[3] ─┤ 7   SOIC      22 ├─ P2[4], MR
ML, P2[1] ─┤ 8             21 ├─ P2[2], MR
Vss ─┤ 9                   20 ├─ P2[0], MR
I2C SCL, ML, P1[7] ─┤ 10   19 ├─ XRES
I2C SDA, ML, P1[5] ─┤ 11   18 ├─ P1[6], MR
ML, P1[3] ─┤ 12            17 ├─ P1[4], MR, EXTCLK
I2C SCL, ML, P1[1] ─┤ 13   16 ├─ P1[2], MR
Vss ─┤ 14                  15 ├─ P1[0], MR, I2C SDATA
```

LEGEND: A = Analog, I = Input, O = Output, M=Analog Mux input, MR= Analog Mux right input, ML= Analog Mux left input, * ISSP pin which is not HiZ at POR.

[+] Feedback

CY8C22545 44-Pin TQFP

Table 4. Pin Definitions

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	ML	P2[5]	Optional ADC External Vref
2	IO	ML	P2[3]	
3	IO	ML	P2[1]	
4	Power		Vdd	Supply Voltage
5	IO	ML	P4[5]	
6	IO	ML	P4[3]	
7	IO	ML	P4[1]	
8	Power		Vss	Ground Connection
9	IO	ML	P3[7]	
10	IO	ML	P3[5]	
11	IO	ML	P3[3]	
12	IO	ML	P3[1]	
13	IO	ML	P1[7]	I2C Serial Clock (SCL)
14	IO	ML	P1[5]	I2C Serial Data (SDA)
15	IO	ML	P1[3]	
16	IO	ML	P1[1]*	Crystal (XTALin), I2C Serial Clock (SCL), TC SCLK
17	Power		Vss	Ground Connection
18	IO	MR	P1[0]*	Crystal (XTALout), I2C Serial Data (SDA), TC SDATA
19	IO	MR	P1[2]	
20	IO	MR	P1[4]	Optional External Clock Input (EXTCLK)
21	IO	MR	P1[6]	
22	IO	MR	P3[0]	
23	IO	MR	P3[2]	
24	IO	MR	P3[4]	
25	IO	MR	P3[6]	
26	Input		XRES	Active High Pin Reset with Internal Pull Down
27	IO	MR	P4[0]	
28	IO	MR	P4[2]	
29	IO	MR	P4[4]	
30	Power		Vss	Ground Connection
31	IO	MR	P2[0]	
32	IO	MR	P2[2]	
33	IO	MR	P2[4]	
34	IO	I, MR	P2[6]	To Compare Column 1
35	IO	I, MR	P0[0]	
36	IO	I, MR	P0[2]	
37	IO	I, MR	P0[4]	

Figure 4. Pin Diagram

[+] Feedback
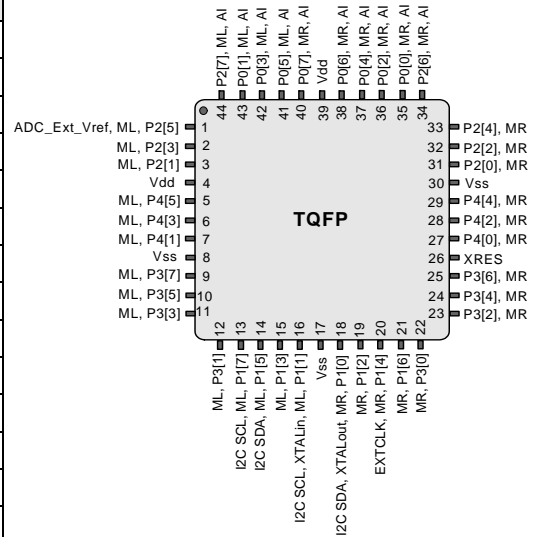
Table 4. Pin Definitions (continued)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
38	IO	I, MR	P0[6]	
39	Power		Vdd	Supply Voltage
40	IO	I, MR	P0[7]	Integration Capacitor for MR
41	IO	I, ML	P0[5]	Integration Capacitor for ML
42	IO	I, ML	P0[3]	
43	IO	I, ML	P0[1]	
44	IO	I, ML	P2[7]	To Compare Column 0

LEGEND: A = Analog, I = Input, O = Output, M=Analog Mux input, MR= Analog Mux right input, ML= Analog Mux left input, * ISSP pin which is not HiZ at POR.

Register Reference

This section lists the registers of this PSoC device family by mapping tables. For detailed register information, refer the PSoC Programmable System-on Chip Technical Reference Manual.

Register Conventions

Abbreviations Used

The register conventions specific to this section are listed in the following table.

Table 5. Abbreviations

Convention	Description
RW	Read and write register or bit(s)
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is also referred to as IO space and is broken into two parts. The XOI bit in the Flag register determines which bank the user is currently in. When the XOI bit is set, the user is said to be in the "extended" address space or the "configuration" registers.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 6. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40	#	ASC10CR0*	80*	RW		C0	RW
PRT0IE	01	RW		41	W		81	RW		C1	RW
PRT0GS	02	RW		42	RW		82	RW		C2	RW
PRT0DM2	03	RW		43	#		83	RW		C3	RW
PRT1DR	04	RW		44	#	ASD11CR0*	84*	RW		C4	RW
PRT1IE	05	RW		45	W		85	RW		C5	RW
PRT1GS	06	RW		46	RW		86	RW		C6	RW
PRT1DM2	07	RW		47	#		87	RW		C7	RW
PRT2DR	08	RW		48	#		88	RW	PWMVREF0	C8	#
PRT2IE	09	RW		49	W		89	RW	PWMVREF1	C9	#
PRT2GS	0A	RW		4A	RW		8A	RW	IDAC_MODE	CA	RW
PRT2DM2	0B	RW		4B	#		8B	RW	PWM_SRC	CB	#
PRT3DR	0C	RW		4C	#		8C	RW	TS_CR0	CC	RW
PRT3IE	0D	RW		4D	W		8D	RW	TS_CMPH	CD	RW
PRT3GS	0E	RW		4E	RW		8E	RW	TS_CMPL	CE	RW
PRT3DM2	0F	RW		4F	#		8F	RW	TS_CR1	CF	RW
PRT4DR	10	RW	CSD0_DR0_L	50	R		90	RW	CUR PP	D0	RW
PRT4IE	11	RW	CSD0_DR1_L	51	W		91	RW	STK_PP	D1	RW
PRT4GS	12	RW	CSD0_CNT_L	52	R		92	RW	PRV PP	D2	RW
PRT4DM2	13	RW	CSD0_CR0	53	#		93	RW	IDX_PP	D3	RW
	14	RW	CSD0_DR0_H	54	R		94	RW	MVR_PP	D4	RW
	15	RW	CSD0_DR1_H	55	W		95	RW	MVW_PP	D5	RW
	16	RW	CSD0_CNT_H	56	R		96	RW	I2C0_CFG	D6	RW
	17	RW	CSD0_CR1	57	RW		97	RW	I2C0_SCR	D7	#
	18	RW	CSD1_DR0_L	58	R		98	RW	I2C0_DR	D8	RW
	19	RW	CSD1_DR1_L	59	W		99	RW	I2C0_MSCR	D9	#
	1A	RW	CSD1_CNT_L	5A	R		9A	RW	INT_CLR0	DA	RW
	1B	RW	CSD1_CR0	5B	#		9B	RW	INT_CLR1	DB	RW
	1C	RW	CSD1_DR0_H	5C	R		9C	RW	INT_CLR2	DC	RW
	1D	RW	CSD1_DR1_H	5D	W		9D	RW	INT_CLR3	DD	RW
	1E	RW	CSD1_CNT_H	5E	R		9E	RW	INT_MSK3	DE	RW
	1F	RW	CSD_CR1	5F	RW		9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW		A1		INT_MSK1	E1	RW
DBC00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RW
DBC01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RW
DBC01DR2	26	RW	CMP_CR1	66	RW		A6		DEC _CR0*	E6	RW
DBC01CR0	27	#		67	RW		A7		DEC_CR1*	E7	RW
DCC02DR0	28	#	ADC0_CR	68	#		A8	W	MUL0_X	E8	W
DCC02DR1	29	W	ADC1_CR	69	#		A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW		AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW		AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW		AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW		AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW		AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW		AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#		70	RW	RDI0RI	B0	RW	CPU A	F0	#
DBC10DR1	31	W		71	RW	RDI0SYN	B1	RW	CPU_T1	F1	#
DBC10DR2	32	RW	ACB00CR1*	72*	RW	RDI0IS	B2	RW	CPU_T2	F2	#
DBC10CR0	33	#	ACB00CR2*	73*	RW	RDI0LT0	B3	RW	CPU_X	F3	#
DBC11DR0	34	#		74	RW	RDI0LT1	B4	RW	CPU PCL	F4	#
DBC11DR1	35	W		75	RW	RDI0RO0	B5	RW	CPU_PCH	F5	#
DBC11DR2	36	RW	ACB01CR1*	76*	RW	RDI0RO1	B6	RW	CPU_SP	F6	#
DBC11CR0	37	#	ACB01CR2*	77*	RW	RDI0DSM	B7	RW	CPU_F	F7	I
DCC12DR0	38	#		78	RW	RDI1RI	B8	RW	CPU_TST0	F8	RW
DCC12DR1	39	W		79	RW	RDI1SYN	B9	RW	CPU_TST1	F9	RW
DCC12DR2	3A	RW		7A	RW	RDI1IS	BA	RW	CPU_TST2	FA	RW
DCC12CR0	3B	#		7B	RW	RDI1LT0	BB	RW	CPU TST3	FB	#
DCC13DR0	3C	#		7C	RW	RDI1LT1	BC	RW	DAC1_D	FC	RW

Shaded fields are Reserved and must not be accessed.   **# Access is bit specific. * has a different meaning.**

[+] Feedback

Table 6. Register Map Bank 0 Table: User Space (continued)

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
DCC13DR1	3D	W		7D	RW	RDI1RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW		7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Shaded fields are Reserved and must not be accessed.   **# Access is bit specific. * has a different meaning.**

Table 7. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	0	RW		40	RW	ASC10CR0*	80*	RW		C0	RW
PRT0DM1	1	RW		41	RW		81	RW		C1	RW
PRT0IC0	2	RW		42	RW		82	RW		C2	RW
PRT0IC1	3	RW		43			83	RW		C3	RW
PRT1DM0	4	RW		44	RW	ASD11CR0*	84*	RW		C4	RW
PRT1DM1	5	RW		45	RW		85	RW		C5	RW
PRT1IC0	6	RW		46	RW		86	RW		C6	RW
PRT1IC1	7	RW		47			87	RW		C7	RW
PRT2DM0	8	RW		48	RW		88	RW		C8	#
PRT2DM1	9	RW		49	RW		89	RW		C9	RW
PRT2IC0	0A	RW		4A	RW		8A	RW		CA	RW
PRT2IC1	0B	RW		4B			8B	RW		CB	RW
PRT3DM0	0C	RW		4C	RW		8C	RW		CC	#
PRT3DM1	0D	RW		4D	RW		8D	RW		CD	RW
PRT3IC0	0E	RW		4E	RW		8E	RW		CE	RW
PRT3IC1	0F	RW		4F			8F	RW		CF	RW
PRT4DM0	10	RW	CMP0CR1	50	RW		90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW	CMP0CR2	51	RW		91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52	RW		92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW	VDAC50CR0	53	RW		93	RW	GDI_E_OU	D3	RW
	14	RW	CMP1CR1	54	RW		94	RW		D4	RW
	15	RW	CMP1CR2	55	RW		95	RW		D5	RW
	16	RW		56	RW		96	RW		D6	RW
	17	RW	VDAC51CR0	57	RW		97	RW		D7	RW
	18	RW	CSCMPCR0	58	#		98	RW	MUX_CR0	D8	RW
	19	RW	CSCMPGOEN	59	RW		99	RW	MUX_CR1	D9	RW
	1A	RW	CSLUTCR0	5A	RW		9A	RW	MUX_CR2	DA	RW
	1B	RW	CMPCOLMUX	5B	RW		9B	RW	MUX_CR3	DB	RW
	1C	RW	CMPPWMCR	5C	RW		9C	RW	DAC_CR1#	DC	RW
	1D	RW	CMPFLTCR	5D	RW		9D	RW	OSC_GO_EN	DD	RW
	1E	RW	CMPCLK1	5E	RW		9E	RW	OSC_CR4	DE	RW
	1F	RW	CMPCLK0	5F	RW		9F	RW	OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	R
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW	ADC0_TR*	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR*	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	V2BG_TR	E7	RW
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	W
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	W
DCC02OU	2A	RW		6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DBC02CR1	2B	RW	CLK_CR3	6B	RW	SADC_CR3TRIM	AB	RW	ECO_TR	EB	W
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_AD	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE	RW	MUX_CR6	EE	RW
DBC03CR1	2F	RW	TMP_DR3	6F	RW		AF	RW	MUX_CR7	EF	RW
DBC10FN	30	RW		70	RW	RDI0RI	B0	RW	CPU A	F0	#
DBC10IN	31	RW		71	RW	RDI0SYN	B1	RW	CPU_T1	F1	#
DBC10OU	32	RW	ACB00CR1*	72	RW	RDI0IS	B2	RW	CPU_T2	F2	#
DBC10CR1	33	RW	ACB00CR2*	73	RW	RDI0LT0	B3	RW	CPU_X	F3	#

Shaded fields are Reserved and must not be accessed.   **# Access is bit specific. * has a different meaning.**

[+] Feedback

Table 7. Register Map Bank 1 Table: Configuration Space (continued)

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
DBC11FN	34	RW		74	RW	RDI0LT1	B4	RW	CPU_PCL	F4	#
DBC11IN	35	RW		75	RW	RDI0RO0	B5	RW	CPU_PCH	F5	#
DBC11OU	36	RW	ACB01CR1*	76*	RW	RDI0RO1	B6	RW	CPU_SP	F6	#
DBC11CR1	37	RW	ACB01CR2*	77*	RW	RDI0DSM	B7	RW	CPU_F	F7	I
DCC12FN	38	RW		78	RW	RDI1RI	B8	RW	FLS_PR0	F8	RW
DCC12IN	39	RW		79	RW	RDI1SYN	B9	RW	FLS TR	F9	W
DCC12OU	3A	RW		7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
DBC12CR1	3B	RW		7B	RW	RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C	RW	RDI1LT1	BC	RW	FAC_CR0	FC	SW
DCC13IN	3D	RW		7D	RW	RDI1RO0	BD	RW	DAC_CR0#	FD	RW
DCC13OU	3E	RW		7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DBC13CR1	3F	RW		7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Shaded fields are Reserved and must not be accessed.   **# Access is bit specific. * has a different meaning.**

[+] Feedback

Electrical Specifications

This section presents the DC and AC electrical specifications of this PSoC device family. For the latest electrical specifications, check the most recent data sheet by visiting the web at http://www.cypress.com/psoc.

Specifications are valid for -40°C $\leq T_A \leq$ 85°C and $T_J \leq$ 100°C, except where noted. Specifications for devices running at greater than 12 MHz are valid for -40°C $\leq T_A \leq$ 70°C and $T_J \leq$ 82°C.

Figure 5. Voltage versus Operating Frequency
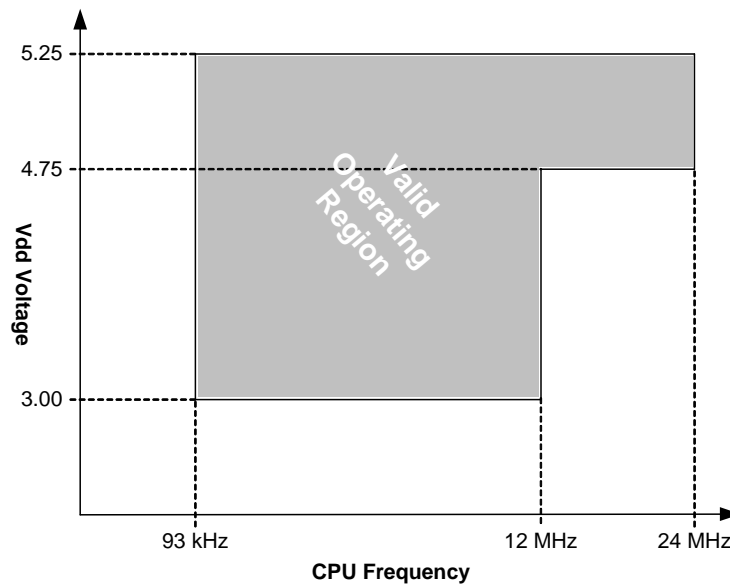
The following table lists the units of measure that are used in this section.

Table 8. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	μW	micro watts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nano ampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	W	ohm
MHz	megahertz	pA	pico ampere
MΩ	megaohm	pF	pico farad
μA	micro ampere	pp	peak-to-peak
μF	micro farad	ppm	parts per million
μH	micro henry	ps	picosecond
μs	microsecond	sps	samples per second
μV	micro volts	s	sigma: one standard deviation
μVrms	micro volts root-mean-square	V	volts

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 9. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	–	+100	°C	Higher storage temperatures reduce data retention time
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IOz}	DC Voltage Applied to Tristate	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD
LU	Latch up Current	–	–	200	mA	

Operating Temperature

Table 10. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 31 on page 25. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip Level Specifications

Table 11 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C, and are for design guidance only, unless specified otherwise.

Table 11. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	3.0	–	5.25	V	See Table 18 on page 17
I_{DD}	Supply Current	–	7	12	mA	Conditions are Vdd = 5.0V, 25°C, CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz VC2 = 93.75 kHz VC3 = 93.75 kHz
I_{DD3}	Supply Current	–	4	7	mA	Conditions are Vdd = 3.3V T_A = 25°C, CPU = 3 MHz 48 MHz = Disabled VC1 = 1.5 MHz, VC2 = 93.75 kHz VC3 = 93.75 kHz
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT[a]	–	3	6.5	μA	Conditions are with internal slow speed oscillator, Vdd = 3.3V -40°C <= T_A <= 55°C
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature[a]	–	4	25	μA	Conditions are with internal slow speed oscillator, Vdd = 3.3V 55°C < T_A <= 85°C
I_{SBXTL}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal [a]	–	4	7.5	μA	Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. Vdd = 3.3V, -40°C <= T_A <= 55°C
I_{SBXTLH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature [a]	–	5	26	μA	Conditions are with properly loaded, 1μW max, 32.768 kHz crystal. Vdd = 3.3 V, 55°C < T_A <= 85°C
V_{REF}	Reference Voltage (Bandgap)	1.275	1.3	1.325	V	Trimmed for appropriate Vdd

a. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This must be compared with devices that have similar functions enabled.

DC General Purpose IO Specifications

Table 12 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only, unless otherwise specified.

Table 12. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (80 mA maximum combined IOH budget)
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (100 mA maximum combined IOL budget)
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.0 to 5.25
V_{IH}	Input High Level	2.1	–		V	Vdd = 3.0 to 5.25

[+] Feedback

Table 12. DC GPIO Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C

DC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C respectively. Typical parameters apply to 5V or 3.3V at 25°C and are for design guidance only.

Table 13. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	10	–	μV/°C	
I_{EBOA}[a]	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 μA
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C
V_{CMOA}	Common Mode Voltage Range	0.0	–	Vdd - 1	V	

a. Atypical behavior: I_{EBOA} of Port 0 Pin 0 is below 1 nA at 25°C; 50 nA over temperature. Use Port 0 Pins 1-7 for the lowest leakage of 200 nA.

Table 14. 3.3V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	10	–	μV/°C	
I_{EBOA}[a]	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 μA
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C
V_{CMOA}	Common Mode Voltage Range	0	–	Vdd - 1	V	

a.Atypical behavior: I_{EBOA} of Port 0 Pin 0 is below 1 nA at 25°C; 50 nA over temperature. Use Port 0 Pins 1-7 for the lowest leakage of 200 nA.

DC Low Power Comparator Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 15. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	Vdd - 1	V
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV

SAR10 ADC DC Specifications

Table 16 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C and are for design guidance only.

Table 16.   SAR10 ADC DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{adcvref}$	Reference voltage at pin P2[5] when configured as ADC reference voltage	3.0	–	5.25	V	When V_{REF} is buffered inside ADC, the voltage level at P2[5] (when configured as ADC reference voltage) must be always maintained to be at least 300 mV less than the chip supply voltage level on Vdd pin. ($V_{adcvref}$ < Vdd)
$I_{adcvref}$	Current when P2[5] is configured as ADC V_{REF}	-	–	0.5	mA	Disables the internal voltage reference buffer
INL at 10 bits	Integral Nonlinearity	-2.5	–	2.5	LSB	For V_{DD} ≥ 3.0V and Vref ≥ 3.0V
		-5.0	–	5.0	LSB	For V_{DD} < 3.0V or Vref < 3.0V
DNL at 10 bits	Differential Nonlinearity	-1.5	–	1.5	LSB	For V_{DD} ≥ 3.0V and Vref ≥ 3.0V
		-4.0	–	4.0	LSB	For V_{DD} < 3.0V or Vref < 3.0V
SPS	Sample per second	–	–	150	ksps	Resolution 10 bits

DC Analog Mux Bus Specifications

Table 17 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C and are for design guidance only.

Table 17.   DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch Resistance to Common Analog Bus	–	–	400	Ω	Vdd ≥ 3.00
R_{gnd}	Resistance of Initialization Switch to gnd	–	–	800	Ω	

DC POR and LVD Specifications

Table 18 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C and are for design guidance only.

Table 18.   DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PPOR1} V_{PPOR2}	Vdd Value for PPOR Trip PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	2.82 4.55	2.95 4.70	V V	Vdd must be greater than or equal to 3.0V during startup, reset from the XRES pin, or reset from Watchdog.
V_{LVD2} V_{LVD3} V_{LVD4} V_{LVD5} V_{LVD6} V_{LVD7}	Vdd Value for LVD Trip VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.95 3.06 4.37 4.50 4.62 4.71	3.02 3.13 4.48 4.64 4.73 4.81	3.09 3.20 4.55 4.75 4.83 4.95	V V V V V V	

[+] Feedback

DC Programming Specifications

Table 19 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C and are for design guidance only.

Table 19. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd$_{IWRITE}$	Supply Voltage for Flash Write Operations	2.70	–	–	V	
I$_{DDP}$	Supply Current during Programming or Verify	–	5	25	mA	
V$_{ILP}$	Input Low Voltage during Programming or Verify	–	–	0.8	V	
V$_{IHP}$	Input High Voltage during Programming or Verify	2.2	–	–	V	
I$_{ILP}$	Input Current when Applying Vilp to P1[0] or P1[1] during Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor
I$_{IHP}$	Input Current when Applying Vihp to P1[0] or P1[1] during Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor
V$_{OLV}$	Output Low Voltage during Programming or Verify	–	–	Vss + 0.75	V	
V$_{OHV}$	Output High Voltage during Programming or Verify	Vdd - 1.0	–	Vdd	V	
Flash$_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block
Flash$_{ENT}$	Flash Endurance (total)[a]	1,800,000	–	–	–	Erase/write cycles
Flash$_{DR}$	Flash Data Retention	10	–	–	Years	

a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

b. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

AC Electrical Characteristics

AC Chip Level Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C and are for design guidance only.

Table 20. 5V and 3.3V AC Chip-Level Specifications

Symbol	Description	Min	Min(%)	Typ	Max	Max(%)	Units	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	22.8		24	25.2[a,b,c]		MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 5 on page 13. SLIMO mode = 0 < 85
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.75	8	6	6.35[a,b,c]	8	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 5 on page 13. SLIMO mode = 0 < 85
F_{CPU1}	CPU Frequency (5V Nominal)	0.93		24	24.6[a,b]		MHz	24 MHz only for SLIMO mode = 0
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93		12	12.3[b,c]		MHz	
F_{BLK5}	Digital PSoC Block Frequency (5V Nominal)	0		48	49.2[a,b,d]		MHz	Refer to Table 25 on page 21.
F_{BLK33}	Digital PSoC Block Frequency (3.3V Nominal)	0		24	24.6[b,d]		MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15		32	75		kHz	
F_{32KU}	Untrimmed Internal Low Speed Oscillator Frequency	5		-	-		kHz	The ILO is not adjusted with the factory trim values until after the CPU starts running. See the "System Resets" section in the Technical Reference Manual.
Jitter32k	32 kHz RMS Period Jitter	–		100	--		ns	
T_{XRST}	External Reset Pulse Width	10		–	–		µs	
DC24M	24 MHz Duty Cycle	40		50	60		%	
Jitter24M1	24 MHz Period Jitter (IMO)	–		300	600		ps	
F_{MAX}	Maximum frequency of signal on row input or row output	–		–	12.3		MHz	
T_{RAMP}	Supply Ramp Time	25		–	–		µs	

a. Valid only for 4.75V < Vdd < 5.25V.
b. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
c. 3.0V < Vdd < 3.6V. See Application Note AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on trimming for opera-
     tion at 3.3V.
d. Refer to the individual user module data sheets for information on maximum frequencies for user modules.

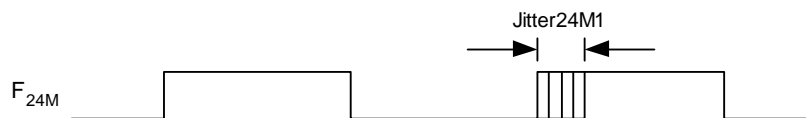**Figure 6. 24 MHz Period Jitter (IMO) Timing Diagram**

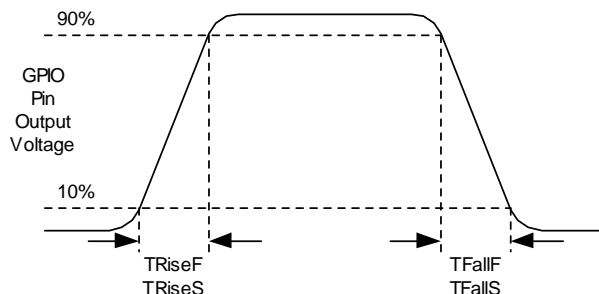**Figure 7. 32 kHz Period Jitter (ILO) Timing Diagram**

AC General Purpose IO Specifications

Table 21 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C and are for design guidance only.

Table 21. 5V and 3.3V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	7	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	7	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

Figure 8. GPIO Timing Diagram

AC Operational Amplifier Specifications

Table 22 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C and are for design guidance only.

Table 22. AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP}	Comparator Mode Response Time, 50 mV			100	ns	Vdd ≥ 3.0V

AC Low Power Comparator Specifications

Table 23 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 23. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}

AC Analog Mux Bus Specifications

Table 24 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C and are for design guidance only.

Table 24. AC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{SW}	Switch Rate	–	–	3.17	MHz	

AC Digital Block Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq$ T$_A$ $\leq$ 85°C or 3.0V to 3.6V and -40°C $\leq$ T$_A$ $\leq$ 85°C, respectively. Typical parameters apply to 5V or 3.3V, at 25°C and are for design guidance only.

Table 25. 5V and 3.3V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency (> 4.75V)			49.2	MHz	4.75V < Vdd < 5.25V
	Maximum Block Clocking Frequency (< 4.75V)			24.6	MHz	3.0V < Vdd < 4.75V
Timer	Capture Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.2	MHz	4.75V < Vdd < 5.25V
	Maximum Frequency, With or Without Capture	–	–	24.6	MHz	
Counter	Enable Pulse Width	50	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.2	MHz	4.75V < Vdd < 5.25V
	Maximum Frequency, Enable Input	–	–	24.6	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50	–	–	ns	
	Disable Mode	50	–	–	ns	
	Maximum Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	50	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking
	Maximum Input Clock Frequency with Vdd $\geq$ 4.75V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking
Receiver	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking
	Maximum Input Clock Frequency with Vdd $\geq$ 4.75V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking

   a. 50 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq$ T$_A$ $\leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq$ T$_A$ $\leq$ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C and are for design guidance only.

Table 26. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F$_{OSCEXT}$	Frequency	0.093	–	24.6	MHz
–	High Period	20.6	–	5300	ns
–	Low Period	20.6	–	–	ns
–	Power Up IMO to Switch	150	–	–	μs

Table 27. 3.3V AC External Clock Specifications

| Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power Up IMO to Switch	150	–	–	μs	

SAR10 ADC AC Specifications

Table 28 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 28. SAR10 ADC AC Specifications

Symbol	Description	Min	Typ	Max	Units
$Freq_3$	Input clock frequency 3V	–	–	2.7	MHz
$Freq_5$	Input clock frequency 5V	–	–	2.7	MHz

AC Programming Specifications

Table 29 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V, or 3.3V at 25°C and are for design guidance only.

Table 29. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
F_{SCLK3}	Frequency of SCLK3	0	–	6	MHz	V_{DD} < 3.6V
T_{ERASEB}	Flash Erase Time (Block)	–	15	–	ms	
T_{WRITE}	Flash Block Write Time	–	30	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	55	ns	3.6 < Vdd; at 30 pF Load
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	65	ns	3.0 $\leq$ Vdd $\leq$ 3.6; at 30 pF Load

AC I²C Specifications

Table 30 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq$ T$_A$ $\leq$ 85°C, and 3.0V to 3.6V and -40°C $\leq$ T$_A$ $\leq$ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 30. AC Characteristics of the I²C SDA and SCL Pins for Vdd $\geq$ 3.0V

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F$_{SCLI2C}$	SCL Clock Frequency	0	100	0	400	kHz
T$_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T$_{LOWI2C}$	LOW Period of the SCL Clock	4.7	–	1.3	–	µs
T$_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs
T$_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs
T$_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs
T$_{SUDATI2C}$	Data Setup Time	250	–	100[a]	–	ns
T$_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs
T$_{BUFI2C}$	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs
T$_{SPI2C}$	Pulse Width of spikes are suppressed by the Input Filter	–	–	0	50	ns

a. A Fast-Mode I2C-bus device may be used in a Standard-Mode I2C-bus system, but the requirement t$_{SU;DAT}$ $\geq$ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t$_{rmax}$ + t$_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Figure 9. Definition for Timing for Fast/Standard Mode on the I²C Bus

[+] Feedback
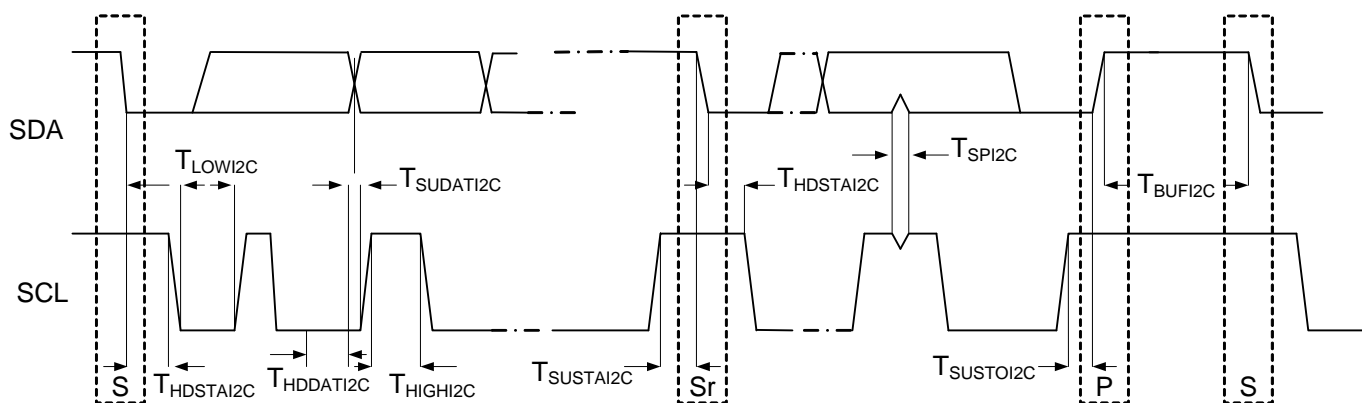
Packaging Information

This section provides the packaging specifications for this PSoC device with the thermal impedances for each package, and the typical package capacitance on crystal pins.
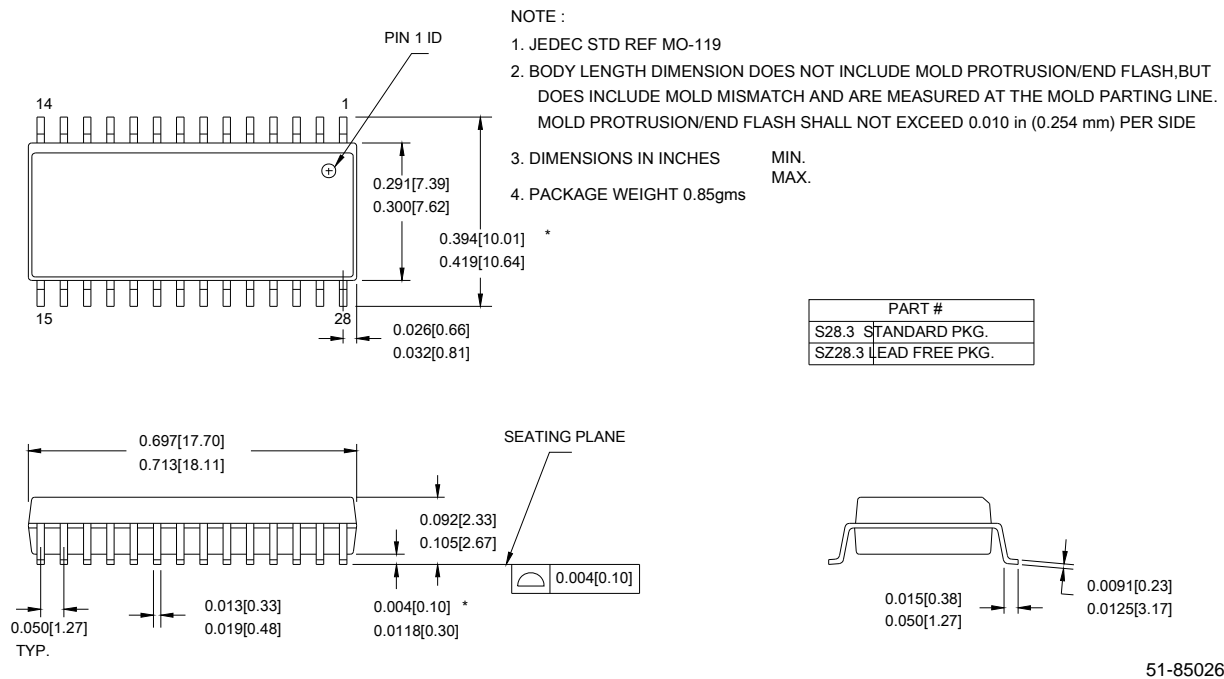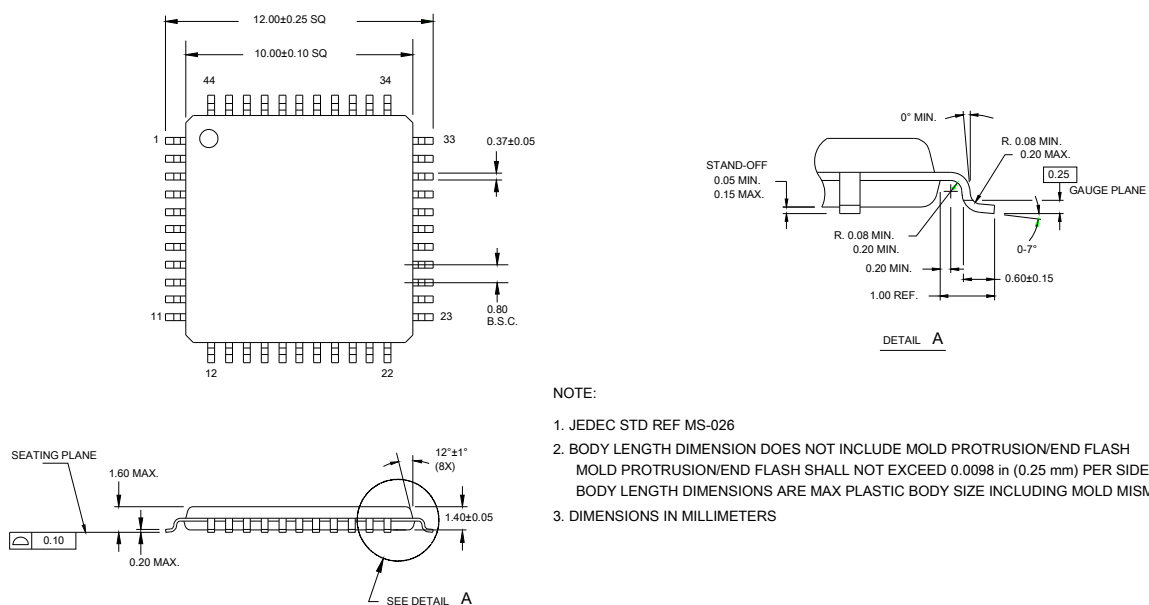
Packaging Dimensions

Figure 10. 28-Pin SOIC

NOTE :

1. JEDEC STD REF MO-119

2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH,BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.010 in (0.254 mm) PER SIDE

3. DIMENSIONS IN INCHES   MIN. / MAX.

4. PACKAGE WEIGHT 0.85gms

PART #	
S28.3	STANDARD PKG.
SZ28.3	LEAD FREE PKG.

51-85026 *D

Figure 11. 44-Pin TQFP

DETAIL A

NOTE:

1. JEDEC STD REF MS-026

2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH

3. DIMENSIONS IN MILLIMETERS

51-85064 *C

[+] Feedback

Thermal Impedances

Table 31. Thermal Impedances per Package

Package	Typical θ_{JA} *
28 SOIC	68°C/W
44 TQFP	61°C/W

* $T_J = T_A + POWER \times \theta_{JA}$

Capacitance on Crystal Pins

Table 32. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28 SOIC	2.7 pF
44 TQFP	2.6 pF

Ordering Information

The following table lists the key package features and ordering codes of this PSoC device family.

Table 33. PSoC Device Family Key Features and Ordering Information

Package	Ordering Code	Flash (Kbytes)	RAM (Bytes)	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital IO Pins	Analog Inputs	Analog Outputs	XRES Pin
28 SOIC	CY8C21345-24SXI	8	512B	-40°C to +85°C	4	6	24	10	0	Y
28 SOIC	CY8C22345-24SXI	16	1K	-40°C to +85°C	8	6	24	10	0	Y
44 TQFP	CY8C22545-24AXI	16	1K	-40°C to +85°C	8	6	38	10	0	Y

Ordering Code Definitions

CY 8 C 2x xxx-SPxx

Package Type:
- P = PDIP
- S = SOIC
- PV = SSOP
- LF = MLF
- A = TQFP

Thermal Rating:
- C = Commercial
- I = Industrial
- E = Extended

Speed: 24 MHz

Part Number

Family Code (21, 22)

Technology Code: C = CMOS

Marketing Code: 8 = Cypress PSoC

Company ID: CY = Cypress Semiconductor
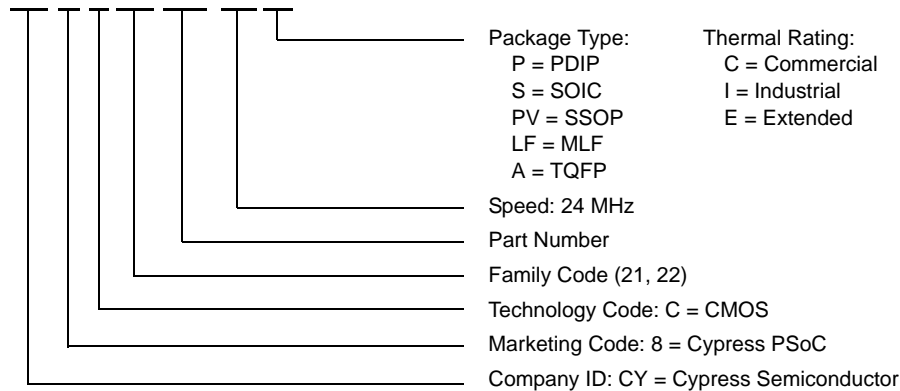
Document History Page

<table>
<tr><td colspan="5">Document Title: CY8C21345, CY8C22345, CY8C22545 PSoC® Programmable System-on-Chip™
Document Number: 001-43084</td></tr>
<tr><th>Revision</th><th>ECN</th><th>Orig. of Change</th><th>Submission Date</th><th>Description of Change</th></tr>
<tr><td>**</td><td>2251907</td><td>PMP/AESA</td><td>See ECN</td><td>New Data sheet</td></tr>
<tr><td>*A</td><td>2506377</td><td>EIJ/AESA</td><td>See ECN</td><td>Changed data sheet status to "Preliminary". Changed part numbers to CY8C22x45. Updated data sheet template.
Added 56-Pin OCD information. Added: "You must put filters on intended ADC input channels for anti-aliasing. This ensures that any out-of-band content is not folded into the Input Signal Band." To Section Analog System on page 3.
Corrected Minimum Electro Static Discharge Voltage in Table 9 on page 14.</td></tr>
<tr><td>*B</td><td>2558750</td><td>PMP/AESA</td><td>08/28/2008</td><td>Updated Features on page 1, PSoC Core on page 2, Analog System on page 3.
Changed DBB to DBC, and DCB to DCC in Register Tables Table 6 on page 10 and Table 7 on page 11.
Removed INL at 8 bit reference in Table 16 on page 17.
Changed IDD3 value Table 18 on page 17 Typ:3.3 mA, Max 6 mA
Added "3.0V < Vdd < 3.6V and -40C < T_A < 85C, IMO can guarantee 5% accuracy only" to Table 20 on page 19.
Updated data sheet template.</td></tr>
<tr><td>*C</td><td>2606793</td><td>NUQ/AESA</td><td>11/19/2008</td><td>Updated data sheet status to "Final". Updated block diagram on page 1.
Removed CY8C22045 56-Pin OCD information. Added part numbers CY8C21345, CY8C22345, and CY8C22545. For more details, see CDT 31271.</td></tr>
<tr><td>*D</td><td>2615697</td><td>PMP/AESA</td><td>12/03/2008</td><td>Confirmed CY8C22345 and CY8C21345 have same pinout on page 8.
Confirmed that IMO has 5% accuracy in Table 20 on page 19.</td></tr>
<tr><td>*E</td><td>2631733</td><td>PMP/PYRS</td><td>01/07/2009</td><td>Updated Table 16. SAR10 ADC DC Specifications and Table 29 AC Programming Specifications. Title changed to "CY8C21345, CY8C22345, CY8C22545 PSoC® Programmable System-on-Chip™"</td></tr>
<tr><td>*F</td><td>2648800</td><td>JHU/AESA</td><td>01/28/2009</td><td>Updated INL, DNL information in Table 16 on page 17, Development Tools on page 4, and T_{DSCLK} parameter in Table 29 on page 22.</td></tr>
<tr><td>*G</td><td>2658078</td><td>HMI/AESA</td><td>02/11/2009</td><td>Updated section Features on page 1.</td></tr>
<tr><td>*H</td><td>2667311</td><td>JHU/AESA</td><td>03/16/2009</td><td>Added parameter "F_{32KU}" and added Min% and Max % to parameter "F_{IMO6}" in Table 20 on page 19, according to updated SLIMO spec.</td></tr>
</table>

[+] Feedback

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products		PSoC Solutions	
PSoC	psoc.cypress.com	General	psoc.cypress.com/solutions
Clocks & Buffers	clocks.cypress.com	Low Power/Low Voltage	psoc.cypress.com/low-power
Wireless	wireless.cypress.com	Precision Analog	psoc.cypress.com/precision-analog
Memories	memory.cypress.com	LCD Drive	psoc.cypress.com/lcd-drive
Image Sensors	image.cypress.com	CAN 2.0b	psoc.cypress.com/can
		USB	psoc.cypress.com/usb

[+] Feedback