FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13738-1E

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90820 Series

MB90822/F822/F823/V820

■ DESCRIPTION

The MB90820 series is a line of general-purpose, Fujitsu 16-bit microcontrollers designed for process control applications which require high-speed real-time processing, such as consumer products.

While inheriting the AT architecture of the F²MC* family, the instruction set for the F²MC-16LX CPU core of the MB90820 series incorporates additional instructions for high-level languages, supports extended addressing modes, and contains enhanced multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions. In addition, the MB90820 series has an on-chip 32-bit accumulator which enables processing of long-word data.

The peripheral resources integrated in the MB90820 series include : an 8/10-bit A/D converter, 8-bit D/A converters, UARTs (SCI) 0, 1, multi-functional timer (16-bit free-running timer, input capture units (ICUs) 0 to 3, output compare units (OCUs) 0 to 5, 16-bit PPG timer 0, waveform generator), 16-bit PPG timer 1, 2, PWC 0, 1, 16-bit reload timer 0, 1 and DTP/external interrupt.

*: F²MC stands for FUJITSU Flexible Microcontroller, a registered trademark of FUJITSU LIMITED.

■ FEATURES

- Minimum execution time of instruction : 42 ns / 4 MHz oscillation (uses PLL clock multiplication) maximum multiplier = 6
- Maximum memory space
  16M bytes
  Linear/bank access

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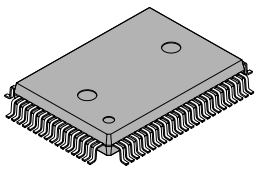
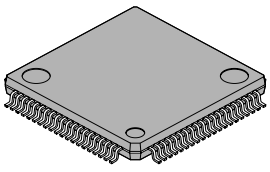
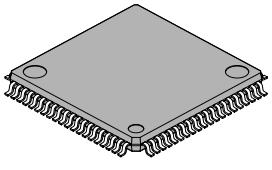
■ PACKAGES

80-pin plastic QFP	80-pin plastic LQFP	80-pin plastic LQFP
		
(FPT-80P-M06)	(FPT-80P-M05)	(FPT-80P-M11)

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- Instruction set optimized for controller applications
  Supported data types : bit, byte, word, and long-word types
  Standard addressing modes : 23 types
  32-bit accumulator enhancing high-precision operations
  Enhanced multiplication/division and RETI instructions
- Enhanced high level language (C) and multi-tasking support instructions
  Use of a system stack pointer
  Symmetrical instruction set and barrel shift instructions
- Program patch function (for two address pointers)
- Increased execution speed : 4-byte instruction queue
- Powerful interrupt function
  Up to eight priority levels programmable
  External interrupt inputs : 8 lines
- Automatic data transmission function independent of CPU operation
  Up to 16 channels for the extended intelligent I/O service
  DTP request inputs : 8 lines
- Internal ROM
  FLASH : 64/128K bytes with flash security
  MASKROM : 64K bytes
- Internal RAM
  EVA : 16K bytes
  FLASH : 4K bytes
  MASKROM : 4K bytes
- General-purpose ports
  Up to 66 channels (pull-up resistor settable input for : 32 channels)
- A/D Converter (RC) : 16 channels
  8/10-bit resolution selectable
  Conversion time : Min 3 µs at 24 MHz operating clock (including sampling time)
- 8-bit D/A Converter : 2 channels
- UART : 2 channels
- 16-bit PPG : 3 channels
  Mode switching function provided (PWM mode or one-shot mode)
  Channel 0 can be worked with multi-functional timer or independently
- 16-bit reload timer : 2 channels
- 16-bit PWC timer : 2 channels
- Multi-functional timer
  Input capture : 4 channels
  Output compare with selectable buffer : 6 channels
  Free-running timer with up or up-down mode selection and selectable buffer: 1 channel
  16-bit PPG : 1 channel
  Waveform generator : (16-bit timer : 3 channels, 3-phase waveform or dead time)
- Timebase counter/watchdog timer : 18-bit
- Low-power consumption mode :
  Sleep mode
  Stop mode
  CPU intermittent operation mode

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- Package :
  LQFP-80 (FPT-80P-M05 : 0.50 mm pitch)
  LQFP-80 (FPT-80P-M11 : 0.65 mm pitch)
  QFP-80 (FPT-80P-M06 : 0.80 mm pitch)
- CMOS technology

■ PRODUCT LINEUP

Part number / Item	MB90V820	MB90F822	MB90F823	MB90822
Classification	Development /evaluation product	Mass-produced products (Flash ROM with flash security)		Mass-produced product (Mask ROM)
ROM size	—	64K bytes	128K bytes	64K bytes
RAM size	16K bytes	4K bytes		
CPU function	Number of instruction : 351 Minimum execution time : 42 ns / 4 MHz (PLL x 6) Addressing mode : 23 Data bit length : 1, 8, 16 bits Maximum memory space: 16M bytes			
I/O port	I/O port (CMOS) : 66			
PWC	Pulse width counter timer : 2 channels Timer function (select the counter timer from three internal clocks) Various pulse width measuring function (H pulse width, L pulse width, rising edge to falling edge period, falling edge to rising edge period, rising edge to rising edge period and falling edge to falling edge period)			
UART	UART : 2 channels With full-duplex double buffer (8-bit length) Clock asynchronized or clock synchronized transmission (with start and stop bits) can be selected and used. Transmission can be one-to-one (bidirectional communication) or one-to-n (master-slave communication).			
16-bit reload timer	Reload timer : 2 channels Reload mode, single-shot mode or event count mode selectable			
16-bit PPG timer	PPG timer : 3 channels PWM mode or single-shot mode selectable Channel 0 can be worked with multi-functional timer or independently.			
Multi-functional timer (for AC/DC motor control)	16-bit free-running timer with up or up-down mode selection and buffer : 1 channel 16-bit output compare : 6 channels 16-bit input capture : 4 channels 16-bit PPG timer : 1 channel Waveform generator (16-bit timer : 3 channels, 3-phase waveform or dead time)			
8/10-bit A/D converter	8/10-bit resolution (16 channels) Conversion time : Min 3 µs (24 MHz internal clock, including sampling time)			
8-bit D/A converter	8/10-bit resolution (2 channels)			
DTP/External interrupt	8 independent channels Interrupt factors : Rising edge, falling edge, “L” level or “H” level			
Low-power consumption	Stop mode / Sleep mode / CPU intermittent operation mode			

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Part number / Item	MB90V820	MB90F822	MB90F823	MB90822
Package	PGA-299	LQFP-80 (FPT-80P-M05 : 0.50 mm pitch) LQFP-80 (FPT-80P-M11 : 0.65 mm pitch) QFP-80 (FPT-80P-M06 : 0.80 mm pitch)		
Power supply voltage for operation*1	4.5 V to 5.5 V*1	3.5 V to 5.5 V : Normal operation when A/D converter and D/A converter are not used 4.0 V to 5.5 V : Normal operation when D/A converter is not used 4.5 V to 5.5 V : Normal operation		
Process	CMOS			
Emulator power supply*2	Included	—		

*1 : Assurance for the MB90V820 is operating temperature 0 °C to +25 °C.

*2 : It is setting of Jumper switch (TOOL VCC) when emulator (MB2147-01) is used.
Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply switching) about details.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB90V820	MB90F822	MB90F823	MB90822
PGA299	○	X	X	X
FPT-80P-M05	X	○	○	○
FPT-80P-M11	X	○	○	○
FPT-80P-M06	X	○	○	○

○ : Available
X : Not available

Note: For more information about each package, see “■ PACKAGE DIMENSIONS”.

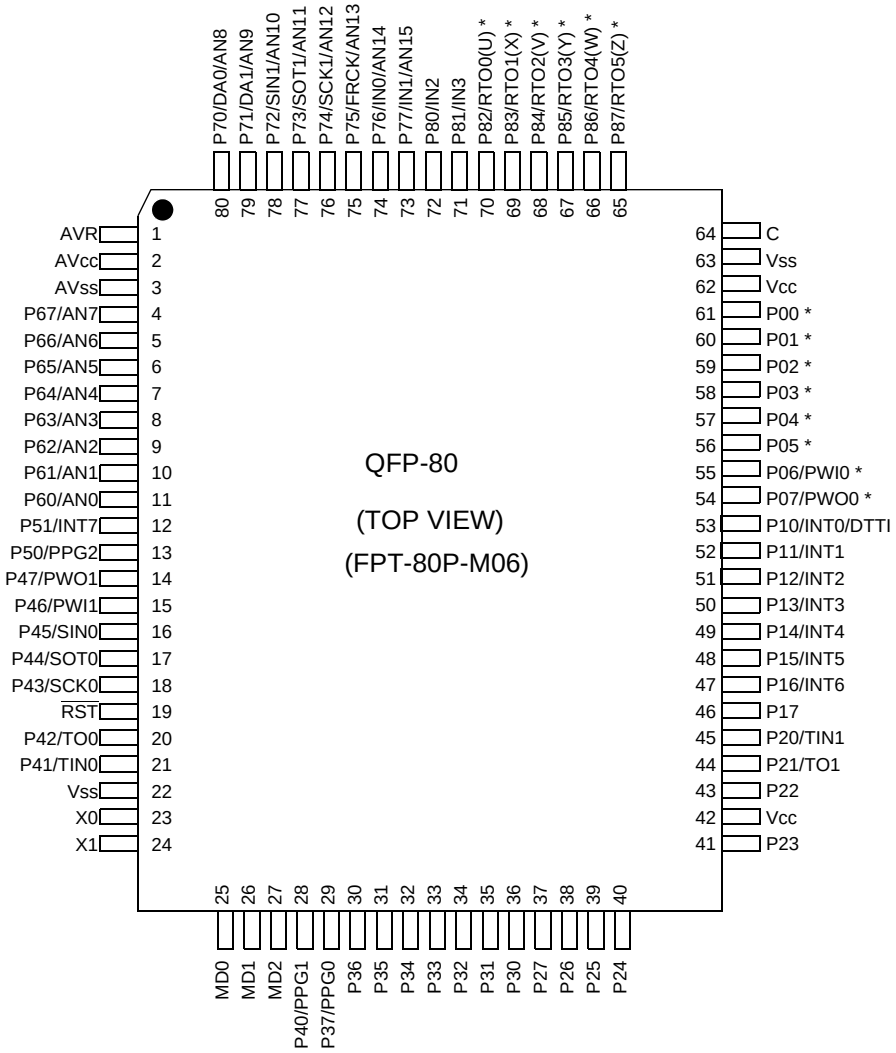
■ DIFFERENCES AMONG PRODUCTS

Memory Size

In evaluation with an evaluation product, note the difference between the evaluation product and the product actually used. The following items must be taken into consideration.

- The MB90V820 does not have an internal ROM, however, operations equivalent to chips with an internal ROM can be evaluated by using a dedicated development tool, enabling selection of ROM size by settings of the development tool.
- In the MB90V820, images from $FF8000_H$ to $FFFFFF_H$ are mapped to bank 00, and $FE0000_H$ to $FF7FFF_H$ are mapped to bank FE and bank FF only. (This setting can be changed by configuring the development tool.)
- In the MB90822/F822/F823, images from $FF8000_H$ to $FFFFFF_H$ are mapped to bank 00, and $FF0000_H$ to $FF7FFF_H$ are mapped to bank FF only. In the MB90F823, images from $FF8000_H$ to $FFFFFF_H$ are mapped to bank 00, and $FE0000_H$ to $FF7FFF_H$ are mapped to bank FE and bank FF only.

■ PIN ASSIGNMENT



* : Heavy current pin.

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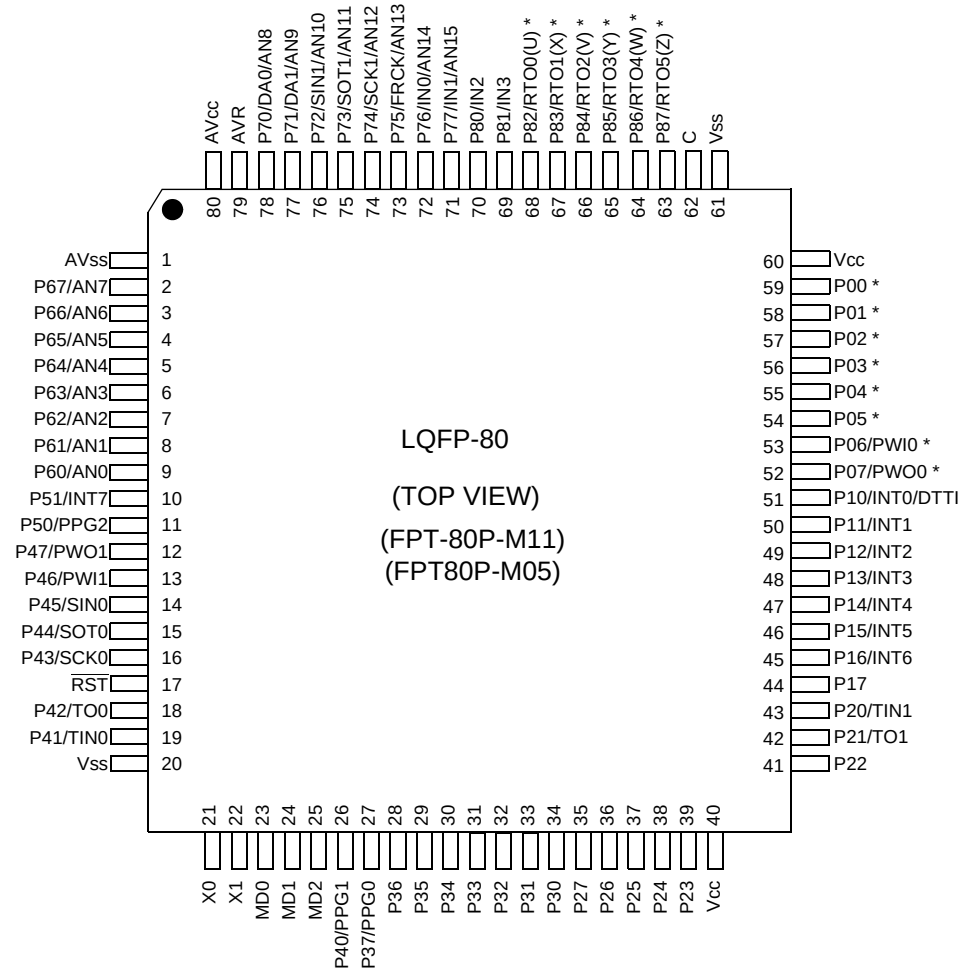

* : Heavy current pin.

■ PIN DESCRIPTION

Pin no.		Pin name	I/O circuit	Pin status during reset	Function
LQFP *1	QFP *2				
21, 22	23, 24	X0,X1	A	Oscillating	Oscillation input pins.
17	19	$\overline{RST}$	B	Reset input	External reset input pin.
59 to 54	61 to 56	P00 to P05	C	Port input	General-purpose I/O ports.
53	55	P06	C		General-purpose I/O ports.
		PWI0			PWC0 signal input pin.
52	54	P07	C		General-purpose I/O ports.
		PWO0			PWC0 signal output pin.
51	53	P10	D		General-purpose I/O ports.
		INT0			Can be used as interrupt request input channel 0. Input is enabled when 1 is set in EN0 in standby mode.
		DTTI			RTO0 to 5 pins for fixed-level input. This function is enabled when the waveform generator specifies its input bits.
50 to 45	52 to 47	P11 to P16	D		General-purpose I/O ports.
		INT1 to INT6			Can be used as interrupt request input channel 1 to 6. Input is enabled when 1 is set in EN1 to EN6 in standby mode.
44	46	P17	D		General-purpose I/O ports.
43	45	P20	D		General-purpose I/O ports.
		TIN1			External clock input pin for reload timer1.
42	44	P21	D		General-purpose I/O ports.
		TO1			Event output pin for reload timer1.
41, 39 to 35	43, 41 to 37	P22 to P27	D		General-purpose I/O ports.
34 to 28	36 to 30	P30 to P36	E		General-purpose I/O ports.
27	29	P37	E		General-purpose I/O ports.
		PPG0			Output pins for PPG channel 0. This function is enabled when output of PPG channel 0 is specified.
26	28	P40	F		General-purpose I/O ports.
		PPG1			Output pins for PPG channel 1. This function is enabled when output of PPG channel 1 is specified.
19	21	P41	F		General-purpose I/O ports.
		TIN0			External clock input pin for reload timer0.
18	20	P42	F		General-purpose I/O ports.
		TO0			Event output pin for reload timer0.

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Pin no.		Pin name	I/O circuit	Pin status during reset	Function
LQFP *1	QFP *2				
16	18	P43	F	Port Input	General-purpose I/O ports.
		SCK0			Serial clock I/O pin for UART channel 0. This function is enabled when clock output of UART channel 0 is specified.
15	17	P44	F		General-purpose I/O ports.
		SOT0			Serial data output pin for UART channel 0. This function is enabled when data output of UART channel 0 is specified.
14	16	P45	G		General-purpose I/O ports.
		SIN0			Serial data input pin for UART channel 0. While UART channel 0 is operating for input, the input of this pin is used as required. This pin must not be used for any other input. CMOS input can be selected by user program.
13	15	P46	F		General-purpose I/O ports.
		PWI1			PWC1 signal input pin.
12	14	P47	F		General-purpose I/O ports.
		PWO1			PWC1 signal output pin.
11	13	P50	F		General-purpose I/O ports.
		PPG2			Output pins for PPG channel 2. This function is enabled when output of PPG channel 2 is specified.
10	12	P51	F		General-purpose I/O ports.
		INT7			Usable as interrupt request input channel 7. Input is enabled when 1 is set in EN7 in standby mode.
9 to 2	11 to 4	P60 to P67	H	Analog input	General-purpose I/O ports.
		AN0 to AN7			A/D converter analog input pins. This function is enabled when the analog input is specified (ADER0).
78, 77	80, 79	P70, P71	I		General-purpose I/O ports.
		DA0, DA1			D/A converter analog output pins. This function is enabled when D/A converter is specified.
		AN8, AN9			A/D converter analog input pins. This function is enabled when the analog input is specified (ADER1).

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Pin no.		Pin name	I/O circuit	Pin status during reset	Function
LQFP *1	QFP *2				
76	78	P72	J	Analog input	General-purpose I/O ports.
		SIN1			Serial data input pin for UART channel 1. While UART channel 1 is operating for input, the input of this pin is used as required. This pin must not be used for any other input. CMOS input can be selected by user program.
		AN10			A/D converter analog input pins. This function is enabled when the analog input is specified (ADER1).
75	77	P73	K		General-purpose I/O ports.
		SOT1			Serial data output pin for UART channel 1. This function is enabled when data output of UART channel 1 is specified.
		AN11			A/D converter analog input pins. This function is enabled when the analog input is specified (ADER1).
74	76	P74	K		General-purpose I/O port.
		SCK1			Serial clock I/O pin for UART channel 1. This function is enabled when clock output of UART channel 1 is specified.
		AN12			A/D converter analog input pins. This function is enabled when the analog input is specified (ADER1).
73	75	P75	K		General-purpose I/O ports.
		FRCK			External clock input pin for free-running timer.
		AN13			A/D converter analog input pins. This function is enabled when the analog input is specified (ADER1).
72, 71	74, 73	P76, P77	K		General-purpose I/O ports.
		IN0, IN1			Trigger input pins for input capture channels 0, 1. When input capture channels 0, 1 are used for input operation, these pins are enabled as required and must not be used for any other input.
		AN14, AN15			A/D converter analog input pins. This function is enabled when the analog input is specified (ADER1).

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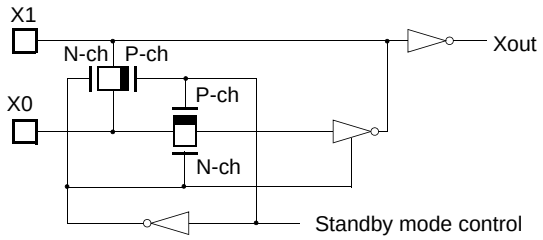
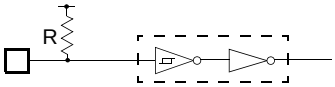
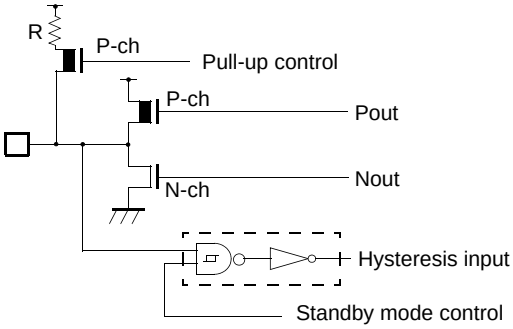
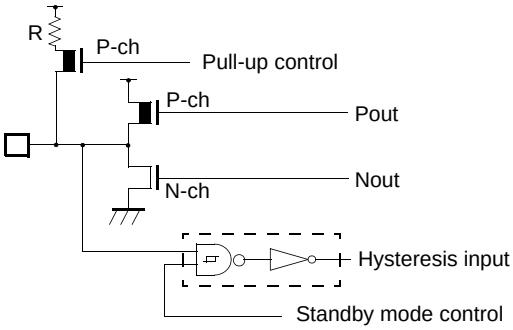
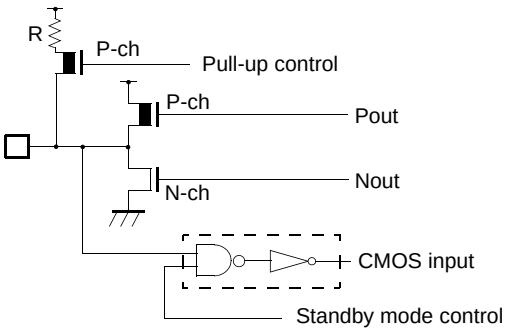
Pin no.		Pin name	I/O circuit	Pin status during reset	Function
LQFP *1	QFP *2				
70, 69	72, 71	P80, P81	F	Port input	General-purpose I/O ports.
		IN2, IN3			Trigger input pins for input capture channels 2, 3. When input capture channels 2, 3 are used for input operation, these pins are enabled as required and must not be used for any other input.
68 to 63	70 to 65	P82 to P87	L		General-purpose I/O ports.
		RTO0 to RTO5			Waveform generator output pins. These pins output the waveforms specified at the waveform generator. Output is generated when waveform generator output is enabled.
25	27	MD0	M	Mode input	Input pin for operation mode specification. Connect this pin directly to Vcc or Vss.
24, 23	26, 25	MD1, MD0	N		Input pin for operation mode specification. Connect this pin directly to Vcc or Vss.
80	2	AV_{CC}	–	Power	Vcc power input pin for analog circuits.
79	1	AVR	–		Vref + input pin for the A/D converter. This voltage must not exceed AVcc. Vref - is fixed to AVss.
1	3	AV_{SS}	–		Vss power input pin for analog circuits.
20, 61	22, 63	Vss	–	Power	Power (0 V) input pin.
40, 60	42, 62	Vcc	–		Power (5 V) input pin.
62	64	C	–	–	Capacity pin for power stabilization. Please connect to an approximately 0.1 μF ceramic capacitor.

*1: FPT-80P-M05, FPT-80P-M11
*2: FPT-80P-M06

■ I/O CIRCUIT TYPE

Classification	Type	Remarks
A		Main clock (main clock crystal oscillator) • Oscillation feedback resistor : approx. 1 MΩ
B		• Hysteresis input • Pull-up resistor : approx. 50 kΩ
C		• CMOS output • Hysteresis input • Selectable pull-up resistor : approx. 50 kΩ • I_{OL} = 12 mA
D		• CMOS output • Hysteresis input • Selectable pull-up resistor : approx. 50 kΩ • I_{OL} = 4 mA
E		• CMOS output • CMOS input • Selectable pull-up resistor : approx. 50 kΩ • I_{OL} = 4 mA

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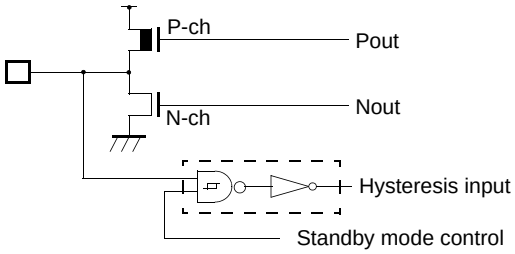
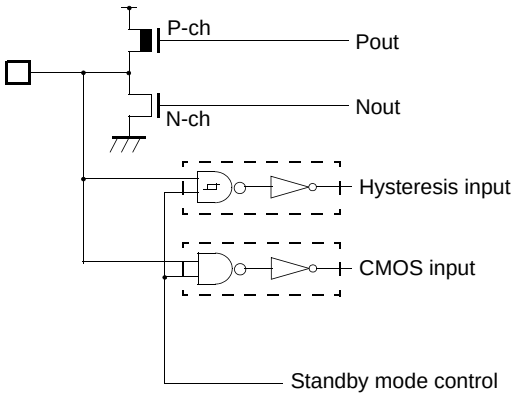
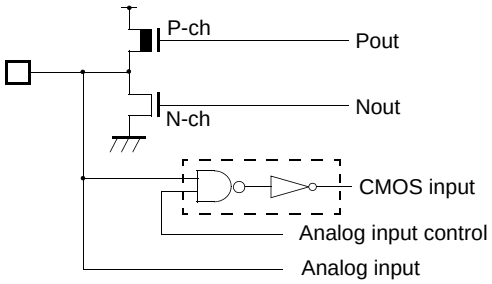
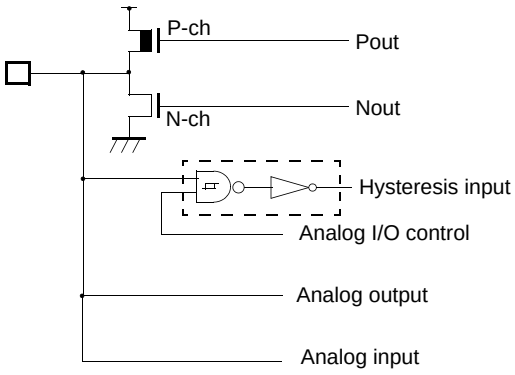
Classification	Type	Remarks
F		• CMOS output • Hysteresis input • I_{OL} = 4 mA
G		• CMOS output • Hysteresis input • CMOS input (selectable for UART0 data input pin) • I_{OL} = 4 mA
H		• CMOS output • CMOS input • Analog input • I_{OL} = 4 mA
I		• CMOS output • Hysteresis input • Analog output • Analog input • I_{OL} = 4 mA

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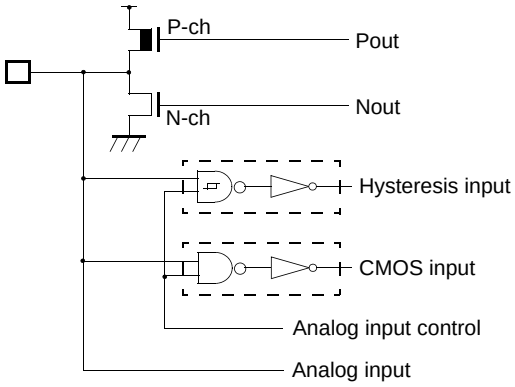
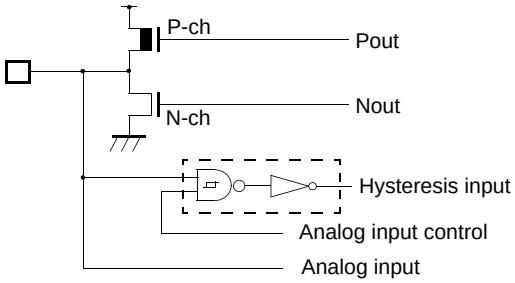
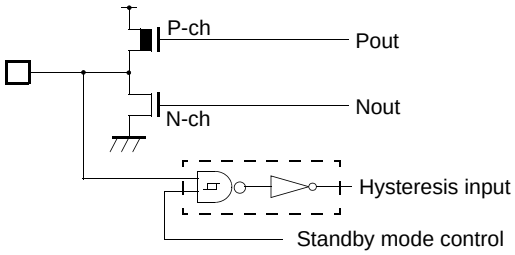
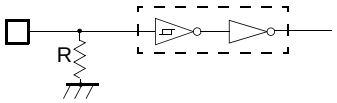
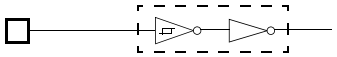
Classification	Type	Remarks
J		• CMOS output • Hysteresis input • CMOS input (selectable for UART1 data input pin) • I_{OL} = 4 mA
K		• CMOS output • Hysteresis input • Analog input • I_{OL} = 4 mA
L		• CMOS output • Hysteresis input • I_{OL} = 12 mA
M		Mask ROM / evaluation product • Hysteresis input • Selectable pull-up resistor : approx. 50 kΩ FLASH product • CMOS input • No pull-down resistor
N		Mask ROM / evaluation product • Hysteresis input FLASH product • CMOS input

■ HANDLING DEVICES

1. Preventing latch-up

CMOS ICs may cause latch-up in the following situations:

- When a voltage higher than V_{CC} or lower than V_{SS} is applied to input or output pins.
- When a voltage exceeding the rating is applied between V_{CC} and V_{SS}.
- When the AV_{CC} power supply is applied before the V_{CC} voltage.

If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Use meticulous care not to exceed the rating.

For the same reason, also be careful not to let the analog power-supply voltage exceed the digital power-supply voltage.

2. Handling unused pins

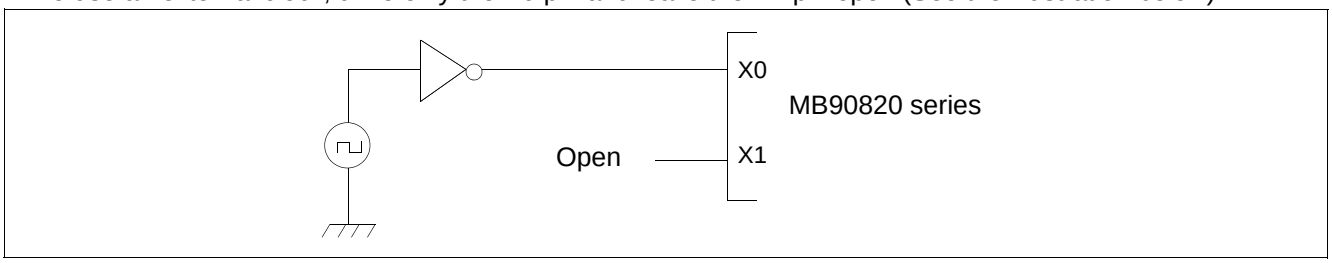
Unused input pins left open may cause abnormal operations, or latch-up leading to permanent damage. Unused input pins should be pulled up or pulled down through at least 2 kΩ resistance.

Unused input/output pins may be left open in output state, but if such pins are in input state they should be handled in the same way as input pins.

If any output pins are unused, set them to open.

3. Use of the external clock

To use an external clock, drive only the X0 pin and leave the X1 pin open (See the illustration below).



4. Power supply pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground lines to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 µF between V_{CC} and V_{SS} near this device.

5. Crystal oscillator circuit

Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator) and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0 and X1 pins surrounded by ground plane because stable operation can be expected with such a layout.

6. Turning-on sequence of power supply to A/D converter and D/A converter

Make sure to turn on the A/D converter and D/A converter power supply (AV_{CC}, AV_{SS}, AVR) and analog inputs (AN0 to AN15) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter and D/A converter supply and analog inputs. In this case, make sure that the voltage of AVR does not exceed AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

7. Connection of unused pins of A/D converter and D/A converter

When the A/D converter and D/A converter are not used, connect the pins as follows: $AV_{CC} = V_{CC}$, $AV_{SS} = AVR = V_{SS}$.

8. N.C. pin

The N.C. (internally connected) pin must be opened for use.

9. Notes on energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more.

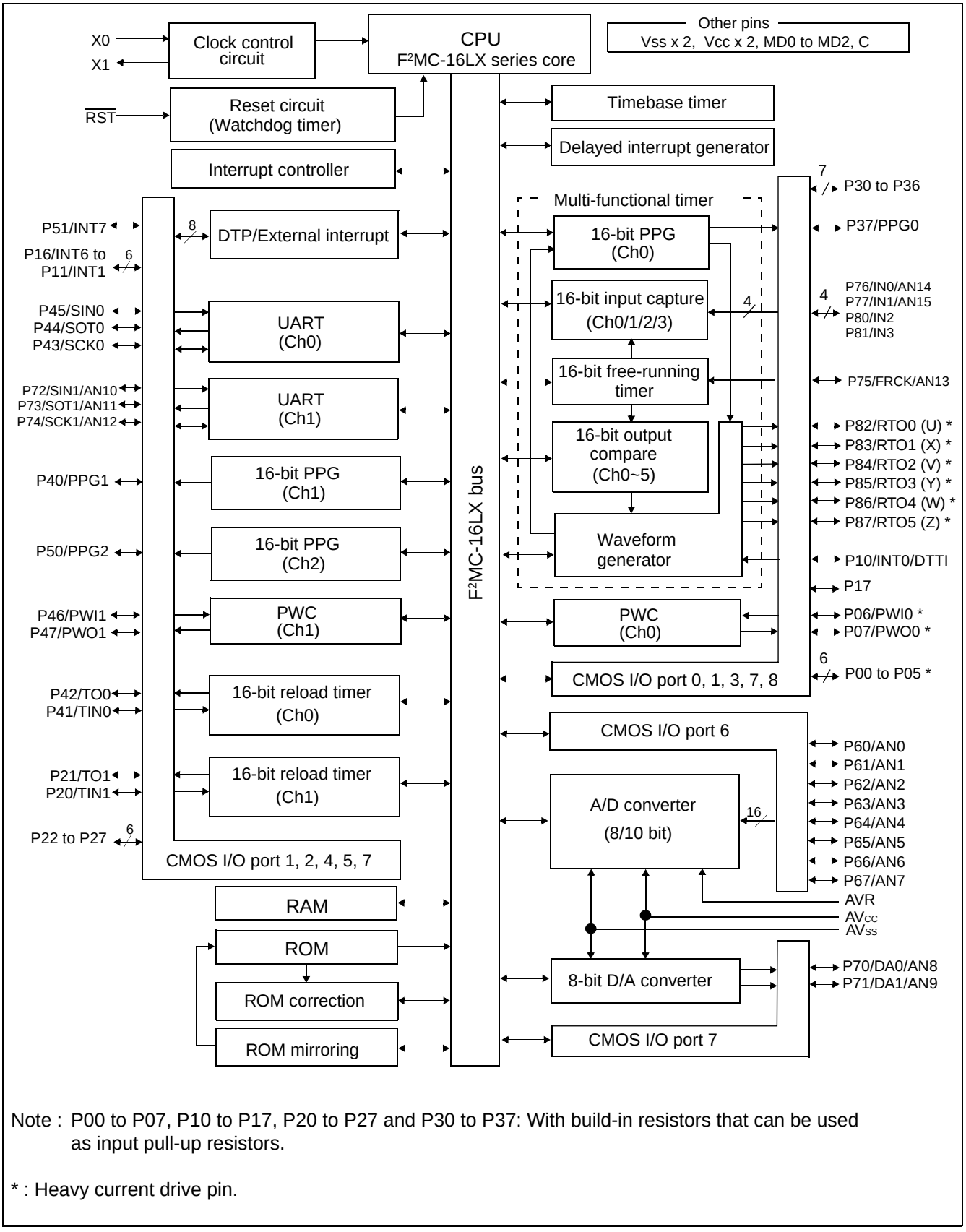
10. Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers turning on the power again.

11. Return from standby state

If the power supply voltage goes below the standby RAM holding voltage in the standby state, the device may fail to return from the standby state. In this case, reset the device via the external reset pin to return to the normal state.

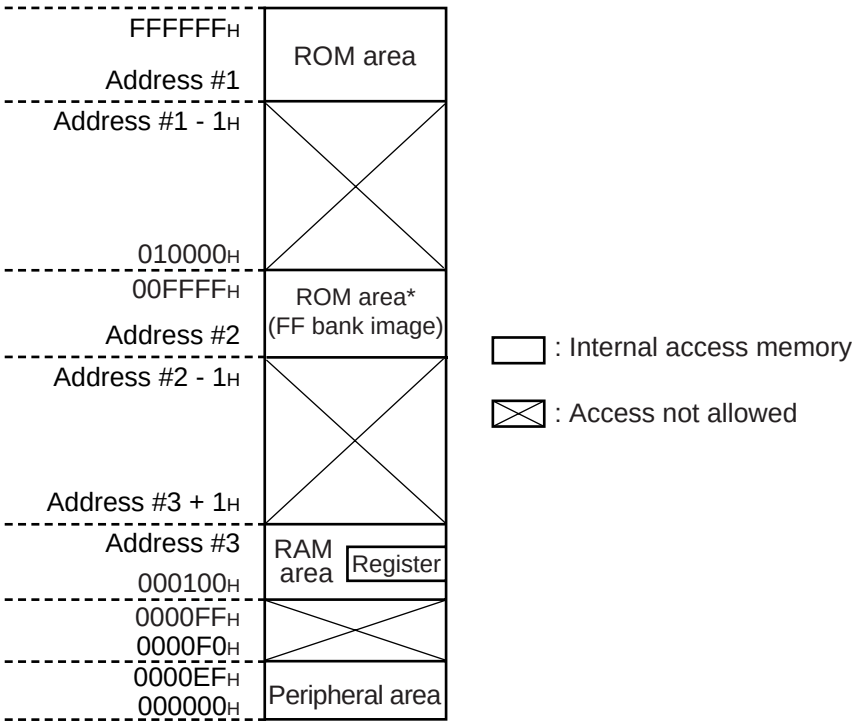
■ BLOCK DIAGRAM



Note : P00 to P07, P10 to P17, P20 to P27 and P30 to P37: With build-in resistors that can be used as input pull-up resistors.

* : Heavy current drive pin.

■ MEMORY MAP



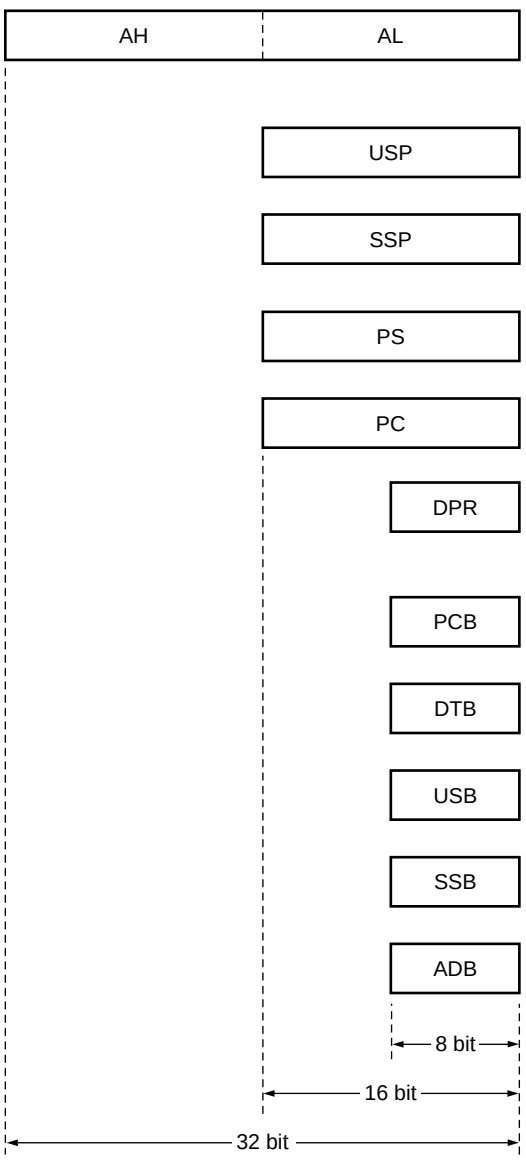
* : In Single chip mode, the mirror function is supported.

Parts no.	Address#1	Address#2	Address#3
MB90822	FF0000H	008000H	0010FFH
MB90F822	FF0000H	008000H	0010FFH
MB90F823	FE0000H	008000H	0010FFH
MB90V820	(FE0000H)	008000H	0040FFH

Note: The ROM data of bank FF is reflected to the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit is assigned to the same address, enabling reference of the table on the ROM without stating “far”. For example, if an attempt has been made to access 00C000H, the contents of the ROM at FFC000H are accessed actually. Since the ROM area of the FF bank exceeds 32K bytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF8000H to FFFFFFH looks, therefore, as if it were the image for 008000H to 00FFFFH. Thus, it is recommended that the ROM data table be stored in the area of FF8000H to FFFFFFH.

■ F²MC-16LX CPU PROGRAMMING MODEL

- Dedicated registers



: Accumulator (A)
Dual 16-bit register used for storing results of calculation etc. The two 16-bit registers can be combined to be used as a sequence of 32-bit register.

: User stack pointer (USP)
The 16-bit pointer indicating the user stack address.

: System stack pointer (SSP)
The 16-bit pointer indicating the system stack address.

: Processor status (PS)
The 16-bit register indicating the system status.

: Program counter (PC)
The 16-bit register indicating storing location of the current instruction code.

: Direct page register (DPR)
The 8-bit register indicating bit 8 through 15 of the operand address in executing of the short direct addressing.

: Program bank register (PCB)
The 8-bit register indicating the program space.

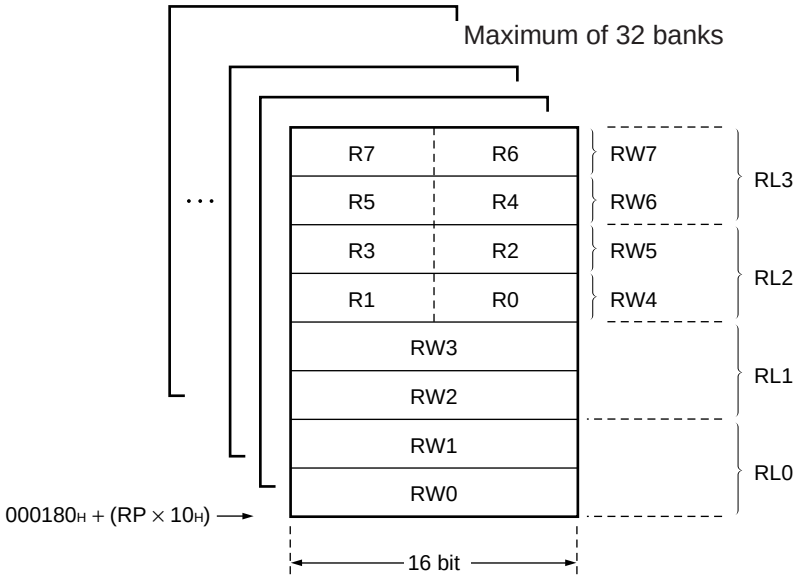
: Data bank register (DTB)
The 8-bit register indicating the data space.

: User stack bank register (USB)
The 8-bit register indicating the user stack space.

: System stack bank register (SSB)
The 8-bit register indicating the system stack space.

: Additional data bank register (ADB)
The 8-bit register indicating the additional

- General-purpose registers



- Processor status (PS)

	ILM			RP					CCR							
	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PS	ILM2	ILM1	ILM0	B4	B3	B2	B1	B0	—	I	S	T	N	Z	V	C
Initial value	0	0	0	0	0	0	0	0	—	0	1	X	X	X	X	X

— : Unused
X : Undefined

■ I/O MAP

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000000H	PDR0	Port 0 data register	R/W	R/W	Port 0	XXXXXXXXB
000001H	PDR1	Port 1 data register	R/W	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 data register	R/W	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 data register	R/W	R/W	Port 5	XXXXXXXXB
000006H	PDR6	Port 6 data register	R/W	R/W	Port 6	XXXXXXXXB
000007H	PDR7	Port 7 data register	R/W	R/W	Port 7	XXXXXXXXB
000008H	PDR8	Port 8 data register	R/W	R/W	Port 8	XXXXXXXXB
000009H to 00000FH	Prohibited area					
000010H	DDR0	Port 0 data direction register	R/W	R/W	Port 0	00000000B
000011H	DDR1	Port 1 data direction register	R/W	R/W	Port 1	00000000B
000012H	DDR2	Port 2 data direction register	R/W	R/W	Port 2	00000000B
000013H	DDR3	Port 3 data direction register	R/W	R/W	Port 3	00000000B
000014H	DDR4	Port 4 data direction register	R/W	R/W	Port 4	00000000B
000015H	DDR5	Port 5 data direction register	R/W	R/W	Port 5	XXXXXX00B
000016H	DDR6	Port 6 data direction register	R/W	R/W	Port 6	00000000B
000017H	DDR7	Port 7 data direction register	R/W	R/W	Port 7	00000000B
000018H	DDR8	Port 8 data direction register	R/W	R/W	Port 8	00000000B
000019H to 00001FH	Prohibited area					
000020H	SMR0	Serial mode register 0	R/W	R/W	UART0	00000000B
000021H	SCR0	Serial control register 0	R/W	R/W		00000100B
000022H	SIDR0 / SODR0	Serial input data register 0 / Serial output data register 0	R/W	R/W		XXXXXXXXB
000023H	SSR0	Serial status register 0	R/W	R/W		00001000B
000024H	SMR1	Serial mode register 1	R/W	R/W	UART1	00000000B
000025H	SCR1	Serial control register 1	R/W	R/W		00000100B
000026H	SIDR1 / SODR1	Serial input data register 1 / Serial output data register 1	R/W	R/W		XXXXXXXXB
000027H	SSR1	Serial status register 1	R/W	R/W		00001000B
000028H	PWCSL1	PWC control status register CH1	R/W	R/W	PWC timer (CH1)	00000000B
000029H	PWCSH1		R/W	R/W		00000000B
00002AH	PWC1	PWC data buffer register CH1	—	R/W		XXXXXXXXB
00002BH						XXXXXXXXB
00002CH	DIV1	Divide ratio control register CH1	R/W	R/W		XXXXXX00B

(Continued)

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
00002DH, 00002EH	Prohibited area					
00002FH	PCKCR	PLL clock control register	W	W	PLL	XXXX0000B
000030H	ENIR	DTP / Interrupt enable register	R/W	R/W	DTP/ external interrupt	00000000B
000031H	EIRR	DTP / Interrupt cause register	R/W	R/W		XXXXXXXXB
000032H	ELVRL	Request level setting register (lower byte)	R/W	R/W		00000000B
000033H	ELVRH	Request level setting register (higher byte)	R/W	R/W		00000000B
000034H	Prohibited area					
000035H	CDCR0	Clock division control register CH0	R/W	R/W	Communication prescaler 0	00XXX000B
000036H	Prohibited area					
000037H	CDCR1	Clock division control register CH1	R/W	R/W	Communication prescaler 1	00XXX000B
000038H	PDCR0	PPG0 down counter register	—	R	16-bit PPG timer (CH0)	11111111B
000039H						11111111B
00003AH	PCSR0	PPG0 period setting register	—	W		XXXXXXXXB
00003BH						XXXXXXXXB
00003CH	PDUT0	PPG0 duty setting register	—	W		XXXXXXXXB
00003DH						XXXXXXXXB
00003EH	PCNTL0	PPG0 control status register	R/W	R/W		XX000000B
00003FH	PCNTH0		R/W	R/W		00000000B
000040H	PDCR1	PPG1 down counter register	—	R	16-bit PPG timer (CH1)	11111111B
000041H						11111111B
000042H	PCSR1	PPG1 period setting register	—	W		XXXXXXXXB
000043H						XXXXXXXXB
000044H	PDUT1	PPG1 duty setting register	—	W		XXXXXXXXB
000045H						XXXXXXXXB
000046H	PCNTL1	PPG1 control status register	R/W	R/W		XX000000B
000047H	PCNTH1		R/W	R/W		00000000B
000048H	PDCR2	PPG2 down counter register	—	R	16-bit PPG timer (CH2)	11111111B
000049H						11111111B
00004AH	PCSR2	PPG2 period setting register	—	W		XXXXXXXXB
00004BH						XXXXXXXXB
00004CH	PDUT2	PPG2 duty setting register	—	W		XXXXXXXXB
00004DH						XXXXXXXXB
00004EH	PCNTL2	PPG2 control status register	R/W	R/W		XX000000B
00004FH	PCNTH2		R/W	R/W		00000000B

(Continued)

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000050H	TMRR0	16-bit timer register 0	—	R/W	Waveform generator	XXXXXXXXB
000051H						XXXXXXXXB
000052H	TMRR1	16-bit timer register 1	—	R/W		XXXXXXXXB
000053H						XXXXXXXXB
000054H	TMRR2	16-bit timer register 2	—	R/W		XXXXXXXXB
000055H						XXXXXXXXB
000056H	DTCR0	16-bit timer control register 0	R/W	R/W		00000000B
000057H	DTCR1	16-bit timer control register 1	R/W	R/W		00000000B
000058H	DTCR2	16-bit timer control register 2	R/W	R/W		00000000B
000059H	SIGCR	Waveform control register	R/W	R/W		00000000B
00005AH	CPCLRB / CPCLR	Compare clear buffer register/ Compare clear register (lower)	—	R/W	16-bit free-running timer	11111111B
00005BH						11111111B
00005CH	TCDT	Timer register (lower)	—	R/W		00000000B
00005DH						00000000B
00005EH	TCCSL	Timer control status register (lower)	R/W	R/W	16-bit free-running timer	00000000B
00005FH	TCCSH	Timer control status register (upper)	R/W	R/W		X0000000B
000060H	IPCP0	Input capture data register CH0	—	R	16-bit input capture (CH0 to CH3)	XXXXXXXXB
000061H						XXXXXXXXB
000062H	IPCP1	Input capture data register CH1	—	R		XXXXXXXXB
000063H						XXXXXXXXB
000064H	IPCP2	Input capture data register CH2	—	R		XXXXXXXXB
000065H						XXXXXXXXB
000066H	IPCP3	Input capture data register CH3	—	R		XXXXXXXXB
000067H						XXXXXXXXB
000068H	PICSL01	Input capture control status register (ch0,1) (lower)	R/W	R/W		00000000B
000069H	PICSH01	PPG output control / Input capture control status register (ch0,1) (upper)	R/W	R/W		00000000B
00006AH	ICSL23	Input capture control status register (ch2, 3) (lower)	R/W	R/W		00000000B
00006BH	ICSH23	Input capture control status register (ch2, 3) (upper)	R	R		XXXXXX00B
00006CH to 00006EH	Prohibited area					

(Continued)

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
00006F$_H$	ROMM	ROM mirroring function selection register	W	W	ROM mirroring function	XXXXXXX1$_B$
000070$_H$	OCCPB0 / OCCP0	Output compare buffer register / Output compare register 0	—	R/W	Output compare (CH0 to CH5)	XXXXXXXX$_B$
000071$_H$						XXXXXXXX$_B$
000072$_H$	OCCPB1 / OCCP1	Output compare buffer register / Output compare register 1	—	R/W		XXXXXXXX$_B$
000073$_H$						XXXXXXXX$_B$
000074$_H$	OCCPB2 / OCCP2	Output compare buffer register / Output compare register 2	—	R/W		XXXXXXXX$_B$
000075$_H$						XXXXXXXX$_B$
000076$_H$	OCCPB3 / OCCP3	Output compare buffer register / Output compare register 3	—	R/W		XXXXXXXX$_B$
000077$_H$						XXXXXXXX$_B$
000078$_H$	OCCPB4 / OCCP4	Output compare buffer register / Output compare register 4	—	R/W		XXXXXXXX$_B$
000079$_H$						XXXXXXXX$_B$
00007A$_H$	OCCPB5 / OCCP5	Output compare buffer register / Output compare register 5	—	R/W		XXXXXXXX$_B$
00007B$_H$						XXXXXXXX$_B$
00007C$_H$	OCS0	Compare control register CH0	R/W	R/W		00000000$_B$
00007D$_H$	OCS1	Compare control register CH1	R/W	R/W		X0000000$_B$
00007E$_H$	OCS2	Compare control register CH2	R/W	R/W		00000000$_B$
00007F$_H$	OCS3	Compare control register CH3	R/W	R/W		X0000000$_B$
000080$_H$	OCS4	Compare control register CH4	R/W	R/W		00000000$_B$
000081$_H$	OCS5	Compare control register CH5	R/W	R/W		X0000000$_B$
000082$_H$	TMCSRL0	Timer control status register CH0 (lower)	R/W	R/W	16-bit reload timer (CH0)	00000000$_B$
000083$_H$	TMCSRH0	Timer control status register CH0 (upper)	R/W	R/W		XXXX0000$_B$
000084$_H$	TMR0 / TMRD0	16 bit timer register CH0 / 16-bit reload register CH0	—	R/W		XXXXXXXX$_B$
000085$_H$						XXXXXXXX$_B$
000086$_H$	TMCSRL1	Timer control status register CH1 (lower)	R/W	R/W	16-bit reload timer (CH1)	00000000$_B$
000087$_H$	TMCSRH1	Timer control status register CH1 (upper)	R/W	R/W		XXXX0000$_B$
000088$_H$	TMR1 / TMRD1	16 bit timer register CH1 / 16-bit reload register CH1	—	R/W		XXXXXXXX$_B$
000089$_H$						XXXXXXXX$_B$
00008A$_H$, 00008B$_H$	Prohibited area					
00008C$_H$	RDR0	Port 0 pull-up resistor setting register	R/W	R/W	Port 0	00000000$_B$
00008D$_H$	RDR1	Port 1 pull-up resistor setting register	R/W	R/W	Port 1	00000000$_B$

(Continued)

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
00008E$_H$	RDR2	Port 2 pull-up resistor setting register	R/W	R/W	Port 2	00000000$_B$
00008F$_H$	RDR3	Port 3 pull-up resistor setting register	R/W	R/W	Port 3	00000000$_B$
000090$_H$ to 00009D$_H$	Prohibited area					
00009E$_H$	PACSR	Program address detection control status register	R/W	R/W	Address match detection	00000000$_B$
00009F$_H$	DIRR	Delayed interrupt cause / clear register	R/W	R/W	Delayed interrupt	XXXXXXX0$_B$
0000A0$_H$	LPMCR	Low-power consumption mode control register	R/W	R/W	Low-power consumption control register	00011000$_B$
0000A1$_H$	CKSCR	Clock selection register	R/W	R/W		11111100$_B$
0000A2$_H$ to 0000A7$_H$	Prohibited area					
0000A8$_H$	WDTC	Watchdog timer control register	R/W	R/W	Watchdog timer	XXXXX111$_B$
0000A9$_H$	TBTC	Timebase timer control register	R/W	R/W	Timebase timer	1XX00100$_B$
0000AA$_H$ to 0000AD$_H$	Prohibited area					
0000AE$_H$	FMCS	Flash memory control status register	R/W	R/W	Flash memory interface circuit	000X0000$_B$
0000AF$_H$	Prohibited area					
0000B0$_H$	ICR00	Interrupt control register 00	R/W	R/W	Interrupt controller	00000111$_B$
0000B1$_H$	ICR01	Interrupt control register 01	R/W	R/W		00000111$_B$
0000B2$_H$	ICR02	Interrupt control register 02	R/W	R/W		00000111$_B$
0000B3$_H$	ICR03	Interrupt control register 03	R/W	R/W		00000111$_B$
0000B4$_H$	ICR04	Interrupt control register 04	R/W	R/W		00000111$_B$
0000B5$_H$	ICR05	Interrupt control register 05	R/W	R/W		00000111$_B$
0000B6$_H$	ICR06	Interrupt control register 06	R/W	R/W		00000111$_B$
0000B7$_H$	ICR07	Interrupt control register 07	R/W	R/W		00000111$_B$
0000B8$_H$	ICR08	Interrupt control register 08	R/W	R/W		00000111$_B$
0000B9$_H$	ICR09	Interrupt control register 09	R/W	R/W		00000111$_B$
0000BA$_H$	ICR10	Interrupt control register 10	R/W	R/W		00000111$_B$
0000BB$_H$	ICR11	Interrupt control register 11	R/W	R/W		00000111$_B$
0000BC$_H$	ICR12	Interrupt control register 12	R/W	R/W		00000111$_B$
0000BD$_H$	ICR13	Interrupt control register 13	R/W	R/W		00000111$_B$
0000BE$_H$	ICR14	Interrupt control register 14	R/W	R/W		00000111$_B$
0000BF$_H$	ICR15	Interrupt control register 15	R/W	R/W		00000111$_B$

(Continued)

(Continued)

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
0000C0H	PWCSL0	PWC control status register CH0	R/W	R/W	PWC timer (CH0)	00000000B
0000C1H	PWCSH0		R/W	R/W		00000000B
0000C2H	PWC0	PWC data buffer register CH0	—	R/W		XXXXXXXXB
0000C3H						XXXXXXXXB
0000C4H	DIV0	Divide ratio control register CH0	R/W	R/W		XXXXXX00B
0000C5H	ADER0	A/D input enable register 0	R/W	R/W	Port 6, A/D	11111111B
0000C6H	ADCS0	A/D control status register 0	R/W	R/W	8/10-bit A/D converter	000XXXX0B
0000C7H	ADCS1	A/D control status register 1	R/W	R/W		0000000XB
0000C8H	ADCR0	A/D data register 0	R	R		00000000B
0000C9H	ADCR1	A/D data register 1	R/W	R/W		XXXXXX00B
0000CAH	ADSR0	A/D setting register 0	R/W	R/W		00000000B
0000CBH	ADSR1	A/D setting register 1	R/W	R/W		00000000B
0000CCH	DAT0	D/A data register 0	R/W	R/W	8-bit D/A converter	XXXXXXXXB
0000CDH	DAT1	D/A data register 1	R/W	R/W		XXXXXXXXB
0000CEH	DACR0	D/A control register 0	R/W	R/W		XXXXXXX0B
0000CFH	DACR1	D/A control register 1	R/W	R/W		XXXXXXX0B
0000D0H	ADER1	A/D input enable register 1	R/W	R/W	Port 7, A/D	11111111B
0000D1H to 0000EFH	Prohibited area					
0000F0H to 0000FFH	External area					
001FF0H	PADRL0	Program address detection register 0 (lower)	R/W	R/W	Address match detection	XXXXXXXXB
001FF1H	PADRM0	Program address detection register 0 (middle)	R/W	R/W		XXXXXXXXB
001FF2H	PADRH0	Program address detection register 0 (higher)	R/W	R/W		XXXXXXXXB
001FF3H	PADRL1	Program address detection register 1 (lower)	R/W	R/W		XXXXXXXXB
001FF4H	PADRM1	Program address detection register 1 (middle)	R/W	R/W		XXXXXXXXB
001FF5H	PADRH1	Program address detection register 1 (higher)	R/W	R/W		XXXXXXXXB

- Meaning of abbreviations used for reading and writing
  R/W: Read and write enabled
  R : Read-only
  W : Write-only
- Explanation of initial values
  0 : The bit is initialized to 0.
  1 : The bit is initialized to 1.
  X : The initial value of the bit is undefined.

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI²OS support	Interrupt vector			Interrupt control register		Priority
		Number		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	—	—	High
INT9 instruction	×	#09	09H	FFFFD8H	—	—	
Exception processing	×	#10	0AH	FFFFD4H	—	—	
A/D converter conversion termination	○	#11	0BH	FFFFD0H	ICR00	0000B0H	
Output compare channel 0 match	○	#12	0CH	FFFFCCH			
End of measurement by PWC timer 0 / PWC timer 0 overflow	○	#13	0DH	FFFFC8H	ICR01	0000B1H	
16-bit PPG timer 0	○	#14	0EH	FFFFC4H			
Output compare channel 1 match	○	#15	0FH	FFFFC0H	ICR02	0000B2H	
16-bit PPG timer 1	○	#16	10H	FFFFBCH			
Output compare channel 2 match	○	#17	11H	FFFFB8H	ICR03	0000B3H	
16-bit reload timer 1 underflow	○	#18	12H	FFFFB4H			
Output compare channel 3 match	○	#19	13H	FFFFB0H	ICR04	0000B4H	
DTP/ext. interrupt channels 0/1 detection	○	#20	14H	FFFFACH			
DTTI	△						
Output compare channel 4 match	○	#21	15H	FFFFA8H	ICR05	0000B5H	
DTP/ext. interrupt channels 2/3 detection	○	#22	16H	FFFFA4H			
Output compare channel 5 match	○	#23	17H	FFFFA0H	ICR06	0000B6H	
End of measurement by PWC timer 1 / PWC timer 1 overflow	○	#24	18H	FFFF9CH			
DTP/ext. interrupt channels 4 detection	○	#25	19H	FFFF98H	ICR07	0000B7H	
DTP/ext. interrupt channels 5 detection	○	#26	1AH	FFFF94H			
DTP/ext. interrupt channels 6 detection	○	#27	1BH	FFFF90H	ICR08	0000B8H	
DTP/ext. interrupt channels 7 detection	○	#28	1CH	FFFF8CH			
Waveform generator 16-bit timers 0/1/2 underflow	△	#29	1DH	FFFF88H	ICR09	0000B9H	
16-bit reload timer 0 underflow	○	#30	1EH	FFFF84H			
16-bit free-running timer zero detect	△	#31	1FH	FFFF80H	ICR10	0000BAH	
16-bit PPG timer 2	○	#32	20H	FFFF7CH			
Input capture channels 0/1	○	#33	21H	FFFF78H	ICR11	0000BBH	
16-bit free-running timer compare clear	△	#34	22H	FFFF74H			
Input capture channels 2/3	○	#35	23H	FFFF70H	ICR12	0000BCH	
Timebase timer	△	#36	24H	FFFF6CH			
UART1 receive	◎	#37	25H	FFFF68H	ICR13	0000BDH	
UART1 send	△	#38	26H	FFFF64H			
UART0 receive	◎	#39	27H	FFFF60H	ICR14	0000BEH	
UART0 send	△	#40	28H	FFFF5CH			
Flash memory status	△	#41	29H	FFFF58H	ICR15	0000BFH	
Delayed interrupt generator module	△	#42	2AH	FFFF54H			Low

◎ : Can be used and support the EI²OS stop request.
○ : Can be used and interrupt request flag is cleared by EI²OS interrupt clear signal.
× : Cannot be used.
△ : Usable when an interrupt cause that shares the ICR is not used.

■ PERIPHERAL RESOURCES

1. Low-power Consumption Control Circuit

The MB90820 series has the following CPU operating mode configured by selection of an operating clock and clock operation control.

- Clock mode

  PLL clock mode : A PLL clock that is a multiple of the oscillation clock (HCLK) frequency is used to operate the CPU and peripheral functions.

  Main clock mode : The main clock, with a frequency one-half that of the oscillation clock (HCLK), is used to operate the CPU and peripheral functions. In main clock mode, the PLL divide circuit is inactive.

- CPU intermittent operation mode

  CPU intermittent operation mode causes the CPU to operate intermittently, while high-speed clock pulses are supplied to peripheral functions, reducing power consumption. In CPU intermittent operation mode, clock pulses are supplied intermittently to the CPU when it is accessing a register, internal memory, a peripheral function, or an external unit.

- Standby mode

  In standby mode, the low power consumption control circuit reduces power consumption by stopping;

  - The supply of the clock to CPU (sleep mode)
  - CPU and peripheral functions (timebase timer mode)
  - The oscillation clock itself (stop mode)

- PLL sleep mode

  PLL sleep mode is activated to stop the CPU operating clock when the microcontroller enters PLL clock mode; other components continue to operate on the PLL clock.

- Main sleep mode

  Main sleep mode is activated to stop the CPU operating clock when the microcontroller enters main clock mode; other components continue to operate on the main clock.

- PLL timebase timer mode

  PLL timebase timer mode causes microcontroller operation, with the exception of the oscillation clock, PLL clock and timebase timer, to stop. All functions other than the timebase timer are deactivated.

- Main timebase timer mode

  Main timebase timer mode causes microcontroller operation, with the exception of the oscillation clock, main clock and the timebase timer, to stop. All functions other than the timebase timer are deactivated.

- Stop mode

  Stop mode causes the source oscillation to stop. All functions are deactivated.

(1) Register configuration

Clock Selection Register

	15	14	13	12	11	10	9	8	⇦ Bit
Address: 00000A1H	Reserved	MCM	WS1	WS0	Reserved	MCS	CS1	CS0	CKSCR
Read/write ⇨	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	1	1	1	1	1	1	0	0	

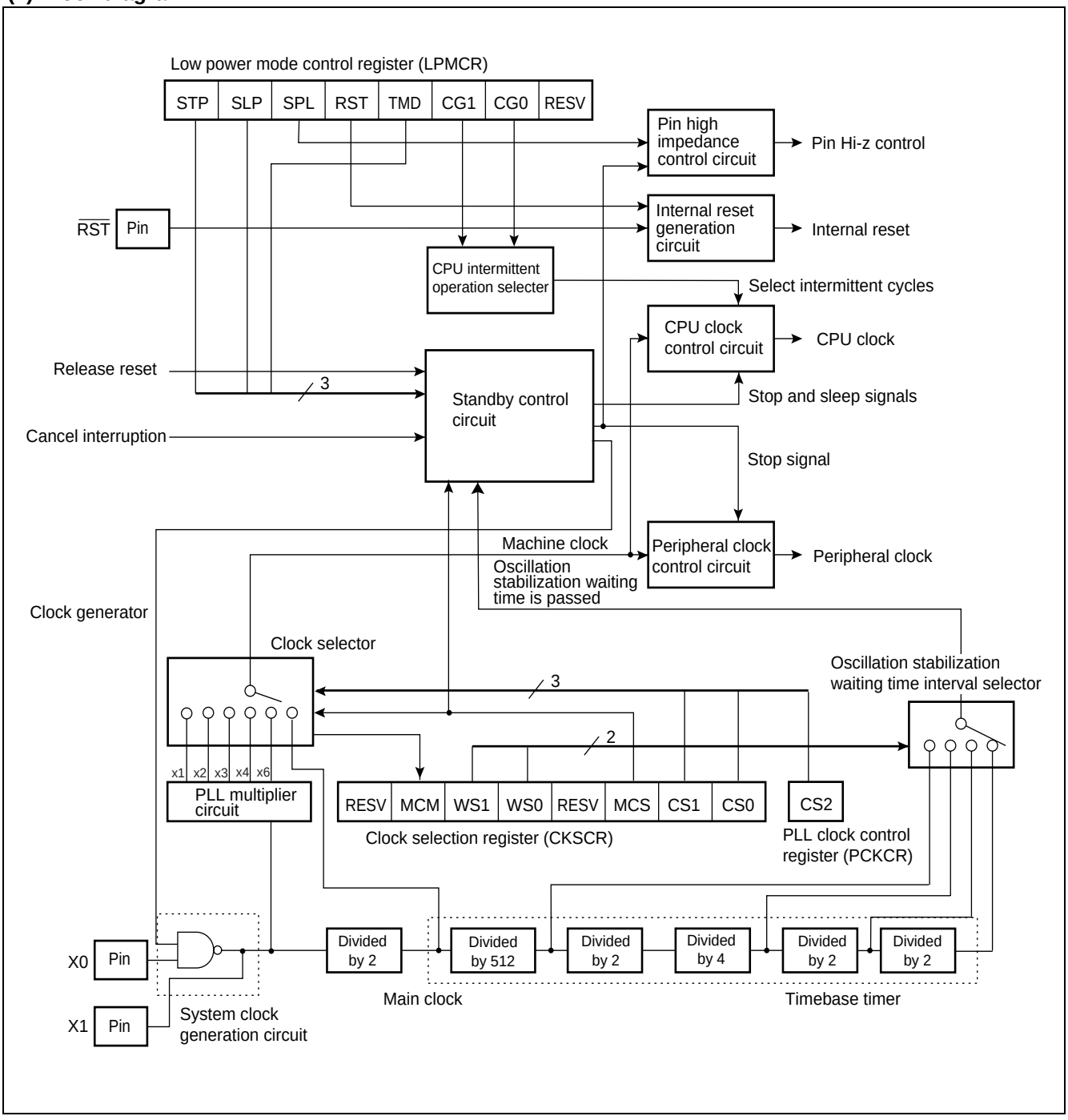
PLL Clock Control Register

	15	14	13	12	11	10	9	8	⇦ Bit
Address: 000002FH	—	—	—	—	Reserved	Reserved	Reserved	CS2	PCKCR
Read/write ⇨	—	—	—	—	W	W	W	W	
Initial value ⇨	X	X	X	X	0	0	0	0	

Low-power Consumption Mode Control Register

	7	6	5	4	3	2	1	0	⇦ Bit
Address: 0000A0H	STP	SLP	SPL	RST	TMD	CG1	CG0	Reserved	LPMCR
Read/write ⇨	W	W	R/W	W	W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	1	1	0	0	0	

(2) Block diagram



2. I/O Ports

(1) Outline of I/O ports

Each I/O port outputs data from CPU to I/O pins or inputs signals from I/O pins to CPU through port data register (PDR). Direction of the data flow (input or output) for each I/O pin can be designated in bit unit by port data direction register (DDR). The function of each port and the resource I/O multiplexed with it are described below:

- Port 0 : General-purpose I/O port/resource (PWC)
- Port 1 : General-purpose I/O port/resources (DTP / Multi-functional timer)
- Port 2 : General-purpose I/O port/resource (16-bit reload timer)
- Port 3 : General-purpose I/O port/resource (16-bit PPG timer)
- Port 4 : General-purpose I/O port/resources (16-bit PPG timer / 16-bit reload timer / UART / PWC)
- Port 5 : General-purpose I/O port/resources (16-bit PPG timer / DTP)
- Port 6 : General-purpose I/O port/resource (8/10-bit A/D converter)
- Port 7 : General-purpose I/O port/resources (8/10-bit A/D converter / 8-bit D/A converter / UART/ 16-bit free-running timer / 16-bit input capture)
- Port 8 : General-purpose I/O port/resources (16-bit input capture / Multi-functional timer)

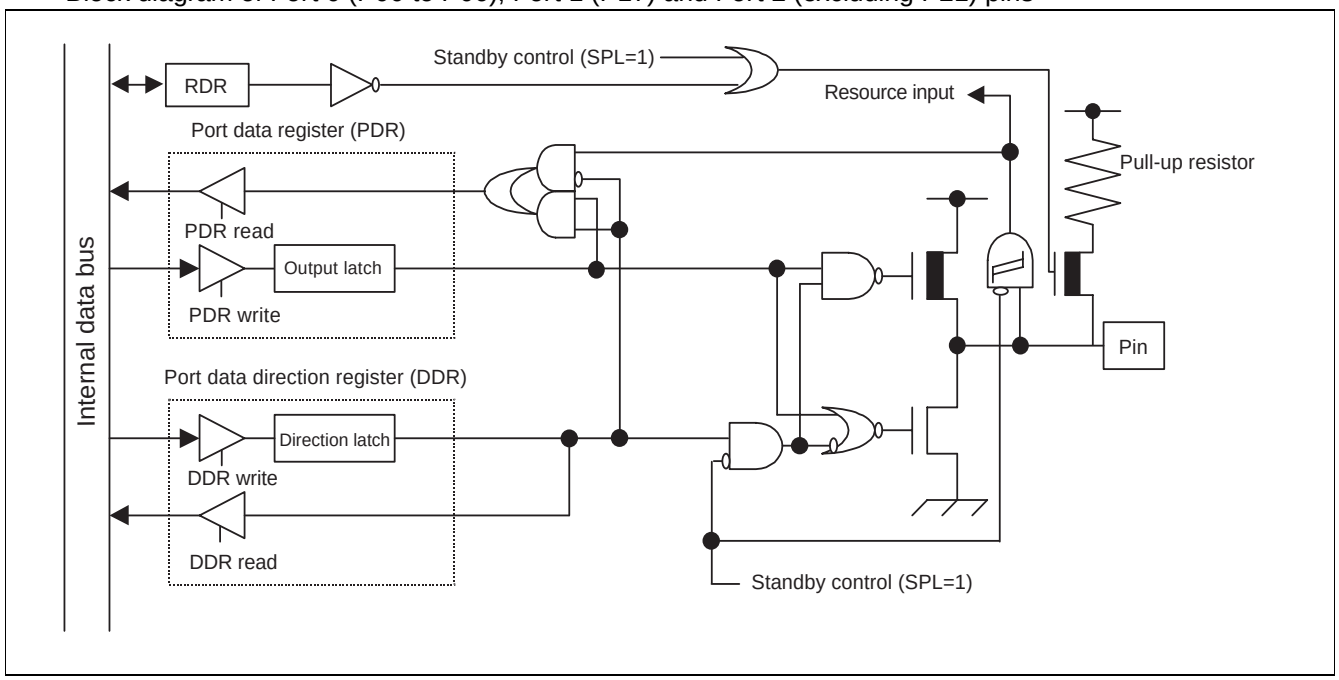
(2) Register configuration

Register	Read/Write	Address	Initial value
Port 0 data register (PDR0)	R/W	000000_H	$XXXXXXXX_B$
Port 1 data register (PDR1)	R/W	000001_H	$XXXXXXXX_B$
Port 2 data register (PDR2)	R/W	000002_H	$XXXXXXXX_B$
Port 3 data register (PDR3)	R/W	000003_H	$XXXXXXXX_B$
Port 4 data register (PDR4)	R/W	000004_H	$XXXXXXXX_B$
Port 5 data register (PDR5)	R/W	000005_H	$XXXXXXXX_B$
Port 6 data register (PDR6)	R/W	000006_H	$XXXXXXXX_B$
Port 7 data register (PDR7)	R/W	000007_H	$XXXXXXXX_B$
Port 8 data register (PDR8)	R/W	000008_H	$XXXXXXXX_B$
Port 0 data direction register (DDR0)	R/W	000010_H	00000000_B
Port 1 data direction register (DDR1)	R/W	000011_H	00000000_B
Port 2 data direction register (DDR2)	R/W	000012_H	00000000_B
Port 3 data direction register (DDR3)	R/W	000013_H	00000000_B
Port 4 data direction register (DDR4)	R/W	000014_H	00000000_B
Port 5 data direction register (DDR5)	R/W	000015_H	$XXXXXX00_B$
Port 6 data direction register (DDR6)	R/W	000016_H	00000000_B
Port 7 data direction register (DDR7)	R/W	000017_H	00000000_B
Port 8 data direction register (DDR8)	R/W	000018_H	00000000_B
A/D input enable register (ADER0)	R/W	$0000C5_H$	11111111_B
A/D input enable register (ADER1)	R/W	$0000D0_H$	11111111_B
Port 0 pull-up resistor setting register (RDR0)	R/W	$00008C_H$	00000000_B
Port 1 pull-up resistor setting register (RDR1)	R/W	$00008D_H$	00000000_B
Port 2 pull-up resistor setting register (RDR2)	R/W	$00008E_H$	00000000_B
Port 3 pull-up resistor setting register (RDR3)	R/W	$00008F_H$	00000000_B

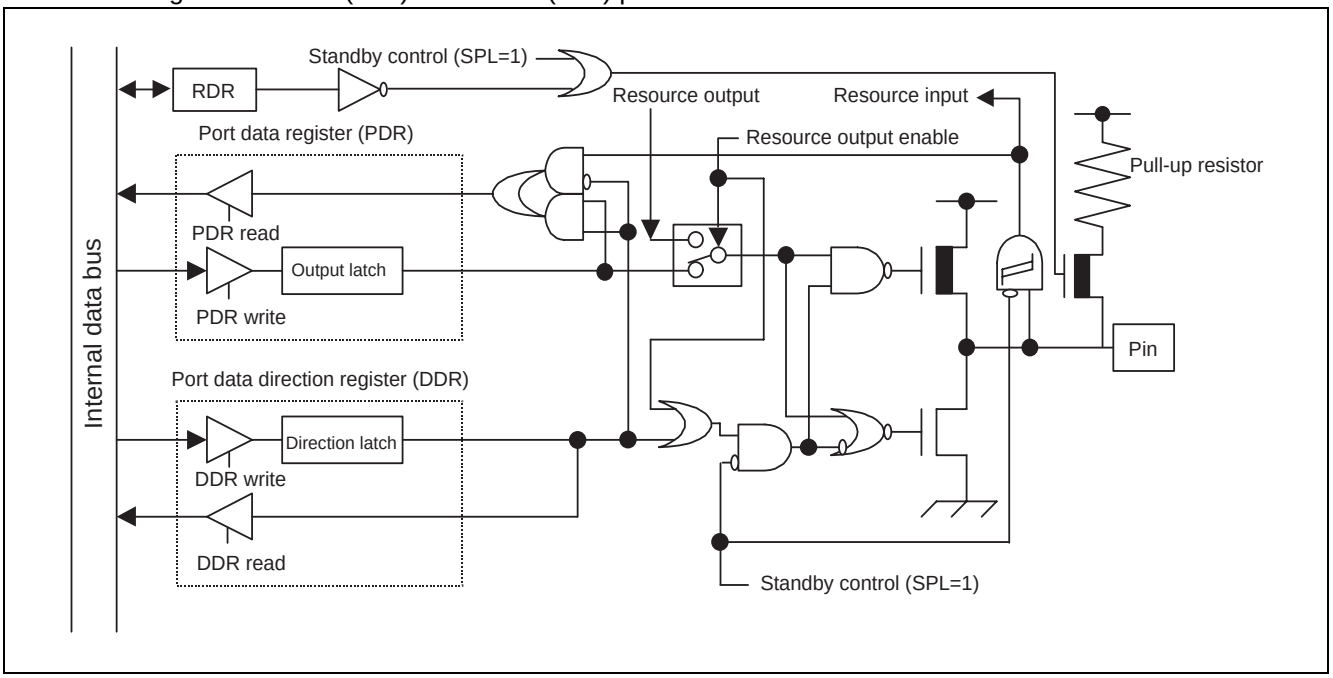
R/W: Read/write enabled
X : Undefined

(3) Block diagram

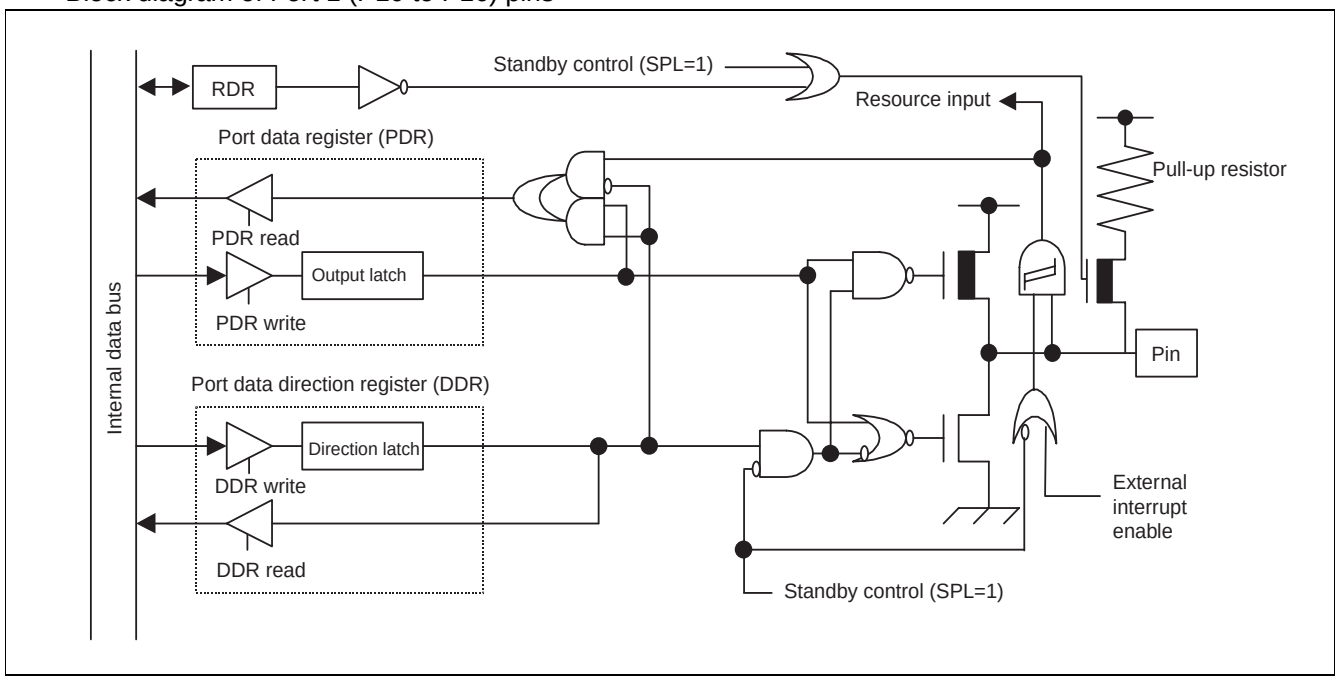
- Block diagram of Port 0 (P00 to P06), Port 1 (P17) and Port 2 (excluding P21) pins



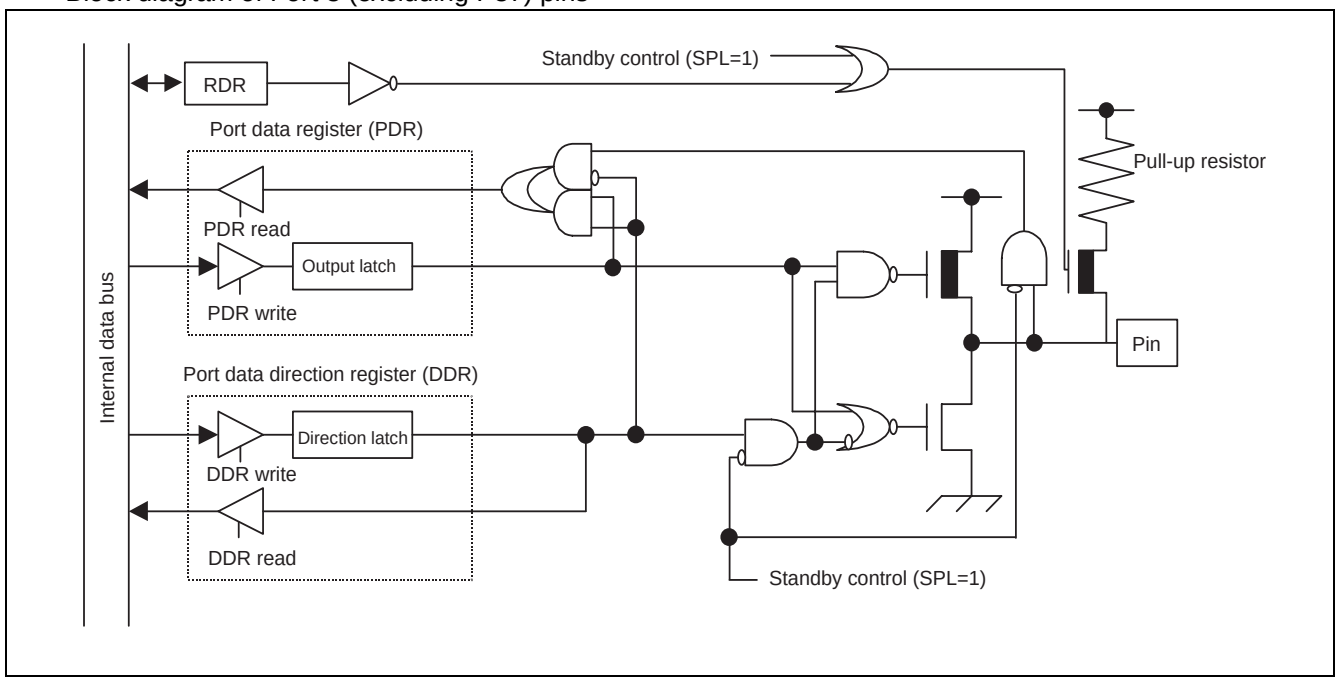
- Block diagram of Port 0 (P07) and Port 2 (P21) pins



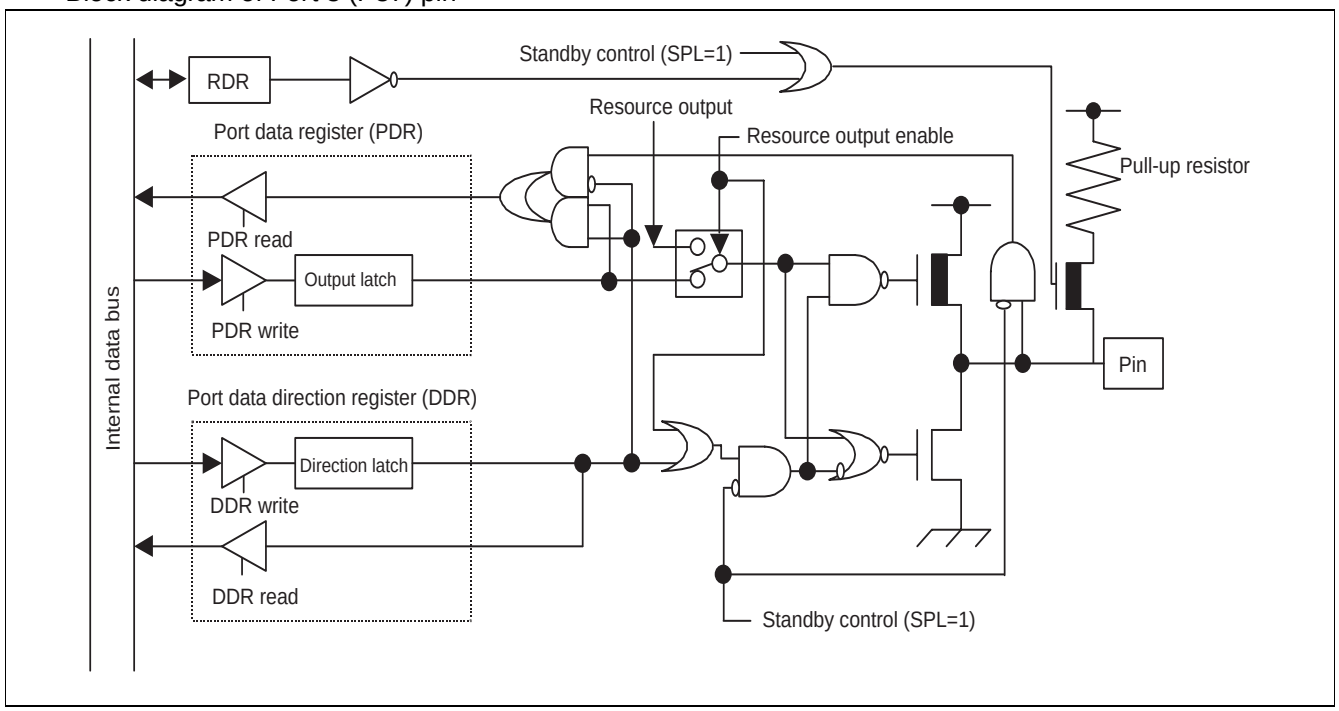
- Block diagram of Port 1 (P10 to P16) pins



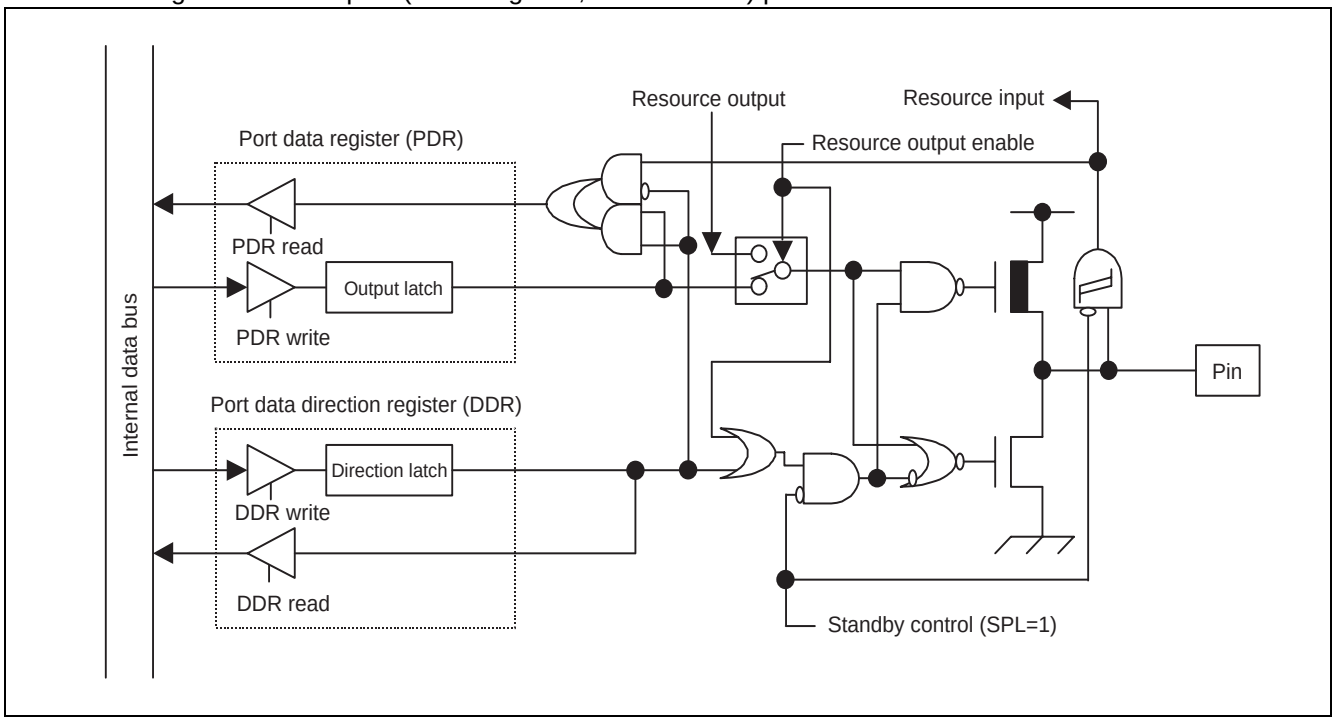
- Block diagram of Port 3 (excluding P37) pins



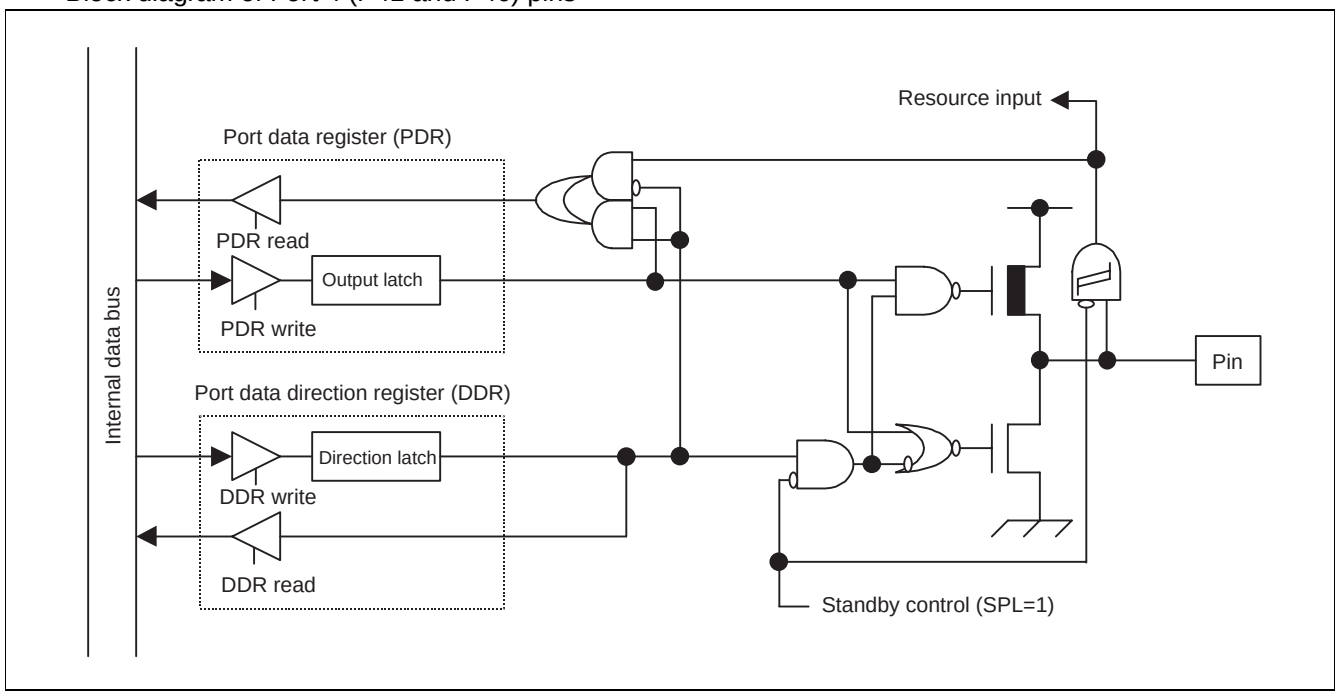
- Block diagram of Port 3 (P37) pin



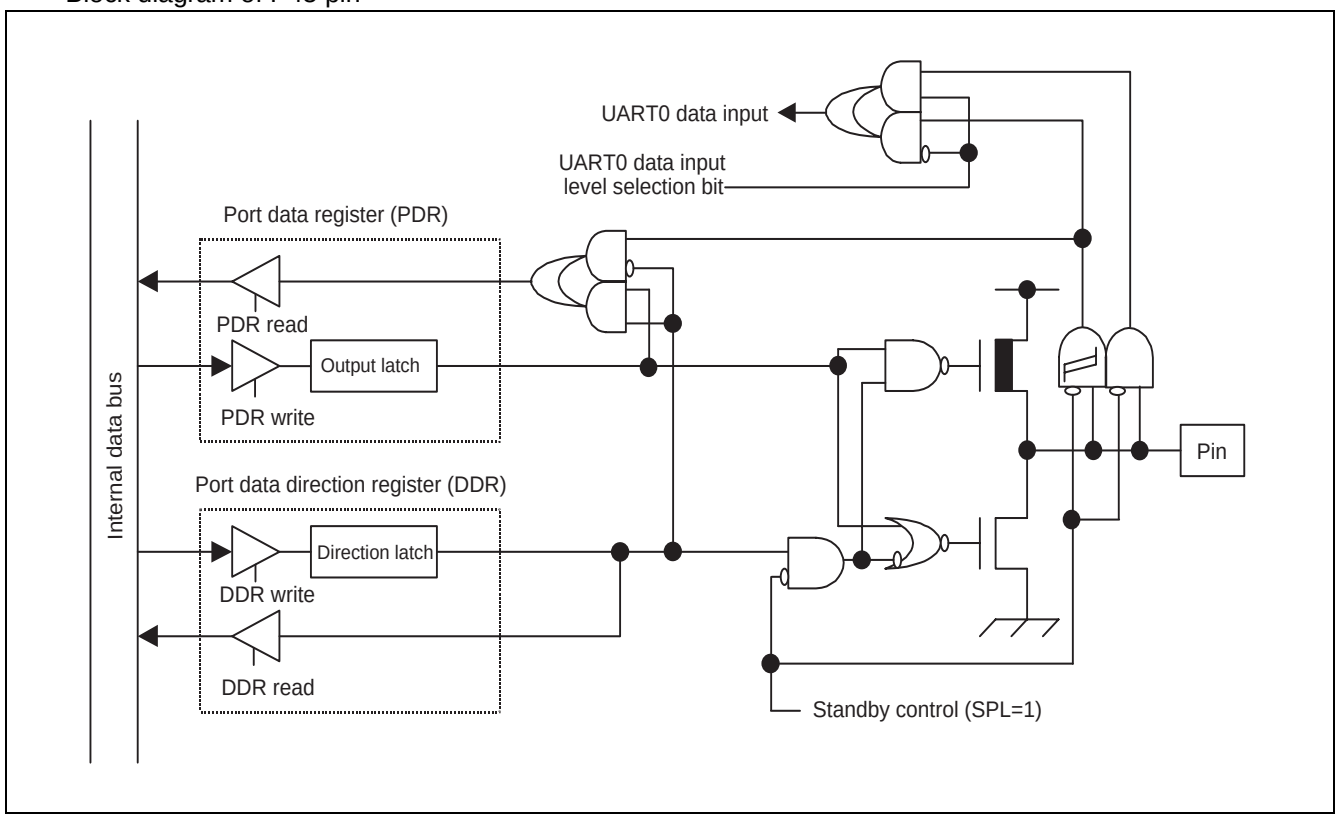
- Block diagram of Port 4 pins (excluding P41, P45 and P46) pins



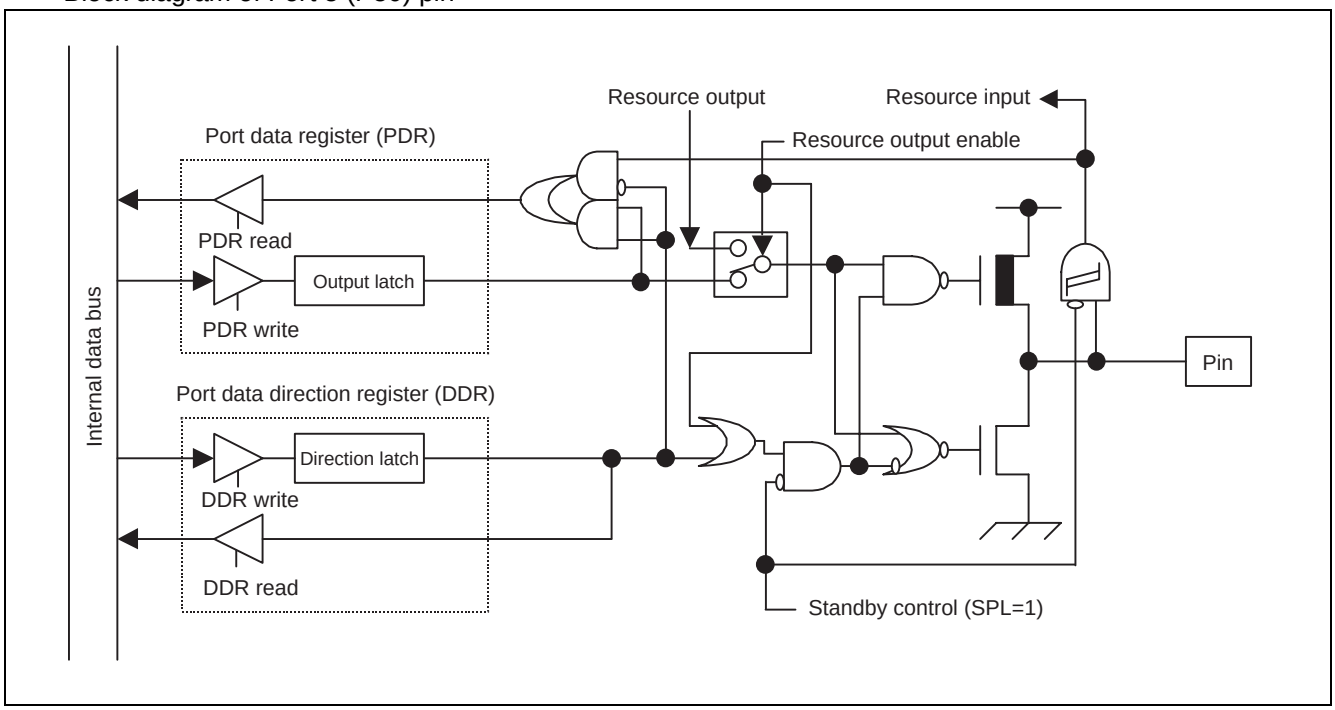
- Block diagram of Port 4 (P41 and P46) pins



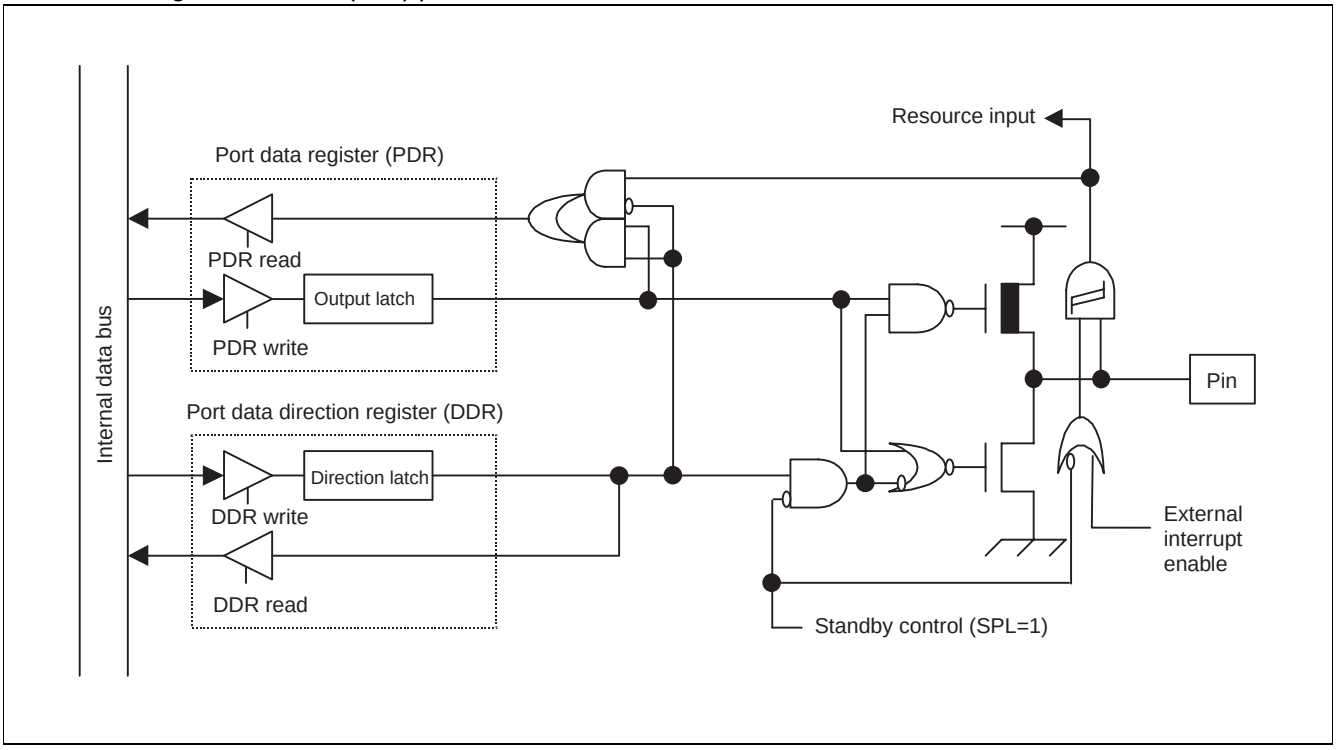
- Block diagram of P45 pin



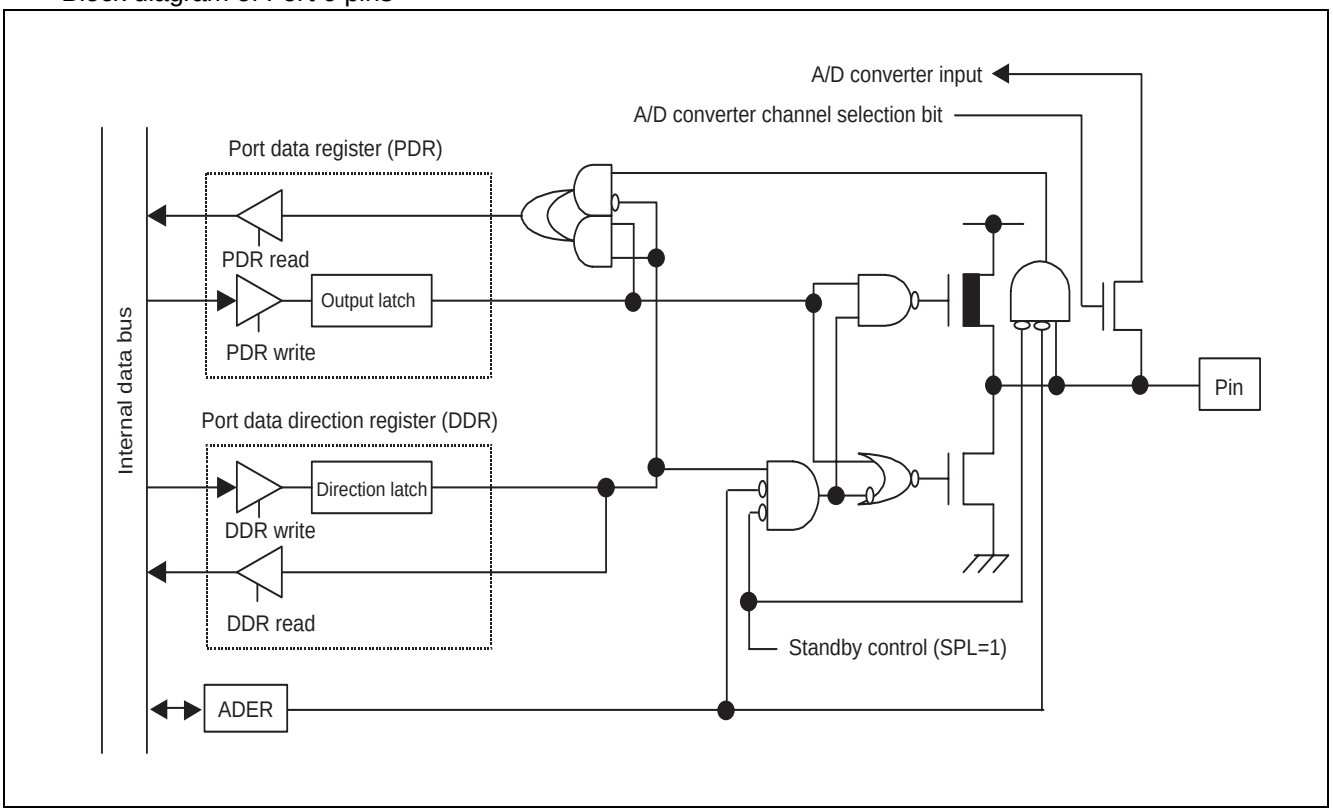
- Block diagram of Port 5 (P50) pin



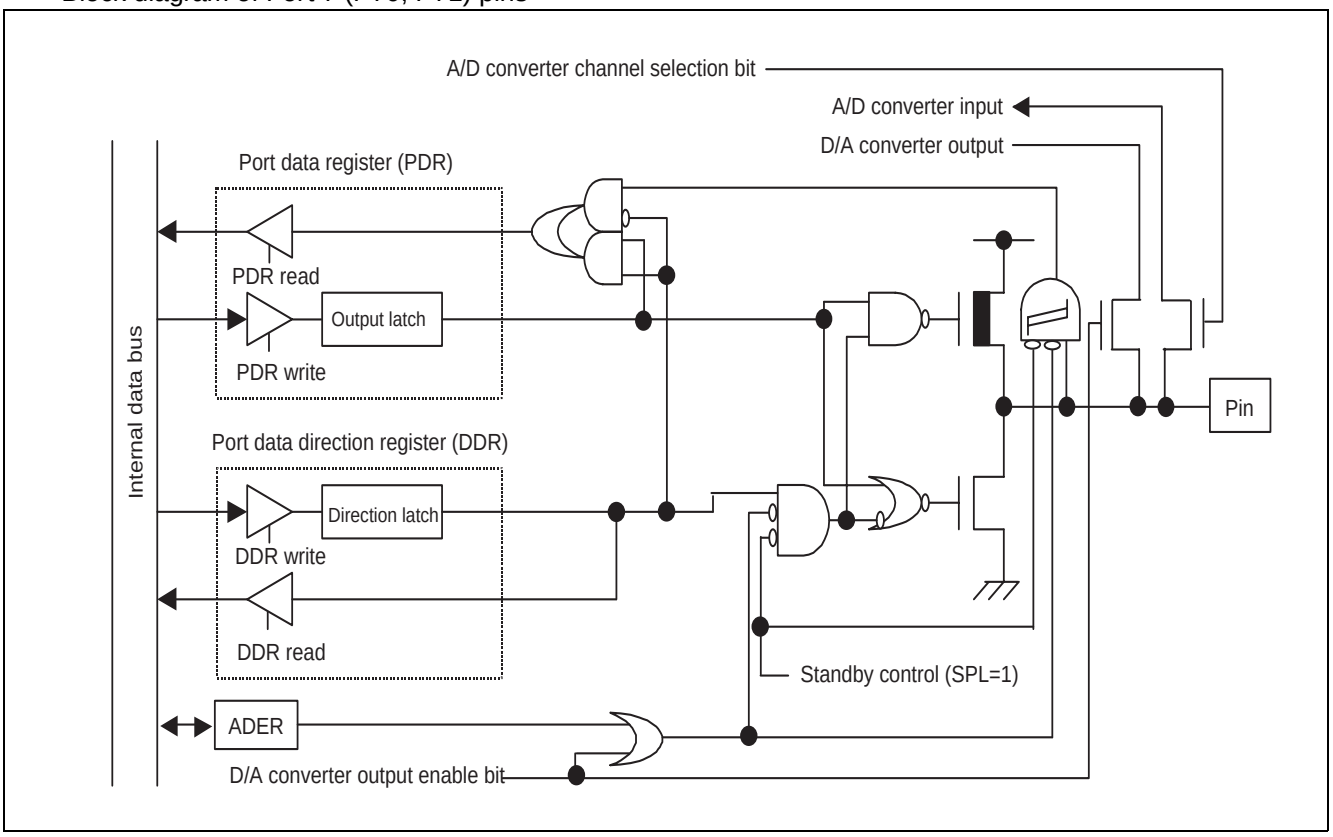
- Block diagram of Port 5 (P51) pin



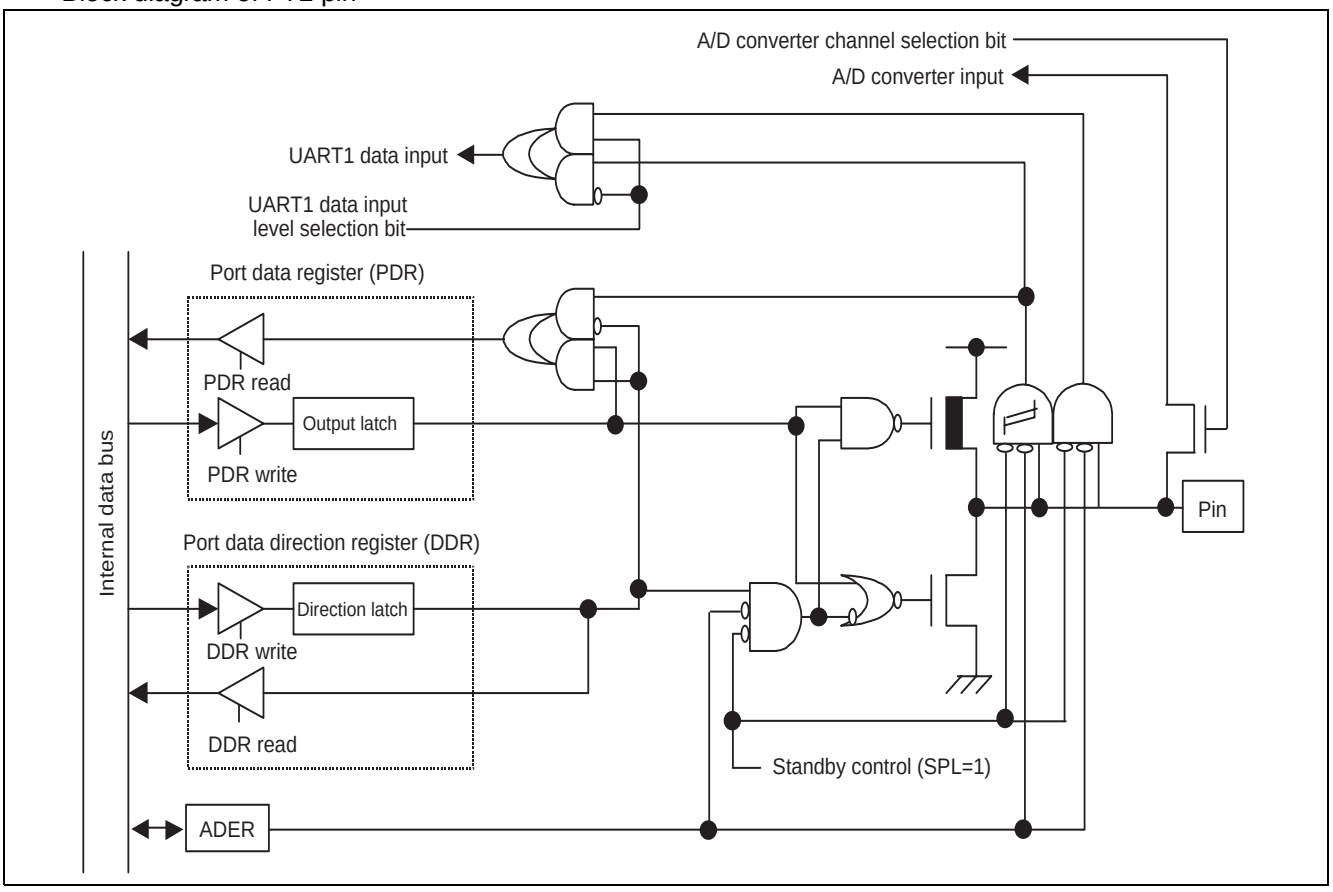
- Block diagram of Port 6 pins



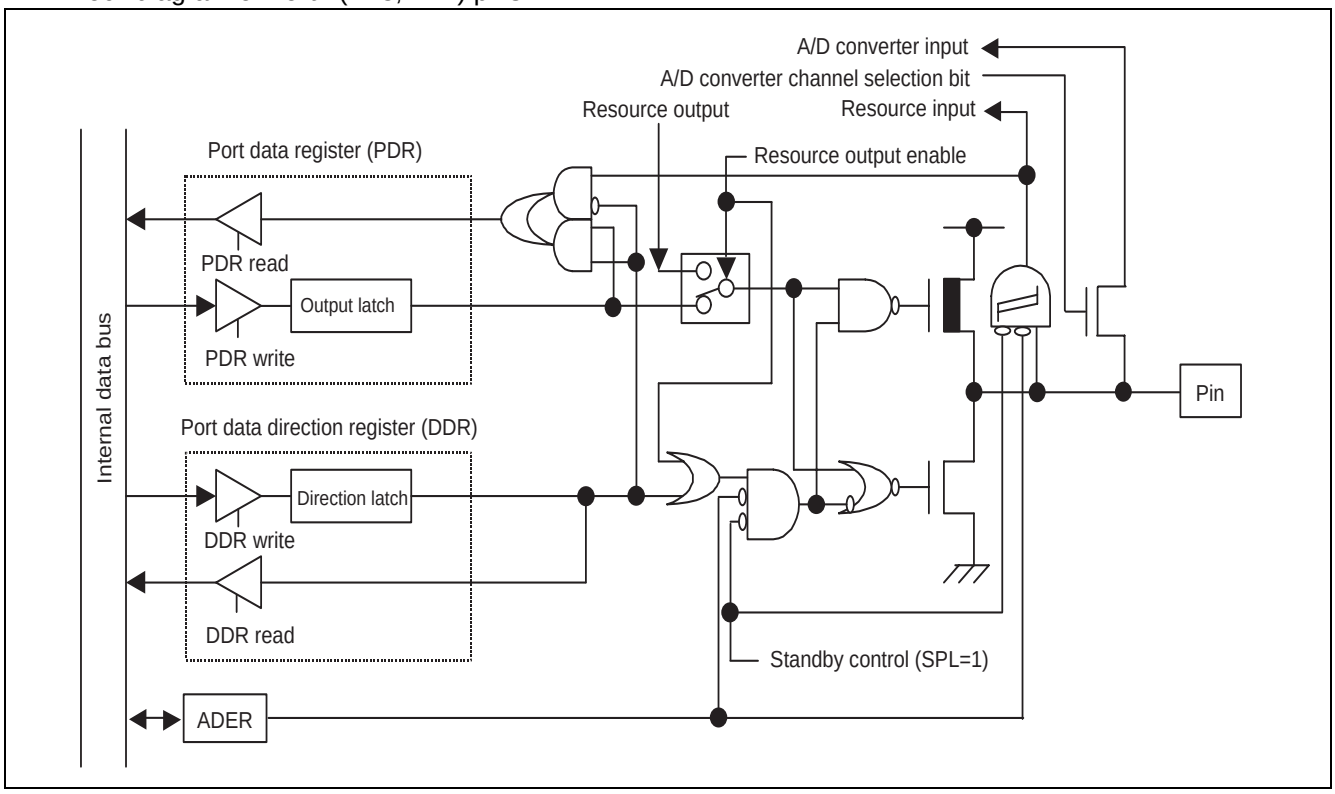
- Block diagram of Port 7 (P70, P71) pins



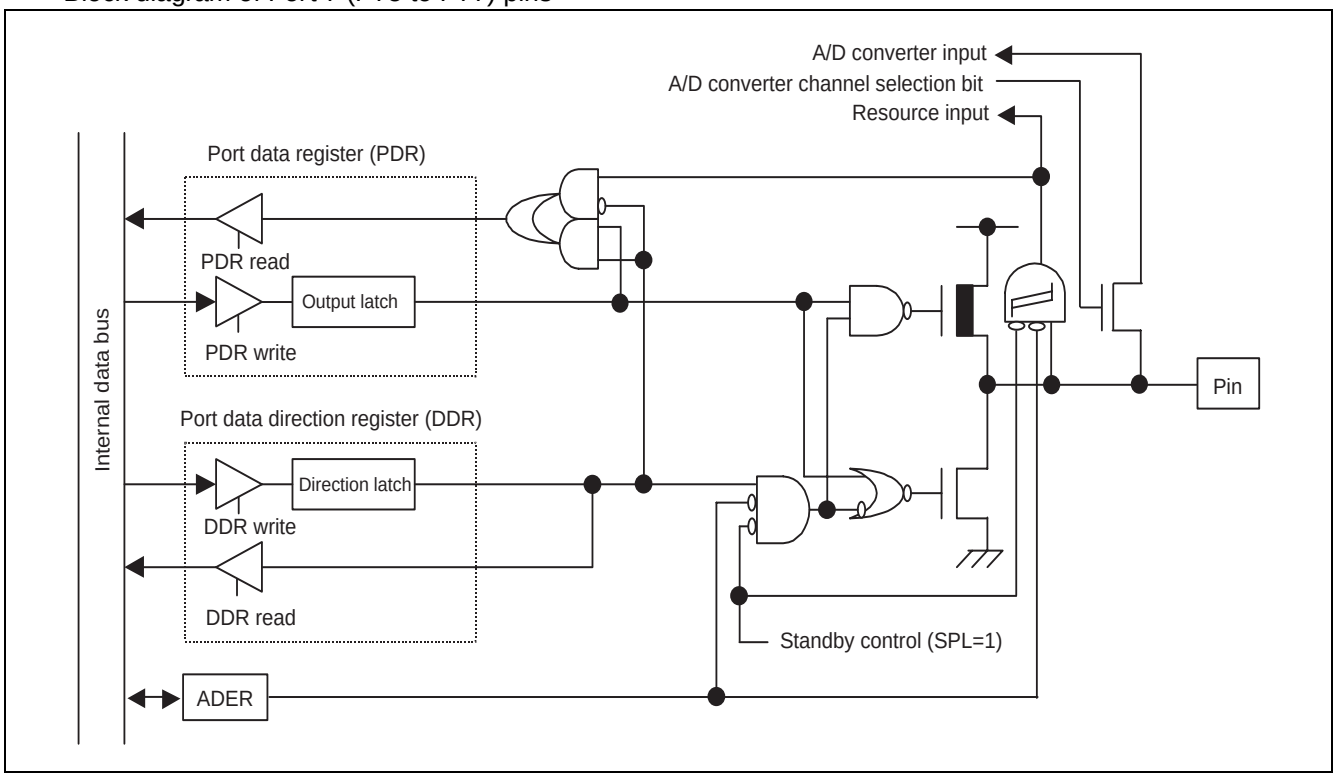
• Block diagram of P72 pin



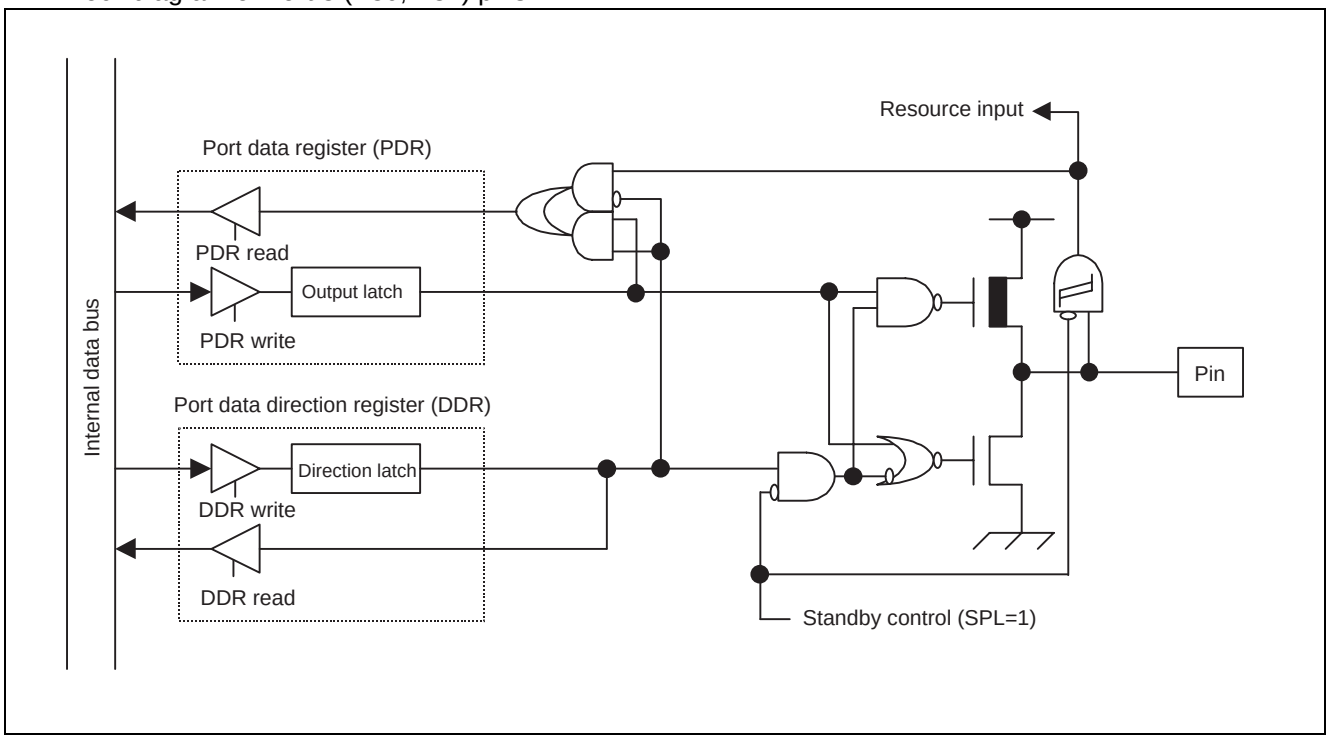
• Block diagram of Port 7(P73, P74) pins



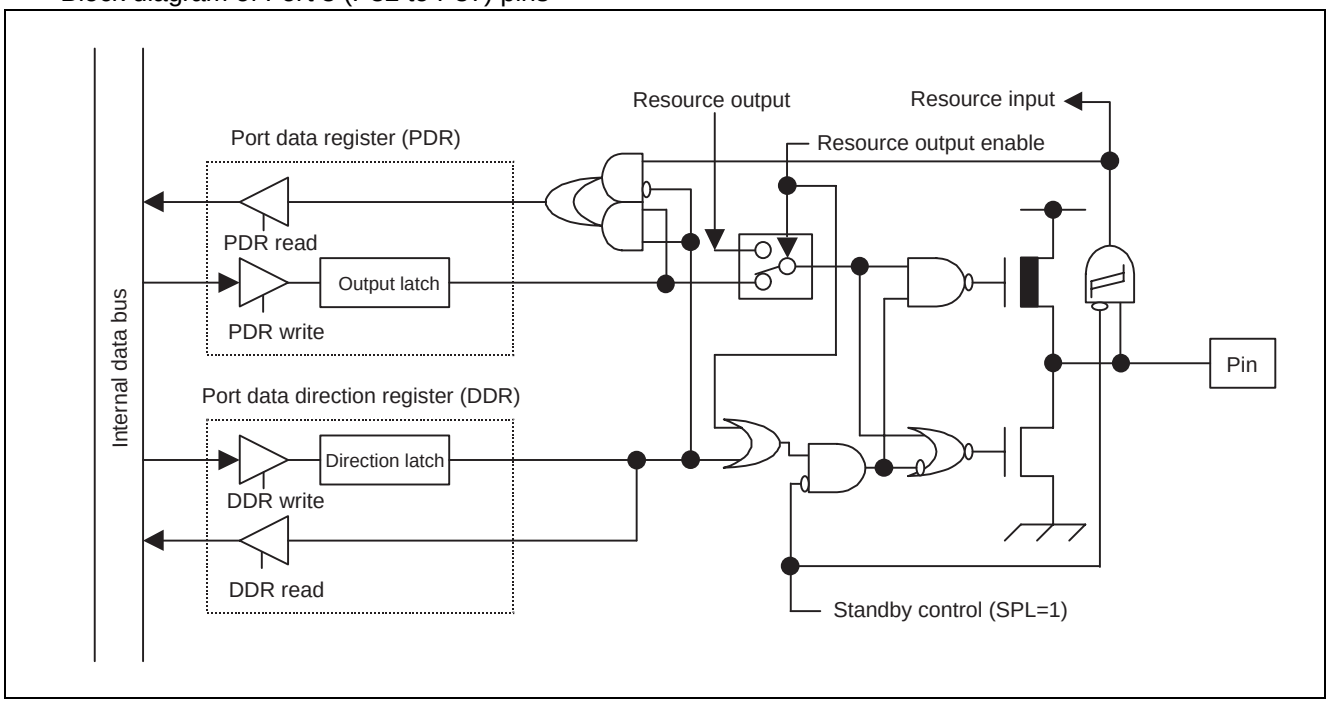
- Block diagram of Port 7 (P75 to P77) pins



- Block diagram of Port 8 (P80, P81) pins



- Block diagram of Port 8 (P82 to P87) pins



3. Timebase Timer

The timebase timer is an 18-bit free-running counter (timebase counter) that counts up in synchronization with the internal count clock (divided by 1/2 of oscillation clock).

Features of timebase timer :

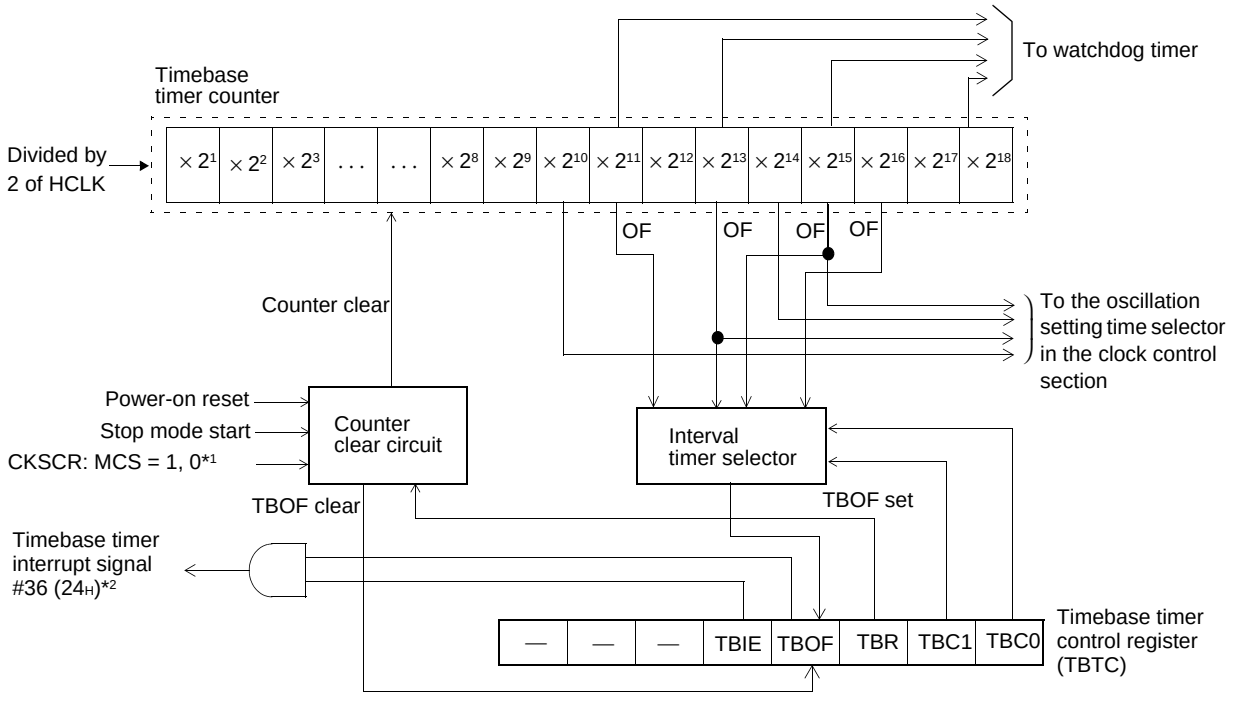
- Generates the interruption at counter-overflow
- Supports for EI^{2}OS
- Interval timer function:
  Generates an interrupt at four different time intervals
- Clock supply function:
  Four different clock can be selected as watchdog timer's count clock
  Supply clock for oscillation stabilization

(1) Register configuration

Timebase Timer Control Register

	15	14	13	12	11	10	9	8	⇦ Bit number
Address: 0000A9$_H$	Reserved	——	——	TBIE	TBOF	TBR	TBC1	TBC0	TBTC
Read/write ⇨	R/W	——	——	R/W	R/W	W	R/W	R/W	
Initial value ⇨	1	X	X	0	0	1	0	0	

(2) Block diagram



OF: Overflow
HCLK: Oscillation clock
*1: Switching of the machine clock from the oscillation clock to the PLL clock
*2: Interrupt number

4. Watchdog Timer

The watchdog timer is a 2-bit counter that uses the timebase timer's supply clock as the count clock. After activation, if the watchdog timer is not cleared within a given period, the CPU will be reset.

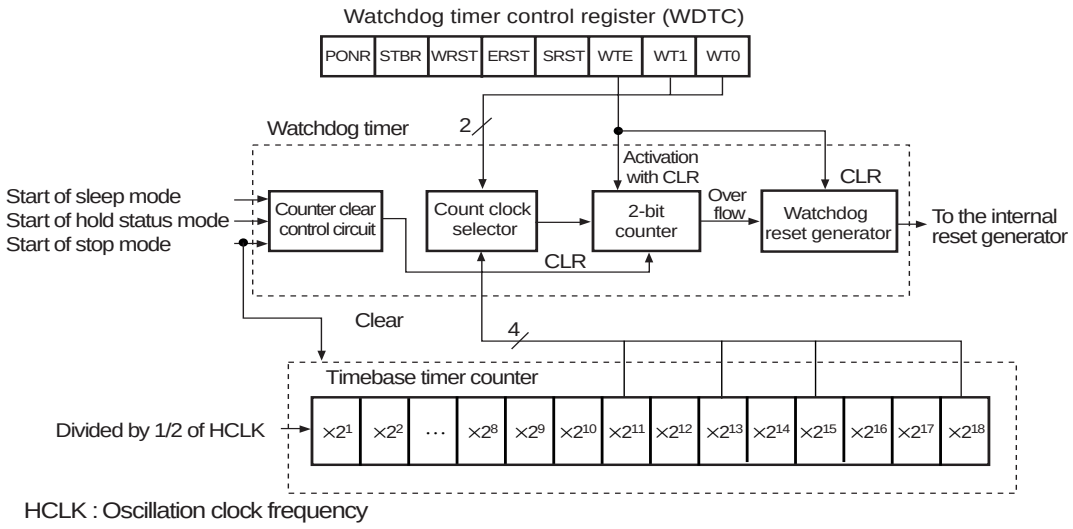
- Features of watchdog timer :
  Reset CPU at four different time intervals
  Indicate the reset causes by status bits

(1) Register configuration

Watchdog Timer Control Register

	7	6	5	4	3	2	1	0	⇦ Bit
Address: 0000A8H	PONR	—	WRST	ERST	SRST	WTE	WT1	WT0	WDTC
Read/write ⇨	R	—	R	R	R	W	W	W	
Initial value ⇨	X	X	X	X	X	1	1	1	

(2) Block diagram



5. 16-bit reload timer (x 2)

The 16-bit reload timer provides two operating mode, internal clock mode and event count mode. In each operating mode, the 16-bit down counter can be reloaded (reload mode) or stopped by underflow (one-shot mode).
Output pins TO1 and TO0 are able to output different waveform according to the counter operating mode. TO1 and TO0 toggles when counter underflows if counter is operated as reload mode. TO1 and TO0 output specified level (H or L) during counting if the counter is in one-shot mode.

Features of the 16-bit reload timer :

- Interrupt when timer underflows
- Supports for EI^{2}OS
- Internal clock operating mode :
  Three internal count clocks can be selected.
  Counter can be activated by software or external trigger (signal at TIN1 and TIN0 pins).
  Counter can be reloaded or stopped when underflow after activated.
- Event count operating mode :
  Counter counts down one by one with specified edge at TIN1 and TIN0 pins.
  Counter can be reloaded or stopped when underflow.

(1) Register configuration

16-bit Timer Register/16-bit Reload Timer Register (Upper)

Address: ch0 000085H, ch1 000089H	15	14	13	12	11	10	9	8	⇦ Bit
	D15	D14	D13	D12	D11	D10	D09	D08	TMR0, TMR1 / TMRD0, TMRD1
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

16-bit Timer Register/16-bit Reload Timer Register (Lower)

Address: ch0 000084H, ch1 000088H	7	6	5	4	3	2	1	0	⇦ Bit
	D07	D06	D05	D04	D03	D02	D01	D00	TMR0, TMR1 / TMRD0, TMRD1
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

Timer Control Status Register (Upper)

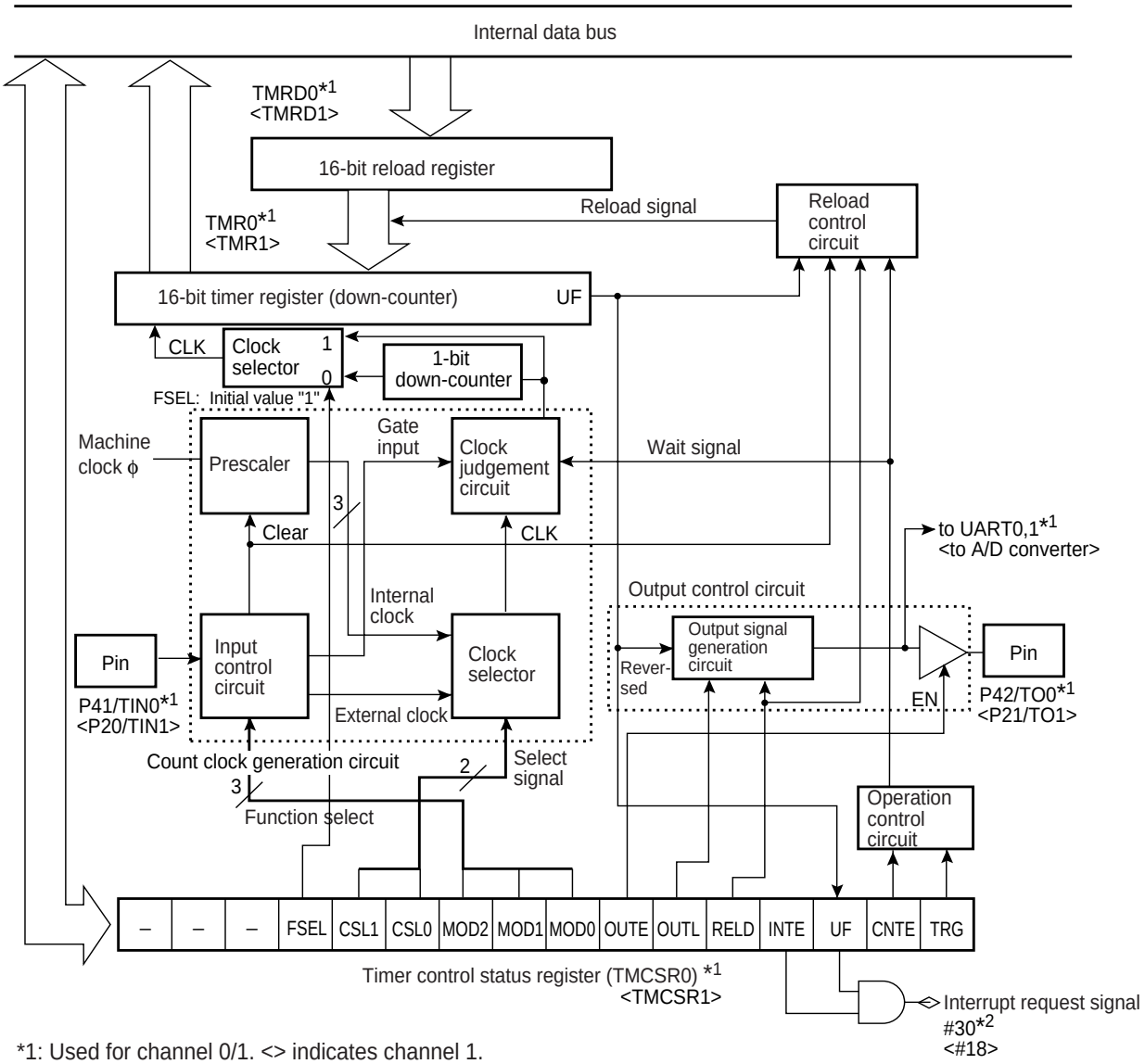
Address: ch0 000083H, ch1 000087H	15	14	13	12	11	10	9	8	⇦ Bit
	—	—	—	FSEL	CSL1	CSL0	MOD2	MOD1	TMCSRH0, TMCSRH1
Read/write ⇨	—	—	—	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	1	0	0	0	0	

Timer Control Status Register (Lower)

Address: ch0 000082H, ch1 000086H	7	6	5	4	3	2	1	0	⇦ Bit
	MOD0	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	TMCSRL0, TMCSRL1
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

Note : Registers TMR0, TMR1/TMRD0, TMRD1 are word access only.

(2) Block diagram



*1: Used for channel 0/1. <> indicates channel 1.
*2: Interrupt number

6. 16-bit PPG Timer (x 3)

The 16-bit PPG timer consists of a 16-bit down counter, prescaler, 16-bit period setting register, 16-bit duty setting register, 16-bit control register and a PPG output pin. This module can be used to output pulses synchronized by software trigger or GATE signal from Multi-functional timer, refer to “7. Multi-functional Timer”.

Features of 16-bit PPG timer :

- Two operating mode : PWM and One-shot mode
- 8 types of counter operation clock (ϕ, ϕ/2, ϕ/4, ϕ/8, ϕ/16, ϕ/32, ϕ/64, ϕ/128) can be selected
- Interrupt is generated when trigger signal arrived, or counter borrow, or change of PPG output
- Supports for EI^{2}OS

(1) Register configuration

PPG Control Status Register (Upper)

Address: ch0 00003F$_H$
ch1 000047$_H$
ch2 00004F$_H$

Bit	15	14	13	12	11	10	9	8
	CNTE	STGR	MDSE	RTRG	CKS2	CKS1	CKS0	PGMS
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value ⇨	0	0	0	0	0	0	0	0

PCNTH0 to PCNTH2

PPG Control Status Register (Lower)

Address: ch0 00003E$_H$
ch1 000046$_H$
ch2 00004E$_H$

Bit	7	6	5	4	3	2	1	0
	—	—	IREN	IRQF	IRS1	IRS0	POEN	OSEL
Read/write ⇨	—	—	R/W	R/W	R/W	R/W	R/W	R/W
Initial value ⇨	X	X	0	0	0	0	0	0

PCNTL0 to PCNTL2

PPG Duty Setting Register (Upper)

Address: ch0 00003D$_H$
ch1 000045$_H$
ch2 00004D$_H$

Bit	15	14	13	12	11	10	9	8
	DU15	DU14	DU13	DU12	DU11	DU10	DU09	DU08
Read/write ⇨	W	W	W	W	W	W	W	W
Initial value ⇨	X	X	X	X	X	X	X	X

PDUT0 to PDUT2

PPG Duty Setting Register (Lower)

Address: ch0 00003C$_H$
ch1 000044$_H$
ch2 00004C$_H$

Bit	7	6	5	4	3	2	1	0
	DU07	DU06	DU05	DU04	DU03	DU02	DU01	DU00
Read/write ⇨	W	W	W	W	W	W	W	W
Initial value ⇨	X	X	X	X	X	X	X	X

PDUT0 to PDUT2

PPG Period Setting Register (Upper)

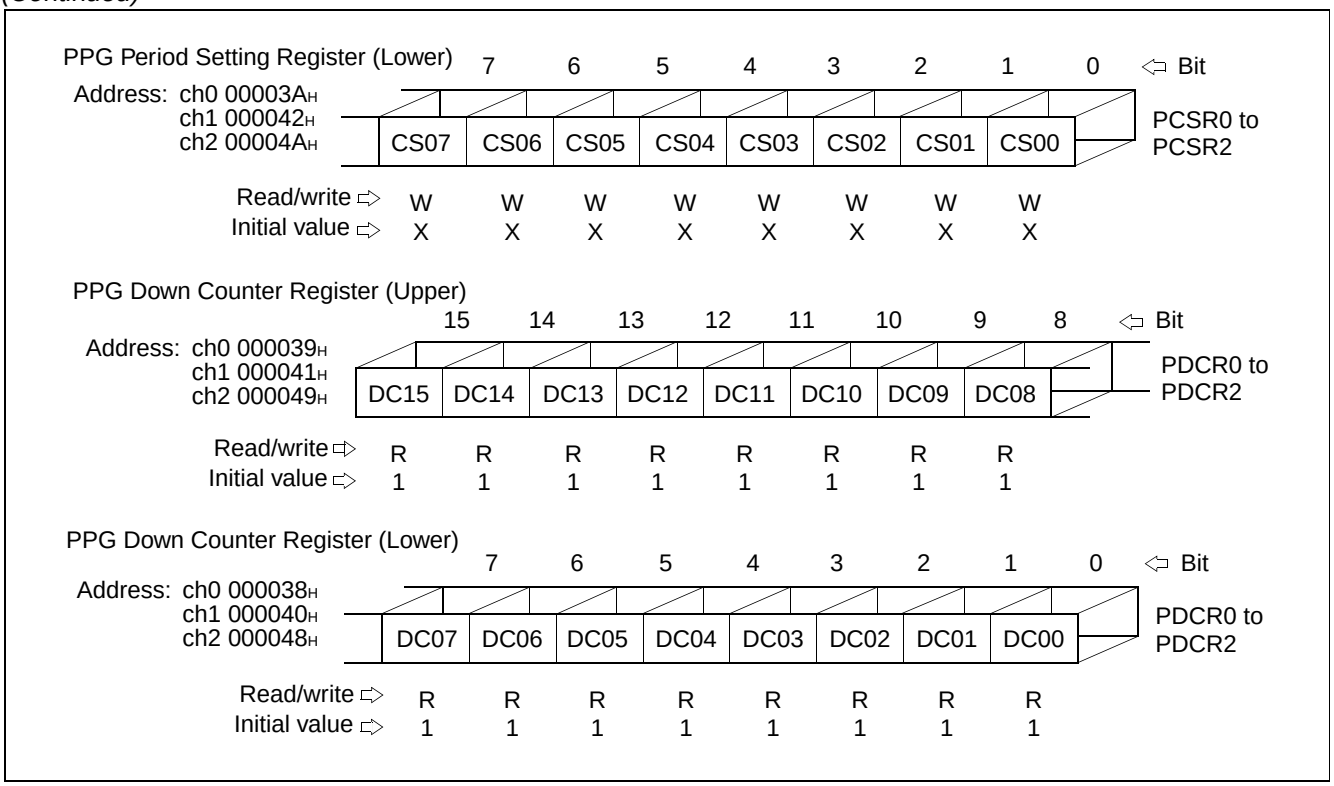
Address: ch0 00003B$_H$
ch1 000043$_H$
ch2 00004B$_H$

Bit	15	14	13	12	11	10	9	8
	CS15	CS14	CS13	CS12	CS11	CS10	CS09	CS08
Read/write ⇨	W	W	W	W	W	W	W	W
Initial value ⇨	X	X	X	X	X	X	X	X

PCSR0 to PCSR2

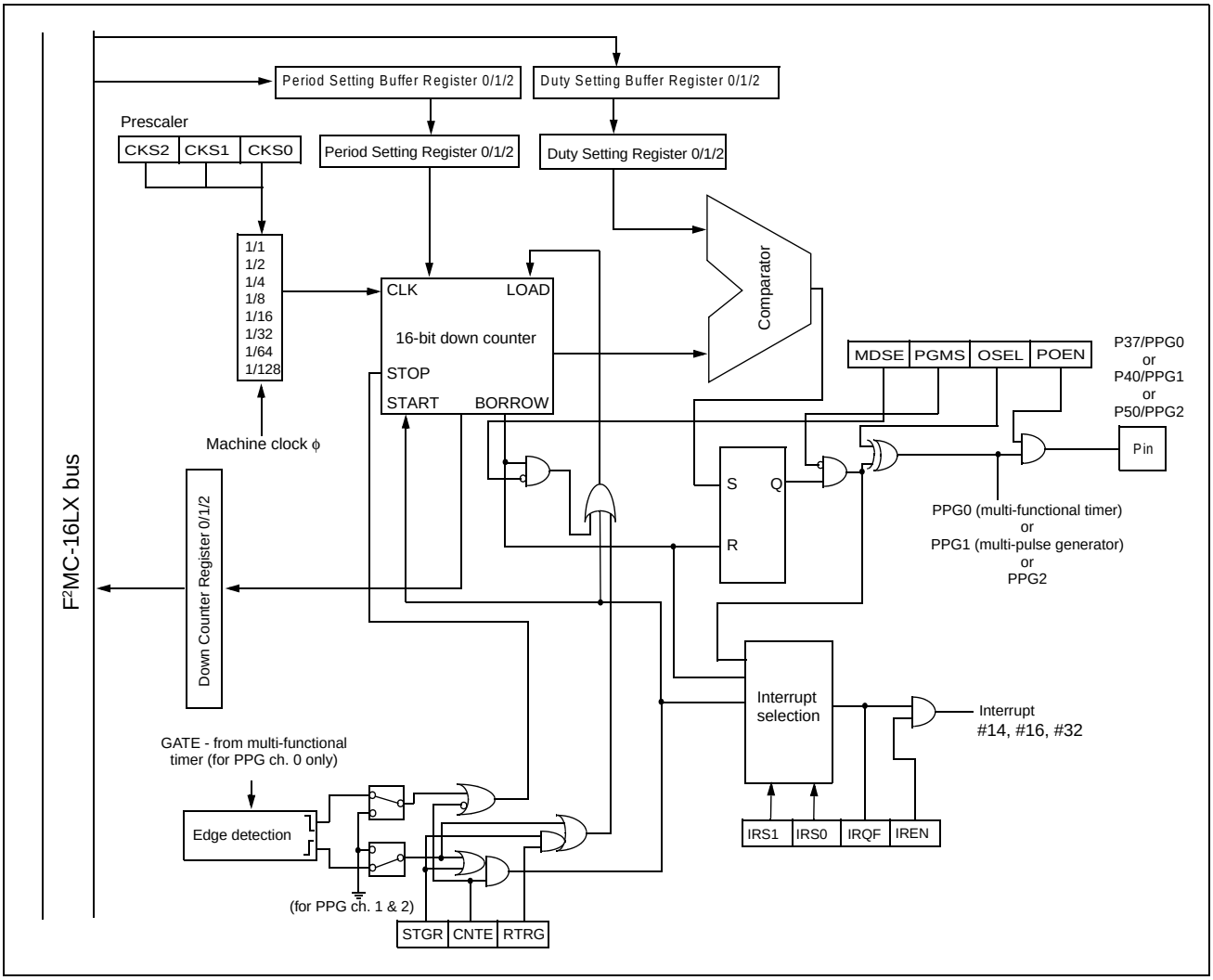
(Continued)

(Continued)



Note : Registers PDCR0 to PDCR2, PDSR0 to PDSR2 and PDUT0 to PDUT2 are word access only.

(2) Block diagram



7. Multi-functional Timer

The 16-bit multi-functional timer module consists of one 16-bit free-running timer, four input capture circuits, six output comparators and one channel of 16-bit PPG timer. This module allows six independent waveforms generated by PPG timer or waveform generator to be outputted. With the 16-bit free-running timer and the input capture circuit, input pulse width and external clock period measurement can be done.

(1) 16-bit free-running timer (1 channel)

- The 16-bit free-running timer consists of a 16-bit up/up-down counter, timer control status register, 16-bit compare clear register (with buffer register) and a prescaler.
- 8 types of counter operation clock (ϕ, ϕ/2, ϕ/4, ϕ/8, ϕ/16, ϕ/32, ϕ/64, ϕ/128) can be selected. (ϕ is the machine clock.)
- Two types of interrupt causes :
  - Compare clear interrupt is generated when there is a comparing match with compare clear register and 16-bit free-running timer.
  - Zero detection interrupt is generated while 16-bit free-running timer is detected as zero in count value.
- EI^{2}OS supported.
- Compare-clear register buffer provided :
  The selectable buffer enables the 16-bit free-running timer update its compare-clear register automatically without stop the timer operation. User can read the next compare-clear value to the compare-clear register when the timer is running. The compare-clear register will be updated when the timer value is "0000$_H$"
- Reset, software clear, compare match with compare clear register in up-count mode will reset the counter value to "0000$_H$".
- Supply clock to output compare module :
  The prescaler output is acted as the count clock of the output compare.

(2) Output compare module (6 channels)

- The output compare module consists of six 16-bit output compare registers (with selectable buffer register), compare output latch and compare control registers. An interrupt is generated and output level is inverted when the value of 16-bit free-running timer and output compare register are matched.
- 6 output compare registers can be operated independently.
- Output pins and interrupt flag are corresponding to each output compare register.
- 2 output compare registers can be paired to control the output pins.
- Inverts output pins by using 2 output compare registers together.
- Setting the initial value for each output pin is possible.
- Interrupt is generated when there is a comparing match with output compare register and 16-bit free-running timer.
- EI^{2}OS supported.

(3) Input capture module (4 channels)

Input capture consists of 4 independent external input pins, the corresponding input capture data register and input capture control status register. By detecting any edge of the input signal from the external pin, the value of the 16-bit free-running timer can be stored in the capture register and an interrupt is generated simultaneously.

- Operations synchronized with the 16-bit free-running timer's count clock.
- 3 types of trigger edge (rising edge, falling edge and both edge) of the external input signal can be selected and there is indication bit to show the trigger edge is rising or falling.
- 4 input captures can be operated independently.
- Two independent interrupts are generated when detecting a valid edge from external input.
- EI^{2}OS supported.

(4) 16-bit PPG timer (1 channel)

The 16-bit PPG timer 0 is used to provide a PPG signal for waveform generator. (See section “6. 16-bit PPG Timer”.)

(5) Waveform generator module

The waveform generator consists of three 16-bit timer registers, three 16-bit timer control registers and a waveform control register.
With waveform generator, it is possible to generate real time output, 16-bit PPG waveform output, non-overlap 3-phase waveform output for inverter control and DC chopper waveform output.

- It is possible to generate a non-overlap waveform output based on dead-time of 16-bit timer. (Dead-time timer function)
- It is possible to generate a non-overlap waveform output when realtime output is operated in 2-channel mode. (Dead-time timer function)
- By detecting realtime output compare match, GATE signal of the PPG timer operation will be generated to start or stop PPG timer operation. (GATE function)
- When a match is detected by real time output compare, the 16-bit timer is activated. The PPG timer can be started or stopped easily by generating a GATE signal for PPG operation until the 16-bit timer stops. (GATE function)
- Force to stop output waveform using DTTI pin input.
- Interrupt is generated when DTTI active or 16-bit timer underflow.
- EI^{2}OS is supported.

(6) Register configuration

- 16-bit free-running timer registers

Timer Control Status Register (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit
Address: 00005F$_H$	ECKE	IRQZF	IRQZE	MSI2	MSI1	MSI0	ICLR	ICRE	TCCSH
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

Timer Control Status Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit
Address: 00005E$_H$	—	BFE	STOP	MODE	SCLR	CLK2	CLK1	CLK0	TCCSL
Read/write ⇨	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	0	1	0	0	0	0	0	

Timer Data Register (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit
Address: 00005D$_H$	T15	T14	T13	T12	T11	T10	T09	T08	TCDT
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

Timer Data Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit
Address: 00005C$_H$	T07	T06	T05	T04	T03	T02	T01	T00	TCDT
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

(Continued)

(Continued)

Compare Clear Buffer Register / Compare Clear Register (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit
Address: 00005B$_H$	CL15	CL14	CL13	CL12	CL11	CL10	CL09	CL08	CPCLRB/CPCLR
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	1	1	1	1	1	1	1	1	

Compare Clear Buffer Register / Compare Clear Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit
Address: 00005A$_H$	CL07	CL06	CL05	CL04	CL03	CL02	CL01	CL00	CPCLRB/CPCLR
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	1	1	1	1	1	1	1	1	

Note : Registers TCDT, CPCLRB/CPCLR are word access only.

- Output compare registers

Compare Control Register (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit
Address: ch1 00007D$_H$ ch3 00007F$_H$ ch5 000081$_H$	—	BTS1	BTS0	CMOD	OTE1	OTE0	OTD1	OTD0	OCS1/3/5
Read/write ⇨	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	1	1	0	0	0	0	0	

Compare Control Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit
Address: ch0 00007C$_H$ ch2 00007E$_H$ ch4 000080$_H$	IOP1	IOP0	IOE1	IOE0	BUF1	BUF0	CST1	CST0	OCS0/2/4
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	1	1	0	0	

Output Compare Buffer Register / Output Compare Register (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit
Address: ch0 000071$_H$ ch1 000073$_H$ ch2 000075$_H$ ch3 000077$_H$ ch4 000079$_H$ ch5 00007B$_H$	OP15	OP14	OP13	OP12	OP11	OP10	OP09	OP08	OCCPB0 to OCCPB5/ OCCP0 to OCCP5
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

Output Compare Buffer Register / Output Compare Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit
Address: ch0 000070$_H$ ch1 000072$_H$ ch2 000074$_H$ ch3 000076$_H$ ch4 000078$_H$ ch5 00007A$_H$	OP07	OP06	OP05	OP04	OP03	OP02	OP01	OP00	OCCPB0 to OCCPB5/ OCCP0 to OCCP5
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

Note : Register OCCPB0 to OCCPB5/OCCP0 to OCCP5 are word access only.

- Input capture registers

Input Capture Control Status Register (2/3) (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit
Address: 00006B$_H$	—	—	—	—	—	—	IEI3	IEI2	ICSH23
Read/write ⇨	—	—	—	—	—	—	R	R	
Initial value ⇨	X	X	X	X	X	X	0	0	

Input Capture Control Status Register (2/3) (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit
Address: 00006A$_H$	ICP3	ICP2	ICE3	ICE2	EG31	EG30	EG21	EG20	ICSL23
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

PPG output control/ Input Capture Control Status Register (0/1) (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit
Address: 000069$_H$	PGEN5	PGEN4	PGEN3	PGEN2	PGEN1	PGEN0	IEI1	IEI0	PICSH01
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R	R	
Initial value ⇨	0	0	0	0	0	0	0	0	

Input Capture Control Status Register (0/1) (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit
Address: 000068$_H$	ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00	PICSL01
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

Input Capture Data Register (Upper)

Address: ch0 000061$_H$
ch1 000063$_H$
ch2 000065$_H$
ch3 000067$_H$

	15	14	13	12	11	10	9	8	⇦ Bit
	CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08	IPCP0 to IPCP3
Read/write ⇨	R	R	R	R	R	R	R	R	
Initial value ⇨	X	X	X	X	X	X	X	X	

Input Capture Data Register (Lower)

Address: ch0 000060$_H$
ch1 000062$_H$
ch2 000064$_H$
ch3 000066$_H$

	7	6	5	4	3	2	1	0	⇦ Bit
	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00	IPCP0 to IPCP3
Read/write ⇨	R	R	R	R	R	R	R	R	
Initial value ⇨	X	X	X	X	X	X	X	X	

Note : Registers IPCP0 to IPCP3 are word access only.

• Waveform generator registers

Waveform Control Register

Bit	15	14	13	12	11	10	9	8	
Address: 000059H	DTIE	DTIF	NRSL	DCK2	DCK1	DCK0	NWS1	NWS0	SIGCR
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

16-bit Timer Control Register

Bit	7	6	5	4	3	2	1	0	
Address: ch0 000056H ch2 000058H	DMOD	GTEN1	GTEN0	TMIF	TMIE	TMD2	TMD1	TMD0	DTCR0, DTCR2
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

16-bit Timer Control Register

Bit	15	14	13	12	11	10	9	8	
Address: ch1 000057H	DMOD	GTEN1	GTEN0	TMIF	TMIE	TMD2	TMD1	TMD0	DTCR1
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

16-bit Timer Register (Upper)

Bit	15	14	13	12	11	10	9	8	
Address: ch0 000051H ch1 000053H ch2 000055H	TR15	TR14	TR13	TR12	TR11	TR10	TR09	TR08	TMRR0 to TMRR2
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	X	X	X	X	X	X	X	X	

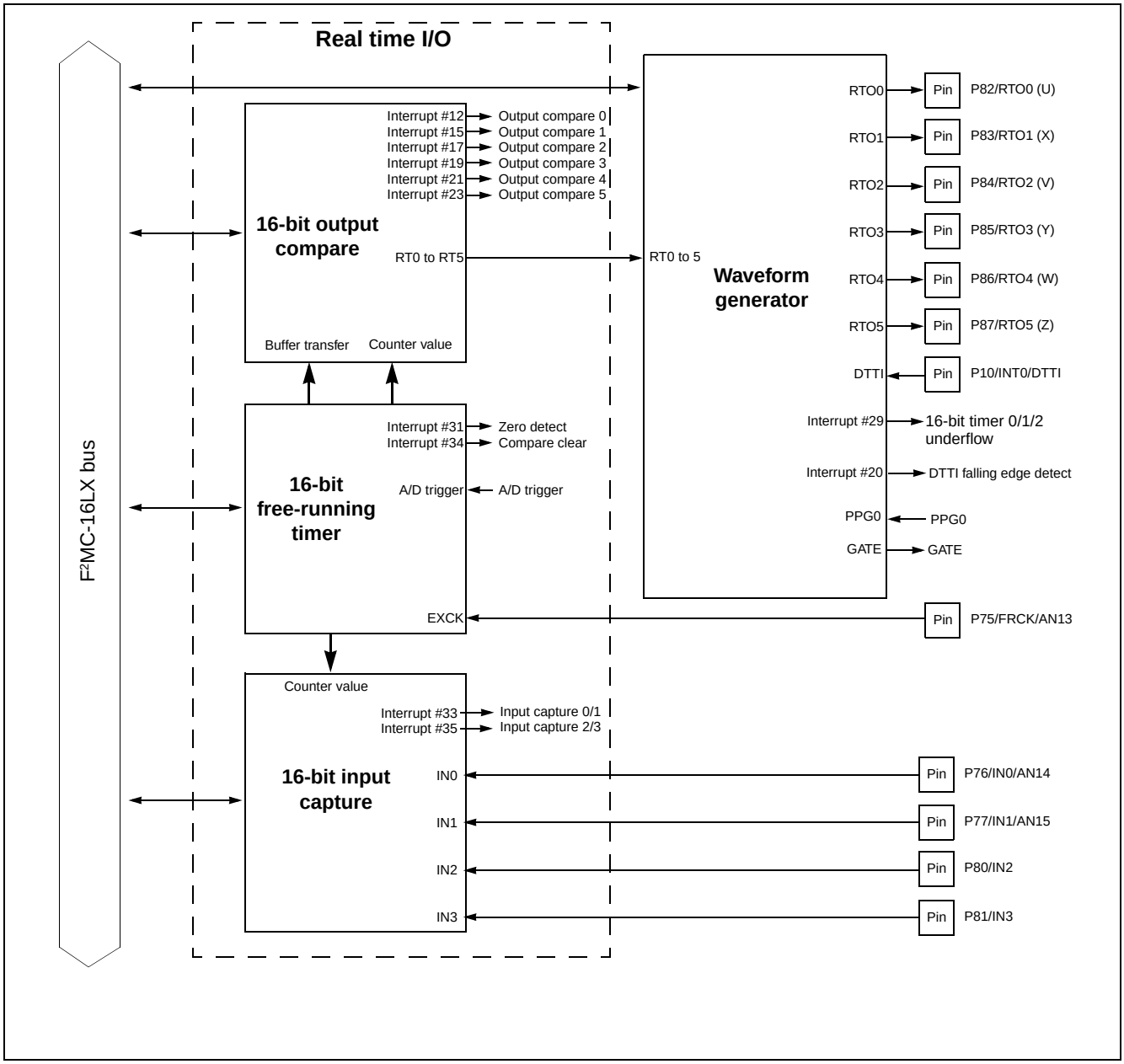
16-bit Timer Register (Lower)

Bit	7	6	5	4	3	2	1	0	
Address: ch0 000050H ch1 000052H ch2 000054H	TR07	TR06	TR05	TR04	TR03	TR02	TR01	TR00	TMRR0 to TMRR2
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	X	X	X	X	X	X	X	X	

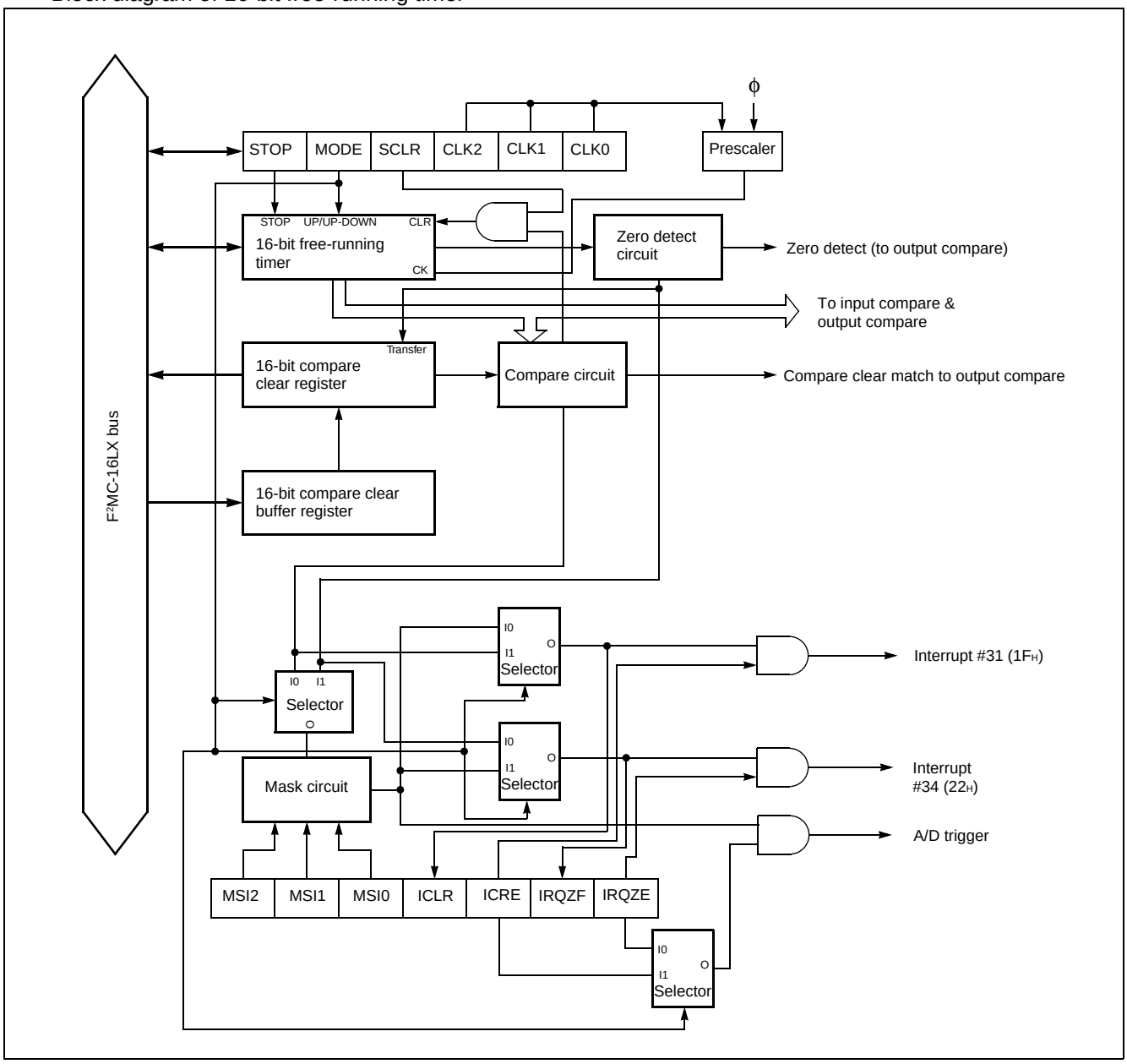
Note : Registers TMRR0 to TMRR2 are word access only.

(7) Block diagram

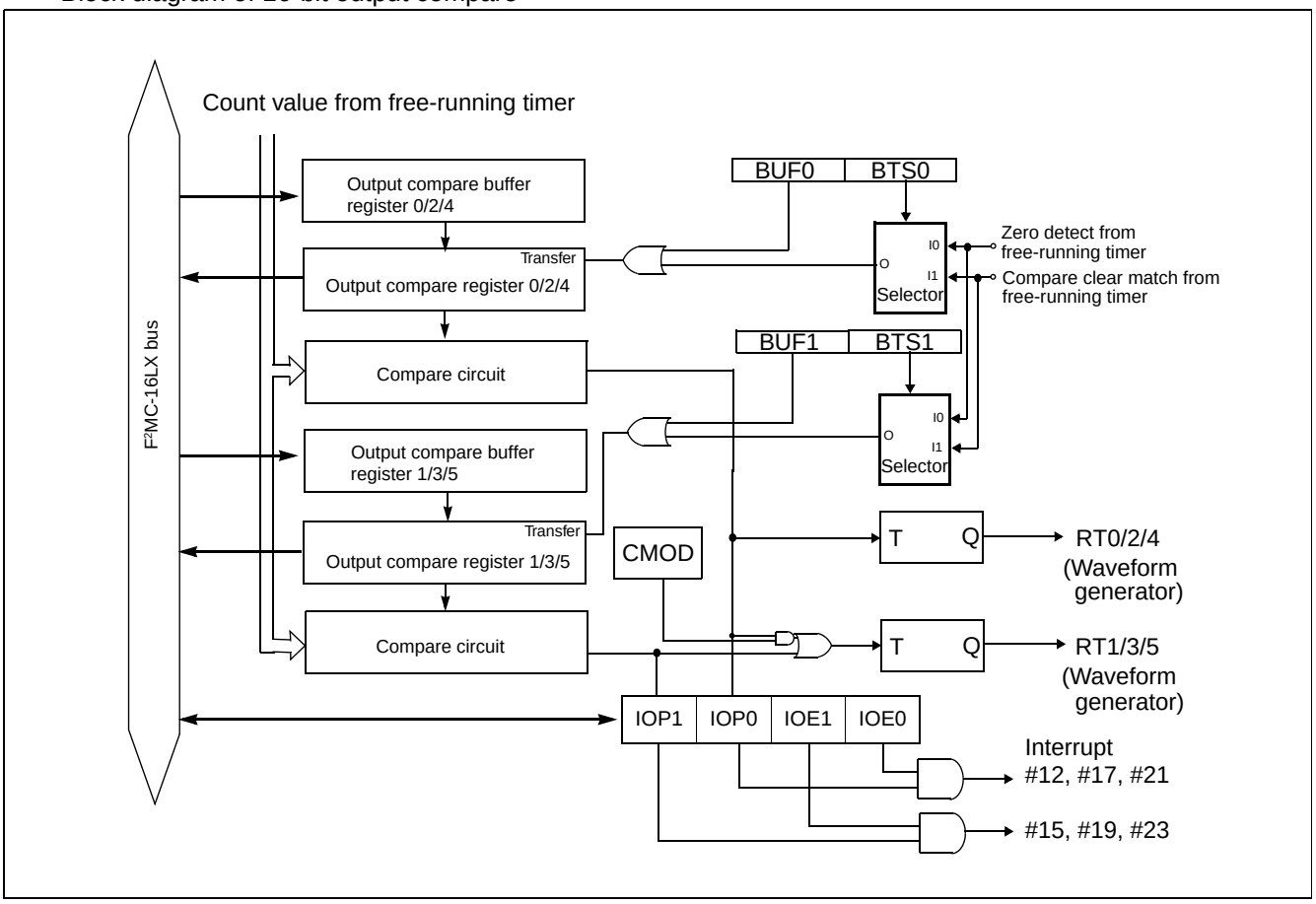
- Block diagram of Multi-functional timer



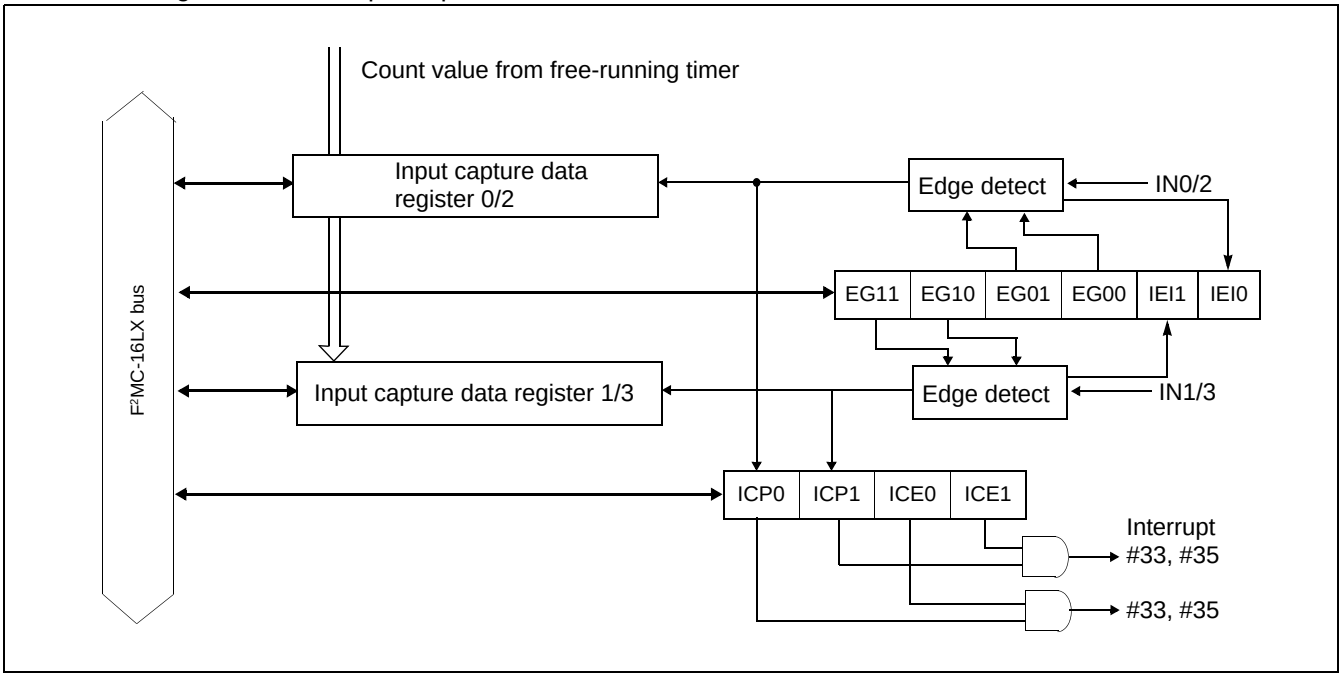
- Block diagram of 16-bit free-running timer



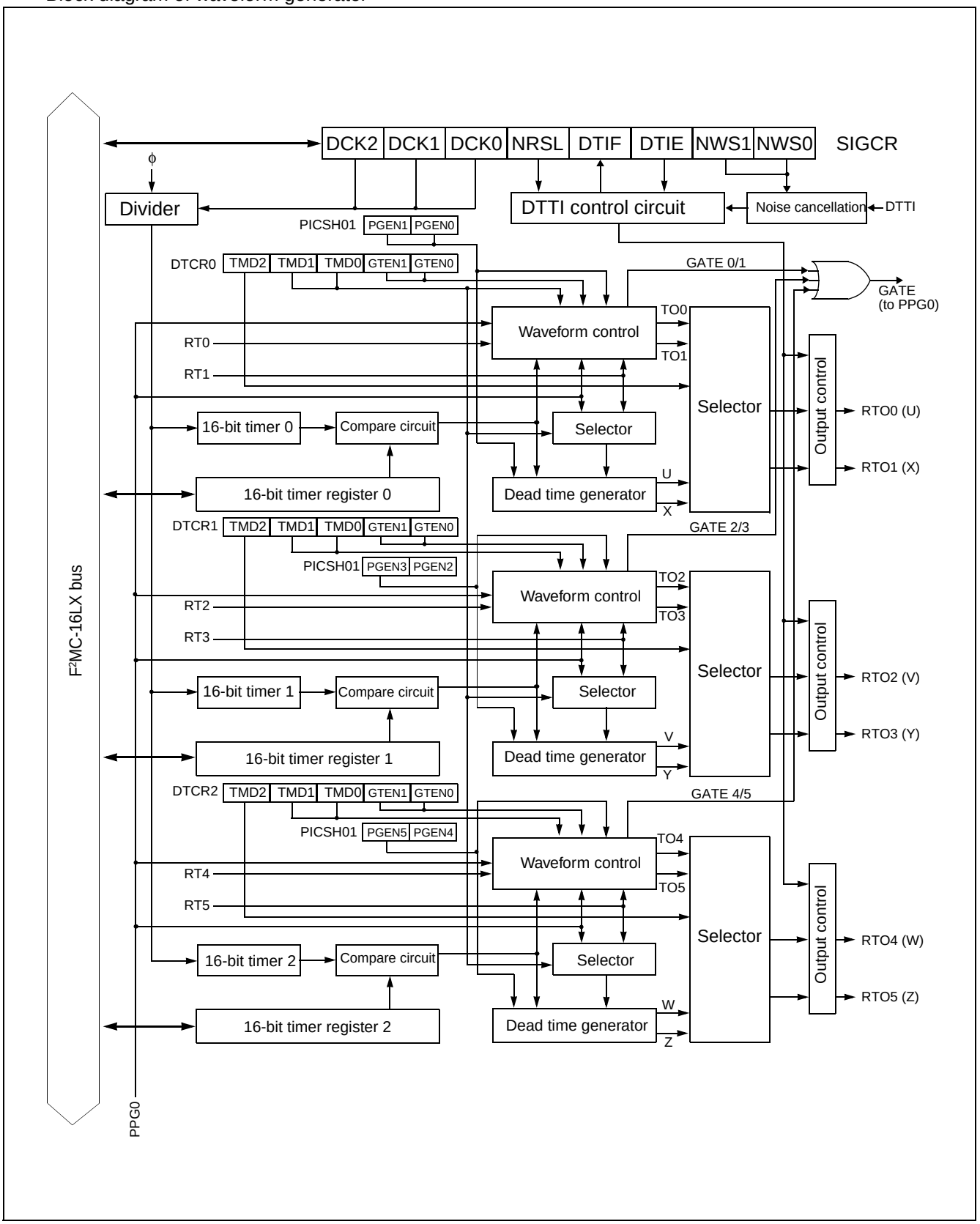
- Block diagram of 16-bit output compare



- Block diagram of 16-bit input capture



- Block diagram of waveform generator



8. PWC Timer (x 2)

The PWC (pulse width count) timer is a 16-bit multi-functional up counter with reload timer functions and input signal pulse width count functions.

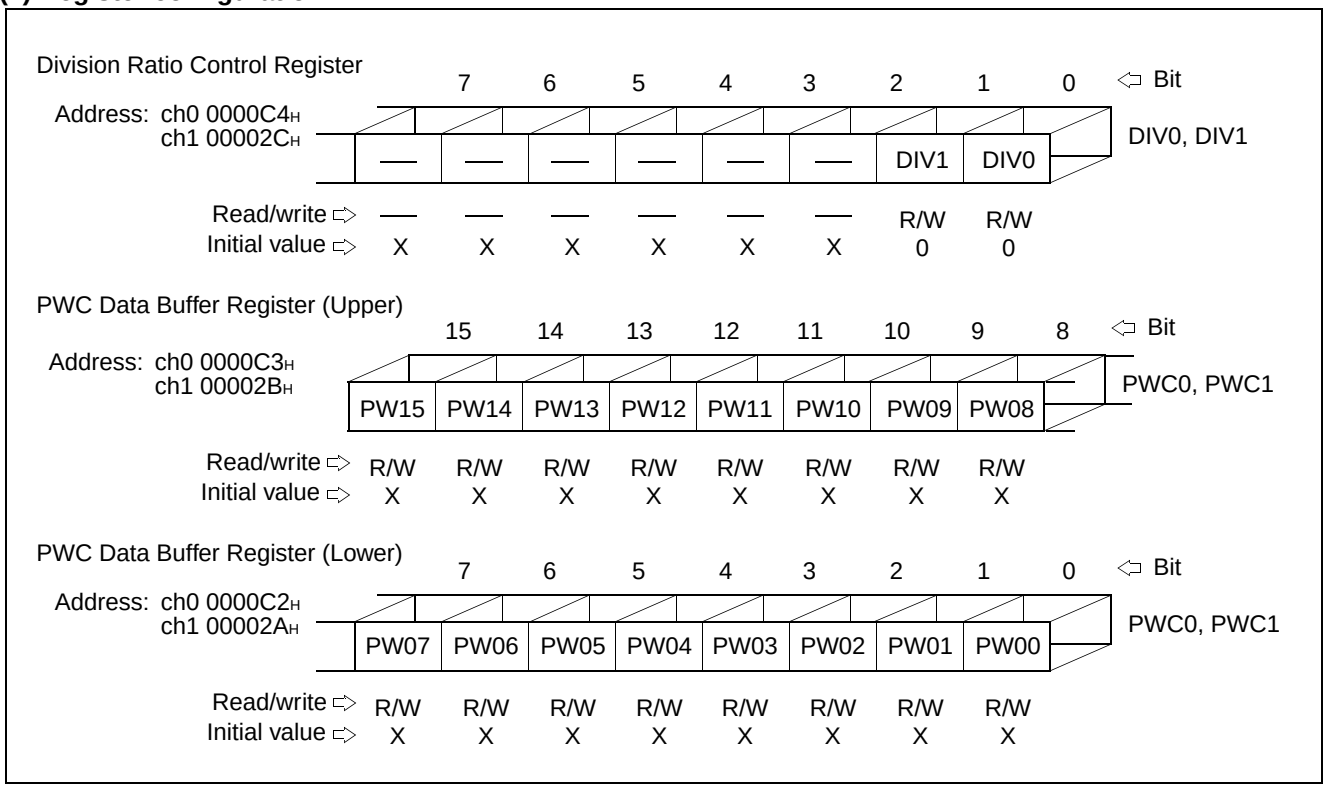
The PWC timer consists of a 16-bit counter, an input pulse divider, a division ratio control register, a count input pin, a pulse output pin, and a 16-bit control register.

The PWC timer has the following features:

- Interruption is generated when timer overflow or end of PWC measurement.
- EI^{2}OS is supported.
- Timer functions :
  - Generates an interrupt request at set time intervals.
  - Outputs pulse signals synchronized with the timer cycle.
  - Selects the counter clock from three internal clocks.
- Pulse-width count functions:
  - Counts the time between external pulse input events.
  - Selects the counter clock from three internal clocks.
  - Count mode:
    - H pulse width (rising edge to falling edge) / L pulse width (falling edge to rising edge)
    - Rising-edge cycle (rising edge to falling edge) / Falling-edge cycle (falling edge to rising edge)
    - Count between edges (rising or falling edge to falling or rising edge)

  Capable of counting cycles by dividing input pulses by 2^2, 2^4, 2^6, 2^8 using an 8-bit input divider.
  Generates an interrupt request upon the completion of count operation.
  Selects single or consecutive count operation.

(1) Register configuration



Note : Registers PWC0 to PWC1 are word access only.

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PWC Control Status Register (Upper)

Address: ch0 0000C1H
ch1 000029H

Bit	15	14	13	12	11	10	9	8	
	STRT	STOP	EDIR	EDIE	OVIR	OVIE	ERR	POUT	PWCSH0, PWCSH1
Read/write	R/W	R/W	R	R/W	R/W	R/W	R	R/W	
Initial value	0	0	0	0	0	0	0	0	

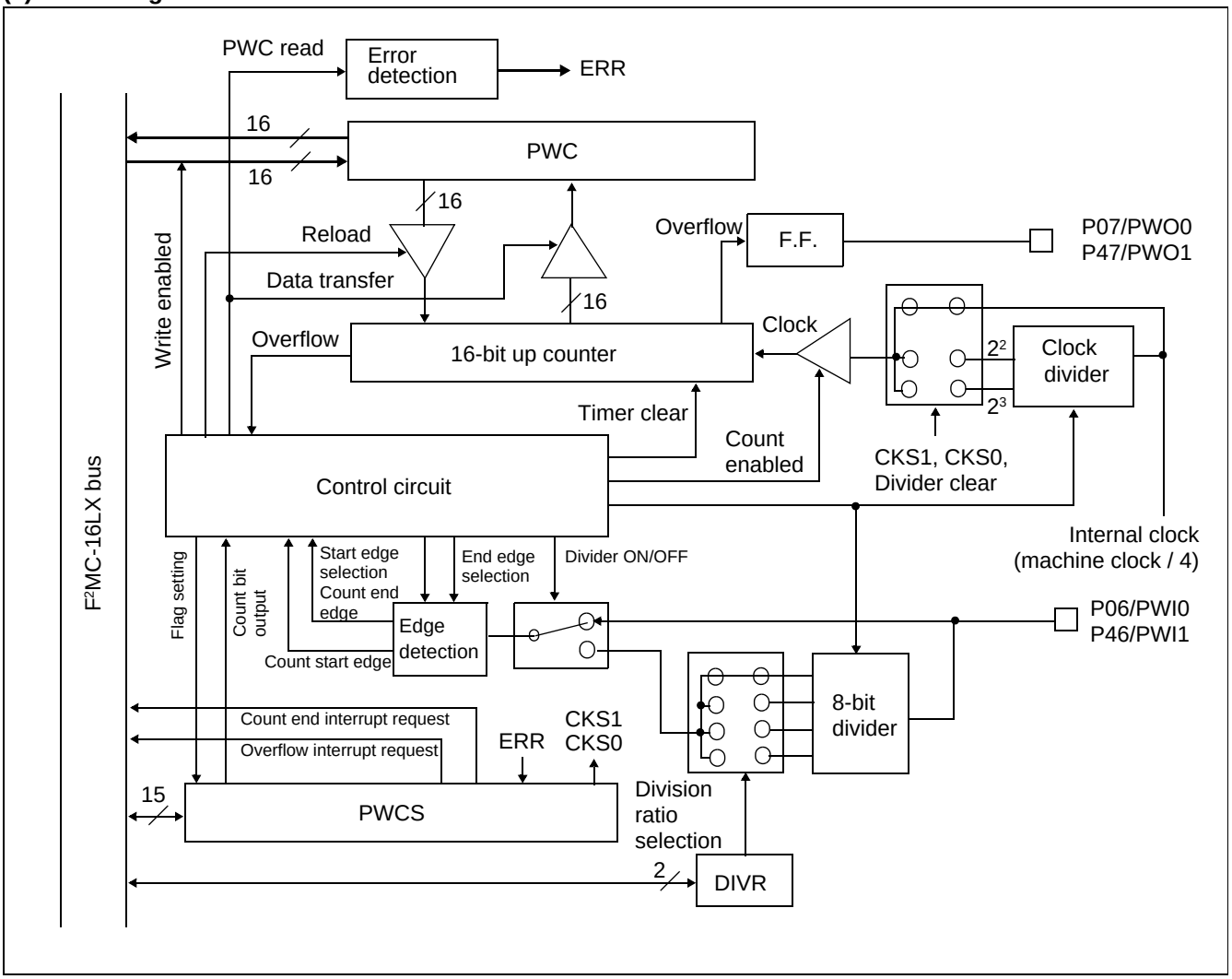
PWC Control Status Register (Lower)

Address: ch0 0000C0H
ch1 000028H

Bit	7	6	5	4	3	2	1	0	
	CKS1	CKS0	Reserved	Reserved	S/C	MOD2	MOD1	MOD0	PWCSL0, PWCSL1
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

Note : Registers PWC0 to PWC1 are word access only.

(2) Block diagram



9. UART (x 2)

The UART is a serial I/O port for asynchronous (start-stop) communication or clock-synchronous communication.
The UART has the following features :

- Full-duplex double buffering
- Capable of asynchronous (start-stop bit) and CLK-synchronous communications
- Support for the multiprocessor mode
- Various method of baud rate generation :
  - External clock input possible
  - Internal clock (a clock supplied from 16-bit reload timer can be used.)
  - Embedded dedicated baud rate generator

Operation	Baud rate
Asynchronous	31250/9615/4808/2404/1202 bps
CLK synchronous	2 M/1 M/500 K/250 K/125 K/62.5K bps

Note : Assuming internal machine clock frequencies of 6 MHz, 8 MHz, 10 MHz, 12 MHz, and 16 MHz.

- Error detection functions (parity, framing, overrun)
- NRZ (Non Return to Zero) signal format
- Interrupt request :
  - Receive interrupt (receive complete, receive error detection)
  - Transmit interrupt (transmission complete)
  - Transmit / receive conforms to extended intelligent I/O service (EI^2OS).

(1) Register configuration

Serial Status Register

Address: ch0 000023H
ch1 000027H

Bit	15	14	13	12	11	10	9	8
	PE	ORE	FRE	RDRF	TDRE	BDS	RIE	TIE
Read/write ⇨	R	R	R	R	R	R/W	R/W	R/W
Initial value ⇨	0	0	0	0	1	0	0	0

SSR0, SSR1

Serial Input Data Register / Serial Output Data Register

Address: ch0 000022H
ch1 000026H

Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value ⇨	X	X	X	X	X	X	X	X

SIDR0, SIDR1/
SODR0, SODR1

Serial Control Register

Address: ch0 000021H
ch1 000025H

Bit	15	14	13	12	11	10	9	8
	PEN	P	SBL	CL	A/D	REC	RXE	TXE
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	W	R/W	R/W
Initial value ⇨	0	0	0	0	0	1	0	0

SCR0, SCR1

Serial Mode Register

Address: ch0 000020H
ch1 000024H

Bit	7	6	5	4	3	2	1	0
	MOD1	MOD0	CS2	CS1	CS0	RST	SCKE	SOE
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value ⇨	0	0	0	0	0	0	0	0

SMR0, SMR1

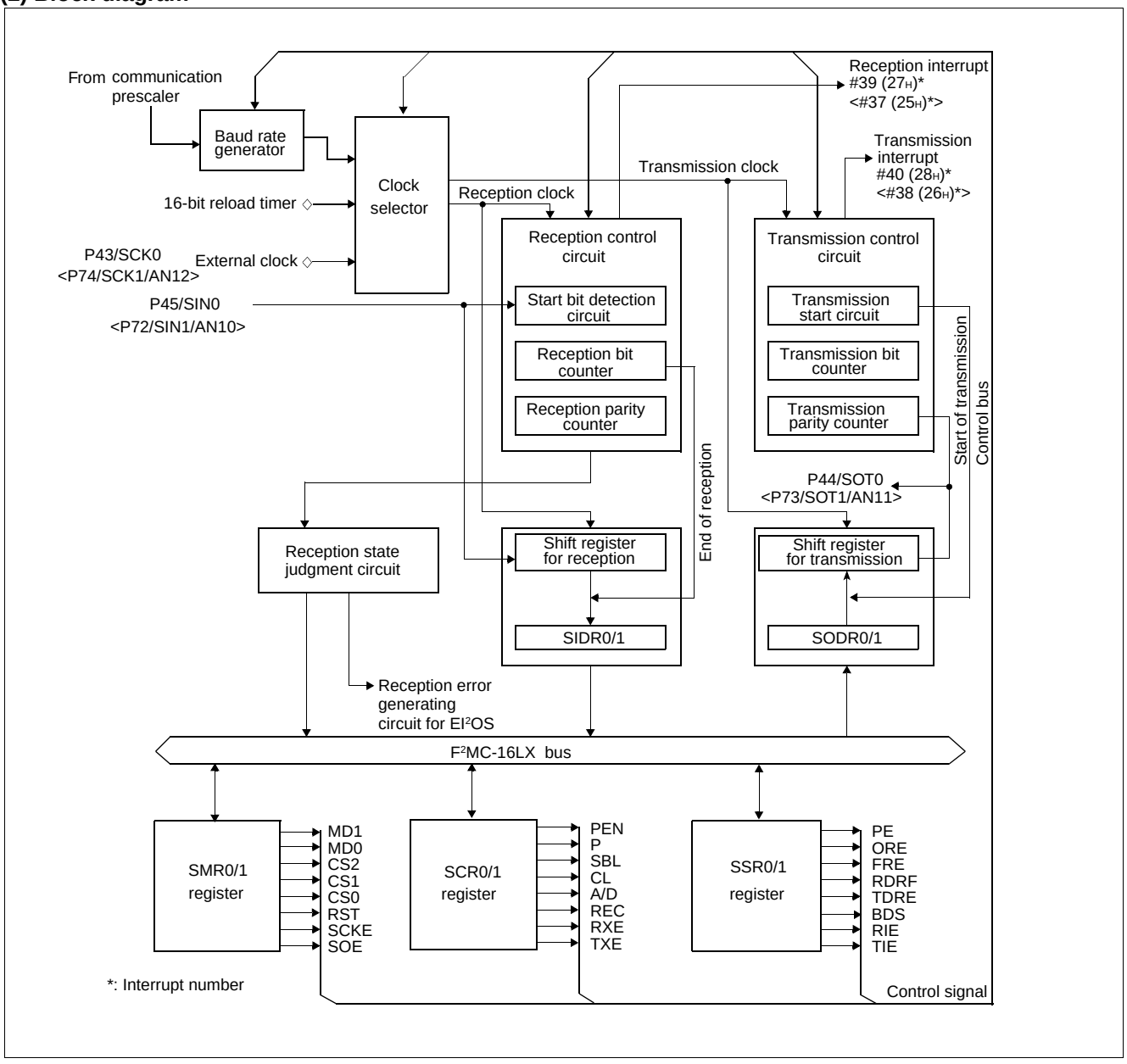
Clock Division Control Register

Address: ch0 000035H
ch1 000037H

Bit	15	14	13	12	11	10	9	8
	MD	ILS	—	—	—	DIV2	DIV1	DIV0
Read/write ⇨	R/W	R/W	—	—	—	R/W	R/W	R/W
Initial value ⇨	0	0	X	X	X	0	0	0

CDCR0,
CDCR1

(2) Block diagram



10. DTP/External Interrupts

The DTP/external interrupt circuit is activated by the signal supplied to a DTP/external interrupt pin. The CPU accepts the signal using the same procedure it uses for normal hardware interrupts and generates external interrupts or activates the extended intelligent I/O service (EI^2OS).

Features of DTP/External Interrupt :

- Total 8 external interrupt channels.
- Two request levels (“H” and “L”) are provided for the intelligent I/O service.
- Four request levels (rising edge, falling edge, “H” level and “L” level) are provided for external interrupt requests.

(1) Register configuration

DTP/Interrupt Source Register

	15	14	13	12	11	10	9	8	⇦ Bit
Address: 0000031H	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	EIRR
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

DTP/Interrupt Enable Register

	7	6	5	4	3	2	1	0	⇦ Bit
Address: 000030H	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	ENIR
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

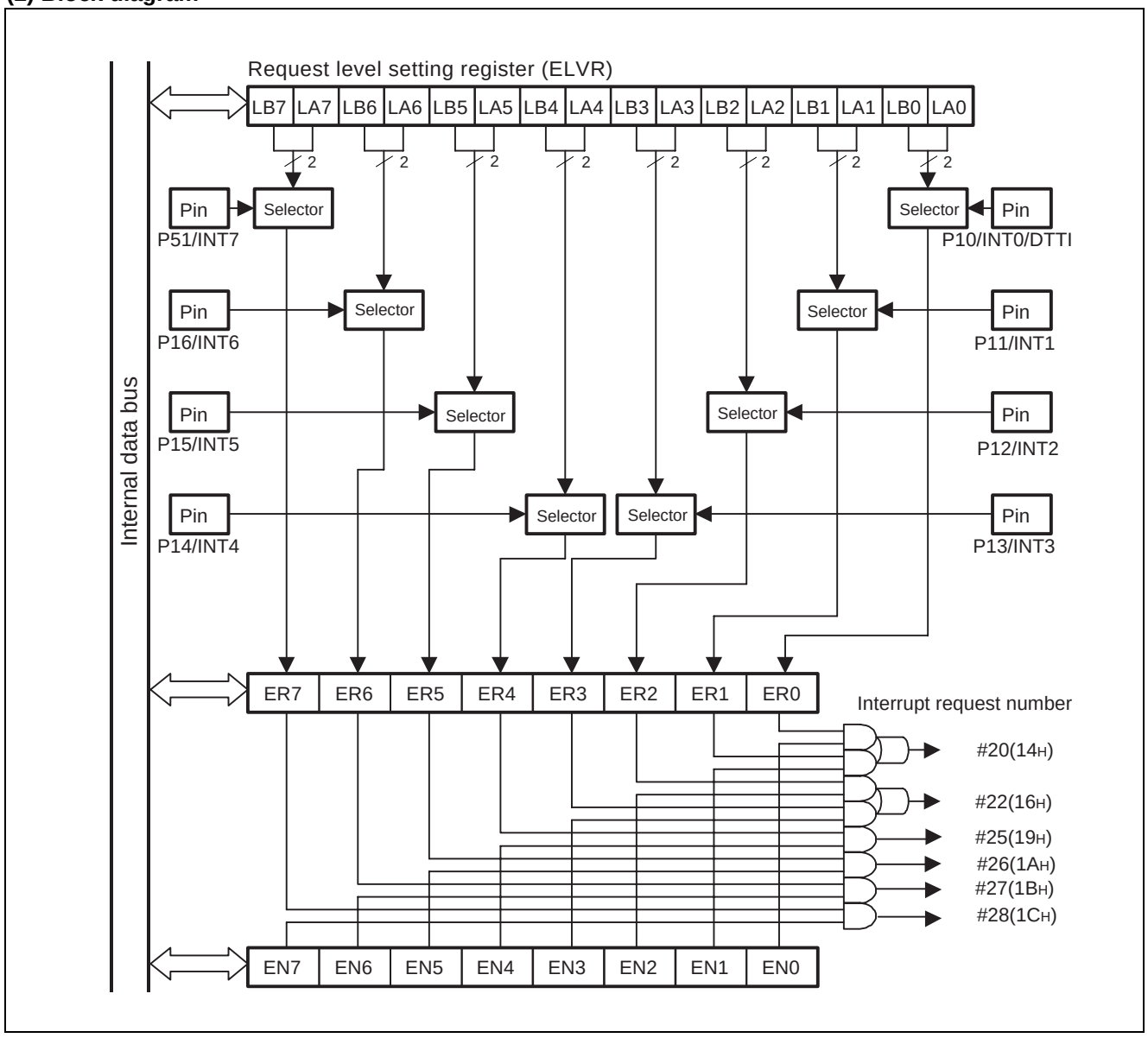
Request Level Setting Register (Upper)

	15	14	13	12	11	10	9	8	⇦ Bit
Address: 0000033H	LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4	ELVRH
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

Request Level Setting Register (Lower)

	7	6	5	4	3	2	1	0	⇦ Bit
Address: 000032H	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0	ELVRL
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

(2) Block diagram



11. Delayed Interrupt Generation Module

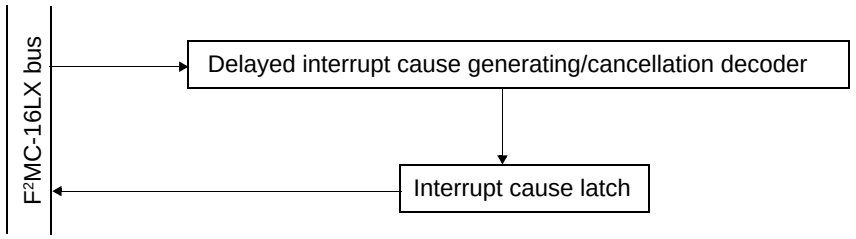
The delayed interrupt generation module is used to generate a task switching interrupt. Interrupt requests to the F²MC-16LX CPU can be generated and cleared by software using this module.

(1) Register configuration

Delay interrupt cause/clear register

	15	14	13	12	11	10	9	8	⇦ Bit
Address: 00009F$_H$	—	—	—	—	—	—	—	R0	DIRR
Read/write ⇨	—	—	—	—	—	—	—	R/W	
Initial value ⇨	X	X	X	X	X	X	X	0	

(2) Block diagram



12. A/D Converter

The A/D converter converts the analog voltage input (input voltage) to an analog input pin to a digital value. It has the following features :

- The minimum conversion time is 3 µs (for a machine clock of 24 MHz; including sampling time).
- The converter uses the RC-type successive approximation conversion method with a sample and hold circuit.
- A resolution of 10 bits or 8 bits can be set.
- Up to 16 channels for analog input pins can be selected by a program.
- Various conversion mode :
  - Single conversion mode : Selectively convert one channel.
  - Scan conversion mode : Continuously convert multiple channels. Maximum of 16 selectable channels.
  - Continuous conversion mode : Repeatedly convert specified channels.
  - Stop conversion mode : Convert one channel then halt until the next activation (enables synchronization of the conversion start timing).
- At the end of A/D conversion, an interrupt request can be generated and EI²OS can be activated.
- In the interrupt-enabled state, the conversion data protection function prevents any part of the data from being lost through continuous conversion.
- The conversion can be activated by software, 16-bit reload timer 1 (rising edge) and 16-bit free-running timer zero detection edge.

(1) Register configuration

A/D Control Status Register (upper)

	15	14	13	12	11	10	9	8	⇦ Bit
Address: 00000C7H	BUSY	INT	INTE	PAUS	STS1	STS0	STRT	—	ADCS1
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	W	—	
Initial value ⇨	0	0	0	0	0	0	0	X	

A/D Control Status Register (lower)

	7	6	5	4	3	2	1	0	⇦ Bit
Address: 0000C6H	MD1	MD0	S10	—	—	—	—	Reserved	ADCS0
Read/write ⇨	R/W	R/W	R/W	—	—	—	—	—	
Initial value ⇨	0	0	0	X	X	X	X	0	

A/D Data Register (upper)

	15	14	13	12	11	10	9	8	⇦ Bit
Address: 00000C9H	—	—	—	—	—	—	D9	D8	ADCR1
Read/write ⇨	—	—	—	—	—	—	R	R	
Initial value ⇨	X	X	X	X	X	X	X	X	

A/D Data Register (lower)

	7	6	5	4	3	2	1	0	⇦ Bit
Address: 0000C8H	D7	D6	D5	D4	D3	D2	D1	D0	ADCR0
Read/write ⇨	R	R	R	R	R	R	R	R	
Initial value ⇨	X	X	X	X	X	X	X	X	

(Continued)

(Continued)

A/D Setting Register (upper)

	15	14	13	12	11	10	9	8	⇦ Bit
Address: 00000CB$_H$	ST2	ST1	ST0	CT2	CT1	CT0	Reserved	ANS3	ADSR1
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

A/D Setting Register (lower)

	7	6	5	4	3	2	1	0	⇦ Bit
Address: 0000CA$_H$	ANS2	ANS1	ANS0	Reserved	ANE3	ANE2	ANE1	ANE0	ADSR0
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	0	0	0	0	0	0	0	0	

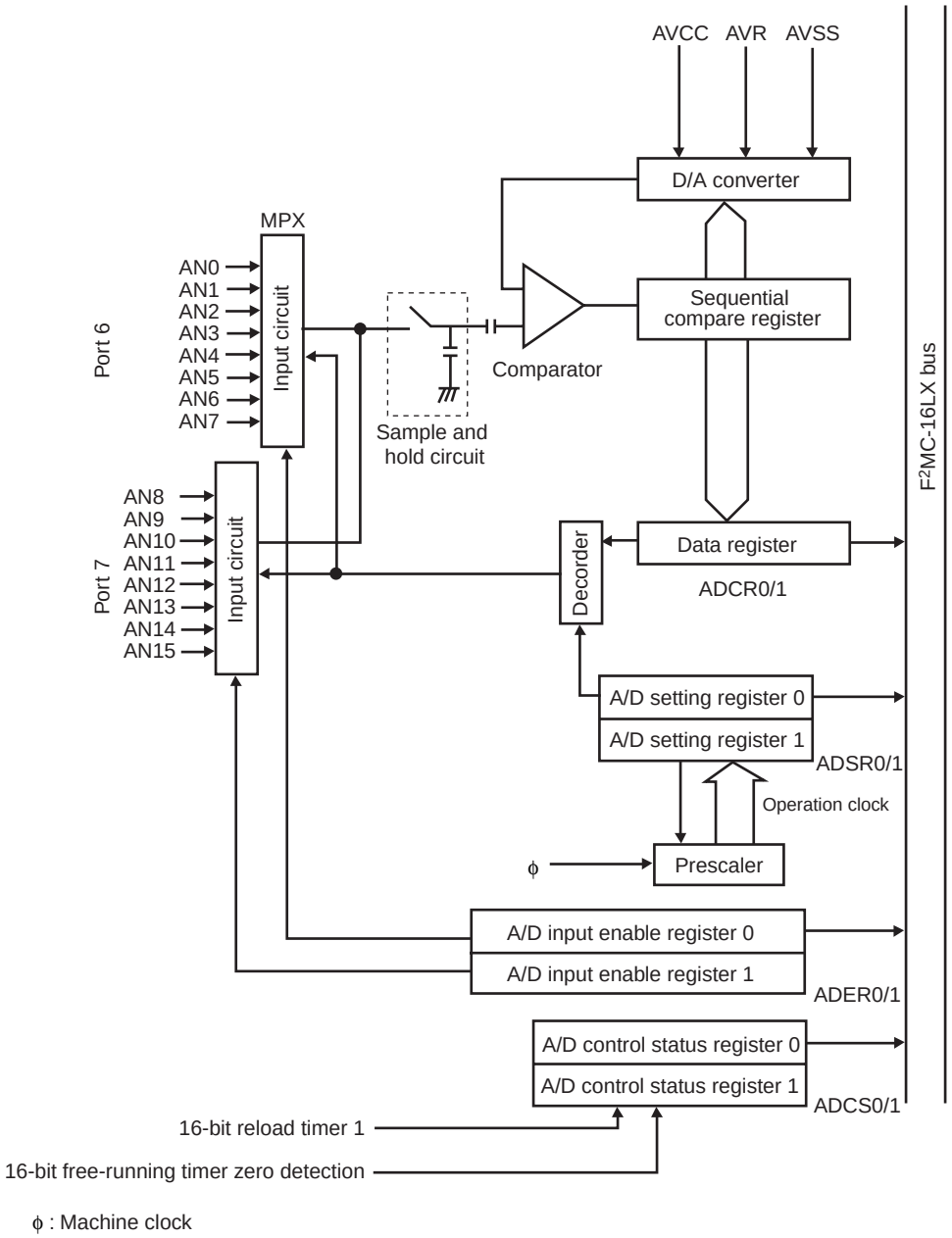
A/D Input Enable Register

	15	14	13	12	11	10	9	8	⇦ Bit
Address: 00000C5$_H$	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0	ADER0
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	1	1	1	1	1	1	1	1	

A/D Input Enable Register

	7	6	5	4	3	2	1	0	⇦ Bit
Address: 0000D0$_H$	ADE15	ADE14	ADE13	ADE12	ADE11	ADE10	ADE9	ADE8	ADER1
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	1	1	1	1	1	1	1	1	

(2) Block diagram



13. D/A Converter

The D/A converter is used to generate an analog output from an 8-bit digital input. By setting the enable bit in the D/A control register (DACR) to 1, it will enable the corresponding D/A output channel. Hence, setting this bit to 0 will disable that channel.

If D/A output is disabled, the analog switch inserted to the output of each D/A converter channel in series is turned off. In the D/A converter, the bit is cleared to 0 and the direct-current path is shut off. The above is also true in the stop mode.

The output voltage of the D/A converter ranges from 0 V to 255/256 x AV_{CC}. To change the output voltage range, adjust the AV_{CC} voltage externally.

The D/A converter output does not have the internal buffer amplifier. The analog switch (= 100 Ω) is inserted to the output in series. To apply load to the output externally, estimate a sufficient stabilization time.

Table below lists the theoretical values of output voltage of the D/A converter.

Value written to DA07 to DA00 and DA17 to DA10	Theoretical value of output voltage
00_H	$0/256 \times AV_{CC}$ (= 0 V)
01_H	$1/256 \times AV_{CC}$
02_H	$2/256 \times AV_{CC}$
:	:
FD_H	$253/256 \times AV_{CC}$
FE_H	$254/256 \times AV_{CC}$
FF_H	$255/256 \times AV_{CC}$

(1) Register configuration

D/A data register 1

Bit	15	14	13	12	11	10	9	8	
Address:0000CD$_H$	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10	DAT1
Read/write →	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value →	X	X	X	X	X	X	X	X	

D/A data register 0

Bit	7	6	5	4	3	2	1	0	
Address:0000CC$_H$	DA07	DA06	DA05	DA04	DA03	DA02	DA01	DA00	DAT0
Read/write →	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value →	X	X	X	X	X	X	X	X	

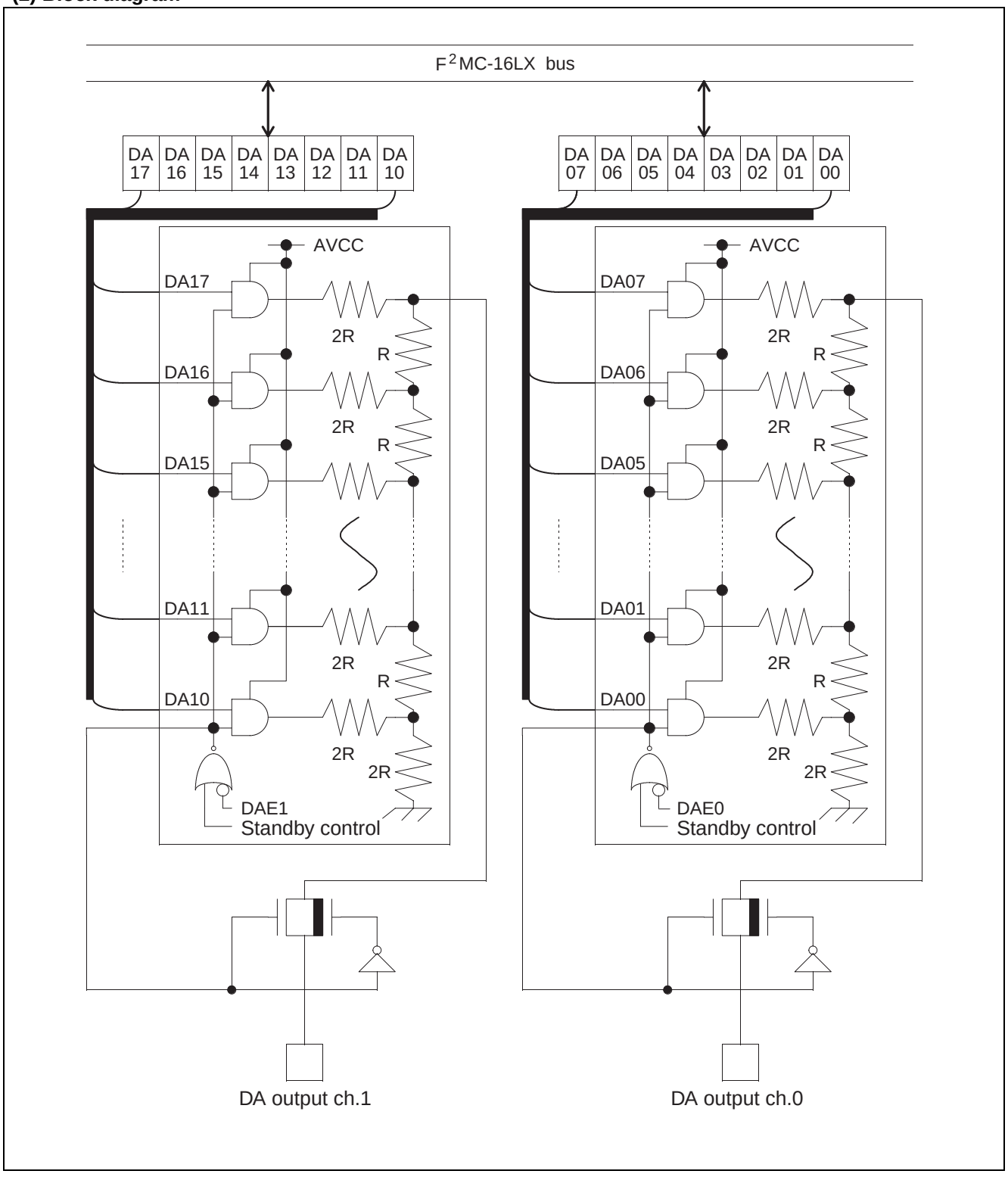
D/A control register 1

Bit	15	14	13	12	11	10	9	8	
Address:0000CF$_H$	-	-	-	-	-	-	-	DAE1	DACR1
Read/write →	-	-	-	-	-	-	-	R/W	
Initial value →	X	X	X	X	X	X	X	0	

D/A control register 0

Bit	7	6	5	4	3	2	1	0	
Address:0000CE$_H$	-	-	-	-	-	-	-	DAE0	DACR0
Read/write →	-	-	-	-	-	-	-	R/W	
Initial value →	X	X	X	X	X	X	X	0	

(2) Block diagram



14. ROM Correction Function

When the corresponding address matches the value set in the address detection register, the instruction code to be loaded into the CPU is forced to be replaced with the INT9 instruction code (01_H). When executing a set instruction, the CPU executes the INT9 instruction. The address detection function is implemented by processing using the INT9 instruction routine.

The device contains two address detection registers, each provided with a compare enable bit. When the value set in the address detection register matches an address and the interrupt enable bit is “1”, the instruction code to be loaded into the CPU is forced to be replaced with the INT9 instruction code.

(1) Register configuration

Program Address Detection Control Status Register

Bit	7	6	5	4	3	2	1	0
Address: 00009E$_H$	—	—	—	—	AD1E	AD1D	AD0E	AD0D
Read/write	—	—	—	—	R/W	R/W	R/W	R/W
Initial value	X	X	X	X	0	0	0	0

PADCSR

Program Address Detection Register 0 (Upper Byte)

Bit	7	6	5	4	3	2	1	0
Address: 001FF2$_H$								
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	X	X	X	X	X	X	X	X

PADRH0

Program Address Detection Register 0 (Middle Byte)

Bit	15	14	13	12	11	10	9	8
Address: 001FF1$_H$								
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	X	X	X	X	X	X	X	X

PADRM0

Program Address Detection Register 0 (Lower Byte)

Bit	7	6	5	4	3	2	1	0
Address: 001FF0$_H$								
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	X	X	X	X	X	X	X	X

PADRL0

Program Address Detection Register 1 (Upper Byte)

Bit	15	14	13	12	11	10	9	8
Address: 001FF5$_H$								
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	X	X	X	X	X	X	X	X

PADRH1

(Continued)

(Continued)

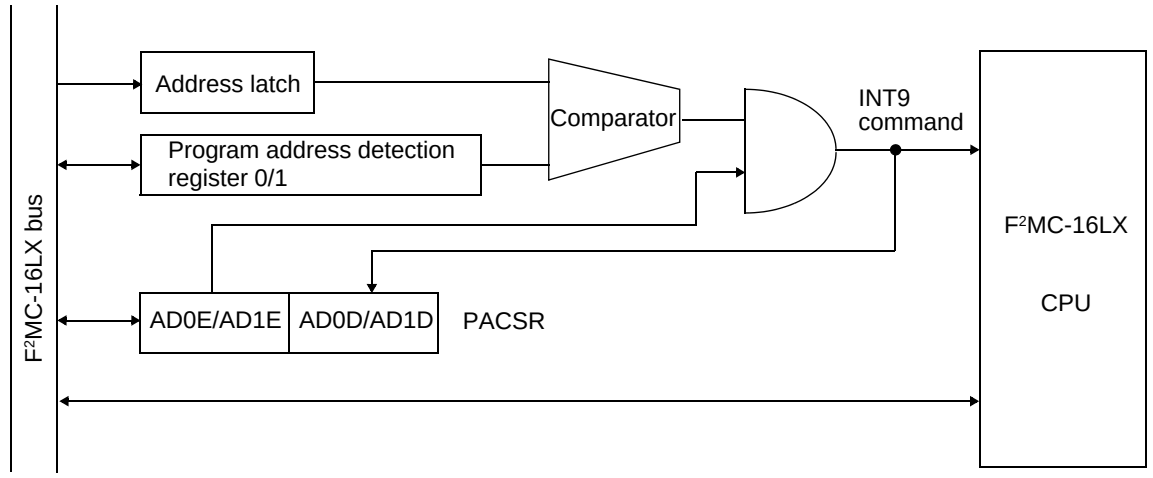
Program Address Detection Register 1 (Middle Byte)

	7	6	5	4	3	2	1	0	⇦ Bit
Address: 001FF4H									PADRM1
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

Program Address Detection Register 1 (Lower Byte)

	15	14	13	12	11	10	9	8	⇦ Bit
Address: 001FF3H									PADRL1
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	

(2) Block diagram



15. ROM Mirroring Function Selection Module

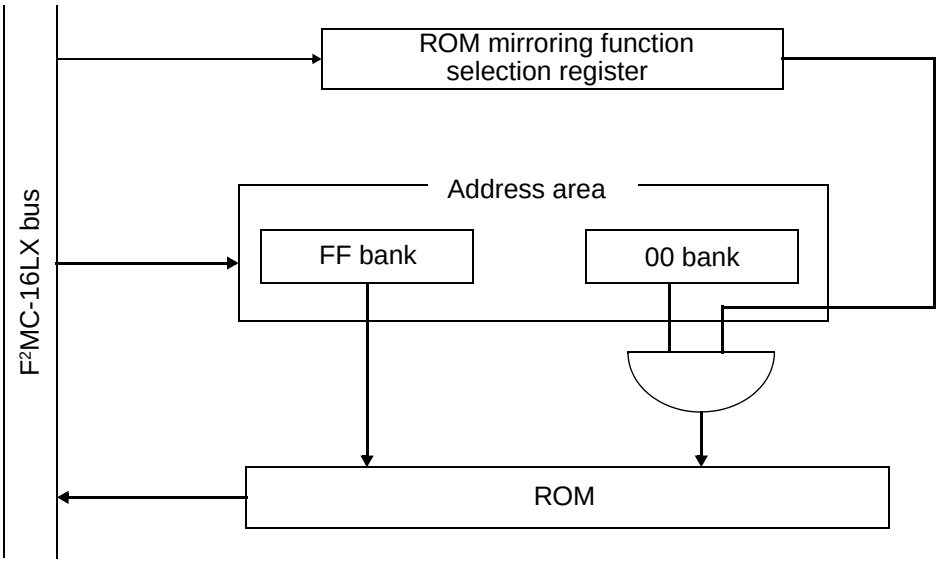
The ROM mirror function selection module sets the data in ROM assigned to FF bank so that the data is read by access to 00 bank.

(1) Register configuration

ROM Mirror Function Selection Register

	15	14	13	12	11	10	9	8	⇦ Bit
Address : 00006F$_H$	—	—	—	—	—	—	—	M1	ROMM
Read/write ⇨	—	—	—	—	—	—	—	R/W	
Initial value ⇨	X	X	X	X	X	X	X	1	

(2) Block diagram



16. 512/1024 Kbit Flash Memory

The 512K bits flash memory is allocated in the FF_H banks on the CPU memory map.

The 1024K bits flash memory is allocated in the FE_H and FF_H banks on the CPU memory map.

Like MaskROM, flash memory is read-accessible and program-accessible to the CPU using the flash memory interface circuit. The flash memory can be programmed/erased by the instruction from the CPU via the flash memory interface circuit. The flash memory can therefore be reprogrammed (updated) while still on the circuit board under integrated CPU control, allowing program code and data to be improved efficiently.
Note that sector operations such as “enable sector protect” cannot be used.

Features of 512/1024K bits flash memory

- 64K x 8 bits/32K x 16 bits (32K + 8K x 2 + 16K) sector configuration for 512K bits flash memory
- 128K x 8 bits/64K x 16 bits (64K + 32K + 8K x 2 + 16K) sector configuration for 1024K bits flash memory
- Automatic program algorithm (same as the Embedded Algorithm* : MBM29F400TA)
- Installation of the deletion temporary stop/delete restart function
- Write/delete completion detected by the data polling or toggle bit
- Write/delete completion detected by the CPU interrupt
- Compatibility with the JEDEC standard-type command
- Each sector deletion can be executed (sectors can be freely combined)
- Flash security function
- Number of write/delete operations are guaranteed 10,000 times.

* : Embedded Algorithm is a trademark of Advanced Micro Devices, Inc.

(1) Register configuration

Flash Memory Control Status Register

	7	6	5	4	3	2	1	0	⇦ Bit number
Address: 0000AE$_H$	INTE	RDYINT	WE	RDY	Reserved	Reserved	Reserved	Reserved	FMCS
Read/write ⇨	R/W	R/W	R/W	R	—	—	—	—	
Initial value ⇨	0	0	0	X	0	0	0	0	

(2) Sector configuration of flash memory

The flash memory has the sector configuration illustrated below. The addresses in the illustration are the upper and lower addresses of each sector.

When 512K bits flash memory is accessed from the CPU, SA0 to SA3 are allocated in the FF bank.

Flash memory	CPU address	*Writer address
SA3 (16K bytes)	$FFFFFF_H$	$7FFFF_H$
	$FFC000_H$	$7C000_H$
SA2 (8K bytes)	$FFBFFF_H$	$7BFFF_H$
	$FFA000_H$	$7A000_H$
SA1 (8K bytes)	$FF9FFF_H$	$79FFF_H$
	$FF8000_H$	78000_H
SA0 (32K bytes)	$FF7FFF_H$	$77FFF_H$
	$FF0000_H$	70000_H

When 1024K bits flash memory is accessed from the CPU, SA0 to SA4 are allocated in the FE and FF bank.

Flash memory	CPU address	*Writer address
SA4 (16K bytes)	$FFFFFF_H$	$7FFFF_H$
	$FFC000_H$	$7C000_H$
SA3 (8K bytes)	$FFBFFF_H$	$7BFFF_H$
	$FFA000_H$	$7A000_H$
SA2 (8K bytes)	$FF9FFF_H$	$79FFF_H$
	$FF8000_H$	78000_H
SA1 (32K bytes)	$FF7FFF_H$	$77FFF_H$
	$FF0000_H$	70000_H
SA0 (64K bytes)	$FE7FFF_H$	$6FFFF_H$
	$FE0000_H$	60000_H

* : The writer address is the address to use instead of the CPU address when writing data from a parallel flash memory writer. Use the writer address when programming or erasing using a general-purpose parallel writer.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$ *2
	AVR	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVR$, $AVR \geq AV_{SS}$
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*5
Total maximum clamp current	$\Sigma \mid I_{CLAMP} \mid$	—	20	mA	*5
“L” level maximum output current	I_{OL}	—	15	mA	*4
“L” level average output current	I_{OLAV1}	—	4	mA	Except for P00 to P07, P82 to P87
	I_{OLAV2}	—	12	mA	P00 to P07, P82 to P87
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	
“H” level maximum output current	I_{OH}	—	–15	mA	*4
“H” level average output current	I_{OHAV}	—	–4	mA	
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–50	mA	
Power consumption	P_D	—	430	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1 : This parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

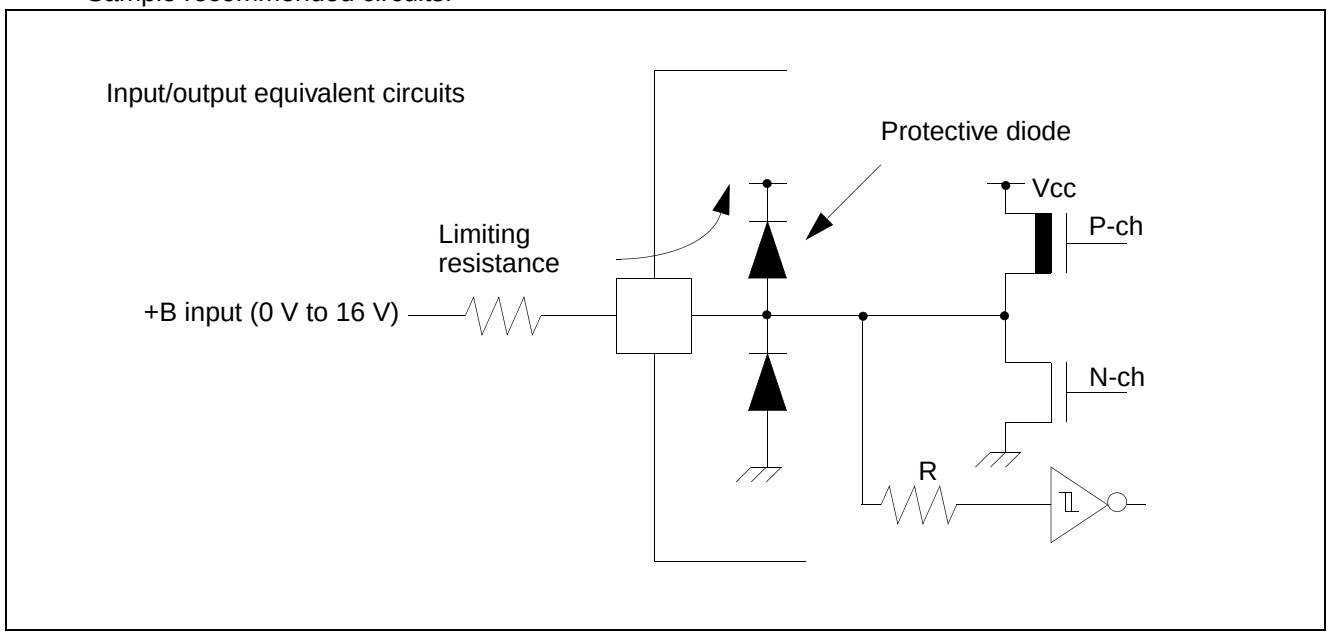
*2 : AV_{CC} must never exceed V_{CC} when the power is turned on.

*3 : V_I and V_O must never exceed V_{CC} + 0.3 V. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4 : The maximum output current is a peak value for a corresponding pin.

*5 :
- Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50, P51, P80 to P87.
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the Vcc pin, and this may affect other devices.

- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins (LCD drive pins and comparator input pins, etc.) other than the A/D input pins cannot accept +B input.
- Sample recommended circuits:



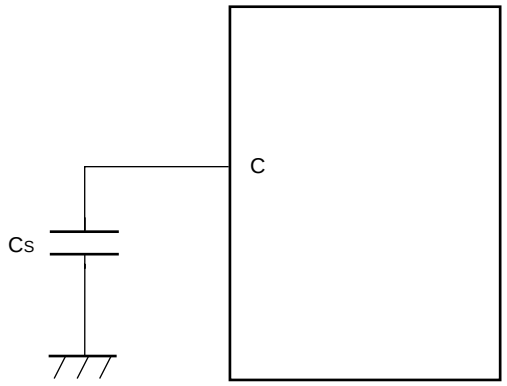
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} AV_{CC}	4.5	5.5	V	Normal operation
		4.0	5.5	V	Normal operation when D/A converter is not used
		3.5	5.5	V	Normal operation when A/D converter and D/A converter are not used
		3.0	5.5	V	Maintains state in stop operation
Smoothing capacitor	C_S	0.1	1.0	µF	Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor to be connected to the V_{CC} pin must have a capacitance value higher than C_S.
Operating temperature	T_A	–40	+85	°C	

• C pin connection circuit



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH}	All output pins	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL1}	All pins except P00 to P07 P82 to P87	V_{CC} = 4.5 V, I_{OL1} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P00 to P07 P82 to P87	V_{CC} = 4.5 V, I_{OL2} = 12.0 mA	—	—	0.4	V	
"H" level input voltage	V_{IH}	P30 to P37 P60 to P67	V_{CC} = 4.5 V to 5.5 V	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS input pin
	V_{IHS}	P00 to P07 P10 to P17 P20 to P27 P40 to P47 *1 P50 to P51 P70 to P77 *1 P80 to P87 $\overline{RST}$		0.8 V_{CC}	—	V_{CC} + 0.3	V	CMOS hysteresis input pin
	V_{IHM}	MD0 to MD2		V_{CC} – 0.3	—	V_{CC} + 0.3	V	MD input pin
"L" level input voltage	V_{IL}	P30 to P37 P60 to P67		V_{SS} – 0.3	—	0.3 V_{CC}	V	CMOS input pin
	V_{ILS}	P00 to P07 P10 to P17 P20 to P27 P40 to P47 *1 P50 to P51 P70 to P77 *1 P80 to P87 $\overline{RST}$		V_{SS} – 0.3	—	0.2 V_{CC}	V	CMOS hysteresis input pin
	V_{ILM}	MD0 to MD2		V_{SS} – 0.3	—	V_{SS} + 0.3	V	MD input pin
Input leakage current	I_{IL}	All input pins	V_{CC} = 5.5 V, $V_{SS} < V_I < V_{CC}$	–5	—	5	µA	
Pull-up resistance	R_{UP}	P00 to P07 P10 to P17 P20 to P27 P30 to P37 $\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	Not available in MB90F822/ MB90F823

(Continued)

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal frequency: 24 MHz, At normal operation	—	35	50	mA	MB90822
				—	45	60	mA	MB90F822/F823
			V_{CC} = 5.0 V, Internal frequency: 24 MHz, At writing in flash memory	—	50	65	mA	MB90822
				—	60	75	mA	MB90F822/F823
			V_{CC} = 5.0 V, Internal frequency: 24 MHz, At erasing memory	—	55	70	mA	MB90822
				—	65	80	mA	MB90F822/F823
	I_{CCS}		V_{CC} = 5.0 V, Internal frequency: 24 MHz, At sleep mode	—	15	25	mA	MB90822
				—			mA	MB90F822/F823
	I_{CTS}		V_{CC} = 5.0 V, Internal frequency: 2 MHz, At main timer mode	—	0.3	0.8	mA	MB90822
				—			mA	MB90F822/F823
	I_{CCT}		V_{CC} = 5.0 V, Internal frequency: 8 MHz, At timer mode, T_A = +25 °C	—	3	7	mA	MB90822
				—			µA	MB90F822/F823
	I_{CCH}		In stop mode, T_A = +25 °C	—	5	20	mA	MB90822
				—			µA	MB90F822/F823
Input capacitance	C_{IN}	Except AV_{CC}, AV_{SS}, AVR, C, V_{CC} and V_{SS}	—	—	5	15	pF	

*1 : UART0, UART1 data input pins P45/SIN0, P72/SIN1 can be selected as CMOS input by user program.

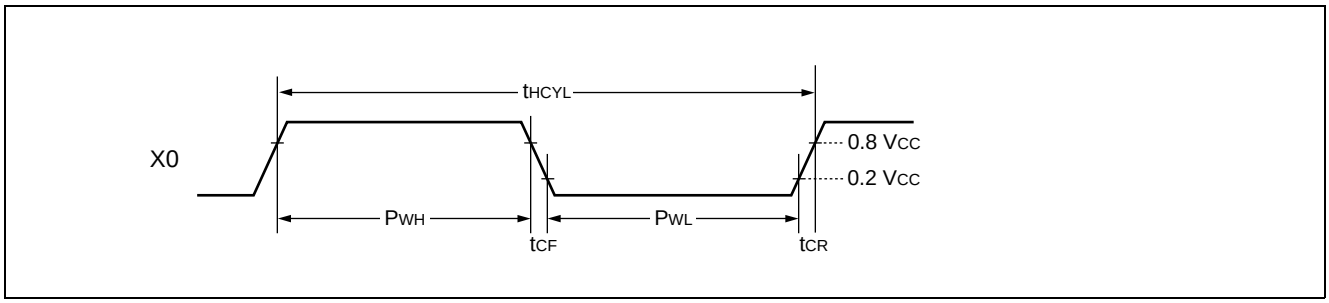
*2 : Current values are tentative. They may be subject to change for enhanced characteristics without previous notice. The power supply current is measured with an external clock.

4. AC Characteristics

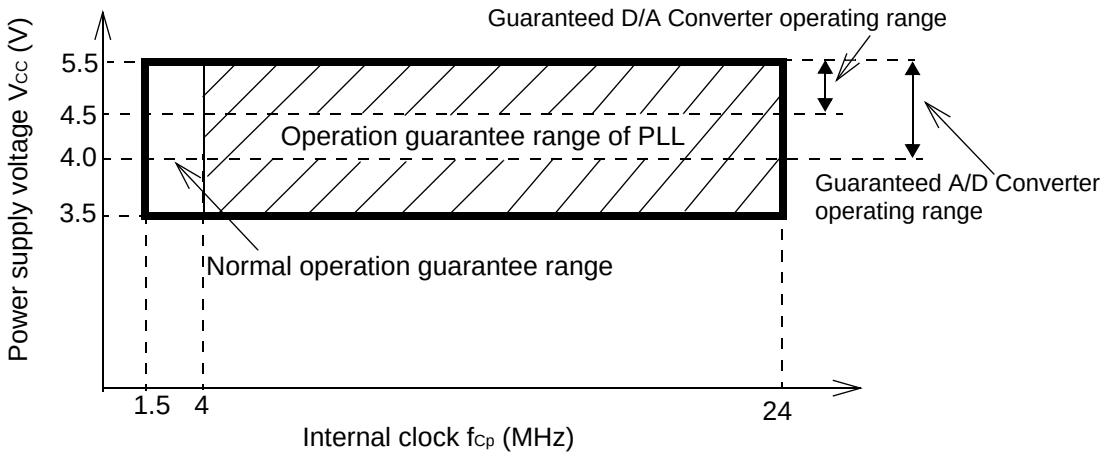
(1) Clock Timings

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

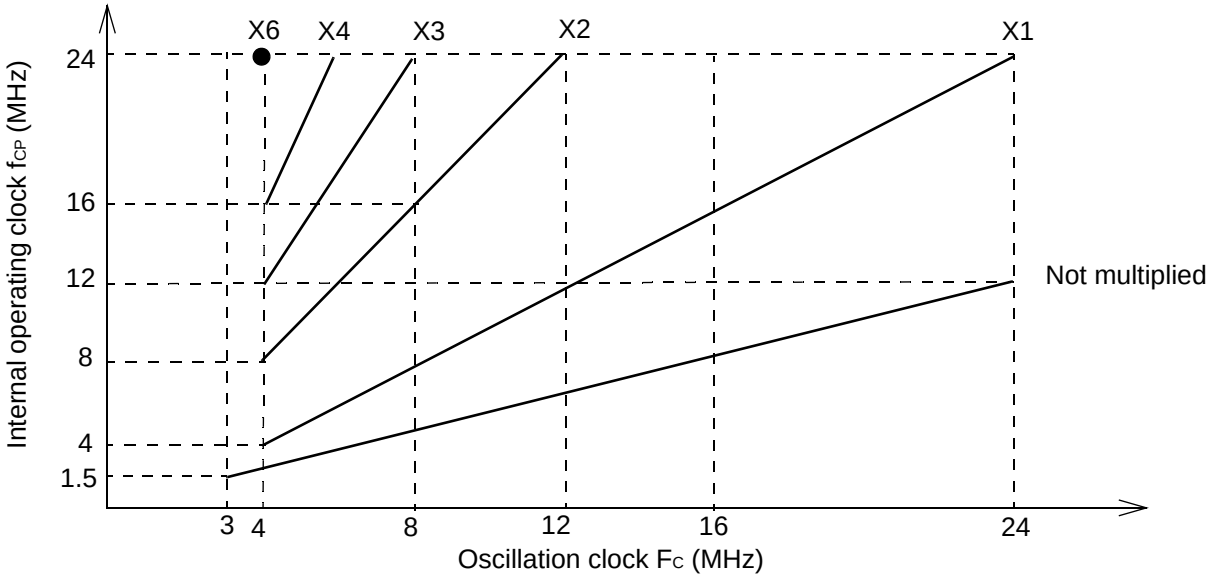
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_C	X0, X1	3	—	16	MHz	Crystal oscillator
			3	—	24	MHz	External clock
Clock cycle time	t_{HCYL}	X0, X1	62.5	—	333	ns	Crystal oscillator
			41.67	—	333	ns	External clock
Input clock pulse width	P_{WH} P_{WL}	X0	10	—	—	ns	Recommend duty ratio of 30% to 70%
Input clock rise/fall time	t_{CR} t_{CF}	X0	—	—	5	ns	External clock operation
Internal operating clock frequency	f_{CP}	—	1.5	—	24	MHz	
Internal operating clock cycle time	t_{CP}	—	41.67	—	666	ns	



Relationship between internal operating clock frequency and power supply voltage



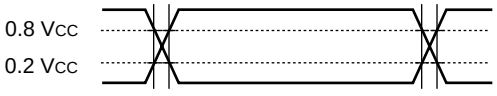
Relationship between oscillating frequency and internal operating clock frequency



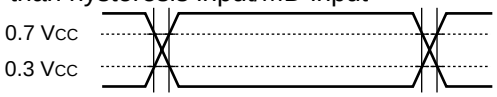
The AC ratings are measured for the following measurement reference voltages

• Input signal waveform

Hysteresis input pin

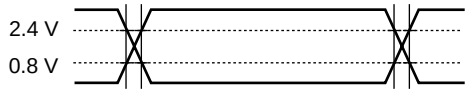


Pins other than hysteresis input/MD input



• Output signal waveform

Output pin



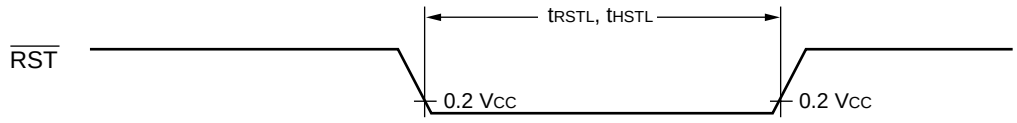
(2) Reset Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

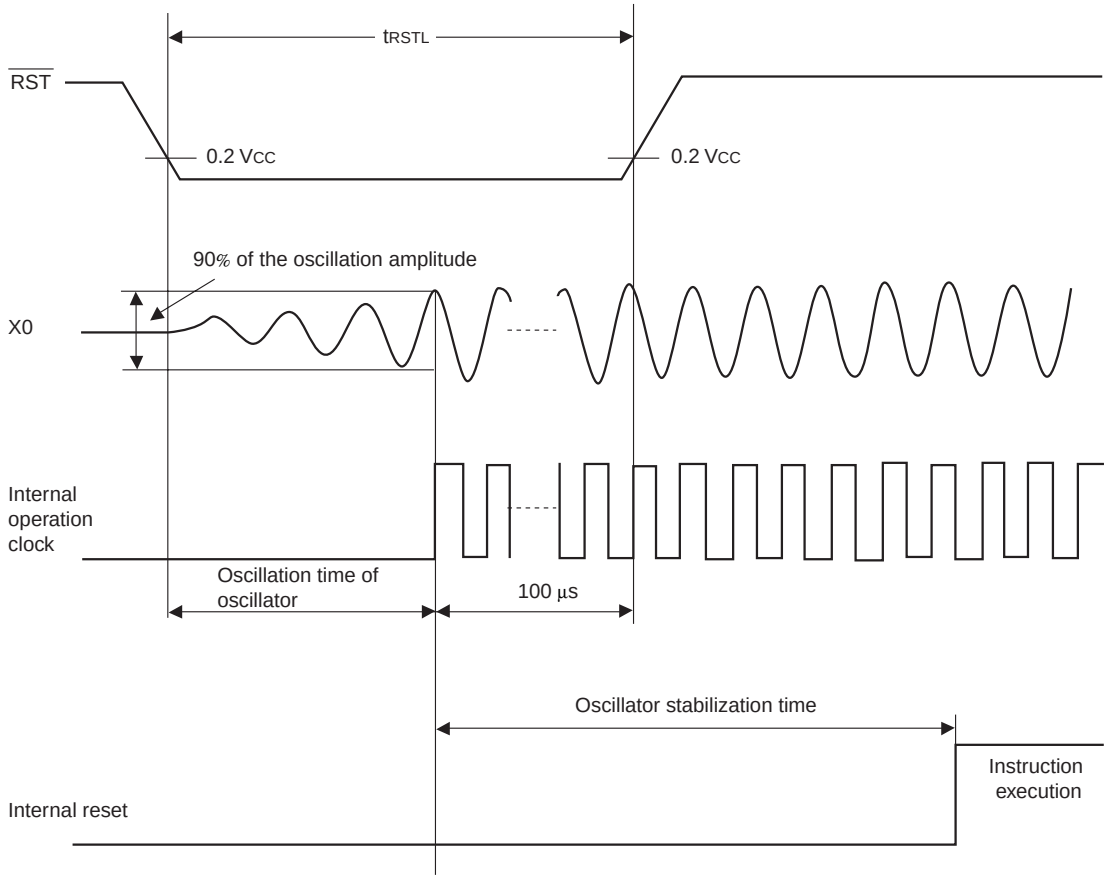
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	—	ns	Normal operation
			Oscillation time of oscillator* + 100	—	µs	Stop mode
			100	—	µs	Timebase timer mode

* : Oscillation time of oscillator is the time to reach to 90% of the oscillation amplitude from stand still. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In FAR/ceramic oscillator, the oscillation time is between hundreds of µs to several ms. In the external clock, the oscillation time is 0 ms.

• In normal operation mode



• In stop mode

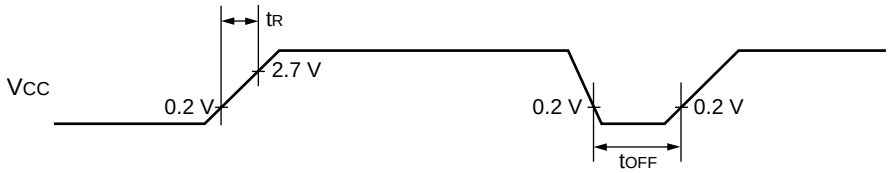


(3) Power-on Reset

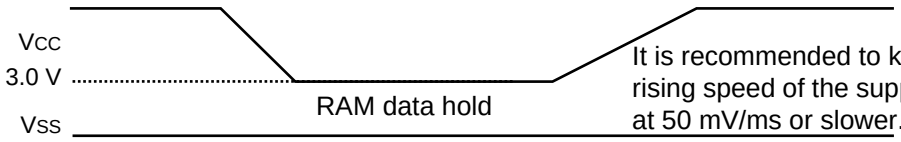
(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rising time	t_R	V_{CC}	—	0.05	30	ms	
Power supply cut-off time	t_{OFF}	V_{CC}		1	—	ms	Due to repeated operations

Notes :
- V_{CC} must be kept lower than 0.2 V before power-on.
- The above values are used for causing a power-on reset.
  Some registers in the device are initialized only upon a power-on reset. To initialize these registers, turn the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V/s, however, you can use the PLL clock.



It is recommended to keep the rising speed of the supply voltage at 50 mV/ms or slower.

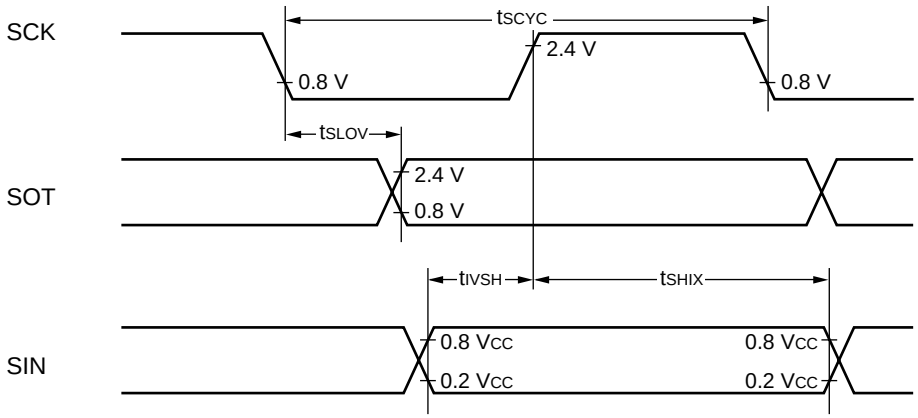
(4) UART0 to UART1

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

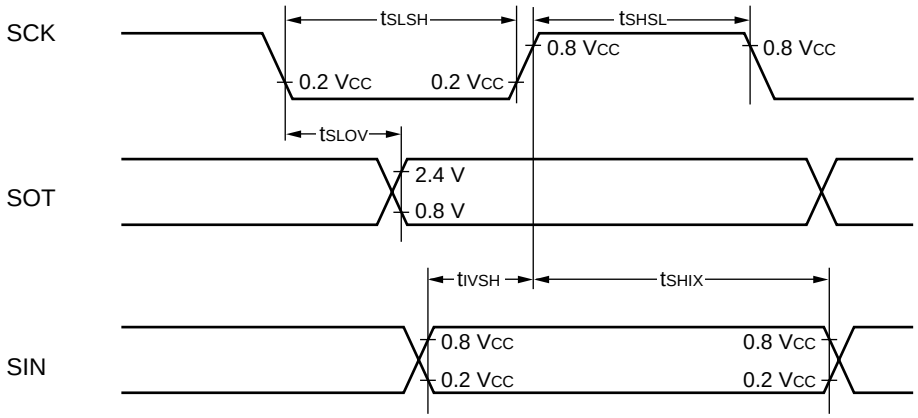
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK1	C_L = 80 pF + 1 TTL for an output pin of internal shift clock mode	8 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK1 SOT0 to SOT1		–80	80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK1 SIN0 to SIN1		100	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK1 SIN0 to SIN1		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK1	C_L = 80 pF + 1 TTL for an output pin of external shift clock mode	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK1		4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK1 SOT0 to SOT1		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK1 SIN0 to SIN1		60	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK1 SIN0 to SIN1		60	—	ns	

Notes : • These are AC ratings in the CLK synchronous mode.
• CL is the load capacitance value connected to pins while testing.
• t_{CP} is machine cycle time (unit : ns).

• Internal shift clock mode



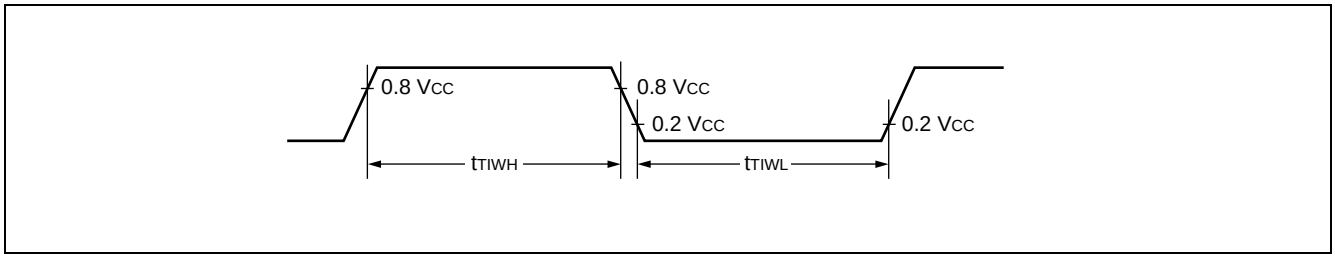
• External shift clock mode



(5) Resources Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

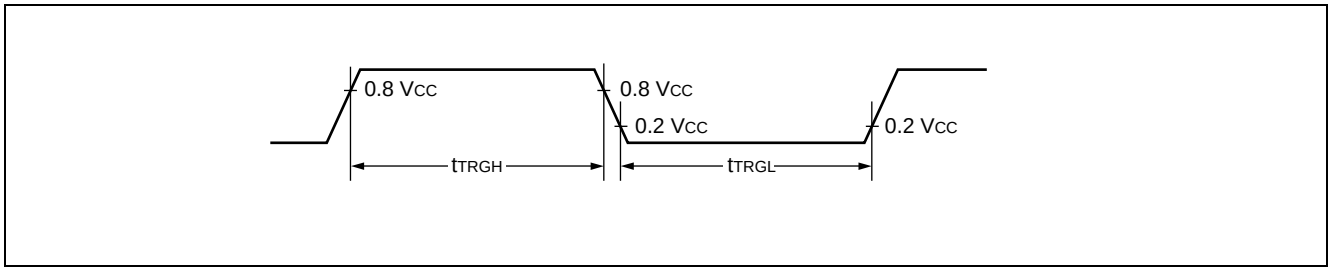
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	IN0 to IN3, TIN0 to TIN1, PWI0 to PWI1, DTTI	—	4 t_{CP}	—	ns	



(6) Trigger Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT7	—	5 t_{CP}	—	ns	



5. A/D Converter Electrical Characteristics

(3.0 V ≤ AVR – AV_{SS}, V_{CC} = AV_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

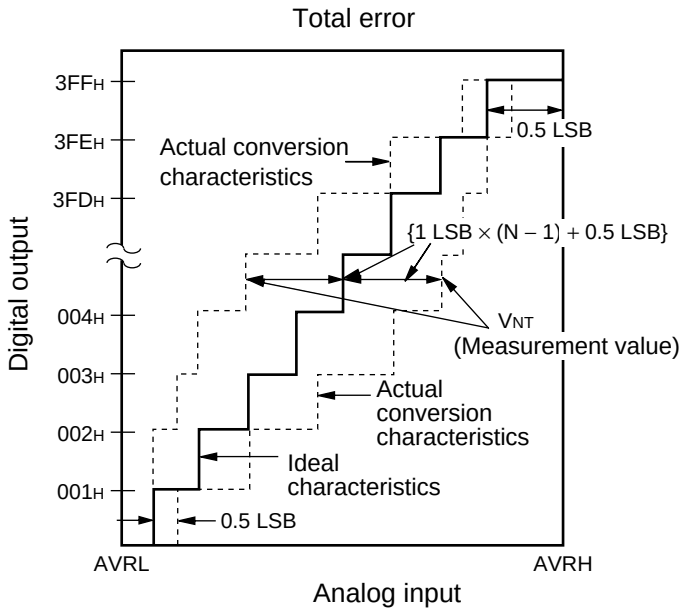
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	10	—	bit	
Total error	—	—	—	—	±3.0	LSB	
Non-linearity error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN15	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	mV	
Full-scale transition voltage	V_{FST}	AN0 to AN15	AVR – 3.5 LSB	AVR – 1.5 LSB	AVR + 0.5 LSB	mV	
Compare time	—	—	1.0	—	—	µs	4.5 V ≤ AVcc ≤ 5.5 V
			2.0	—	—	µs	4.0 V ≤ AVcc < 4.5 V
Sampling time	—	—	0.5	—	—	µs	4.5 V ≤ AVcc ≤ 5.5 V
			1.2	—	—	µs	4.0 V ≤ AVcc < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN15	- 0.3	—	+ 0.3	µA	
Analog input voltage	V_{AIN}	AN0 to AN15	AV_{SS}	—	AVR	V	
Reference voltage	—	AVR	AV_{SS} + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	2.4	4.7	mA	
	I_{AH}		—	—	5	µA	*
Reference voltage supply current	I_R	AVR	—	600	900	µA	
	I_{RH}		—	—	5	µA	*
Offset between channels	—	AN0 to AN15	—	—	4	LSB	

* : The current when the A/D converter is not operating or the CPU is in stop mode (for V_{CC} = AV_{CC} = AVR = 5.0 V)

Note : The error increases proportionally as |AVR - AV_{SS}| decreases.

6. A/D Converter Glossary

Resolution	:	Analog variation that is recognized by an A/D converter.
Non linearity error	:	Deviation between a line across zero-transition line (“00 0000 0000”↔“00 0000 0001”) and full-scale transition line (“11 1111 1110”↔“11 1111 1111”) and actual conversion characteristics.
Differential linearity error	:	Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value
Total error	:	Difference between an actual value and an ideal value. Atotal error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{AVR - AVss}{1024}\ [V]$$

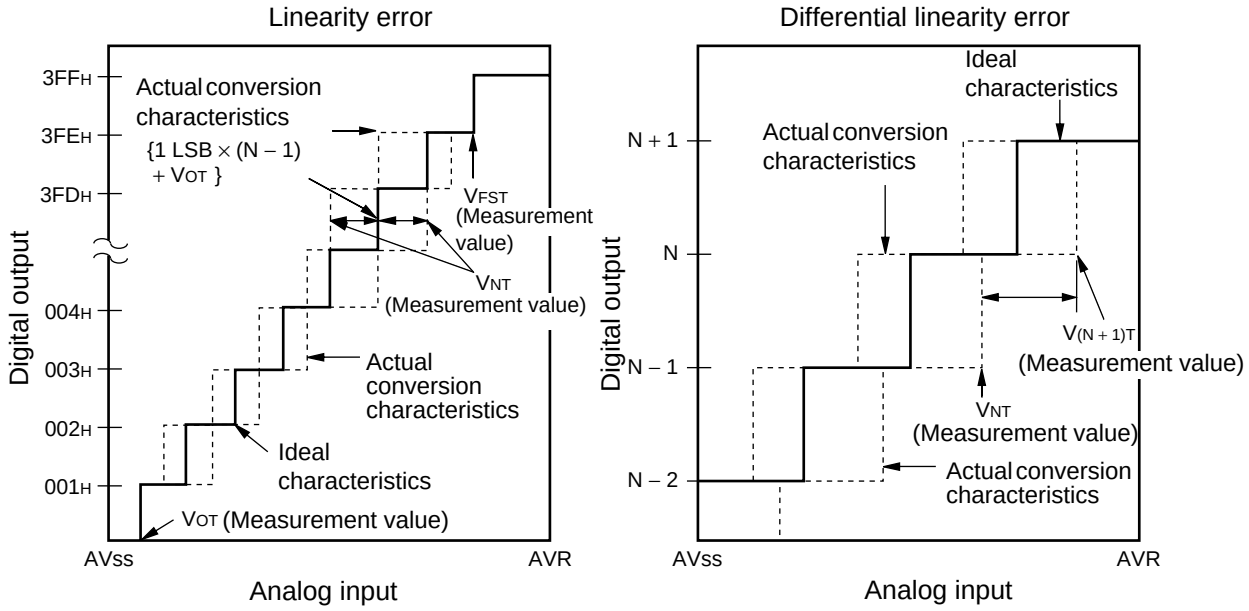
V_{OT}(Ideal value) = AVss + 0.5 LSB [V]

V_{FST}(Ideal value) = AVR – 1.5 LSB [V]

V_{NT} : Voltage at which of digital output transitions from (N – 1) to N.

(Continued)

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{[LSB]}$$

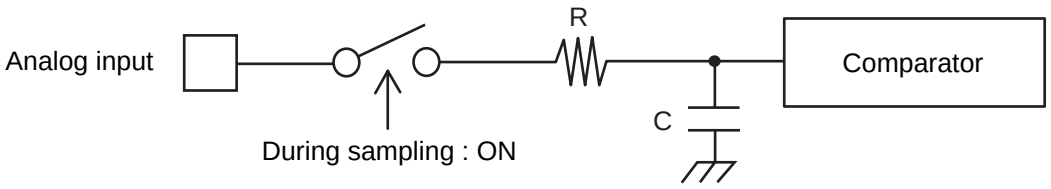
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

V_{OT} : Voltage at which of digital output transmissions from “000_H” to “001_H”.
V_{FST} : Voltage at which of digital output transmissions from “$3FE_H$” to “$3FF_H$”.

7. Notes on Using A/D Converter

- **About the external impedance of the analog input and its sampling time**
  - A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- Analog input circuit model



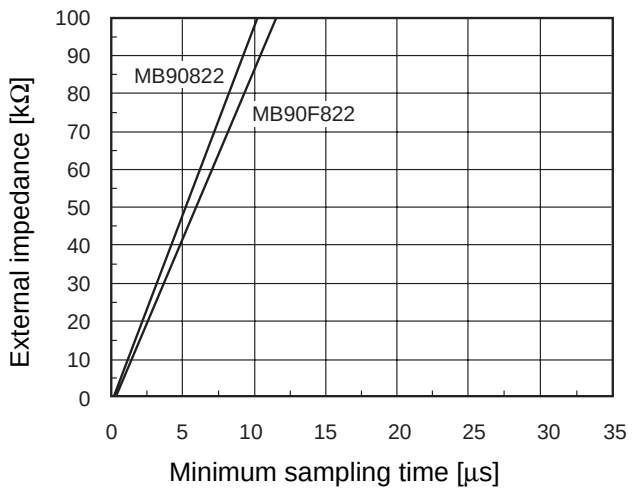
	R	C
MB90822	2.0 kΩ (Max)	14.4 pF (Max)
MB90F822	2.0 kΩ (Max)	16.0 pF (Max)

Note : The values are reference values.

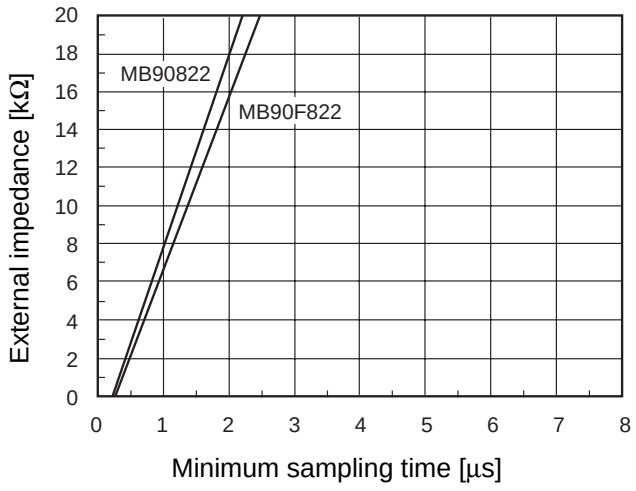
- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

- The relationship between the external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- About the error
  The accuracy gets worse as | AVR–AVSS | becomes smaller.

8. Electrical Characteristics of D/A convertor

(V_{CC} = AV_{CC} = 4.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	8	—	bit	
Differential linearity error	—	—		—	—	±0.5	LSB	
Conversion time	—	—		—	0.45	—	µs	*
Analog output impedance	—	—		—	2.9	3.8	kΩ	
Power supply current	I_{DVR}	AV_{CC}		—	160	920	µA	
	I_{DVRS}			—	0.1	—	µA	D/A stops

* : With load capacitance 20 pF.

9. Flash Memory Program/Erase Characteristics

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = +25 °C V_{CC} = 5.0 V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16 bit width) programing time		—	16	3,600	µs	Except for the overhead time of the system
Program/Erase cycle	—	10,000	—	—	cycle	
Flash data retention time	Average T_A = +85 °C	20	—	—	Year	*

* : This value comes from the technorogy qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

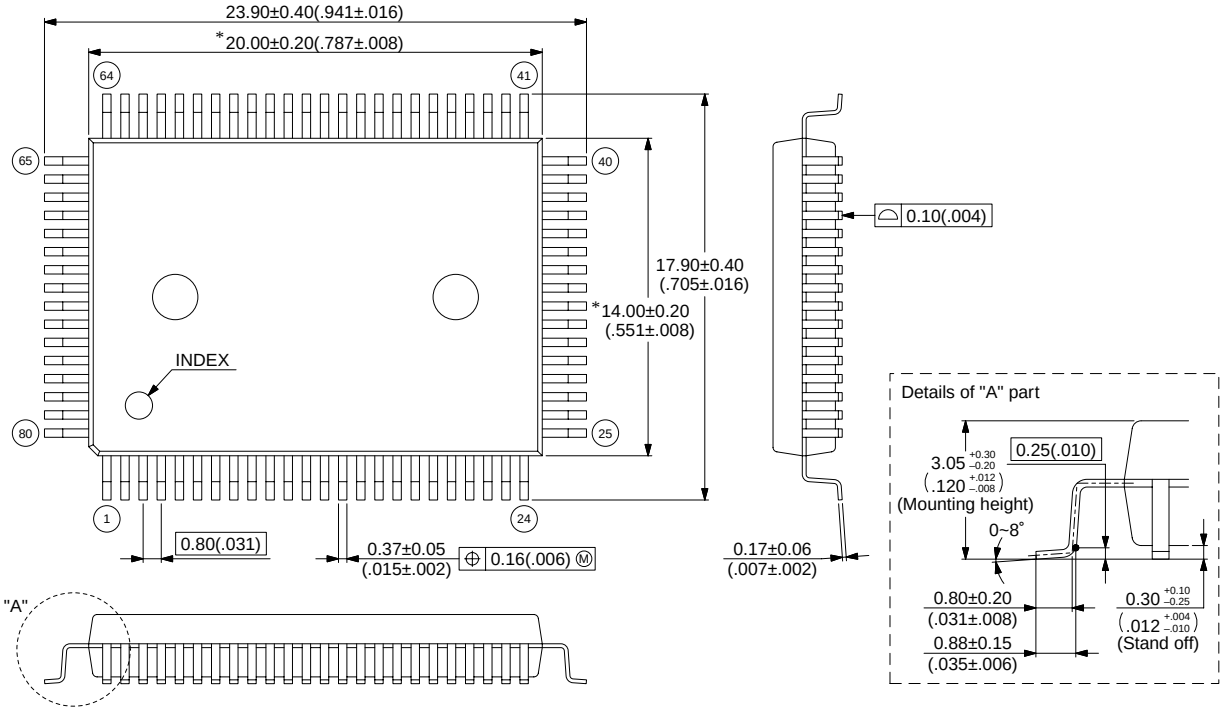
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F823PFV MB90F822PFV MB90822PFV	80-pin Plastic LQFP (FPT-80P-M05)	
MB90F823PFM MB90F822PFM MB90822PFM	80-pin Plastic LQFP (FPT-80P-M11)	
MB90F823PF MB90F822PF MB90822PF	80-pin Plastic QFP (FPT-80P-M06)	

■ PACKAGE DIMENSIONS

80-pin plastic QFP
(FPT-80P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

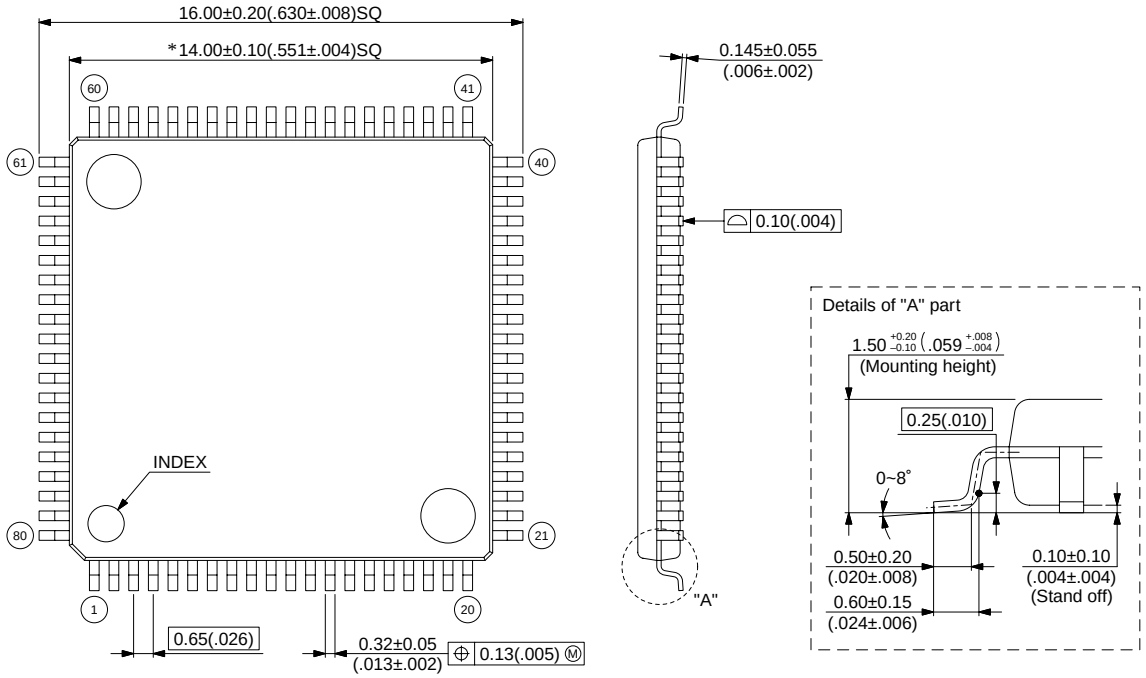


Dimensions in mm (inches)
Note : The values in parentheses are reference values.

(Continued)

80-pin plastic LQFP
(FPT-80P-M11)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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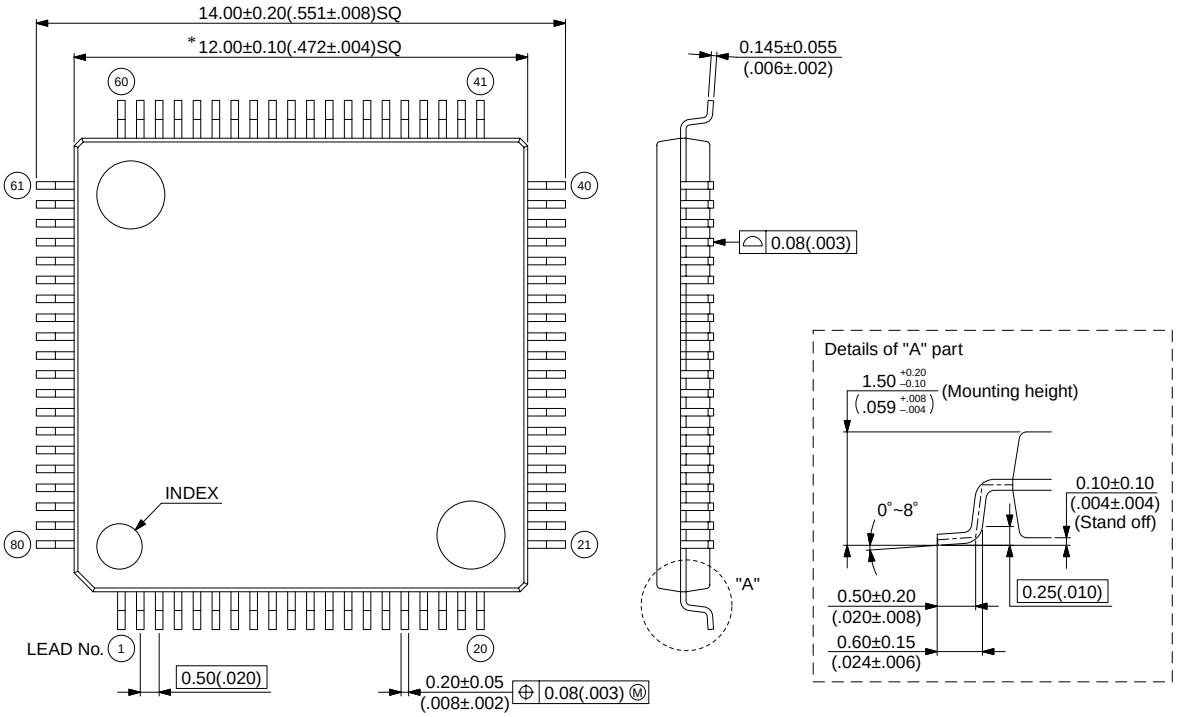
80-pin plastic LQFP
(FPT-80P-M05)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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