F75334DG

Performance Controller

Release Date: July, 2007
Version: V0.25P

F75334DG Datasheet Revision History

Version	Date	Page	Revision History
V0.10P	2005/09/01	-	Preliminary Version
V0.20P	2005/09/02	-	Added Register Description and Application Circuit
V0.21P	2005/10/13	-	Updated I2C Address Strapping Description of Function Description
V0.22P	2005/12/19	-	Updated Schematic
V0.23P	2006/07/04	-	Added function on pin7/pin13/pin29
		-	Added Hardware Monitor Register description (CR 0Ah ~ CR0Eh)
		-	Modified Hardware Monitor Register description (CR02h/93h/9Fh/AFh/BFh/CFh)
		-	Added Global Register CR1Ch
		-	Updated application circuit
V0.24P	2006/12/28	-	Added Electrical Characteristic Chapter
		2	Added Patent Note
V0.25P	2007/7/6	-	Company readdress

Table of Content

1. General Description

The F75334DG is an integrated performance control IC. The F75334DG integrated Hardware Monitor, PWM Loading Gauge, VID controller and GPIO functions inside. Part of the Hardware Monitor is for system protection including 6 channels voltage monitor, 4 sets dual current sources temperature sensor, 3 sets fan speed sensor and controller. Besides, provides Intel new generational temperature interfaces PECI/SST for temperature reading and also supports AMDSI interface for AMD series CPU temperature reading. PWM Loading Gauge is sensing the PWM signal change of duty cycle to react related functions for over/under-clocking application. VID controller is the dynamic voltage ID controller chip to provide the advanced CPU voltage programming when over/under clocking. The dynamic VID spec. is for new generation Intel/AMD CPU and also compatible to VRM9.0/VRM10.0/VRM10.X /VRM11.0 spec.. Additionally, the F75334DG provides easy voltage sensor input/output (VSI/VSO) function to sense Vcore voltage, then output the offset voltage for over/under voltage change use. Otherwise, F75334DG provides 21 GPIO pins for flexible application.

The F75334DG supports three main features for system protection, system over/under-clocking and dynamic voltage ID control. The F75334DG can easy save total cost and improve system performance. Especially the Loading Gauge feature will achieve multi-steps dynamic over/under-clocking being easy function. The F75334DG support 2 wire I2C interface, packaged in 48-pin LQFP green package and powered by 3.3V.

2. Feature List

- **General Functions**
  - Support 6 channels voltage monitor
  - Provide 4 temperature sensors
  - Support 3 sets fan control
  - Loading gauge for device loading sensing
  - Provide VID controller with OTF
  - 21 GPIO pins for flexible application
  - Easy voltage sensor I/O (VSI/VSO) for easy over/under voltage change use.
  - Support Intel PECI/SST interfaces for temperature reading.
  - Support AMDSI interface for temperature reading.
  - 2 wire I2C interface
  - 3VCC operation and packaged in 48-LQFP green package

- **Hardware Monitor**
  - Voltage Monitor

1. Provide 2.048V VREF
2. Support 6 channels voltage monitor(VCC3 V + VSB3V + 4 Externals)
3. Voltage monitor resolution is 8mv per LSB
4. Support 8bits high limit and low limit for each voltage channel

- Temperature Monitor
  1. Support 4 temperature sensor (1 local + 3 remote)
  2. Remote sensors support 2 types sensor (thermistor and transistor/thermal diode(Default))
  3. ±1°C accuracy on remote channel (60°C ~ 100°C)
  4. ±3°C accuracy on local channel (60°C ~ 100°C)
  5. Support temperature range from -25°C ~ 145°C
  6. Support high limit for each temperature sensor
  7. Support OVT(over temperature) limit for each temperature sensor
  8. Each temperature with hysteresis for high limit and OVT limit (0°C~15°C)
- Fan Controller and Monitor
  1. Support 3 sets fan speed sensor and fan control
  2. 50K fan speed sampling rate
  3. Support Intel 4-Fan control mode

  (1. Auto RPM Mode 2. Auto Duty Mode(Default) or manual duty 3. Manual RPM)

- **Loading Gauge**
  - Provide 1 PWMIN detection pins
  - Duty cycle reading resolution is 16bits
  - Support 4 duty limit (5 segments), and the resolution is 12 bits
  - Support 4 hysteresis registers for each limit (± offset)
  - Support 3 TURBO# output signals to control CLK Gen.
  - Support 1 STOP# output signal to chipset (Timing flexible)

- **VID controller**
  - Support VRM9.0, VRM10.0, VRM10 extend and VRM11.0
  - Support 5 offset registers to mapping 5 different loading range
  - Support Intel and AMD CPU
  - Easy voltage sensor I/O (VSI/VSO) for easy over/under voltage change use.

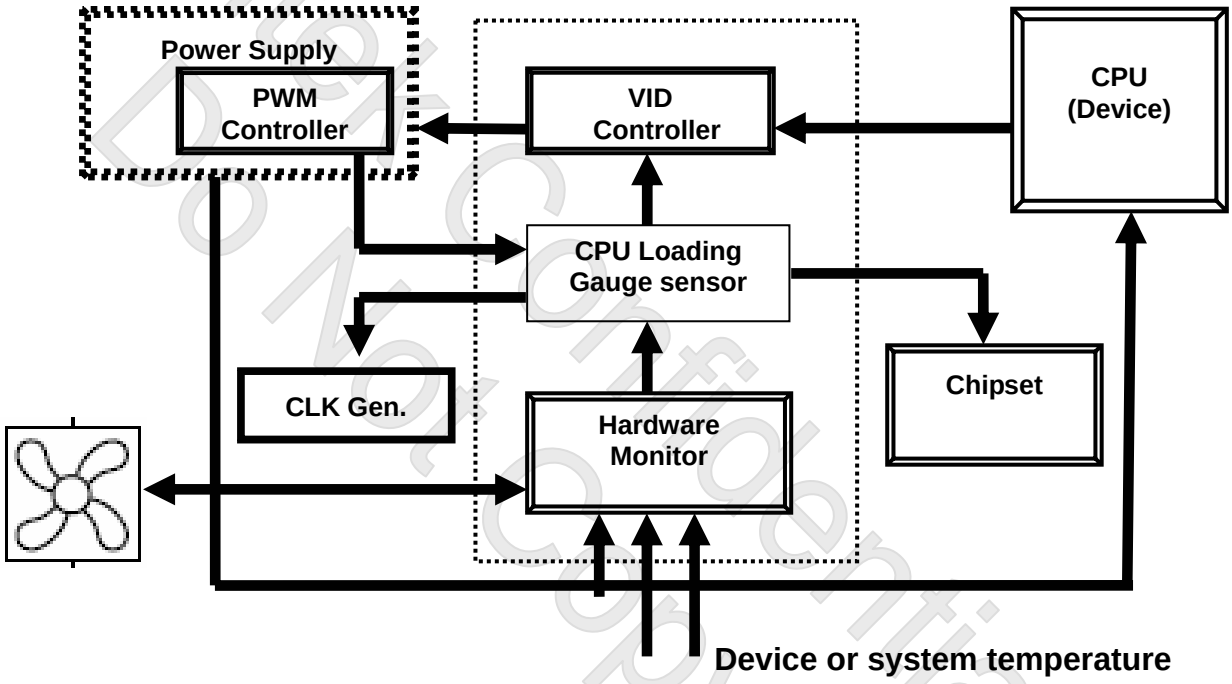
- **GPIO**
  - Support 21 GPIO pins
  - Only support level mode GP output control
  - GPIO pin status can be read by registers

Noted: Patented TWI235553 TWI263778

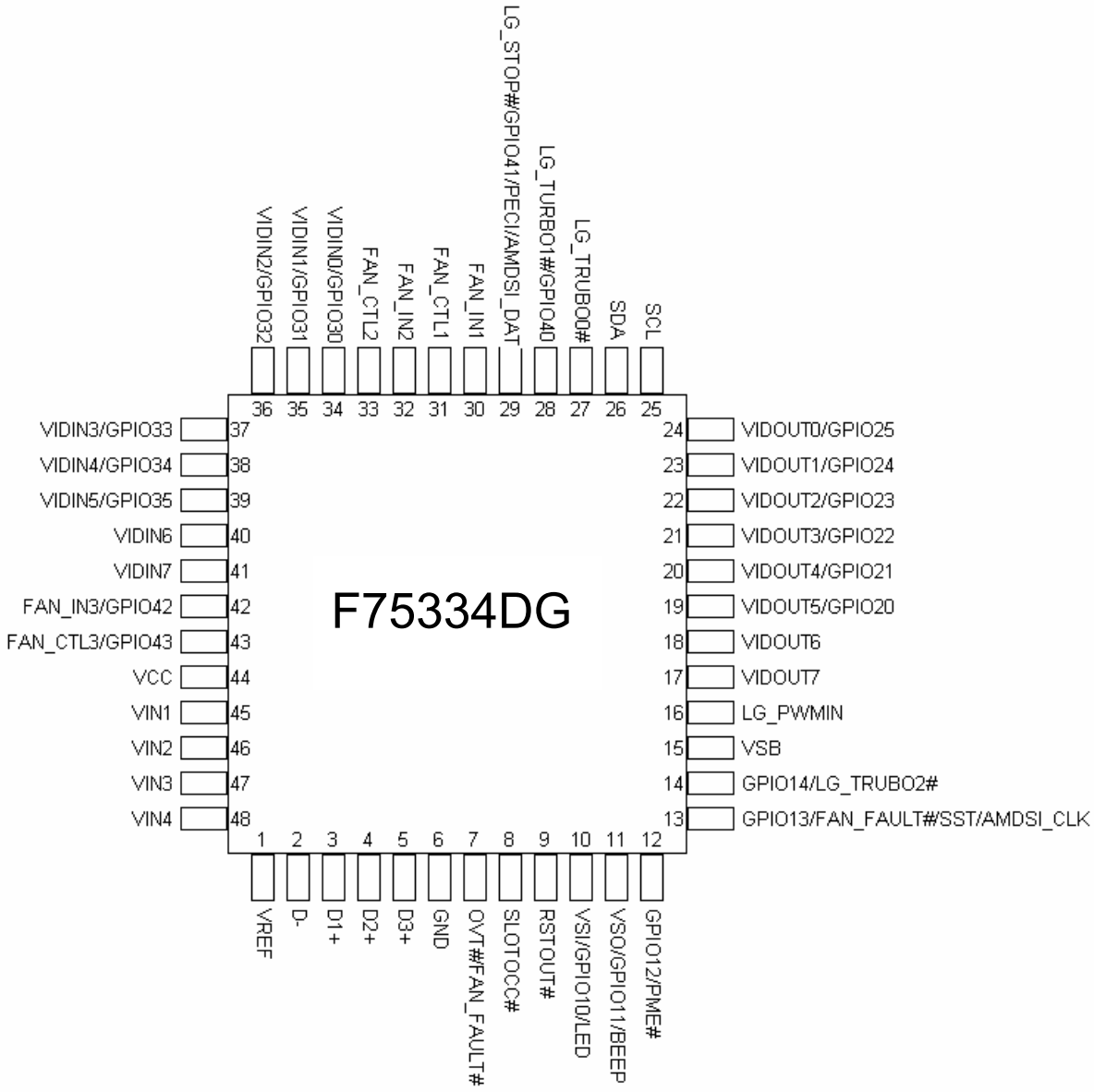
3. Key Specification

- Supply Voltage 3.0V to 3.6V
- Operating Supply Current 2.5 mA typ.

4. Block Diagram



5. Pin Configuration



6. Pin Description

I/OD_{12st} - TTL level bi-directional pin with schmitt trigger, Open-drain output with12 mA sink capability.
I/O_{12st} - TTL level bi-directional pin with schmitt trigger and with 12mA source-sink capability.
I/OOD_{12st} - TTL level bi-directional pin with schmitt trigger, Output pin with 12mA source-sink capability, and can programming to open-drain function.
I/OOD_{12lv} - Low level bi-directional pin, Output pin with 12mA source-sink capability, and can programming to open-drain function.
I_{Lv}/O_{D8-S1} - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.). Output with 8mA drive and 1mA sink capability.
I_{Lv}/OD_{12} - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.). Output with 12mA sink capability.
OD_{12} - Open-Drain output pin with 12mA sink capability.
OOD_{12} - Output pin with 12mA source-sink capability, and can programming to open-drain function.
IN_{st} - TTL level input pin with schmitt trigger.
IN_{lv} - Low level input pin
AIN - Input pin(Analog).
AOUT - Output pin(Analog).
P - Power.

6.1 Power Pin

Pin No.	Pin Name	Type	Description
15	VSB	P	3.3V Standby Power
44	VCC	P	3.3V VCC Power
6	GND	P	Ground

6.2 Hardware Monitor Pin

Pin No.	Pin Name	Type	PWR	Description
1	VREF	AOUT	VCC3V	Reference voltage output 2.304V.
2	D-	AIN	VCC3V	Temperature sensor ground pin.
3, 4, 5	D0+ ~ D2+	AIN	VCC3V	CPU thermal diode/transistor temperature sensor input.
7	OVT#	I/OD_{12st}	VSB3V	Over temperature signal output. Default open drain active-low output. This pin will be a logic LOW when the temperature exceeds its limit. Default output enable when the temperature exceeds 100°C on initial.
	FAN_FAULT#	OD_{12}		Fan fault signal output pin.
12	GPIO12	I/OOD_{12st}	VSB3V	GPIO pin.
	PME#	OD_{12}		PME# signal output pin. System management interrupt (Pure open drain). This pin will be active low when there is something wrong with voltage,

				temperature and fan. See register description index 33h.
13	GPIO13	I/OOD_{12st}	VSB3V	GPIO pin.
	FAN_FAULT#	OD_{12}		Fan fault signal output pin.
	SST	I_{Lv}/O_{D8-S1}		Intel SST hardware monitor interface.
	AMDSI_CLK	OD_{12}		Clock output for AMD SI interface.
30	FAN_IN1	IN_{st}	VCC3V (5V-tolerance)	Fan 1 tachometer input.
31	FAN_CTL1	OOD_{12}	VCC3V (5V-tolerance)	Use PWM duty cycle to control fan1 speed.
		AOUT		Use linear voltage output (0~3.3V) to control fan1 speed.
32	FAN_IN2	IN_{st}	VCC3V (5V-tolerance)	Fan 2 tachometer input.
33	FAN_CTL2	OOD_{12}	VCC3V (5V-tolerance)	Use PWM duty cycle to control fan2 speed.
		AOUT		Use linear voltage output (0~3.3V) to control fan2 speed.
42	FAN_IN3	IN_{st}	VCC3V (5V-tolerance)	Fan 3 tachometer input.
	GPIO42	I/OOD_{12st}		GPIO pin.
43	FAN_CTL3	OOD_{12}	VCC3V	Use PWM duty cycle to control fan3 speed.
		AOUT		Use linear voltage output (0~3.3V) to control fan3 speed.
	GPIO43	I/OOD_{12st}		GPIO pin.
45 – 48	VIN1 ~ VIN4	AIN	VCC3V	Voltage monitor pin1~4. (0V ~ 2.048V)

6.3 VID Controlling Pin

Pin No.	Pin Name	Type	PWR	Description
17-18	VIDOUT[7:6]	OD_{12}	VCC3V	CPU VID output pin
19-24	VIDOUT[5:0]	OD_{12}	VCC3V	CPU VID output pin
	GPIO2[0:5]	I/OOD_{12st}		GPIO pin
39-34	VIDIN[5:0]	IN_{lv}	VCC3V	CPU VID input pins. Special level input VIH→ 0.9, VIL → 0.6.
	GPIO3[5:0]	I/OOD_{12lv}		GPIO pin
41-40	VIDIN[7:6]	IN_{lv}	VCC3V	CPU VID input pins. Special level input VIH→ 0.9, VIL → 0.6.
8	SLOTOCC#	IN_{st}	VSB3V	CPU SLOTOCC# input.
9	RSTOUT#	OD_{12st}	VSB3V	Reset out signal output.

6.4 Loading Gauge Pin

Pin No.	Pin Name	Type	PWR	Description
10	VSI	AIN	VSB3V	Voltage sensor input for Vcore voltage sensing.
	GPIO10	I/OOD_{12st}		GPIO pin.
	LED	OD_{12}		LED flashing pin.
11	VSO	AOUT	VSB3V	Voltage sensor output for over/under voltage use.
	GPIO11	I/OOD_{12st}		GPIO pin.
	BEEP	OD_{12}		BEEP pin.
14	GPIO14	I/OOD_{12st}	VSB3V	GPIO pin.
	LG_TURBO2#	OD_{12}		Turbo 2 pin for CLK Gen over/under clocking.

16	LG_PWMIN	IN_{st}	VCC3V (5V-tolerance)	PWM duty cycle sensing pin.
25	SCL	IN_{st}	VCC3V (5V-tolerance)	Serial clock input pin.
26	SDA	I/OD_{12st}	VCC3V (5V-tolerance)	Serial data pin.
27	LG_TURBO0#	O_{12}	VCC3V	Turbo 0 pin for CLK Gen over/under clocking.
28	LG_TURBO1#	OD_{12}	VCC3V	Turbo 1 pin for CLK Gen over/under clocking.
	GPIO40	I/OOD_{12st}		GPIO pin.
29	LG_STOP#	OD_{12}	VCC3V	Stop signal for chipset use.
	GPIO41	I/OOD_{12st}		GPIO pin.
	PECI	I_{Lv}/O_{D8-S1}		Intel PECI hardware monitor interface.
	AMDSI_DAT	I_{Lv}/OD_{12}		AMD SI data interface.

7. Function Description

The F75334DG provides a pin27 for functions/addresses trapping. Remember to select the function/address before you implement this chip. Trapping table is as below.

	Pull down 4.7k (00)	Pull down 200k (10)	Pull up 200k (11)	Pull up 4.7k (01)
I2C address	8'h66	8'h6A	8'h6C	8'h68
Fan type	DC (linear fan)	DC (linear fan)	PWM fan control	PWM fan control
Pwm polarity	PWM_IN#	PWM_IN#	PWM_IN	PWM_IN

7.1 Hardware monitor

For the 8-bit ADC has the 8mv LSB, the maximum input voltage of the analog pin is 2.048V. Therefore the voltage under 2.048V (ex:1.5V) can be directly connected to these analog inputs. The voltage higher than 2.048V should be reduced by a factor with external resistors so as to obtain the input range. Only 3Vcc is an exception for it is main power of the F75334DG. Therefore 3Vcc can directly connect to this chip's power pin and need no external resistors. There are two functions in this pin with 3.3V. The first function is to supply internal analog power of the F75334DG and the second function is that voltage with 3.3V is connected to internal serial resistors to monitor the +3.3V voltage. The internal serial resistors are two 150K ohm, so that the internal reduced voltage is half of +3.3V.

There are four voltage inputs in the F75334DG and the voltage divided formula is shown as follows:

$$VIN = V_{+12V} \times \frac{R_2}{R_1 + R_2}$$ where V_{+12V} is the analog input voltage, for example.

If we choose R1=27K, R2=5.1K, the exact input voltage for V+12v will be 1.907V, which is within the tolerance. As for application circuit, it can be refer to the figure shown as follows.

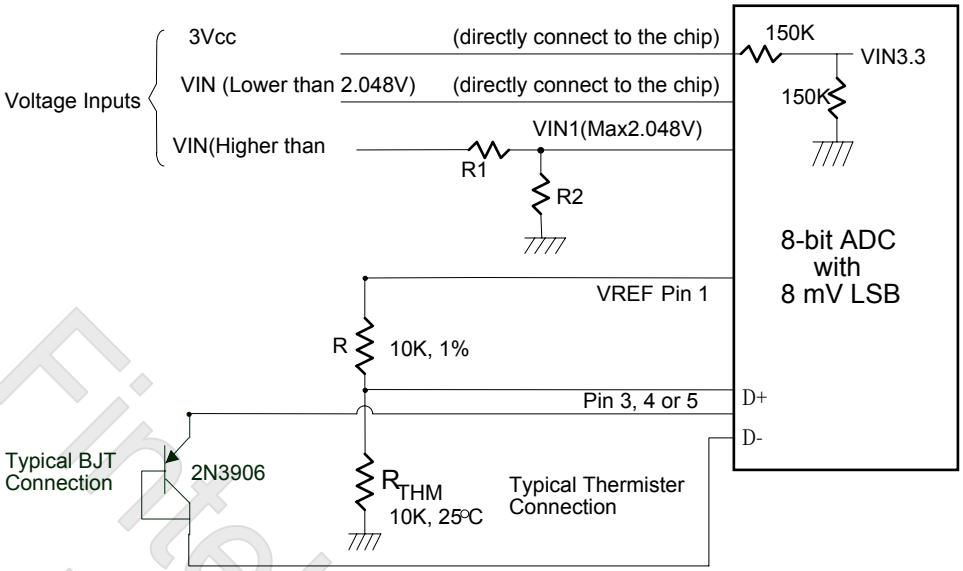


Fig 7-1

SMI# interrupt for voltage is shown as figure. Voltage exceeding or going below high limit will cause an interrupt if the previous interrupt has been reset by writing "1" all the interrupt Status Register. Voltage exceeding or going below low limit will result the same condition as voltage exceeding or going below high limit.

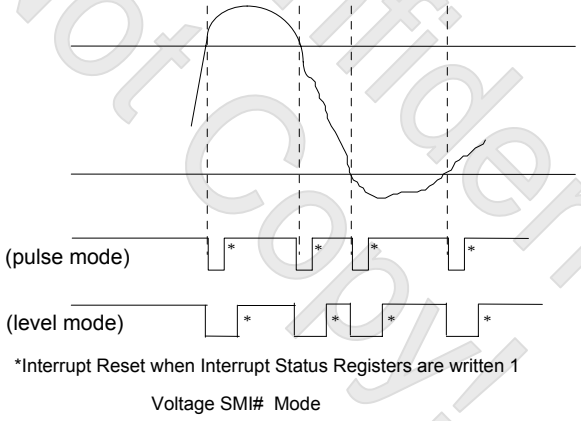
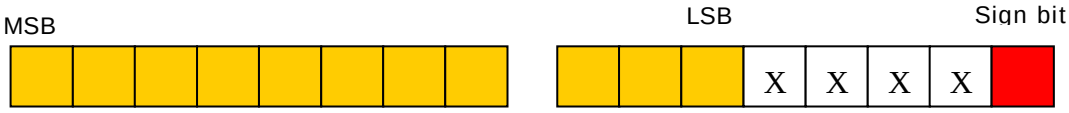


Fig 7-2

The F75334DG monitors a local and three remote temperature sensors. Both can be measured from -25°C to 145°C. The temperature format is as the following table:



00000000_001xxxx0→ 0.125

10000000_001xxxx0→ 128.125

10010001 111xxxx0→ 145.785

11010000_111xxxx0→ 208.785 (145.785 + 63) (offset)

11111111 111xxxx1→ - 0.125

11011011 111xxxx1→ - 25.125

11010000_111xxxx1→ -48.125 (-25.125 - 23) (offset)

Remote-sensor transistor manufacturers

Manufacturer	Model Number
Panasonic	2SB0709 2N3906
Philips	PMBT3906

Monitor Temperature from "thermistor"

The F75334DG can connect three thermistor to measure environment temperature or remote temperature. The specification of thermistor should be considered to (1) β value is 3435K (2) resistor value is 10K ohm at 25°C. In the Figure 7-1, the thermistor is connected by a serial resistor with 10K ohm, then connected to VREF.

Monitor Temperature from "thermal diode"

Also, if the CPU, GPU or external circuits provide thermal diode for temperature measurement, the F75334DG is capable to these situations. The build-in reference table is for PNP 2N3906 transistor, and each different kind of thermal diode should be matched with specific BJT gain. In the Figure 7-1, the transistor is directly connected into temperature pins.

ADC Noise Filtering

The ADC is integrating type with inherently good noise rejection. Micro-power operation places constraints on high-frequency noise rejection; therefore, careful PCB board layout and suitable external filtering are required for high-accuracy remote measurement in electronically noisy environment. High frequency EMI is best filtered at D+ and D- with an external 2200pF capacitor. Too high capacitance may introduce errors due to the rise time of the switched current source. Nearly all noise sources tested cause the ADC measurement to be higher than the actual temperature, depending on the frequency and amplitude.

Over Temperature Signal (OVT#)

OVT# alert for temperature is shown as figure 7-3. When monitored temperature exceeds the over-temperature threshold value, OVT# will be asserted until the temperature goes below the hysteresis temperature.

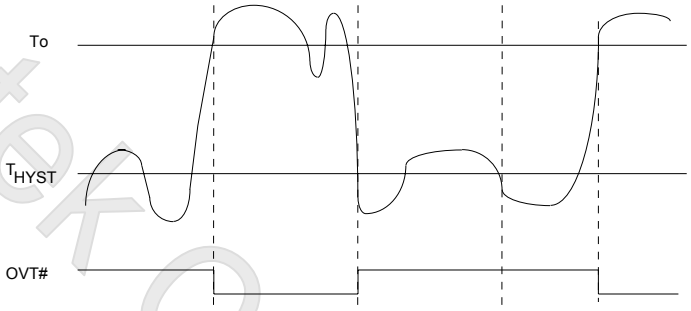
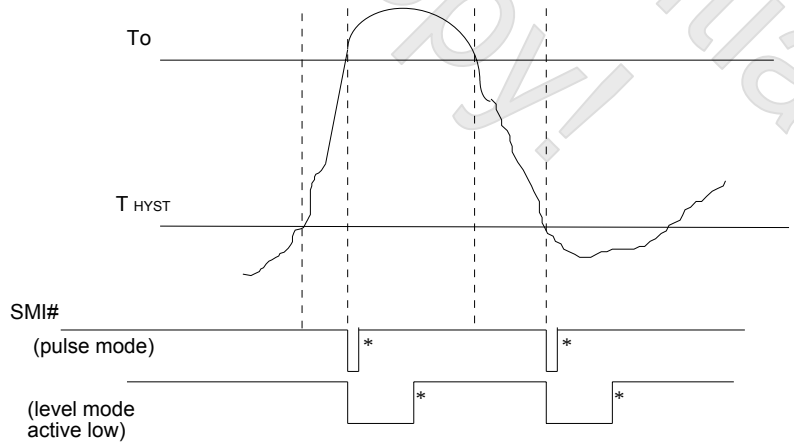


Fig 7-3

Temperature PME#

PME# interrupt for temperature is shown as figure 7-4. Temperature exceeding high limit or going below hysteresis will cause an interrupt if the previous interrupt has been reset by writing "1" all the interrupt Status Register.

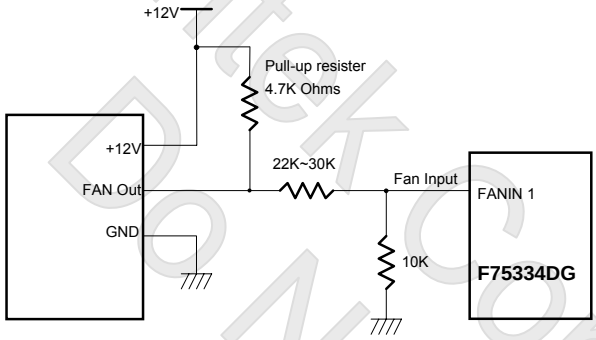


*Interrupt Reset when Interrupt Status Registers are written 1

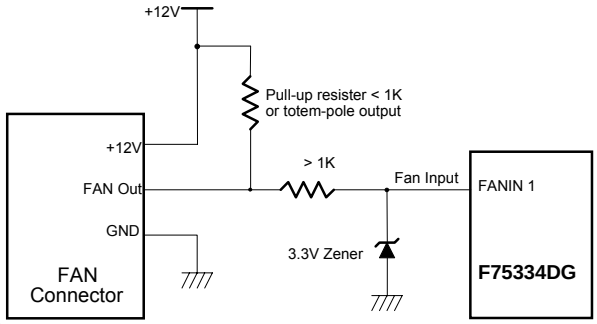
Fig 7-4

Fan speed count

Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over 5V. If the input signals from the tachometer outputs are over the 5V, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as follows:

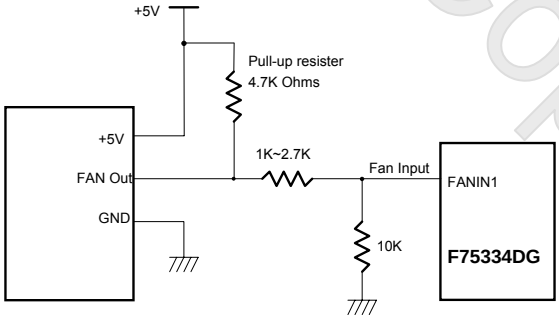


Fan with Tach Pull-Up to +12V, or Totern-Pole Output and Register Attenuator

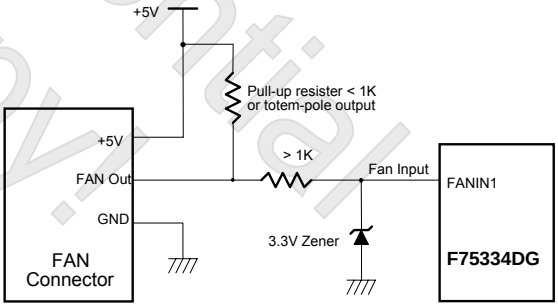


Fan with Tach Pull-Up to +12V, or Totem-Pole Putput and Zener Clamp

Fig 7-5 / 7-6



Fan with Tach Pull-Up to +5V, or Totern-Pole Output and Register Attenuator



Fan with Tach Pull-Up to +5V, or Totem-Pole Putput and Zener Clamp

Fig 7-7 / 7-8

Determine the fan counter according to:

$$Count = \frac{1.5 \times 10^6}{RPM}$$

In other words, the fan speed counter has been read from register, the fan speed can be

evaluated by the following equation. As for fan, it would be best to use 2 pulses tachometer output per round.

$$RPM = \frac{1.5 \times 10^6}{Count}$$

Fan speed control

The F75334DG provides 2 fan speed control methods:

1. LINEAR FAN CONTROL 2. PWM DUTY CYCLE

Linear Fan Control

The range of DC output is 0~3.3V, controlled by 8-bit register. 1 LSB is about 0.013V. The output DC voltage is amplified by external OP circuit, thus to reach maximum FAN OPERATION VOLTAGE, 12V. The output voltage will be given as followed:

$$\text{Output\_voltage (V)} = 3.3 \times \frac{\text{Programmed 8bit Register Value}}{255}$$

And the suggested application circuit for linear fan control would be:

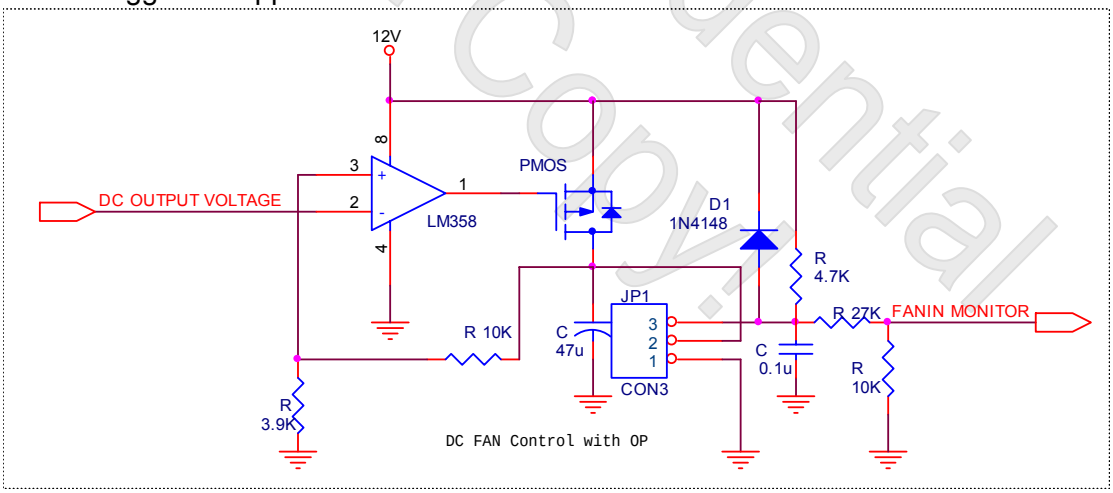


Fig 7-9

PWM duty Fan Control

The duty cycle of PWM can be programmed by a 8-bit register. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be

represented as follows.

$$\text{Duty\_cycle}(\%) = \frac{\text{Programmed 8bit Register Value}}{255} \times 100\%$$

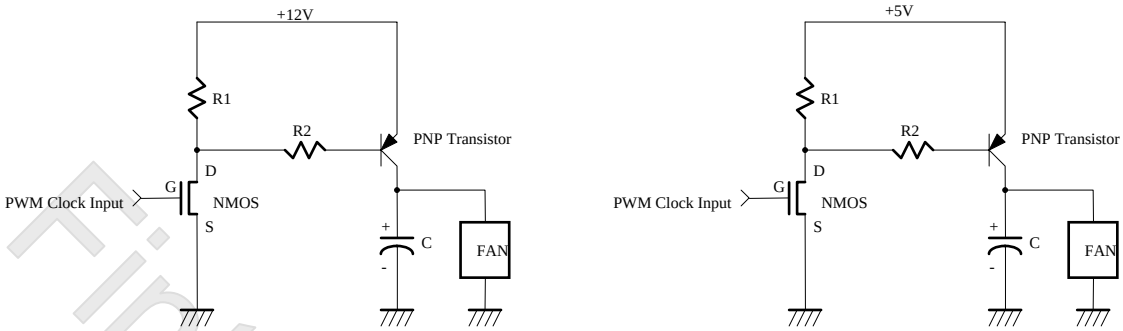


Fig 7-10

Fan speed control mechanism

There are some modes to control fan speed and they are 1. Auto RPM Mode 2. Auto Duty Mode(Default) or manual duty 3. Manual RPM. More detail please refer register description.

Manual mode

For manual mode, it generally acts as software fan speed control.

Temperature mode

At this mode, the F75334DG provides automatic fan speed control related to temperature variation of CPU/GPU or the system. The F75334DG can provide four temperature boundaries and five intervals, and each interval has its related fan speed count. All these values should be set by BIOS first. Take figure 7-11 as example. When temperature boundaries are set as 45, 55, 65, and 75°C and there are five intervals (each interval is 10°C). The related desired fan speed counts for each interval are 0500h, 0400h, 0300h, 0200h and 0100h. When the temperature is within 55~65°C, the fan speed count 300h will be load into FAN EXPECT COUNT that define in registers. Then, the F75334DG will adjust PWMOUT duty-cycle to meet the expected value. It can be said that the fan will be turned on with a specific speed set by BIOS and automatically controlled with the temperature variation. The F75334DG will take charge of all the fan speed control and need no software support.

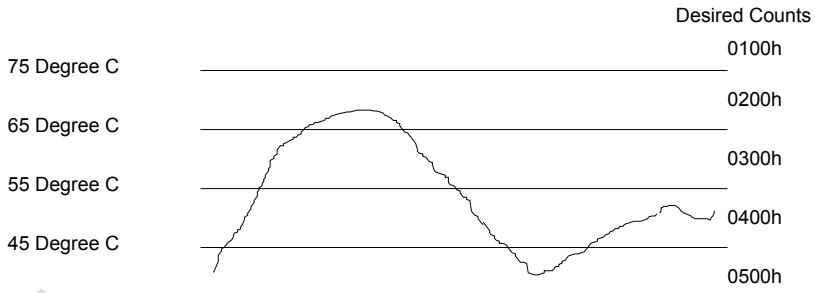


Figure 7-11

PWMOUT Duty-cycle operating process

In both “Manual RPM” and “Temperature RPM” modes, the F75334DG adjust PWMOUT duty-cycle according to current fan count and expected fan count. It will operate as follows:

(1). When expected count is 0xFFF, PWMOUT duty-cycle will be set to 0x00 to turn off fan.

(2). When expected count is 0x000, PWMOUT duty-cycle will be set to 0xFF to turn on fan with full speed.

(3). If both (1) and (2) are not true,

(4). When PWMOUT duty-cycle decrease to MIN_DUTY(≠ 00h), obviously the duty-cycle will decrease to 00h next, the F75334DG will keep duty-cycle at 00h for 1.6 seconds. After that, the F75334DG starts to compare current fan count and expected count in order to increase or decrease its duty-cycle. This ensures that if there is any glitch during the period, the F75334DG will ignore it.

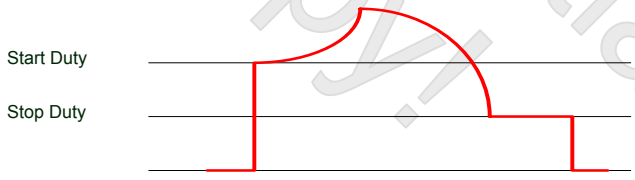


Fig 7-12

FAN_FAULT#

Fan_Fault# will be asserted when the fan speed doesn’t meet the expected fan speed within a programmable period (default is 11 seconds) or when fan stops with respect to PWM duty-cycle which should be able to turn on the fan. There are two conditions may cause the FAN_FAULT# event.

(1). When PWM_Duty reaches 0xFF, the fan speed count can’t reach the fan expected

count in time. (Figure 7-13)

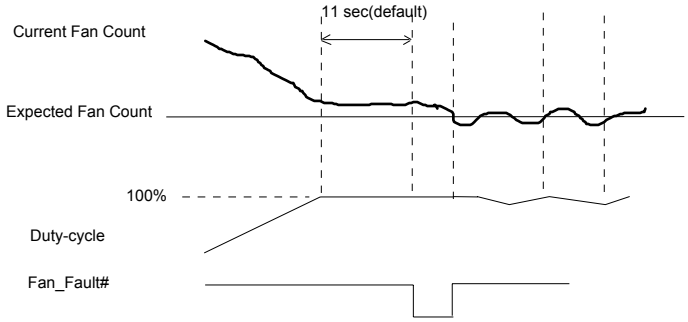


Fig 7-13

(2). After the period of detecting fan full speed, when PWM_Duty > Min. Duty, and fan count still in 0xFFF.

7.2 Loading Gauge

F75334DG support 16 bit PWM duty reading value and four duty limits (12 bits) for auto control system performance.

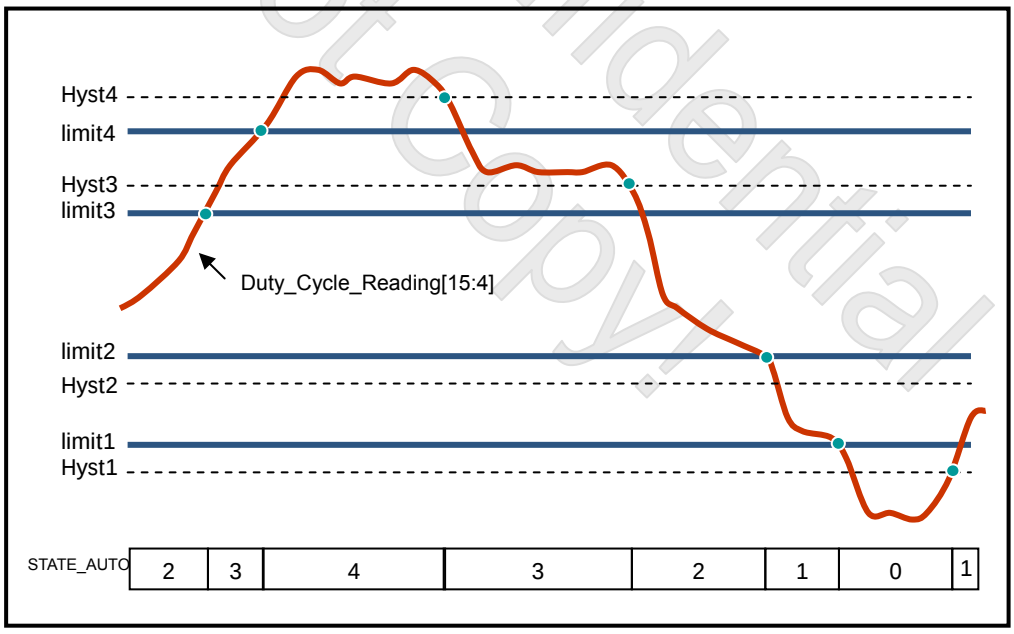


Fig 7-14

F75334DG support three turbo# pin to over or under clocking, when F7334DG detect CPU loading it will output relative turbo# value that define in internal register. (Fig 7-15)

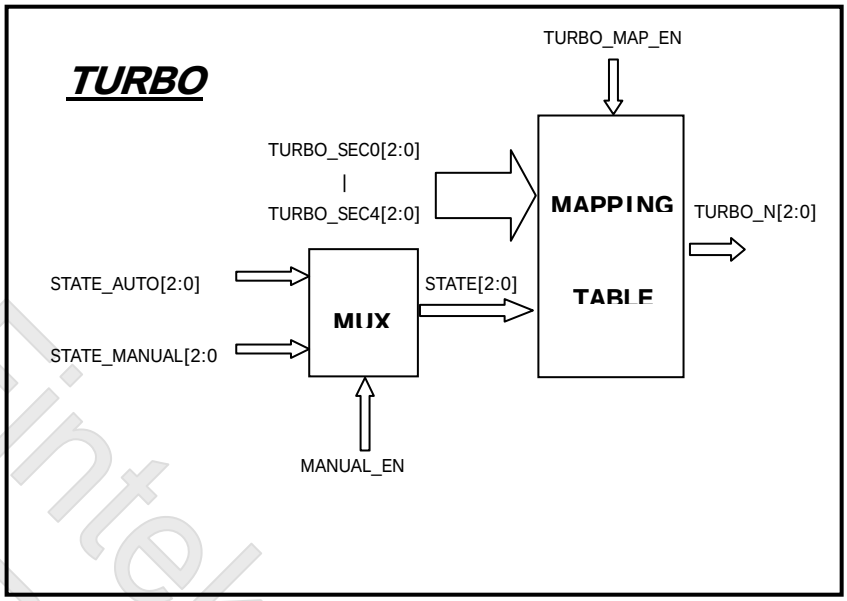


Fig 7-15

When under clocking F75334DG will decrease system frequency after 20ms it start to change VID value to deduce CPU Vcore voltage, In order to prevent chipset fail during frequency change, F75334DG use STOP# signal to disable chipset temporarily.

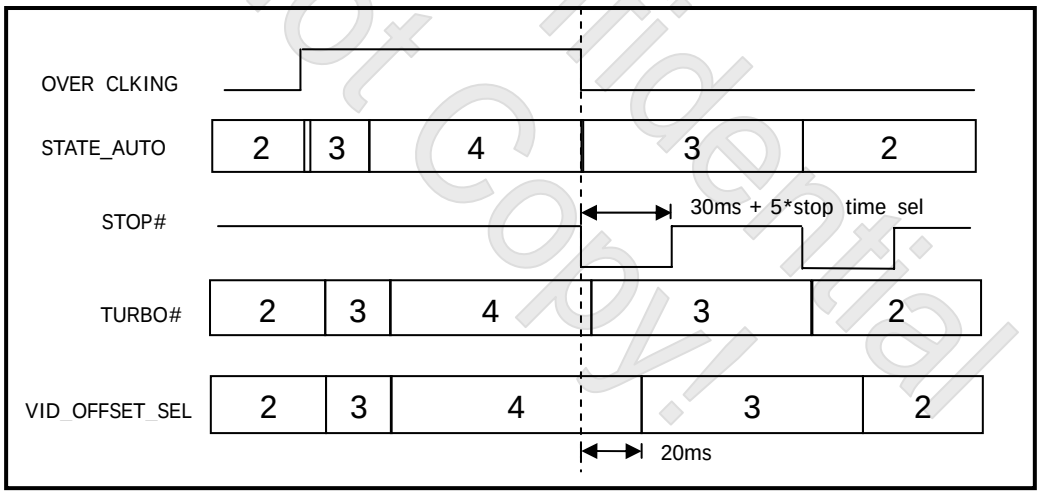


Fig 7-16

7.3 VID on the fly control

1. Support VRM9.0, VRM10.0, VRM10 extend and VRM11.0
2. Support 5 offset registers to mapping 5 different loading (PWM duty) ranges.

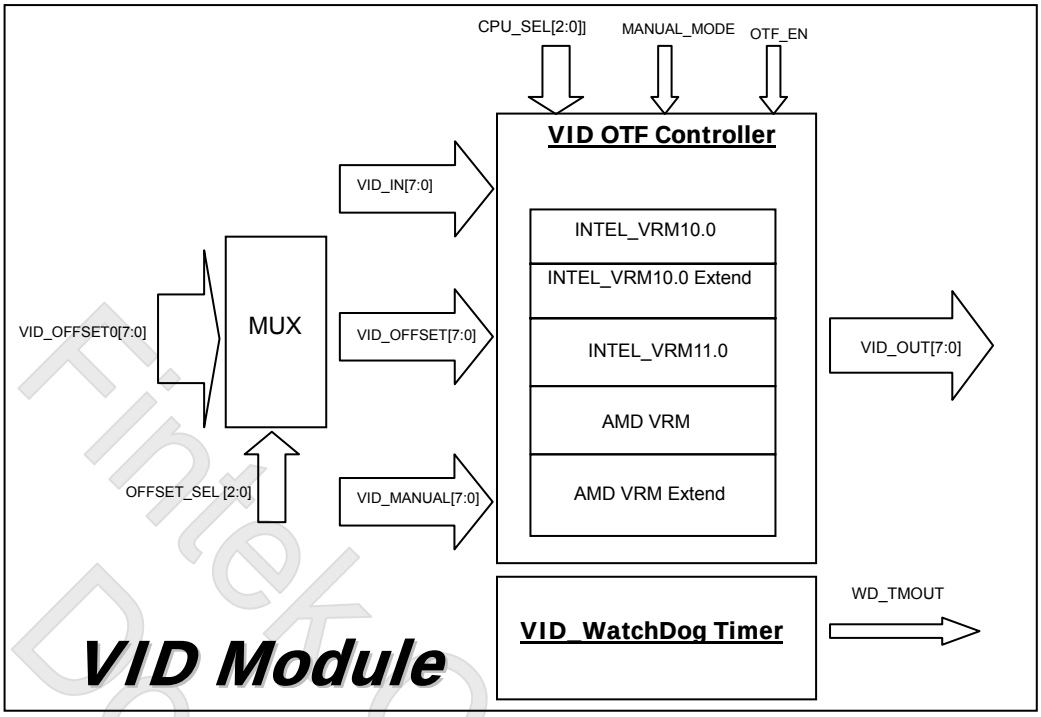


Fig 7-17

7.4 Other

BEEP

BEEP pin is power by standby power; it will be alerted by two conditions 1. over temperature shutdown. 2. over loading shutdown.

When enable over temperature shutdown function and the OVT# event turn-off the system power VCC then BEEP will output 833Hz/416Hz clock (Fig 7-18)

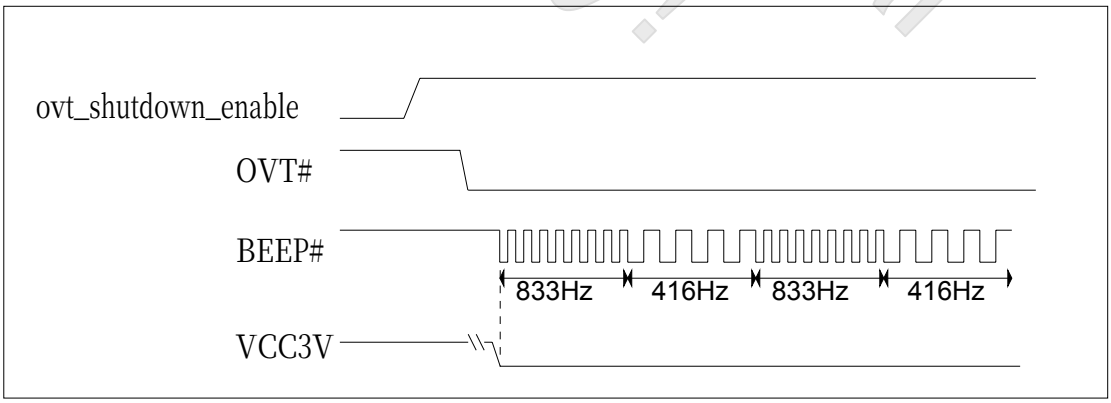


Fig 7-18

When enable over loading shutdown function and the TURBO2# event turn-off the

system power VCC then BEEP will output 833Hz/416Hz clock (Fig 7-19)

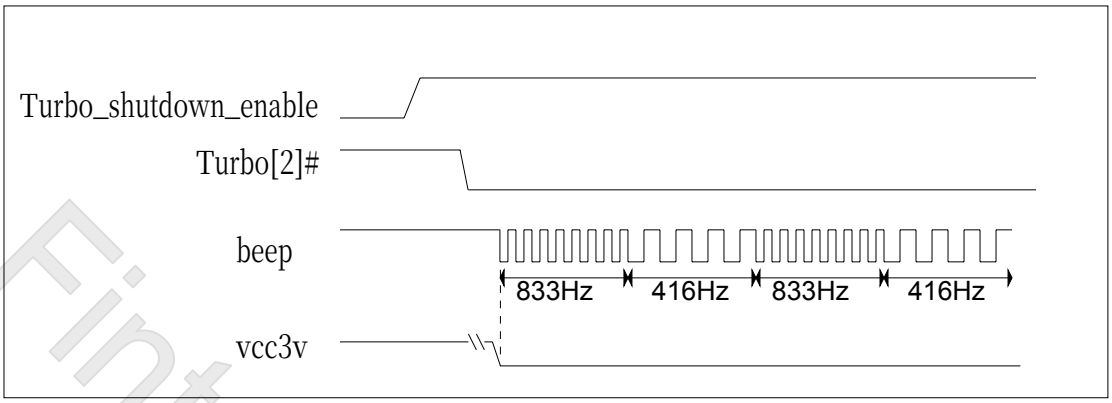


Fig 7-19

LED

When normal operation LED pin will output relative frequency for different CPU/GPU loading (Fig 7-20),

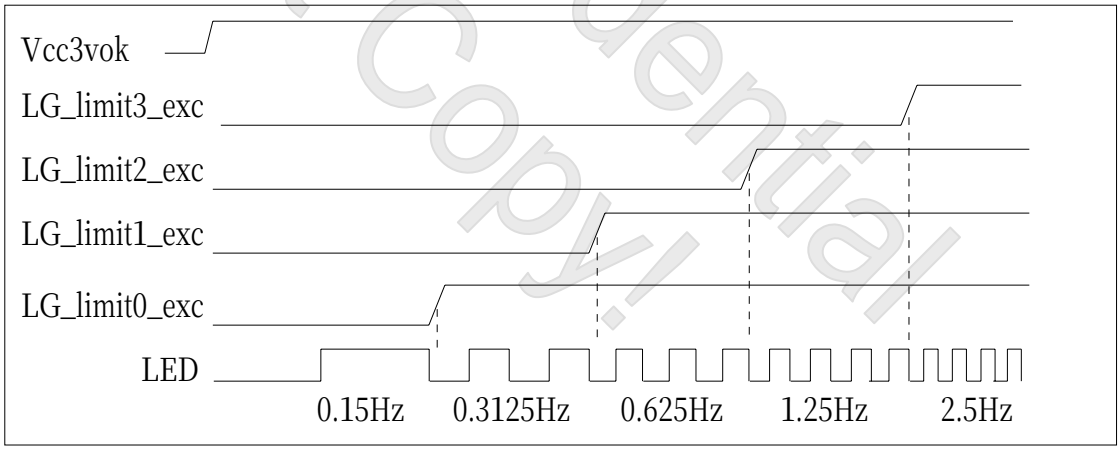


Fig 7-20

But if over temperature shutdown function is enabled and after the system power turn-off then the LED pin will output 0.625Hz clock(Fig 7-21),

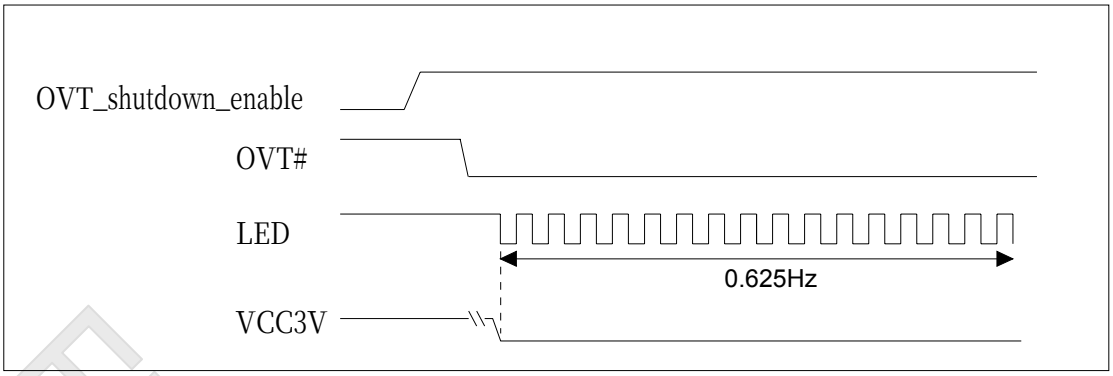


Fig 7-21

If over loading shutdown function is enabled then after the system power shutdown then the LED pin will output 0.312Hz clock(Fig 7-22),

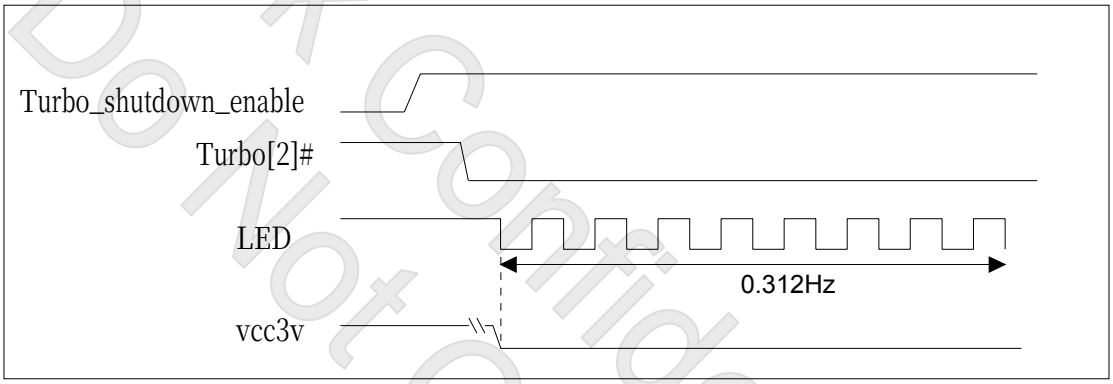


Fig 7-22

8. Register Description

8.1 Global Registers

8.1.1 Configuration Register — Index 00h

Bit	Name	R/W	Default	Description
7	SOFT_RST	R/W	0	Set 1 to reset whole chip.
6	POWR_DOWN	R/W	0	Set 1 to power down whole chip.
5-3	Reserved	R	0h	Reserved/
0	DEVICE_SEL	R/W	3h	Device select: 2'b00: Select to hardware monitor module. 2'b01: Select to loading gauge module. 2'b10: Select to VID control module. 2'b11: Select to global function.

8.1.2 Global function Configuration Register — Index 01h

Bit	Name	R/W	Default	Description
7	ARA_EN	R/W	0	Enable ARA mode, when F75334DG receive ARA command will auto clear GLOBAL_PME_EN bit (CR01 bit 4)
6	PME_POLARITY	R/W	0	0: PME event will be low active. 1: PME event will be high active.
5	PME_MODE	R/W	0	0: pulse mode (pulse width 120us) 1: level mode.
4	GLOBAL_PME_EN	R/W	1	Set 1 to enable PME event output function, if clear to 0 the PME output function will be disable. When ARA mode is enabled and F75334DG receive an ARA command then this bit will be auto clear.
3-0	Reserved	--	0h	Reserved

8.1.3 Global PME Status Register — Index 02h

Bit	Name	R/W	Default	Description
7-4	Reserved	--	0h	--
3	LG_PME	R	0	Loading gauge events are asserted. After users clear Loading gauge PME status, this bit will return to 0.
2	FAN_PME	R	0	Hardware monitor fan events are asserted. After users clear hardware monitor fan PME status, this bit will return to 0.
1	VOLTAGE_PME	R	0	Hardware monitor voltage events are asserted. After users clear hardware monitor voltage PME status, this bit will return to 0.
0	TEMP_PME	R	0	Hardware monitor temperature events are asserted. After users clear hardware monitor temperature PME status, this bit will return to 0.

8.1.4 Global PME Status Register — Index 03h (Power by VSB3V)

Bit	Name	R/W	Default	Description
7-6	Reserved	--	0h	--

5	Reserved	R/W	0h	Dummy register.
4	OVT_DISTURBO_EN	R/W	0	Enable internal over temperature (OVT) event or OVT# pin input to disable turbo function.
3	TURBO_SHUTDOWN_EN	R/W	0	Loading gauge events are asserted. After users clear Loading gauge PME status this bit will return to 0.
2	OVT_SHUTDOWN_EN	R/W	0	Hardware monitor fan events are asserted. After users clear hardware monitor fan PME status this bit will return to 0.
1	TURBO_SHUTDOWN	R	0	Hardware monitor voltage events are asserted. After users clear hardware monitor voltage PME status this bit will return to 0.
0	OVT_SHUTDOWN	R	0	Hardware monitor temperature events are asserted. After users clear hardware monitor temperature PME status this bit will return to 0.

8.1.5 GPIO1 Pin Function Select Register — Index 04h (Power by VSB3V)

Bit	Name	R/W	Default	Description
7-5	Reserved	--	0	Reserved
4	GPIO14_EN	R/W	1	1: Pin 14 will be GPIO14. 0: Pin 14 will use as TURBO2# function.
3	GPIO13_EN	R/W	1	1: Pin 13 will be GPIO13. 0: Pin 13 will use as FAN_FAULT# function.
2	GPIO12_EN	R/W	1	1: Pin 12 will be GPIO12. 0: Pin 12 will use as PME# function.
1	GPIO11_EN	R/W	1	1: Pin 11 will be GPIO11. 0: Pin 11 will use as BEEP function. **User must disable over_voltage_en bit in VID bank CR0C before use this function.**
0	GPIO10_EN	R/W	1	1: Pin 10 will be GPIO10 0: Pin 10 will use as LED function **User must disable over_voltage_en bit in VID bank CR0C before use this function.**

8.1.6 GPIO2/GPIO3 Pin Function Select Register

These function select registers please refer VID bank registers.

8.1.7 GPIO4 Pin Function Select Register — Index 07h

Bit	Name	R/W	Default	Description
7-4	Reserved	--	0h	--
3	GPIO43_EN	R/W	0	1: pin 43 will be GPIO43. 0: Pin 43 will use as FAN_CTRL3 function.
2	GPIO42_EN	R/W	0	1: pin 42 will be GPIO42. 0: Pin 42 will use as FAN_IN3 function.
1	GPIO41_EN	R/W	0	1: pin 29 will be GPIO41. 0: Pin 29 will use as STOP# function.
0	GPIO40_EN	R/W	0	1: pin 28 will be GPIO40. 0: Pin 28 will use as TURBO1# function.

8.1.8 GPIO1X Output Data Register — Index 10h (Power by VSB3V)

Bit	Name	R/W	Default	Description
7-5	Reserved	--	0h	--
4-0	GPIO1X_DATA	R/W	0h	GPIO14~GPIO10 output data, when output function was enable, the data set in these registers will be output.

8.1.9 GPIO1X Output Data Enable Register — Index 11h (Power by VSB3V)

Bit	Name	R/W	Default	Description
7-5	Reserved	--	0h	--
4-0	GPIO1X_OUT_EN	R/W	0h	GPIO14~GPIO10 output control pins, when set to 1 the relative pin output function will be enable.

8.1.10 GPIO1X Output Mode Select Register — Index 12h (Power by VSB3V)

Bit	Name	R/W	Default	Description
7-5	Reserved	--	0h	--
4-0	GPIO1X_O_MODE	R/W	0h	0: for open drain 1: for push pull

8.1.11 GPIO1X Pin Status Register — Index 13h (Power by VSB3V)

Bit	Name	R/W	Default	Description
7-5	Reserved	--	0h	--
4-0	GPIO1_PIN_ST	R	--	These registers are read only, they reflect the relative pin real status

8.1.12 GPIO2X Output Data Register — Index 14h (Power by VSB3V)

Bit	Name	R/W	Default	Description
7-6	Reserved	--	0h	--
5-0	GPIO2X_DATA	R/W	0h	GPIO25~GPIO20 output data, when output function was enable, the data set in these registers will be output.

8.1.13 GPIO2X Output Data Enable Register — Index 15h (Power by VSB3V)

Bit	Name	R/W	Default	Description
7-6	Reserved	--	0h	--
5-0	GPIO2X_OUT_EN	R/W	0h	GPIO25~GPIO20 output control pins, when set to 1 the relative pin output function will be enable.

8.1.14 GPIO2X Output Mode Select Register — Index 16h (Power by VSB3V)

Bit	Name	R/W	Default	Description
7-6	Reserved	--	0h	--
5-0	GPIO2X_O_MODE	R/W	0h	0: for open drain 1: for push pull

8.1.15 GPIO2X Pin Status Register — Index 17h (Power by VSB3V)

Bit	Name	R/W	Default	Description
7-6	Reserved	--	0h	--

5-0	GPIO2_PIN_ST	R	--	These registers are read only, they reflect the relative pin real status

8.1.16 GPIO3X Output Data Register — Index 18h (Power by VSB3V)

Bit	Name	R/W	Default	Description
7-6	Reserved	--	0h	--
5-0	GPIO3X_DATA	R/W	0h	GPIO35~GPIO30 output data, when output function was enable, the data set in these registers will be output.

8.1.17 GPIO3X Output Data Enable Register — Index 19h (Power by VSB3V)

Bit	Name	R/W	Default	Description
7-6	Reserved	--	0h	--
5-0	GPIO3X_OUT_EN	R/W	0h	GPIO35~GPIO30 output control pins, when set to 1 the relative pin output function will be enable.

8.1.18 GPIO3X Output Mode Select Register — Index 1Ah (Power by VSB3V)

Bit	Name	R/W	Default	Description
7-6	Reserved	--	0h	--
5-0	GPIO3X_O_MODE	R/W	0h	0: for open drain 1: for push pull

8.1.19 GPIO3X Pin Status Register — Index 1Bh (Power by VSB3V)

Bit	Name	R/W	Default	Description
7-6	Reserved	--	0h	--
5-0	GPIO3_PIN_ST	R	--	These registers are read only, they reflect the relative pin real status

8.1.20 OVT and Fan_Fault Pin Select Register — Index 1Ch (Power by VSB3V)

Bit	Name	R/W	Default	Description
7-2	Reserved	--	0h	--
1-0	Pin_Select	R/W	01b	00: Disable function output 01: Pin7 will be a OVT function pin 10: Pin7 will be a Fan_Fault function pin 11: Pin7 will be a OVT + Fan_Fault functions pin

8.1.21 GPIO4X Output Data Register — Index 20h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	--
3-0	GPIO4_DATA	R/W	0	GPIO43~GPIO40 output control pins, when set to 1 the relative pin output function will be enable.

8.1.22 GPIO4X Output Data Enable Register — Index 21h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	--
3-0	GPIO4_OUT_EN	R/W	0	GPIO43~GPIO40 output control pins, when set to 1 the relative pin output function will be enable.

8.1.23 GPIO4X Output Mode Select Register — Index 22h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	--
3-0	GPIO4_OUT_MODE	R/W	0	0: for open drain 1: for push pull

8.1.24 GPIO4X Pin Status Register — Index 23h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	--
3-0	GPIO4_PIN_ST	R	--	These registers are read only, they reflect the relative pin real status

8.1.25 CHIPID(1) Register – Index 5Ah

Bit	Name	R/W	Default	Description
7-0	CHIPID	RO	04h	Chip ID, High byte (8'h04).

8.1.26 CHIPID(2) Register – Index 5Bh

Bit	Name	R/W	Default	Description
7-0	CHIPID	RO	14h	Chip ID, Low byte (8'h14).

8.1.27 VENDOR ID(1) Register – Index 5Dh

Bit	Name	R/W	Default	Description
7-0	VENDOR1	R/W	19h	Vendor ID, high byte (8'h19)

8.1.28 VENDOR ID(2) Register – Index 5Eh

Bit	Name	R/W	Default	Description
7-0	VENDOR2	RO	34h	Vendor ID, low byte (8'h34)

8.2 Hardware Monitor Registers

8.2.1 Configuration Register — Index 01h

Bit	Name	R/W	Default	Description
7-3	Reserved	0h	0	Reserved
2	POWER_DOWN	R/W	0	Hardware monitor function power down.
1	FAN_START	R/W	1	et one to enable startup of fan monitoring operations; a zero puts the part in standby mode.
0	V_T_START	R/W	1	Set one to enable startup of temperature and voltage monitoring operations; a zero puts the part in standby mode.

8.2.2 Configuration Register — Index 02h

Bit	Name	R/W	Default	Description
7-6	Reserved	R/W	0	Dummy registeres.
5-4	OVT_MODE	R/W	0	00: The OVT# will be low active level mode. 01: The OVT# will be high active level mode. 10: The OVT# will indicate by 1Hz LED function. 11: The OVT# will indicate by (400/800HZ) BEEP output.
3-2	Reserved	R/W	0	Dummy registers.
1-0	F_FAULT_MODE	R/W	0	00: The fan fault will be low active level mode. 01: The fan fault will be high active level mode. 10: The fan fault will indicate by 1Hz LED function. 11: The fan fault will indicate by (400/800HZ) BEEP output.

8.2.3 PECI SST AMDSI Interface Configuration Register — Index 0Ah

Bit	Name	R/W	Default	Description
7-6	Reserved	R/W	0	Reserved.
5	T1_IIR_EN	R/W	1	Set 1 to enable the IIR for AMDSI/PECI reading.
4	SST_EN	R/W	0	Enable SST Interface.
3-2	PECI_POWER_SEL	R/W	00	00: PECI output high level will be 1.23V 01: PECI output high level will be 1.13V 10: PECI output high level will be 1.00V 11: PECI output high level will be 1.00V
1-0	MEAS_TYPE	R/W	0	Select the CPU temperature measure method 00: External thermal diode. 01: PECI interface. 10: AMDSI interface. 11: Reserved.

8.2.4 AMDSI Version Register — Index 0Bh (MEAS_TYPE ==2'b10)

Bit	Name	R/W	Default	Description
7-0	AMDSI_VER	R	-	When AMDSI interface enable, this will be AMDSI version register. Return the AMDSI version.

8.2.5 Dual Single Core select Register — Index 0Bh (MEAS_TYPE ==2'b01)

Bit	Name	R/W	Default	Description
7-1	Reserved	R	-	Reserved

0	DualCore_EN	R/W	0	When PECI interface enable, this will be Dual Single Core select register. 0: Single Core CPU selection 1: Dual Core CPU selection

8.2.6 TCC Activation Temperature Register — Index 0Ch (MEAS_TYPE == 2'b01)

Bit	Name	R/W	Default	Description
7-0	TCC_TEMP	R/W	0	TCC Activation Temperature. The absolute value of CPU temperature is calculated by the equation: CPU_TEMP = TCC_TEMP + PECI Reading. The range of this register is 0 ~ 255.

8.2.7 AMDSI Node ID Register — Index 0Ch (MEAS_TYPE ==2'b10)

Bit	Name	R/W	Default	Description
7-0	NODE_ID	R	-	Return the AMDSI node id.

8.2.8 SST Address Register — Index 0Dh

Bit	Name	R/W	Default	Description
7-0	SST_ADDR	R/W	8'h4C	Address for SST interface. Programmable.

8.2.9 CPU Temp. Measure Select Register — Index 0Eh

Bit	Name	R/W	Default	Description
7-4	Reserved	-	0	Reserved.
3	ADD	R/W	0	Temperature scale selection. 1: Temp. Measure = Reading Value + Reading Value* $2^{-Scale[2:0]}$ 0: Temp. Measure = Reading Value - Reading Value* $2^{-Scale[2:0]}$
2-0	SCALE[2:0]	R/W	000	When ADD=1, the Temp. Measure is 000: 1 * Reading Value 001: 3/2 * Reading Value …….. 110: 65/64 * Reading Value 111: 129/128 * Reading Value ---------- When ADD=0, the Temp. Measure is 000: 1 * Reading Value 001: 1/2 * Reading Value …….. 110: 63/64 * Reading Value 111: 127/128 * Reading Value

8.2.10 Voltage PME# Enable Register — Index 10h

Bit	Name	R/W	Default	Description
7-6	Reserved	--	0	Reserved
5	EN_VSB3V_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt
4	EN_V4_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt
3	EN_V3_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt
2	EN_V2_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt.
1	EN_V1_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt
0	EN_VCC3V_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt.

8.2.11 Voltage Interrupt Status Register — Index 11h

Bit	Name	R/W	Default	Description
7-6	Reserved	--	0	Reserved
5	VSB3V_EXC_STS	R/W	0	This bit is set when the VSB3V is over the high limit or under the low limit. Write 1 to clear this bit, write 0 will be ignored.
4	V4_ EXC _STS	R/W	0	This bit is set when the VIN3 is over the high limit or under the low limit. Write 1 to clear this bit, write 0 will be ignored.
3	V3_ EXC _STS	R/W	0	This bit is set when the VIN3 is over the high limit or under the low limit. Write 1 to clear this bit, write 0 will be ignored.
2	V2_ EXC _STS	R/W	0	This bit is set when the VIN2 is over the high limit or under the low limit. Write 1 to clear this bit, write 0 will be ignored.
1	V1_ EXC _STS	R/W	0	This bit is set when the VIN1 is over the high limit or under the low limit. Write 1 to clear this bit, write 0 will be ignored.
0	VCC3V_ EXC _STS	R/W	0	This bit is set when the VCC is over the high limit or under the low limit. Write 1 to clear this bit, write 0 will be ignored.

8.2.12 Voltage Exceeds Real Time Status Register 1 — Index 12h

Bit	Name	R/W	Default	Description
7-4	Reserved	--	0	Reserved
6	VSB3V_EXC	RO	0	A one indicates VSB3V exceeds the high or low limit. A zero indicates VSB3V is in the safe region.
5	V4_EXC	RO	0	A one indicates VIN4 exceeds the high or low limit. A zero indicates VIN4 is in the safe region.
3	V3_4EXC	RO	0	A one indicates VIN3 exceeds the high or low limit. A zero indicates VIN3 is in the safe region.
2	V2_EXC	RO	0	A one indicates VIN2 exceeds the high or low limit. A zero indicates VIN2 is in the safe region.
1	V1_EXC	RO	0	A one indicates VIN1 exceeds the high or low limit. A zero indicates VIN1 is in the safe region.
0	VCC3V_EXC	RO	0	A one indicates VCC exceeds the high or low limit. A zero indicates VCC is in the safe region.

8.2.13 Voltage Mode select Register — Index 13h

Bit	Name	R/W	Default	Description
7-5	Reserved	--	0	Reserved
4	V4_LOW_V	R/W	0	Extend voltage 4 reading to 16 bit.
3	V3_LOW_V	R/W	0	Extend voltage 3 reading to 16 bit.
2-0	Reserved	--	0	

8.2.14 Voltage reading and limit— Index 20h- 4Fh

Address	Attribute	Default Value	Description
20h	RO	--	VCC3V reading. The unit of reading is 8mV.
21h	RO	--	V1 reading. The unit of reading is 8mV.
22h	RO	--	V2 reading. The unit of reading is 8mV.
23h	RO	--	V3 reading (MSB). The unit of reading is 8mV.
24h	RO	--	V4 reading (MSB). The unit of reading is 8mV.
25h	RO	--	VSB3V reading. The unit of reading is 8mV.

26~2Fh	RO	FF	Reserved
30h	R/W	FFh	VCC3V High Limit. The unit is 8mV. The last LSB bit is fixed to 1'b1.
31h	R/W	00h	VCC3V Low Limit. The unit is 8mV. The last LSB bit is fixed to 1'b0.
32h	R/W	FFh	V1 High Limit. The unit is 8mV. The last LSB bit is fixed to 1'b1.
33h	R/W	00h	V1 Low Limit. The unit is 8mV. The last LSB bit is fixed to 1'b0.
34h	R/W	FFh	V2 High Limit. The unit is 8mV. The last LSB bit is fixed to 1'b1.
35h	R/W	00h	V2 Low Limit. The unit is 8mV. The last LSB bit is fixed to 1'b0.
36h	R/W	FFh	V3 High Limit. The unit is 8mV. The last LSB bit is fixed to 1'b1.
37h	R/W	00h	V3 Low Limit. The unit is 8mV. The last LSB bit is fixed to 1'b0.
38h	R/W	FFh	V4 High Limit. The unit is 8mV. The last LSB bit is fixed to 1'b1.
39h	R/W	00h	V4 Low Limit. The unit is 8mV. The last LSB bit is fixed to 1'b0.
3Ah	R/W	FFh	VSB3V High Limit. The unit is 8mV. The last LSB bit is fixed to 1'b1.
3Bh	R/W	00h	VSB3V Low Limit. The unit is 8mV. The last LSB bit is fixed to 1'b0.

8.2.15 Temperature PME# Enable Register — Index 60h

Bit	Name	R/W	Default	Description
7	EN_ T3_OVT_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt
6	EN_ T2_ OVT_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt.
5	EN_ T1_ OVT_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt
4	EN_ L_ OVT_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt.
3	EN_ T3_EXC_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt
2	EN_ T2_EXC_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt.
1	EN_ T1_EXC_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt
0	EN_L_EXC_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt.

8.2.16 Temperature Interrupt Status Register — Index 61h

Bit	Name	R/W	Default	Description
7	T3_OVT_STS	R/W	0	A one indicates TEMP3 temperature sensor has exceeded OVT limit or below the "OVT limit –hysteresis". Write 1 to clear this bit, write 0 will be ignored.
6	T2_OVT _STS	R/W	0	A one indicates TEMP2 temperature sensor has exceeded OVT limit or below the "OVT limit –hysteresis". Write 1 to clear this bit, write 0 will be ignored.
5	T1_OVT _STS	R/W	0	A one indicates TEMP1 temperature sensor has exceeded OVT limit or below the "OVT limit –hysteresis". Write 1 to clear this bit, write 0 will be ignored.
4	LOCAL_OVT _STS	R/W	0	A one indicates temperature sensor (local temperature) has exceeded the OVT limit or below the "OVT limit –hysteresis". Write 1 to clear this bit, write 0 will be ignored.
3	T3_EXC _STS	R/W	0	A one indicates TEMP3 temperature sensor has exceeded high limit or below the "high limit –hysteresis". Write 1 to clear this bit, write 0 will be ignored.
2	T2_EXC _STS	R/W	0	A one indicates TEMP2 temperature sensor has exceeded high limit or below the "high limit –hysteresis" limit. Write 1 to clear this bit, write 0 will be ignored.
1	T1_EXC _STS	R/W	0	A one indicates TEMP1 temperature sensor has exceeded high limit or below the "high limit –hysteresis" limit. Write 1 to clear this bit, write 0 will be ignored.

0	LOCAL_EXC _STS	R/W	0	A one indicates temperature sensor (local temperature) has exceeded the high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 will be ignored.

8.2.17 Temperature Real Time Status Register — Index 62h

Bit	Name	R/W	Default	Description
7	T3_OVT	R/W	0	Set when the TEMP3 exceeds the OVT limit. Clear when the TEMP3 is below the “OVT limit –hysteresis” temperature.
6	T2_OVT	R/W	0	Set when the TEMP2 exceeds the OVT limit. Clear when the TEMP2 is below the “OVT limit –hysteresis” temperature.
5	T1_OVT	R/W	0	Set when the TEMP1 exceeds the OVT limit. Clear when the TEMP1 is below the “OVT limit –hysteresis” temperature.
4	LOCAL_OVT	R/W	0	Set when the local temperature exceeds the OVT limit. Clear when the local temperature is below the “OVT limit –hysteresis” temperature.
3	T3_EXC	R/W	0	Set when the TEMP3 exceeds the high limit. Clear when the TEMP3 is below the “high limit –hysteresis” temperature.
2	T2_EXC	R/W	0	Set when the TEMP2 exceeds the high limit. Clear when the TEMP2 is below the “high limit –hysteresis” temperature.
1	T1_EXC	R/W	0	Set when the TEMP1 exceeds the high limit. Clear when the TEMP1 is below the “high limit –hysteresis” temperature.
0	LOCAL_EXC	R/W	0	Set when the local temperature exceeds the high limit. Clear when the local temperature is below the “high limit –hysteresis” temperature.

8.2.18 OVT Output Enable Register 1 — Index 66h

Bit	Name	R/W	Default	Description
7-6	Reserved	R	0h	--
5	Reserved	R	0	Reserved
4	Reserved	R	0	Reserved
3	EN_T3_OVT	R/W	0	Enable over temperature mechanism of temperature3.
2	EN_T2_OVT	R/W	0	Enable over temperature mechanism of temperature2.
1	EN_T1_OVT	R/W	1	Enable over temperature mechanism of temperature1.
0	EN_LOCAL_OVT	R/W	0	Enable over temperature mechanism of local temperature..

8.2.19 Temperature Sensor Type Register — Index 6Bh

Bit	Name	R/W	Default	Description
7-6	Reserved	RO	0	--
5	Reserved	RO	0	Reserved
4	Reserved	RO	0	Reserved
3	T3_MODE	R/W	1	0: TEMP3 is connected to a thermistor 1: TEMP3 is connected to a BJT.(default)
2	T2_MODE	R/W	1	0: TEMP2 is connected to a thermistor. 1: TEMP2 is connected to a BJT. (default)
1	T1_MODE	R/W	1	0: TEMP1 is connected to a thermistor 1: TEMP1 is connected to a BJT.(default)
0	LOCAL_T_MODE	RO	1	1: local is connected to a BJT.

8.2.20 LOCAL and TEMP1 Limit Hystersis Select Register -- Index 6Ch

Bit	Name	R/W	Default	Description
7-4	TEMP1_HYS	R/W	4h	TEMP1 will exceeds when over limit until under then “limit - TEMP1_HYS (hystersis)”
3-0	LOCAL_HYS	R/W	2h	L TEMP will exceeds when over limit until under then “limit – L TEMP_HYS (hystersis)”

8.2.21 TEMP2 and TEMP3 Limit Hystersis Select Register -- Index 6Dh

Bit	Name	R/W	Default	Description
7-4	TEMP3_HYS	R/W	2h	TEMP3 will exceeds when over limit until under then “limit - TEMP1_HYS (hystersis)”
3-0	TEMP2_HYS	R/W	4h	TEMP 2 will exceeds when over limit until under then “limit – L TEMP_HYS (hystersis)”

8.2.22 DIODE OPEN Status Register -- Index 6Fh

Bit	Name	R/W	Default	Description
7-6	Reserved	RO	0h	Reserved
5	Reserved	RO	0h	Reserved
4	Reserved	RO	0h	Reserved
3	T3_DIODE_OPEN	RO	0h	External diode 3 is open or short
2	T2_DIODE_OPEN	RO	0h	External diode 2 is open or short
1	T1_DIODE_OPEN	RO	0h	External diode 1 is open or short
0	T0_DIODE_OPEN	RO	0h	Internal diode 0 is open or short

8.2.23 Temperature — Index 70h- 8Fh

Address	Attribute	Default Value	Description
70h	RO	--	Local temperature[10:3] reading. The unit of reading is 1°C.At the moment of reading this register. (when open or short this byte will return 0)
71h	RO	--	CR71 bit7-bit5 are the Local temperature reading value[2:0]. The unit of reading is 0.125°C. CR71 bit 0 is the sign bit of the Local temperature. (when open or short this byte will return 1, “sign bit set to 1”)
72h	RO	--	Temperature 1 reading. The unit of reading is 1°C.At the moment of reading this register.
73h	RO	--	CR73 bit7-bit5 are the temperature 1 reading value[2:0]. The unit of reading is 0.125°C. CR73 bit 0 is the sign bit of the temperature 1. (when open or short this byte will return 1, “sign bit set to 1”)
74h	RO	--	Temperature 2 reading. The unit of reading is 1°C.At the moment of reading this register.
75h	RO	--	CR75 bit7-bit5 are the temperature 2 reading value[2:0]. The unit of reading is 0.125°C. CR75 bit 0 is the sign bit of the temperature 2. (when open or short this byte will return 1, “sign bit set to 1”)
76h	RO	--	Temperature 3 reading. The unit of reading is 1°C.At the moment of reading this register.
77h	RO	--	CR77 bit7-bit5 are the temperature 3 reading value[2:0]. The unit of reading is

			0.125°C. CR77 bit 0 is the sign bit of the temperature 3. (when open or short this byte will return 1, “sign bit set to 1”)
78h	RO	--	Reserved
79h	RO	--	Reserved
7Ah	RO	--	Reserved
7Bh	RO	--	Reserved
7C-7Fh	RO	FFh	Reserved
80h	R/W	46h	Local Temperature sensor OVT limit. The unit is 1°C.
81h	R/W	3Ch	Local Temperature sensor high limit. The unit is 1°C.
82h	R/W	64h	Temperature sensor 1 OVT limit. The unit is 1°C.
83h	R/W	55h	Temperature sensor 1 high limit. The unit is 1°C.
84h	R/W	64h	Temperature sensor 2 OVT limit. The unit is 1°C.
85h	R/W	55h	Temperature sensor 2 high limit. The unit is 1°C.
86h	R/W	55h	Temperature sensor 3 OVT limit. The unit is 1°C.
87h	R/W	46h	Temperature sensor 3 high limit. The unit is 1°C.
88h	RO	--	Reserved
89h	RO	--	Reserved
8Ah	RO	--	Reserved
8Bh	RO	--	Reserved
8C~8Dh	RO	FFH	Reserved

8.2.24 Temperature Filter Select Register -- Index 8Eh

Bit	Name	R/W	Default	Description
7-6	IIR-QUEUR3	R/W	1h	The queue time for second filter to quickly update values. 00: 8 times. 01: 16 times (default). 10: 24 times. 11: 32 times.
5-4	IIR-QUEUR2	R/W	1h	The queue time for second filter to quickly update values. 00: 8 times. 01: 16 times (default). 10: 24 times. 11: 32 times.
3-2	IIR-QUEUR1	R/W	1h	The queue time for second filter to quickly update values. 00: 8 times. 01: 16 times (default). 10: 24 times. 11: 32 times.
1-0	IIR-QUEUR-LOCAL	R/W	1h	The queue time for second filter to quickly update values. 00: 8 times. 01: 16 times (default). 10: 24 times. 11: 32 times.

8.2.25 FAN PME# Enable Register — Index 90h

Bit	Name	R/W	Default	Description
7-6	Reserved	RO	0h	Reserved
5	Reserved	RO	0h	Reserved
4	Reserved	RO	0h	Reserved
3	Reserved	RO	0h	Reserved

2	EN_FAN3_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt.
1	EN_FAN2_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt
0	EN_FAN1_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt.

8.2.26 FAN Interrupt Status Register — Index 91h

Bit	Name	R/W	Default	Description
7-6	Reserved	RO	0h	Reserved
5	Reserved	RO	0h	Reserved
4	Reserved	RO	0h	Reserved
3	Reserved	RO	0h	Reserved
2	FAN3_STS	R/W	--	This bit is set when the fan3 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
1	FAN2_STS	R/W	--	This bit is set when the fan2 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
0	FAN1_STS	R/W	--	This bit is set when the fan1 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.

8.2.27 FAN Real Time Status Register — Index 92h

Bit	Name	R/W	Default	Description
7-6	Reserved	--	0h	Reserved
5	Reserved	RO	0h	Reserved
4	Reserved	RO	0h	Reserved
3	Reserved	RO	0h	Reserved
2	FAN3_EXC	RO	--	This bit set to high mean that fan3 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.
1	FAN2_EXC	RO	--	This bit set to high mean that fan2 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.
0	FAN1_EXC	RO	--	This bit set to high mean that fan1 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.

8.2.28 FAN FAULT# Enable Register — Index 93h

Bit	Name	R/W	Default	Description
7	FULL_WITH_T3_EN	R/W	0	Set one will enable FAN to force full speed when T3 over high limit.
6	FULL_WITH_T2_EN	R/W	0	Set one will enable FAN to force full speed when T2 over high limit.
5	FULL_WITH_T1_EN	R/W	0	Set one will enable FAN to force full speed when T1 over high limit.
4	FULL_WITH_T0_EN	R/W	0	Set one will enable FAN to force full speed when T0 (Local Temperature) over high limit.
3	Reserved	Ro	0	Reserved
2	EN_FAN3_ FAULT	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt.
1	EN_FAN2_ FAULT	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt
0	EN_FAN1_ FAULT	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt.

8.2.29 Fan Type Select Register -- Index 94h

Bit	Name	R/W	Default	Description
7-6	Reserved	R/W	2'b0S	Reserved

5-4	FAN3_TYPE	R/W	2'b 0S	00: Output PWM mode (pushpull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal . 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved.
3-2	FAN2_TYPE	R/W	2'b 0S	00: Output PWM mode (pushpull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal . 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved.
1-0	FAN1_TYPE	R/W	2'b 0S	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal . 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved.

S: Register default values are decided by trapping.

8.2.30 Fan mode Select Register -- Index 96h

Bit	Name	R/W	Default	Description
7-6	Reserved	R/W	1h	Reserved
5-4	FAN3_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that define in 0xC6-0xCE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** that define in 0xC6-0xCE. 10: Manual mode fan control, user can write expect **RPM** count to 0xC2-0xC3, and F75334 will auto control duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed. 11: Reserved
3-2	FAN2_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that define in 0xB6-0xBE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** (voltage) that define in 0xB6-0xBE. 10: Manual mode fan control, user can write expect **RPM** count to 0xB2-0xB3, and F75334 will auto control duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed. 11: Reserved
1-0	FAN1_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that define in 0xA6-0xAE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** that define in 0xA6-0xAE. 10: Manual mode fan control, user can write expect **RPM** count to 0xA2-0xA3, and F75334 will auto control duty cycle (PWM fan type) or voltage(linear fan type) to control fan speed. 11: Reserved

8.2.31 Auto Fan1 and Fan2 Boundary Hystersis Select Register -- Index 98h

Bit	Name	R/W	Default	Description
7-4	FAN2_HYS	R/W	4h	0000: Boundary hysteresis. (0~15 degree C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).
3-0	FAN1_HYS	R/W	4h	0000: Boundary hysteresis. (0~15 degree C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

8.2.32 Auto Fan3 Boundary Hystersis Select Register -- Index 99h

Bit	Name	R/W	Default	Description
7-4	Reserved S	R/W	2h	Reserved
3-0	FAN3_HYS	R/W	2h	0000: Boundary hysteresis. (0~15 degree C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

8.2.33 Fan1~Fan3 Duty Change Rate Select Register -- Index 9Bh

Bit	Name	R/W	Default	Description
7-6	Reserved	R/W	0h	Reserved
5-4	FAN3_RATE_SEL	R/W	0h	x0: Duty change per 200ms, x1: Duty change per Sec.
3-2	FAN2_RATE_SEL	R/W	0h	x0: Duty change per 200ms, x1: Duty change per Sec.
1-0	FAN1_RATE_SEL	R/W	0h	x0: Duty change per 200ms, x1: Duty change per Sec.

8.2.34 FAN1 and FAN2 START UP DUTY-CYCLE/VOLTAGE — Index 9Ch

Bit	Name	R/W	Default	Description
7-4	FAN2_MIN_DUTY	R/W	5h	When fan start, the FAN_CTRL2 will increase duty-cycle from 0 to this (value x 8) directly. And if fan speed is down, the FAN_CTRL 2 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).
3-0	FAN1_MIN_DUTY	R/W	5h	When fan start, the FAN_CTRL 1 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 1 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

8.2.35 FAN3 START UP DUTY-CYCLE/VOLTAGE — Index 9Dh

Bit	Name	R/W	Default	Description
7-4	Reserved	R/W	5h	Reserved
3-0	FAN3_MIN_DUTY	R/W	5h	When fan start, the FAN_CTRL 3 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 3 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

8.2.36 Fan Fault Time Register -- Index 9Fh

Bit	Name	R/W	Default	Description
7	Reserved	R/W	0	Reserved
6	FAN3_LD_BEFORE_EN	R/W	0	Set 1 that fan speed will keep current temp. status before system re-boot up.
5	FAN2_LD_BEFORE_EN	R/W	0	Set 1 that fan speed will keep current temp. status before system re-boot up.
4	FAN1_LD_BEFORE_EN	R/W	0	Set 1 that fan speed will keep current temp. status before system re-boot up.

3-0	F_FAULT_TIME	R/W	Ah	This register determines the time of fan fault. The condition to cause fan fault event is: When PWM_Duty reaches FFh, if the fan speed count can't reach the fan expect count in time. The unit of this register is 1 second. The default value is 11 seconds. (Set to 0 , means 1 seconds. ; Set to 1, means 2 seconds. Set to 2, means 3 seconds. ….) Another condition to cause fan fault event is fan stop and the PWM duty is greater than the minimum duty programmed by the register index 97-98h.

Fan1 Index A0h- AFh

Address	Attribute	Default Value	Description
A0h	RO	8'h0f	FAN1 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A1h	RO	8'hff	FAN1 count reading (LSB).
A2h	R/W	8'h00	**RPM mode(CR96 bit0=0):** FAN1 expect speed count value (MSB), in auto fan mode (CR96 bit1➔0) this register is auto updated by hardware. **Duty mode(CR96 bit0=1):** This byte is reserved byte.
A3h	R/W	8'h01	**RPM mode(CR96 bit0=0):** FAN1 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. **Duty mode(CR96 bit0=1):** The Value programming in this byte is duty value. In auto fan mode(CR96 bit1➔0) this register is updated by hardware. Ex: 5 ➔ 5*100/255 % 255 ➔ 100%
A4h	R/W	8'h03	FAN1 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A5h	R/W	8'hff	FAN1 full speed count reading (LSB).

8.2.37 VT1 BOUNDARY 1 TEMPERATURE – Index A6h

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Return 0 when read.
6-0	BOUND1TMP1	R/W	3Ch (60^oC)	The 1st BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is **exceed** this boundary, FAN1 expect value will load from segment **1** register (index AA)h. When VT1 temperature is **below** this boundary – hysteresis, FAN1 expect value will load from segment **2** register (index AAh).

8.2.38 VT1 BOUNDARY 2 TEMPERATURE – Index A7

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Return 0 when read.

6-0	BOUND2TMP1	R/W	32 (50°C)	The 2st BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is **exceed** this boundary, FAN1 expect value will load from segment **2** register (index AB)h. When VT1 temperature is **below** this boundary – hysteresis, FAN1 expect value will load from segment **3** register (index ABh).

8.2.39 VT1 BOUNDARY 3 TEMPERATURE – Index A8h

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Return 0 when read.
6-0	BOUND3TMP1	R/W	28h (40°C)	The 3st BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is **exceed** this boundary, FAN1 expect value will load from segment **3** register (index AC)h. When VT1 temperature is **below** this boundary – hysteresis, FAN1 expect value will load from segment **4** register (index ACh).

8.2.40 VT1 BOUNDARY 4 TEMPERATURE – Index A9

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Return 0 when read.
6-0	BOUND4TMP1	R/W	1Eh (30°C)	The 4st BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is **exceed** this boundary, FAN1 expect value will load from segment **4** register (index ADh). When VT1 temperature is **below** this boundary – hysteresis, FAN1 expect value will load from segment **5** register (index ADh).

8.2.41 FAN1 SEGMENT 1 SPEED COUNT – Index AAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED1	R/W	FFh (100%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: $Expectspeed = \left(\frac{32}{32+value}\right) \times Fullspeed$ 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.2.42 FAN1 SEGMENT 2 SPEED COUNT – Index ABh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED1	R/W	D9h (85%)	Depend on the FAN1_MODE(CR96[1:0]) register setting: **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.2.43 FAN1 SEGMENT 3 SPEED COUNT – Index ACh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED1	R/W	B2h (70%)	Depend on the FAN1_MODE(CR96[1:0]) register setting: **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.2.44 FAN1 SEGMENT 4 SPEED COUNT – Index ADh

Bit	Name	R/W	Default	Description
7-0	SEC4SPEED1	R/W	99h (60%)	Depend on the FAN1_MODE(CR96[1:0]) register setting: **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.2.45 FAN1 SEGMENT 5 SPEED COUNT – Index AEh

Bit	Name	R/W	Default	Description
7-0	SEC5SPEED1	R/W	80h (50%)	Depend on the FAN1_MODE(CR96[1:0]) register setting: **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.2.46 FAN1 Temperature Mapping Select – Index AFh

Bit	Name	R/W	Default	Description
7	FAN1_PRE_UP_EN	R/W	0	If this bit set to 1, when detect loading increase acutely, fan1 will pre-up fan speed
6	FAN1_NO_STOP	R/W	0	If this bit set to 1, fan1 min duty will in duty that define in CR9C
5	FAN1_UP_T_EN	R/W	0	Set 1 to force FAN1 to the highest speed if any temperature over its high limit.
4	FAN1_INTERPOLATION_EN	R/W	0	Set 1 will enable the interpolation of the fan expect table. (Auto Linear Mode)
3	FAN1_JUMP_HIGH_EN	R/W	1	Set 1 that FAN1 speed will jump to FAN1 SEGMENT 1 SPEED when temperature over T1 Boundary 1. Set 0 that FAN1 speed will raise up to FAN1 SEGMENT 1 SPEED by slop value(CR9B) when temperature over T1 Boundary 1.
2	FAN1_JUMP_LOW_EN	R/W	1	Set 1 that FAN1 speed will jump to FAN1 SEGMENT 2 SPEED when temperature under FAN1 Boundary Hystersis. Set 0 that FAN1 speed will decrease to FAN1 SEGMENT 2 SPEED by slop value(CR9B) when temperature under FAN1 Boundary Hystersis.
1-0	Fan1_temp_sel	R/W	1	0: fan1 follow local temperature. 1: fan1 follow temperature 1. 2: fan1 follow temperature 2. 3: fan1 follow temperature 3.

Fan2 Index B0h- BFh

Address	Attribute	Default Value	Description
B0h	RO	8'h0f	FAN2 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B1h	RO	8'hff	FAN2 count reading (LSB).
B2h	R/W	8'h00	**RPM mode(CR96 bit2=0):** FAN2 expect speed count value (MSB), in auto fan mode(CR96 bit3➔0) this register is auto updated by hardware. **Duty mode(CR96 bit2=1):** This byte is reserved byte.
B3h	R/W	8'h01	**RPM mode(CR96 bit2=0):** FAN2 expect speed count value (LSB) or expect PWM duty , in auto fan mode this register is auto updated by hardware and read only. **Duty mode(CR96 bit2=1):** The Value programming in this byte is duty value. In auto fan mode(CR96 bit3➔0) this register is updated by hardware. Ex: 5 ➔ 5*100/255 % 255 ➔ 100%
B4h	R/W	8'h03	FAN2 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B5h	R/W	8'hff	FAN2 full speed count reading (LSB).

8.2.47 VT2 BOUNDARY 1 TEMPERATURE – Index B6h

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Return 0 when read.
6-0	BOUND1TMP2	R/W	3Ch (60^oC)	The 1st BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is **exceed** this boundary, FAN2 expect value will load from segment **1** register (index BA)h. When VT2 temperature is **below** this boundary – hysteresis, FAN2 expect value will load from segment **2** register (index BAh).

8.2.48 VT2 BOUNDARY 2 TEMPERATURE – Index B7

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Return 0 when read.
6-0	BOUND2TMP2	R/W	32 (50^oC)	The 2st BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is **exceed** this boundary, FAN2 expect value will load from segment **2** register (index BB)h. When VT2 temperature is **below** this boundary – hysteresis, FAN2 expect value will load from segment **3** register (index BBh).

8.2.49 VT2 BOUNDARY 3 TEMPERATURE – Index B8h

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Return 0 when read.
6-0	BOUND3TMP2	R/W	28h (40^oC)	The 3st BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is **exceed** this boundary, FAN2 expect value will load from segment **3** register (index BC)h. When VT2 temperature is **below** this boundary – hysteresis, FAN2 expect value will load from segment **4** register (index BCh).

8.2.50 VT2 BOUNDARY 4 TEMPERATURE – Index B9

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Return 0 when read.
6-0	BOUND4TMP2	R/W	1Eh (30^oC)	The 4st BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is **exceed** this boundary, FAN2 expect value will load from segment **4** register (index BDh). When VT2 temperature is **below** this boundary – hysteresis, FAN2 expect value will load from segment **5** register (index BDh).

8.2.51 FAN2 SEGMENT 1 SPEED COUNT – Index BAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED2	R/W	FFh (100%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: $Expectspeed=\left(\frac{32}{32+value}\right)\times Fullspeee$ 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.2.52 FAN2 SEGMENT 2 SPEED COUNT – Index BBh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED2	R/W	D9h (85%)	Depend on the FAN2_MODE(CR96[3:2]) register setting: **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.2.53 FAN2 SEGMENT 3 SPEED COUNT – Index BCh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED2	R/W	B2h (70%)	Depend on the FAN2_MODE(CR96[3:2]) register setting: **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.2.54 FAN2 SEGMENT 4 SPEED COUNT – Index BDh

Bit	Name	R/W	Default	Description

7-0	SEC4SPEED2	R/W	99h (60%)	Depend on the FAN2_MODE(CR96[3:2]) register setting: **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.2.55 FAN2 SEGMENT 5 SPEED COUNT – Index BEh

Bit	Name	R/W	Default	Description
7-0	SEC5SPEED2	R/W	80h (50%)	Depend on the FAN2_MODE(CR96[3:2]) register setting: **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.2.56 FAN2 Temperature Mapping Select – Index BFh

Bit	Name	R/W	Default	Description
7	FAN2_PRE_UP_EN	R/W	0	If this bit set to 1, when detect loading increase acutely, fan2 will pre-up the fan speed.
6	FAN2_NO_STOP	R/W	0	If this bit set to 1, fan2 min duty will in duty that define in CR9C
5	FAN2_UP_T_EN	R/W	0	Set 1 to force FAN2 to the highest speed if any temperature over its high limit.
4	FAN2_INTERPOLATION_EN	R/W	0	Set 1 will enable the interpolation of the fan expect table. (Auto Linear Mode)
3	FAN2_JUMP_HIGH_EN	R/W	1	Set 1 that FAN2 speed will jump to FAN2 SEGMENT 1 SPEED when temperature over T2 Boundary 1. Set 0 that FAN2 speed will raise up to FAN2 SEGMENT 1 SPEED by slop value(CR9B) when temperature over T2 Boundary 1.
2	FAN2_JUMP_LOW_EN	R/W	1	Set 1 that FAN2 speed will jump to FAN2 SEGMENT 2 SPEED when temperature under FAN2 Boundary Hystersis. Set 0 that FAN2 speed will decrease to FAN2 SEGMENT 2 SPEED by slop value(CR9B) when temperature under FAN2 Boundary Hystersis.
1-0	Fan2_temp_sel	R/W	2	0: fan2 follow local temperature. 1: fan2 follow temperature 1. 2: fan2 follow temperature 2. 3: fan2 follow temperature 3.

Fan3 Index C0h- CFh

Address	Attribute	Default Value	Description
C0h	RO	8'h0F	FAN3 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C1h	RO	8'hff	FAN3 count reading (LSB).
C2h	R/W	8'h00	**RPM mode(CR96 bit4=0):** FAN3 expect speed count value (MSB), in auto fan mode(CR96 bit5➔0) this register is auto updated by hardware. **Duty mode(CR96 bit4=1):** This byte is reserved byte.
C3h	R/W	8'h01	**RPM mode(CR96 bit4=0):**

			FAN3 expect speed count value (LSB) or expect PWM duty , in auto fan mode this register is auto updated by hardware and read only. **Duty mode(CR96 bit4=1):** The Value programming in this byte is duty value. In auto fan mode(CR96 bit5➔0) this register is updated by hardware. Ex: 5 ➔ 5*100/255 % 255 ➔ 100%
C4h	R/W	8'h03	FAN3 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C5h	R/W	8'hff	FAN3 full speed count reading (LSB).

8.2.57 VT3 BOUNDARY 1 TEMPERATURE – Index C6h

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Return 0 when read.
6-0	BOUND1TMP3	R/W	3Ch (60^oC)	The 1st BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is **exceed** this boundary, FAN3 expect value will load from segment **1** register (index CA)h. When VT3 temperature is **below** this boundary – hysteresis, FAN3 expect value will load from segment **2** register (index CAh).

8.2.58 VT3 BOUNDARY 2 TEMPERATURE – Index C7

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Return 0 when read.
6-0	BOUND2TMP3	R/W	32 (50^oC)	The 2st BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is **exceed** this boundary, FAN3 expect value will load from segment **2** register (index CB)h. When VT3 temperature is **below** this boundary – hysteresis, FAN3 expect value will load from segment **3** register (index CBh).

8.2.59 VT3 BOUNDARY 3 TEMPERATURE – Index C8h

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Return 0 when read.
6-0	BOUND3TMP3	R/W	28h (40^oC)	The 3st BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is **exceed** this boundary, FAN3 expect value will load from segment **3** register (index CC)h. When VT3 temperature is **below** this boundary – hysteresis, FAN3 expect value will load from segment **4** register (index CCh).

8.2.60 VT3 BOUNDARY 4 TEMPERATURE – Index C9

Bit	Name	R/W	Default	Description
7	Reserved	RO	0	Return 0 when read.
6-0	BOUND4TMP3	R/W	1Eh (30^oC)	The 4st BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is **exceed** this boundary, FAN3 expect value will load from segment **4** register (index CDh). When VT3 temperature is **below** this boundary – hysteresis, FAN3 expect value will load from segment **5** register (index CDh).

8.2.61 FAN3 SEGMENT 1 SPEED COUNT – Index CAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED3	R/W	FFh (100%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: $Expect\_speed = \left(\frac{32}{32+value}\right) \times Full\_speed$ 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.2.62 FAN3 SEGMENT 2 SPEED COUNT – Index CBh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED3	R/W	D9h (85%)	Depend on the FAN3_MODE(CR96[5:4]) register setting: **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.2.63 FAN3 SEGMENT 3 SPEED COUNT – Index CCh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED3	R/W	B2h (70%)	Depend on the FAN3_MODE(CR96[5:4]) register setting: **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.2.64 FAN3 SEGMENT 4 SPEED COUNT – Index CDh

Bit	Name	R/W	Default	Description
7-0	SEC4SPEED3	R/W	99h (60%)	Depend on the FAN3_MODE(CR96[5:4]) register setting: **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.2.65 FAN3 SEGMENT 5 SPEED COUNT – Index CEh

Bit	Name	R/W	Default	Description
7-0	SEC5SPEED3	R/W	80h (50%)	Depend on the FAN3_MODE(CR96[5:4]) register setting: **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.2.66 FAN3 Temperature Mapping Select – Index CFh

Bit	Name	R/W	Default	Description
7	FAN3_PRE_UP_EN	R/W	0	If this bit set to 1, when detect loading increase acutely, fan3 will pre-up fan speed

6	FAN3_NO_STOP	R/W	0	If this bit set to 1, fan3 min duty will in duty that define in CR9D
5	FAN3_UP_T_EN	R/W	0	Set 1 to force FAN3 to the highest speed if any temperature over its high limit.
4	FAN3_INTERPOLATION_EN	R/W	0	Set 1 will enable the interpolation of the fan expect table. (Auto Linear Mode)
3	FAN3_JUMP_HIGH_EN	R/W	1	Set 1 that FAN3 speed will jump to FAN3 SEGMENT 1 SPEED when temperature over T3 Boundary 1. Set 0 that FAN3 speed will raise up to FAN3 SEGMENT 1 SPEED by slop value(CR9B) when temperature over T3 Boundary 1.
2	FAN3_JUMP_LOW_EN	R/W	1	Set 1 that FAN3 speed will jump to FAN3 SEGMENT 2 SPEED when temperature under FAN3 Boundary Hystersis. Set 0 that FAN3 speed will decrease to FAN3 SEGMENT 2 SPEED by slop value(CR9B) when temperature under FAN3 Boundary Hystersis.
1-0	Fan3_temp_sel	R/W	3	0: fan3 follow local temperature. 1: fan3 follow temperature 1. 2: fan3 follow temperature 2. 3: fan3 follow temperature 3.

8.3 Loading Gauge Registers

8.3.1 Loading Gauge Configuration Register — Index 01h

Bit	Name	R/W	Default	Description
7	GAUGE_DIS	R/W	0	If this bit is set to 1, loading gauge is disabled.
6	MUL_EN	R/W	0	If this bit is set to 1, gauging multi-phase pwm is enabled.
5-4	PWM_MUL	R/W	0	Select PWMIN type : 0: Single phase 1: Two phase 2: Three phase 3: Four phase
3	LPF_DIS	R/W	0	If this bit is set to 1, low pass filter of loading gauge reading is disabled.
2-0	TIME_SEL	R/W	4	Set these to select gauging period. 0: 0x3FF_FFFF Loading gauge cycles 1: 0x1FF_FFFF Loading gauge cycles 2: 0x0FF_FFFF Loading gauge cycles 3: 0x07F_FFFF Loading gauge cycles 4: 0x03F_FFFF Loading gauge cycles 5: 0x01F_FFFF Loading gauge cycles 6: 0x00F_FFFF Loading gauge cycles 7: 0x007_FFFF Loading gauge cycles

8.3.2 Loading Gauge Configuration Register — Index 02h

Bit	Name	R/W	Default	Description
7	OFFSET_SEL_MANUAL_EN	R/W	1	If this bit is set to 1, offset_sel will be offset_sel_manual.
6-4	OFFSET_SEL_MANUAL	R/W	7	If offset_sel_manual_en is set to 1, offset_sel will be forced to this value
3	STOP_DIS	R/W	0	If this bit is set to 1, stop# is disabled
2-1	LG_CLK_SEL	R/W	1	Loading gauge clock will be -- 0: 6.25 Mhz 1: 12.5 Mhz 2, 3: 25Mhz
0	PWM_INV	R/W	0	0: Gauge high level of PWMIN 1: Gauge low level of PWMIN

8.3.3 Loading Gauge Reading Register (MSB) — Index 03h

Bit	Name	R/W	Default	Description
7-0	LG_READING[15:8]	R	0	MSB of loading gauge reading

8.3.4 Loading Gauge Reading Register (LSB) — Index 04h

Bit	Name	R/W	Default	Description
7-0	LG_READING[7:0]	R	0	LSB of loading gauge reading

8.3.5 Loading Gauge Limit 1 Register (MSB) — Index 05h

Bit	Name	R/W	Default	Description
7-0	LIMIT1[11:4]	R/W	0	MSB of loading gauge limit1

8.3.6 Loading Gauge Limit 1 Register (LSB) — Index 06h

Bit	Name	R/W	Default	Description
7-4	LIMIT1[3:0]	R/W	0	LSB of loading gauge limit1. Limit1[0] is used to set overclocking(set to 1) or underclocking (set to 0)
3-0	reserved	R	0	reserved

8.3.7 Loading Gauge Hysteresis 1 Register (MSB) — Index 07h

Bit	Name	R/W	Default	Description
7-0	HYST1[11:4]	R/W	0	MSB of loading gauge hysteresis1

8.3.8 Loading Gauge Hysteresis 1 Register (LSB) — Index 08h

Bit	Name	R/W	Default	Description
7-4	HYST1[3:0]	R/W	0	LSB of loading gauge hysteresis1
3-0	reserved	R	0	reserved

8.3.9 Loading Gauge Limit 2 Register (MSB) — Index 09h

Bit	Name	R/W	Default	Description
7-0	LIMIT2[11:4]	R/W	0	MSB of loading gauge limit2

8.3.10 Loading Gauge Limit 2 Register (LSB) — Index 0Ah

Bit	Name	R/W	Default	Description
7-4	LIMIT2[3:0]	R/W	0	LSB of loading gauge limit2 Limit2[0] is used to set overclocking(set to 1) or underclocking (set to 0)
3-0	reserved	R	0	reserved

8.3.11 Loading Gauge Hysteresis 2 Register (MSB) — Index 0Bh

Bit	Name	R/W	Default	Description
7-0	HYST2[11:4]	R/W	0	MSB of loading gauge hysteresis2

8.3.12 Loading Gauge Hysteresis 2 Register (LSB) — Index 0Ch

Bit	Name	R/W	Default	Description
7-4	HYST2[3:0]	R/W	0	LSB of loading gauge hysteresis2
3-0	reserved	R	0	reserved

8.3.13 Loading Gauge Limit 3 Register (MSB) — Index 0Dh

Bit	Name	R/W	Default	Description
7-0	LIMIT3[11:4]	R/W	0	MSB of loading gauge limit3

8.3.14 Loading Gauge Limit 3 Register (LSB) — Index 0Eh

Bit	Name	R/W	Default	Description
7-4	LIMIT3[3:0]	R/W	0	LSB of loading gauge limit3 Limit3[0] is used to set overclocking (set to 1) or underclocking (set to 0)
3-0	reserved	R	0	reserved

8.3.15 Loading Gauge Hysteresis 3 Register (MSB) — Index 0Fh

Bit	Name	R/W	Default	Description
7-0	HYST3[11:4]	R/W	0	MSB of loading gauge hysteresis3

8.3.16 Loading Gauge Hysteresis 3 Register (LSB) — Index 10h

Bit	Name	R/W	Default	Description
7-4	HYST3[3:0]	R/W	0	LSB of loading gauge hysteresis3
3-0	reserved	R	0	reserved

8.3.17 Loading Gauge Limit 4 Register (MSB) — Index 11h

Bit	Name	R/W	Default	Description
7-0	LIMIT4[11:4]	R/W	0	MSB of loading gauge limit4

8.3.18 Loading Gauge Limit 4 Register (LSB) — Index 12h

Bit	Name	R/W	Default	Description
7-4	LIMIT4[3:0]	R/W	0	LSB of loading gauge limit4 Limit4[0] is used to set overclocking(set to 1) or underclocking (set to 0)
3-0	reserved	R	0	reserved

8.3.19 Loading Gauge Hysteresis 4 Register (MSB) — Index 13h

Bit	Name	R/W	Default	Description
7-0	HYST4[11:4]	R/W	0	MSB of loading gauge hysteresis4

8.3.20 Loading Gauge Hysteresis 4 Register (LSB) — Index 14h

Bit	Name	R/W	Default	Description
7-4	HYST4[3:0]	R/W	0	LSB of loading gauge hysteresis4
3-0	reserved	R	0	reserved

8.3.21 Loading Gauge Section Mapping Register 1— Index 15h

Bit	Name	R/W	Default	Description
7	reserved	R	0	Reserved
6-4	SEC1	R/W	1	Section1 mapping value
3	reserved	R	0	Reserved

2-0	SEC0	R/W	0	Section0 mapping value

8.3.22 Loading Gauge Section Mapping Register 2 — Index 16h

Bit	Name	R/W	Default	Description
7	reserved	R	0	Reserved
6-4	SEC3	R/W	3	Section3 mapping value
3	reserved	R	0	Reserved
2-0	SEC2	R/W	2	Section2 mapping value

8.3.23 Loading Gauge Section Mapping Register 3 — Index 17h

Bit	Name	R/W	Default	Description
7-3	reserved	R	0	Reserved
2-0	SEC4	R/W	4	Section4 mapping value

8.3.24 Loading Gauge Real Time Status Register — Index 18h

Bit	Name	R/W	Default	Description
7	reserved	R	0	Reserved
6-4	CURRENT_SEC	R	-	Indicate current section. (Original section value, not mapped)
3	reserved	R	0	Reserved
2-0	TURBO_N	R	-	Indicate current TURBO_N status.(mapped)

8.3.25 Loading Gauge PME status register — Index 20h

Bit	Name	R/W	Default	Description
7-1	reserved	R	0	Reserved
0	LG_PME_STS	R	-	If the section value changes and the relative limitx_pme_en is enabled, this bit will be set to 1. Write 1 to clear this bit.

8.3.26 Loading Gauge PME Control register — Index 21h

Bit	Name	R/W	Default	Description
7-4	reserved	R/W	0	Reserved (Dummy registers)
3	Limit4_pme_en	R/W	0	If loading gauge reading moves across limit4 (up or down) and this bit is set to 1, the LG_PME_STS will be set to 1.
2	Limit3_pme_en	R/W	0	If loading gauge reading moves across limit3 (up or down) and this bit is set to 1, the LG_PME_STS will be set to 1.
1	Limit2_pme_en	R/W	0	If loading gauge reading moves across limit2 (up or down) and this bit is set to 1, the LG_PME_STS will be set to 1.
0	Limit1_pme_en	R/W	0	If loading gauge reading moves across limit1 (up or down) and this bit is set to 1, the LG_PME_STS will be set to 1.

8.3.27 Loading Gauge Stop Time Control register — Index 22h

Bit	Name	R/W	Default	Description
7-4	Reserved	R	0	Reserved
3-0	STOP_CNT	R/W	0	Set STOP_CNT can modify the pulse period of pin STOP#. Stop time = 30 + (5*STOP_CNT) ms

8.3.28 Loading Gauge Hysteresis Timeout Control register — Index 23h

Bit	Name	R/W	Default	Description
7-3	Reserved	R	0	Reserved
4-0	TIMEOUT_CNT	R/W	5	If loading gauge reading is located at one of the hysteresis range and stay at this range for TIMEOUT_CNT monitoring times, the current section will return to the previous one.

8.3.29 Loading Increasing Control register 1— Index 25h

Bit	Name	R/W	Default	Description
7-3	Reserved	R	0	Reserved
2-0	LOAD_RANGE_SEL	R/W	0	These bits are for pre-control machine use that is for fan control by loading status. When loading status increases promptly over the setting as below, fan control system will pre-control fan speed up to cool down the predict raising temperature. This value is base on LG_READING [17:6] register. 000: 0x01 001: 0x02 010: 0x04 011: 0x08 100: 0x0F 101: 0x1F 110: 0x3F 111: 0x7F

8.3.30 Loading Increasing Control register 2— Index 26h

Bit	Name	R/W	Default	Description
7	Reserved	R	0	Reserved
6-4	LOAD_HOLD_TIME	R/W	7	Default 6.4 seconds (800ms per step). These bits will be used with Loading Increase Control register. When fan speed increasing to expect status (follow the LOAD_UP_TIME), user can fill out these two bits register to decide period of hold time.
3-0	LOAD_UP_TIME	R/W	9	Default 4 seconds (400ms per step). When loading status run over LOAD_RANGE_SEL setting, user can set the raising time of fan speed.

8.3.31 Loading Gauge Sorting & One Shot Control register — Index 30h

Bit	Name	R/W	Default	Description
7	SORTING_EN	R/W	0	Set this bit to 1 for sorting hysteresis. It will be auto cleared after finish sorting.
6-1	Reserved	R	0	Reserved
0	ONE_SHOT_EN	R/W	0	Set this bit to enable one-shot. If one-shot is finished, gauge_counter_dis bit will be set to 1. If another one-shot is needed, just write gauge_counter_dis bit to 0

8.4 VID Controller Registers

8.4.1 VID Configuration Register — Index 01h

Bit	Name	R/W	Default	Description
7	Reserved	R/W	0	Reserved
6	WDOUT_EN	R/W	0	If this bit is set to 1 and watchdog timeout event occurs, RSTOUT# output is enabled.
5	KEY_OK	R	0	If private keys are entered correctly, this bit will be set to 1.
4	OTF_EN	R/W	0	If this bit is set to 1 and "MANUAL_MODE" is 0, VID on the fly is enabled and VID_OUT will be new VID_OUT. If this bit is set to 0, VID_OUT will be VID_IN. This bit is also cleared by slotocc and reset signal of watchdog timeout. (Protected by serial key)
3	MANUAL_MODE	R/W	0	If this bit is set to 1 and "OTF_EN" is 1, VID_OUT will be "VID_MANUAL" in register index 0x04. (Protected by serial key)
2-0	VRM_SEL	R/W	0	This bit is protected by serial key. 0: Intel VRM10.0 1: Intel extended VRM10.0 2: Intel VRM11.0 3: AMD VRM 4~7: Reserved

8.4.2 VID Configuration Register — Index 02h

Bit	Name	R/W	Default	Description
7-0	KEY_VALUE	R/W	0	Private key value (0x32→0x5d→0x42→0xac)

8.4.3 VID_IN Reading Register — Index 03h

Bit	Name	R/W	Default	Description
7-0	VID_IN	R	-	VID_IN reading from CPU. If GP2_SEL[1] is 0, the VID_IN is current VID of CPU. If GP2_SEL[1] is set from 0 to 1, the VID of CPU is latched at this time.

8.4.4 VID Manual Register — Index 04h

Bit	Name	R/W	Default	Description
7-0	VID_MANUAL	R/W	0	If "MANUAL_MODE" is set to 1 and "OTF_EN" is set to 0, VID_OUT will be VID_MANUAL. (Protected by serial key)

8.4.5 VID Offset Register 1— Index 05h

Bit	Name	R/W	Default	Description
7-0	VID_OFFSET0	R/W	0	If "CURRENT_SEC" in loading gauge register (Index 18h) is 0, VID_OFFSET0 is selected as the offset of VID. VID_OFFSET0[7] is a sign bit. (Protected by serial key)

8.4.6 VID Offset Register 2— Index 06h

Bit	Name	R/W	Default	Description
7-0	VID_OFFSET1	R/W	0	If "CURRENT_SEC" in loading gauge register (Index 18h) is 1, VID_OFFSET1 is selected as the offset of VID. VID_OFFSET1[7] is a sign bit. (Protected by serial key)

8.4.7 VID Offset Register 3 — Index 07h

Bit	Name	R/W	Default	Description
7-0	VID_OFFSET2	R/W	0	If "CURRENT_SEC" in loading gauge register (Index 18h) is 2, VID_OFFSET2 is selected as the offset of VID. VID_OFFSET2[7] is a sign bit. (Protected by serial key)

8.4.8 VID Offset Register 4 — Index 08h

Bit	Name	R/W	Default	Description
7-0	VID_OFFSET3	R/W	0	If "CURRENT_SEC" in loading gauge register (Index 18h) is 3 VID_OFFSET3 is selected as the offset of VID. VID_OFFSET3[7] is a sign bit. (Protected by serial key)

8.4.9 VID Offset Register 5 — Index 09h

Bit	Name	R/W	Default	Description
7-0	VID_OFFSET4	R/W	0	If "CURRENT_SEC" in loading gauge register (Index 18h) is 4 VID_OFFSET4 is selected as the offset of VID. VID_OFFSET4[7] is a sign bit. (Protected by serial key)

8.4.10 VID Watchdog Timer Configuration Register — Index 0Ah

Bit	Name	R/W	Default	Description
7	Reserved	R	0	Reserved
6	WDTMOUT_STS	R/W	0	If watchdog timeout event occurs, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	WD_EN	R/W	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	0	Select output mode (0: level, 1: pulse) of RSTOUT# by setting this bit.
3	WD_UNIT	R/W	0	Select time (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	0	Select output polarity of RSTOUT# (0: high active, 1: low active) by setting this bit.
1-0	WD_PSWIDTH	R/W	0	Select output pulse width of RSTOUT# 0: 1 ms 1: 25 ms 2: 125 ms 3: 5 sec

8.4.11 VID Watchdog Time Register— Index 0Bh

Bit	Name	R/W	Default	Description
7-0	WD_TIME	R/W	0	Time of watchdog timer

8.4.12 VID Switch Control Register— Index 0Ch

Bit	Name	R/W	Default	Description
7	SWITCH_AUTO_EN	R/W	0	If this bit is set to 1, the switch value equals to the selected vid offset[3:0] (Protected by serial key)
6	OVER_VOLTAGE_EN	R/W	1	Set to 1 the pin GPIO10/LED and GPIO11/BEEP will short. (Protected by serial key)
5-4	reserved	R/W	0	Reserved (Dummy registers) (Protected by serial key)

3-0	SWITCH_SEL	R/W	7	If switch_auto_en is 0, switch value equals to SWITCH_SEL. There are total 16 switches (0~15). Switch value is 5 means that the sixth switch is on. This bit is also cleared by slotocc and reset signal of watchdog timeout. (Protected by serial key)

8.4.13 VID_IN/VID_OUT Function Select Register— Index 0Dh

Bit	Name	R/W	Default	Description
7	GP3_SEL_CLR_DIS	R/W	0	If this bit is set to 1, GP3_SEL1 and GP3_SEL0 will not be cleared by slotocc and reset signal of watchdog timeout. (Protected by serial key)
6	GP2_SEL_CLR_DIS	R/W	0	If this bit is set to 1, GP2_SEL1 and GP2_SEL0 will not be cleared by slotocc and reset signal of watchdog timeout. (Protected by serial key)
5:4	Reserved	R	0	reserved
3	GP3_SEL1	R/W	0	This bit is function select of VID_IN[4:0] / GPIO3[4:0]. If GP3_SEL1 is 0, the selected function is VID_IN. This bit is also cleared by slotocc and reset signal of watchdog timeout if GP3_SEL_CLR_DIS is 0. (Protected by serial key).
2	GP3_SEL0	R/W	0	This bit is function select of VID_IN[5] / GPIO3[5]. If GP3_SEL0 is 0, the selected function is VID_IN. This bit is also cleared by slotocc and reset signal of watchdog timeout if GP3_SEL_CLR_DIS is 0. (Protected by serial key)
1	GP2_SEL1	R/W	0	This bit is function select of VID_OUT[4:0] / GPIO2[1:5]. If GP2_SEL1 is 0, the selected function is VID_OUT. This bit is also cleared by slotocc and reset signal of watchdog timeout if GP2_SEL_CLR_DIS is 0. (Protected by serial key)
0	GP2_SEL0	R/W	0	This bit is function select of VID_OUT[5] / GPIO2[0]. If GP2_SEL0 is 0, the selected function is VID_OUT. This bit is also cleared by slotocc and reset signal of watchdog timeout if GP2_SEL_CLR_DIS is 0. (Protected by serial key)

9. Electrical Characteristics

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 5.5	V
Input Voltage	-0.5 to VCC+0.5	V
Operating Temperature	0 to +140	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

9.2 DC Characteristics

(T_A = 0° C to 70° C, VCC = 3.3V ± 10%, VSS = 0V)

Parameter	Conditions	MIN	TYP	MAX	Unit
Temperature Error, Remote Diode	60 °C < T_D < 100 °C, VCC = 3.0V to 3.6V -25 °C <T_D < 60°C 100 °C <T_D < 145°C		± 1 ± 1	 ± 3	°C
Temperature Error, Local Diode	0 °C < T_A < 100 °C, VCC = 3.0V to 3.6V		± 1	± 3	°C
Supply Voltage range		3.0	3.3	3.6	V
Average VCC operating supply current	FAN and loading gauge in ILDE mode, I2C interface polling.		2.2		mA
Average VCC standby supply current	FAN and loading gauge in ILDE mode, I2C interface stop.		2.0		mA
Average VSB supply current			250		uA
Power down current			60		uA
Resolution			1		°C
Power on reset threshold			2.2	2.4	V
Diode source current	High Level		95		uA
	Low Level		10		uA

DC Characteristics, continued

(Ta = 0° C to 70° C, VCC = 3.3V ± 10%, VSS = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/OD_{12st}-TTL level bi-directional pin with schmitt trigger, Open-drain output with12 mA sink capability.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VCC
Input Low Leakage	ILIL	-1			μA	VIN = 0V

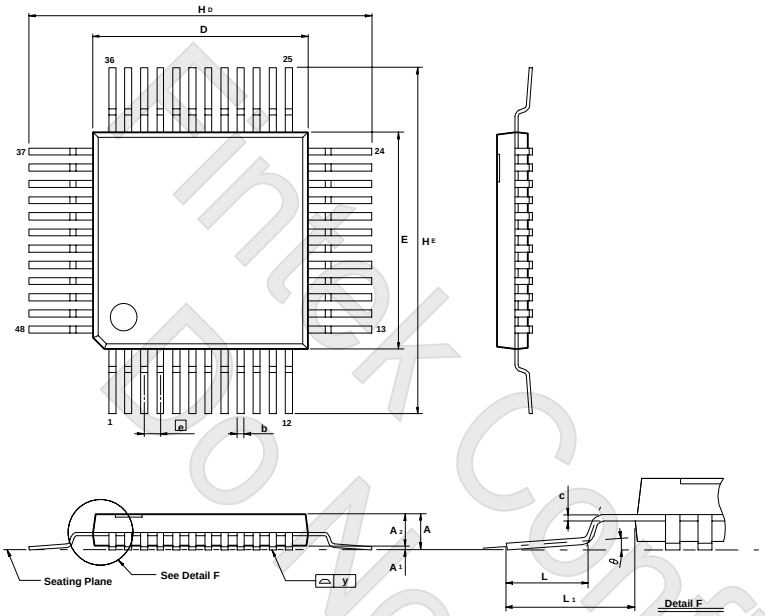
I/OOD$_{12st}$-TTL level bi-directional pin with schmitt trigger, Output pin with 12mA source-sink capability, and can programming to open-drain function.						
Input Low Threshold Voltage	Vt-			0.8	V	VCC = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VCC = 3.3 V
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VCC
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OOD$_{12lv}$-Low voltage bi-directional pin with schmitt trigger, Output pin with 12mA source-sink capability, and can programming to open-drain function.						
Input Low Threshold Voltage	Vt-			0.6	V	VCC = 3.3 V
Input High Threshold Voltage	Vt+	0.9			V	VCC = 3.3 V
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = 1.2V
Input Low Leakage	ILIL	-1			μA	VIN = 0V
IN$_{st}$ - TTL level input pin with schmitt trigger						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VCC
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
IN$_{lv}$ - Low level input pin						
Input Low Voltage	VIL			0.6	V	
Input High Voltage	VIH	0.9			V	
Input High Leakage	ILIH			+1	μA	VIN = 1.2V
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
OD$_{12}$-Open-drain output with12 mA sink capability.						
Output Low Current	IOL		-12		mA	VOL = 0.4V
OOD$_{12}$- Output pin with 12mA source-sink capability, and can programming to open-drain function.						
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V

10.Ordering Information

Part Number	Package Type	Production Flow
F75334DG	48-LQFP Green Package	Commercial, 0°C to +70°C

11.Package Dimensions

48pin-LQFP (7mm*7mm)



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A				---	---	1.60
A_1				0.05	---	0.15
A_2				1.35	1.40	1.45
b				0.17	0.20	0.27
c				0.09	---	0.20
D					7.00	
E					7.00	
e					0.50	
H_D					9.00	
H_E					9.00	
L				0.45	0.60	0.75
L_1					1.00	
y				---	0.08	---
θ				0	3.5°	7

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

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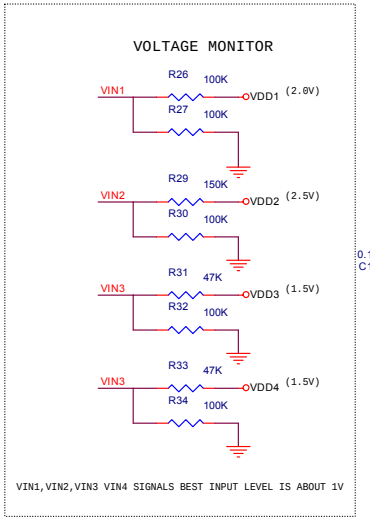
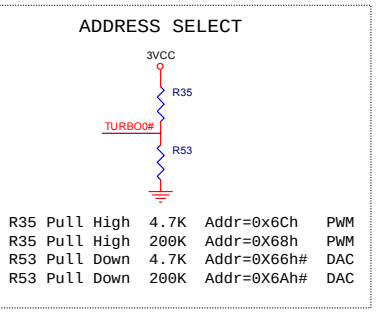
12.Application Circuit





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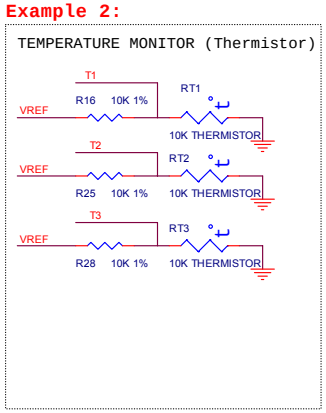

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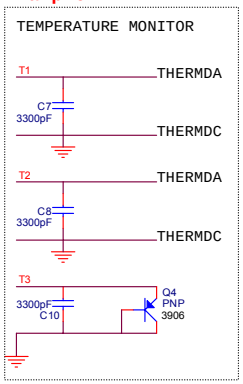

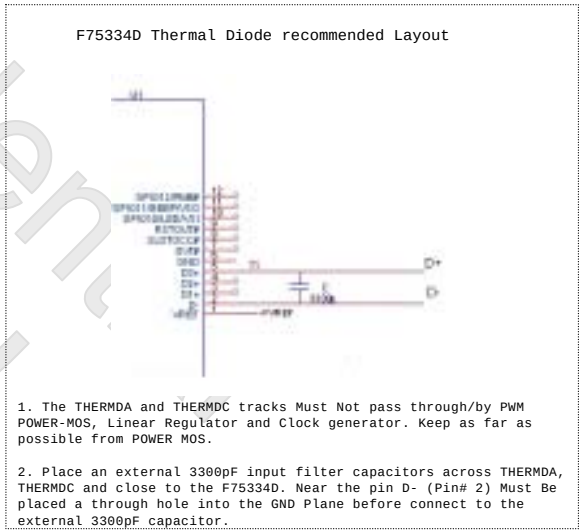

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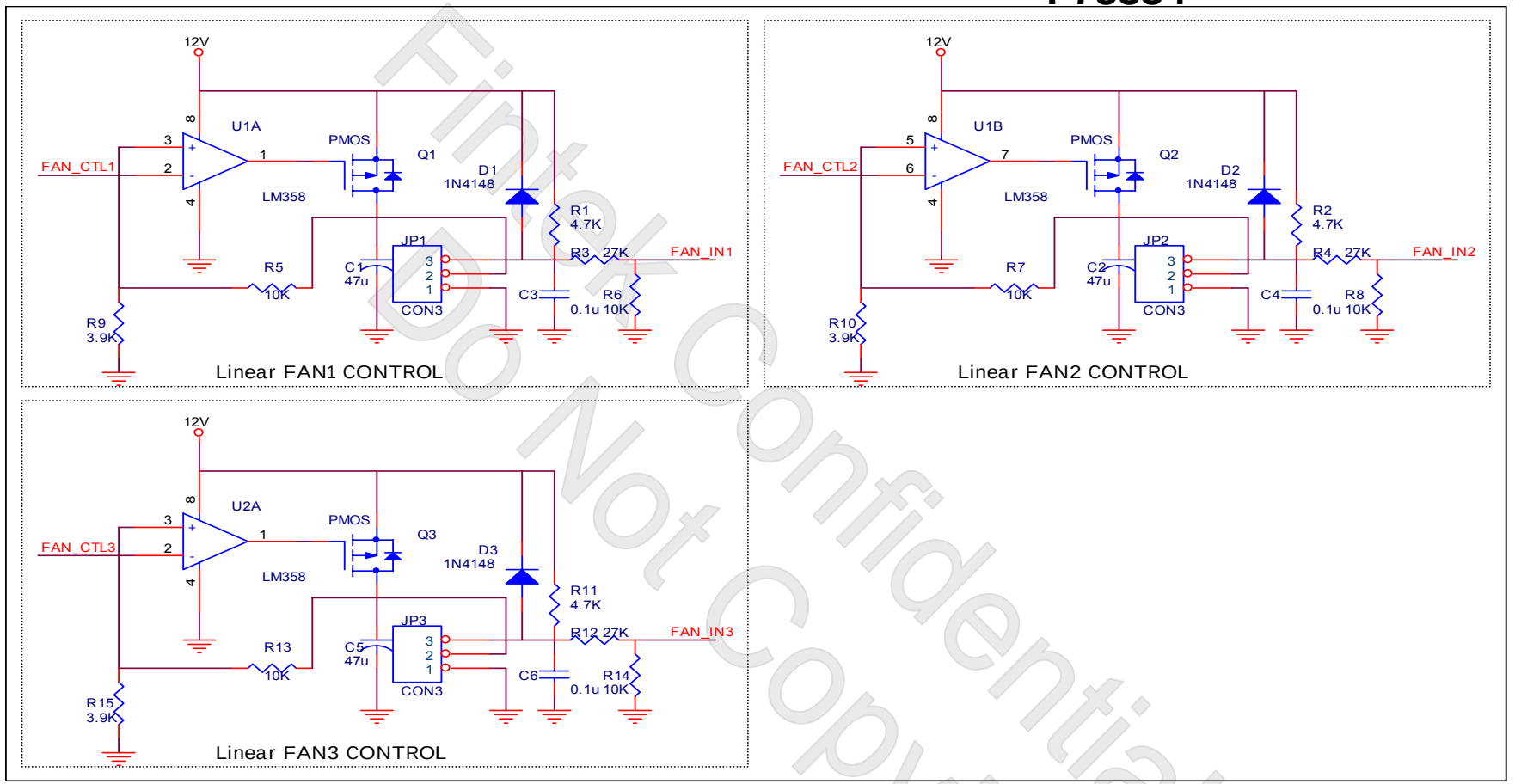

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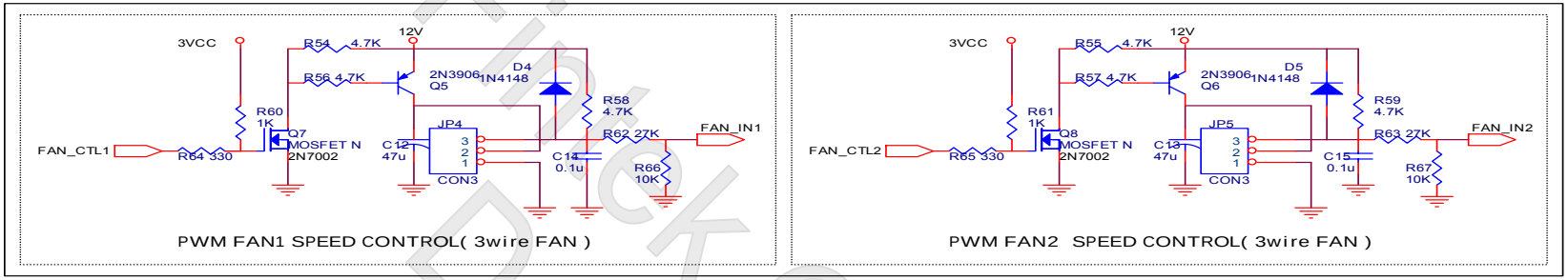

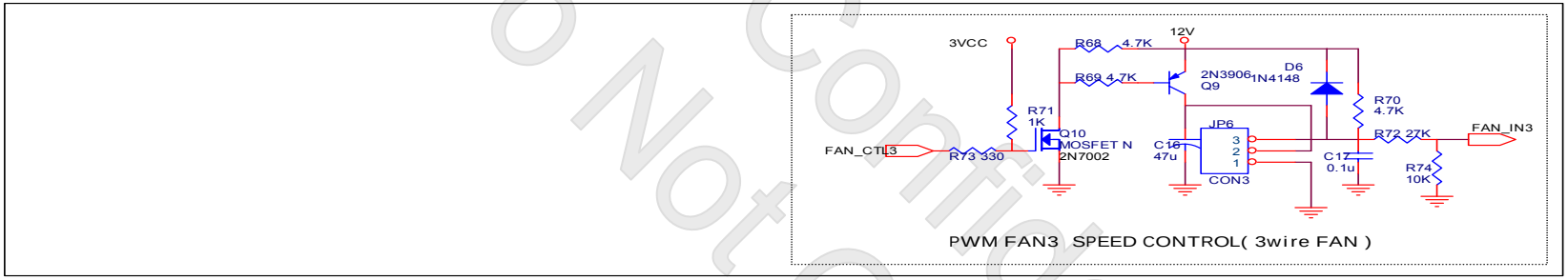

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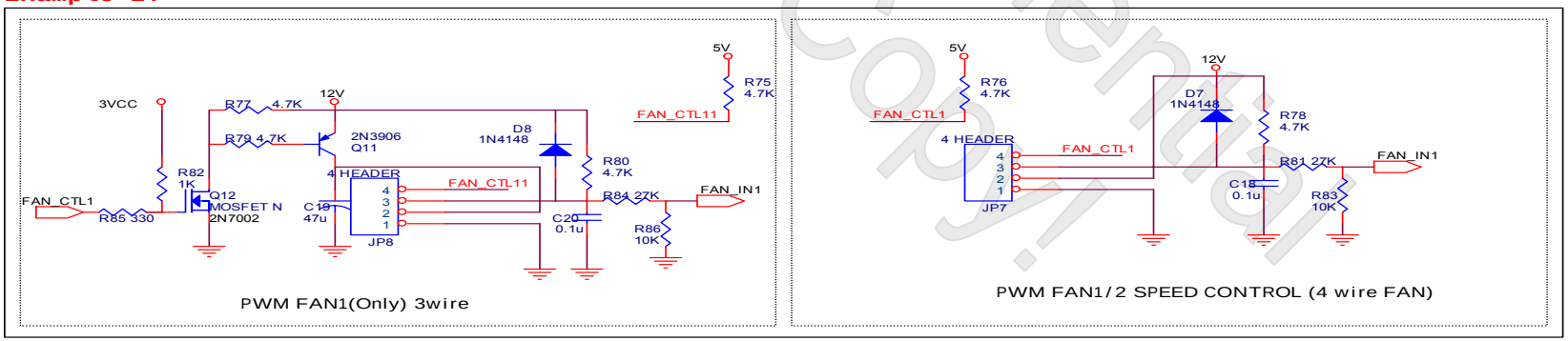

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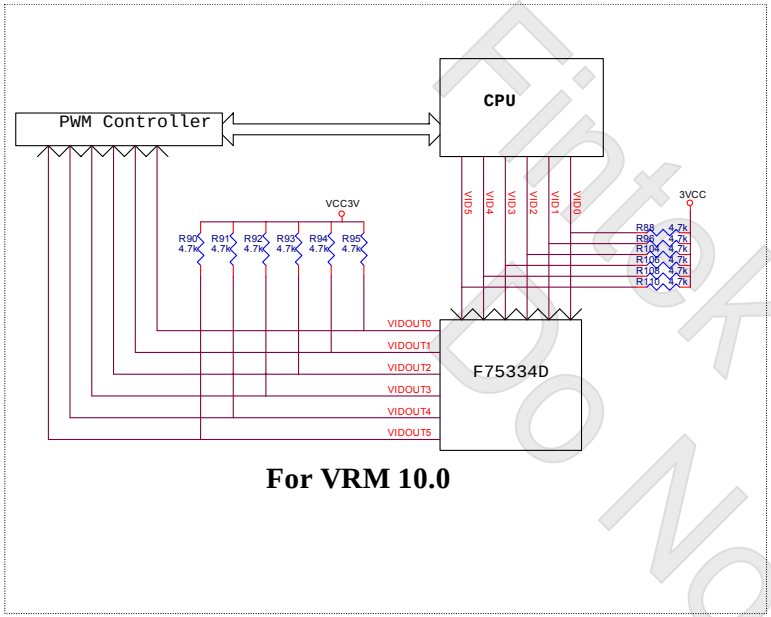
Date: Monday, July 03, 2006	Sheet 3 of 4	



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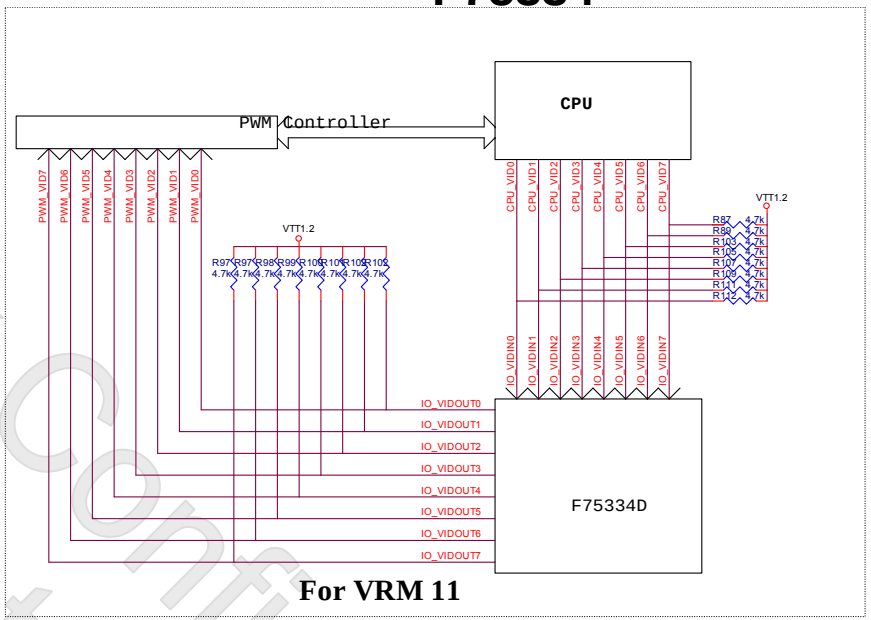
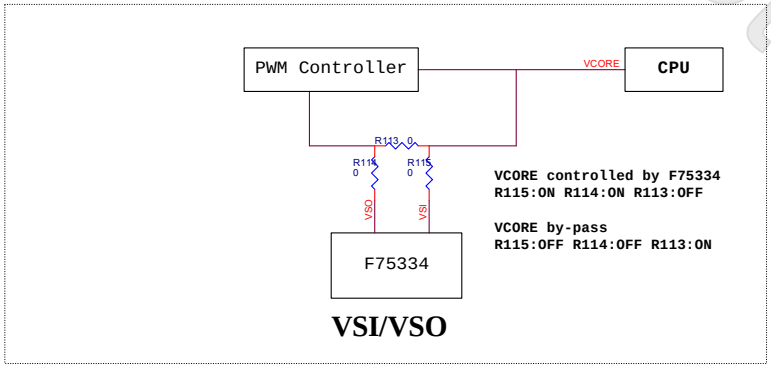
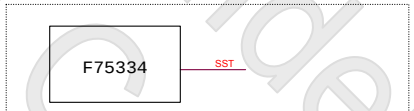


For VRM 11



VSI/VSO



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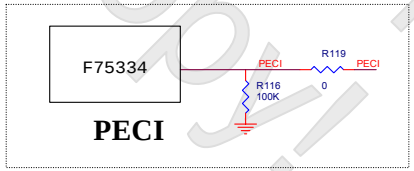

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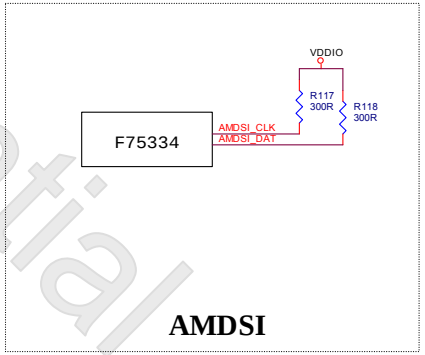

AMDSI

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