Wireless Components

ASK/FSK Single Conversion Receiver

TDA7210 Version 1.0

Data Sheet December 2008

Revision History		
Current Version: 1.0 as of 03.12.08		
Previous Version: none		
Page (in previous Version)	Page(s) (in current Version)	Subjects (major changes since last revision)

We Listen to Your Comments
Is there any information in this document that you feel is wrong, unclear or missing?
Your feedback will help us to continuously improve the quality of this document.
Please send your proposal (including a reference to this document) to:
wirelesscontrol@infineon.com

Edition December 2008

Published by Infineon Technologies AG,
Am Campeon 1 - 12
85579 Neubiberg, Germany

Attention please!

The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Information

For further information on technology, delivery terms and conditions, and prices, please contact the nearest Infineon Technologies Office in Germany or the Infineon Technologies Companies and Infineon Technologies Representatives worldwide (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

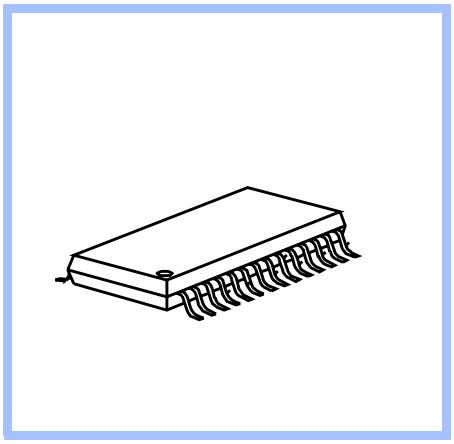
Infineon Technologies Components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/ or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Product Info

General Description

The IC is a very low power consumption single chip FSK/ASK Superheterodyne Receiver (SHR) for the frequency bands 810 to 870 MHz and 400 to 440 MHz that is pin compatible with the Receiver TDA5210. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a PLL FSK demodulator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

Package



Features

- Low supply current (typ. at 868MHz I_S = 5.9mA in FSK mode, I_S = 5.2mA in ASK mode)
- Supply voltage range 5V ±10%
- Power down mode with very low supply current (50nA typ)
- FSK and ASK demodulation capability
- Fully integrated VCO and PLL Synthesiser
- ASK sensitivity < –107dBm
- Selectable frequency ranges 810-870 MHz and 400-440 MHz
- Limiter with RSSI generation, operating at 10.7MHz
- Selectable reference frequency
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold
- FSK sensitivity <-100dBm

Application

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

Ordering Information

Type	Ordering Code	Package
TDA7210	SP000524274	PG-TSSOP-28
samples available on tape and reel		

1 Table of Contents

2 Product Description

Contents of this Chapter

2.1 Overview

The IC is a very low power consumption single chip FSK/ASK Superheterodyne Receiver (SHR) for the frequency bands 810 to 870 MHz and 400 to 440 MHz that is pin compatible with the Receiver TDA5210. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a PLL FSK demodulator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

2.2 Application

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

2.3 Features

- Low supply current (at 868MHz I_S = 5.9 mA typ. FSK mode, 5.2mA typ. ASK mode)
- Supply voltage range 5V ±10%
- Power down mode with very low supply current (50nA typ)
- FSK and ASK demodulation capability
- Fully integrated VCO and PLL Synthesiser
- RF input sensitivity ASK < –107dBm
- RF input sensitivity FSK < –100dBm
- Selectable frequency ranges 810-870 MHz and 400-440 MHz
- Selectable reference frequency
- Limiter with RSSI generation, operating at 10.7MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold

2.4 Package Outlines

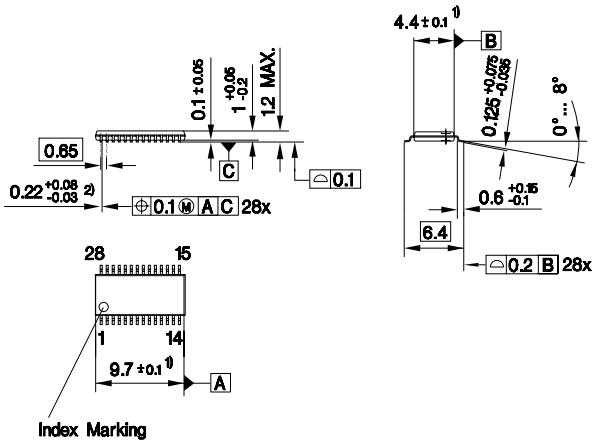


Figure 2-1 PG-TSSOP-28 package outlines

3 Functional Description

Contents of this Chapter

3.1 Pin Configuration

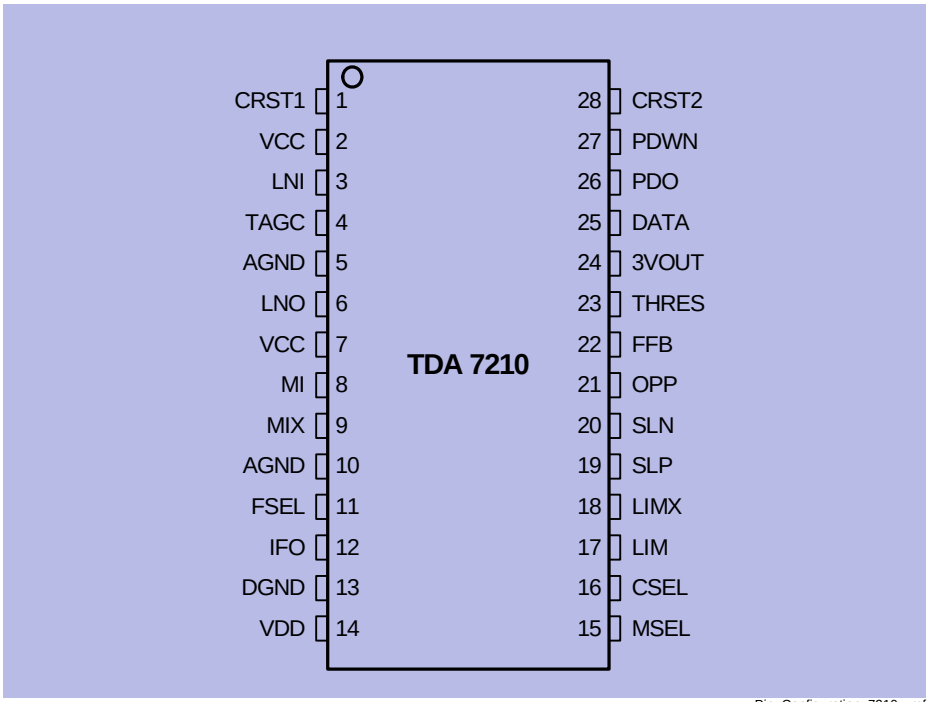


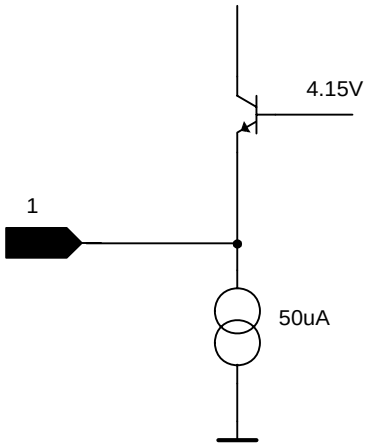
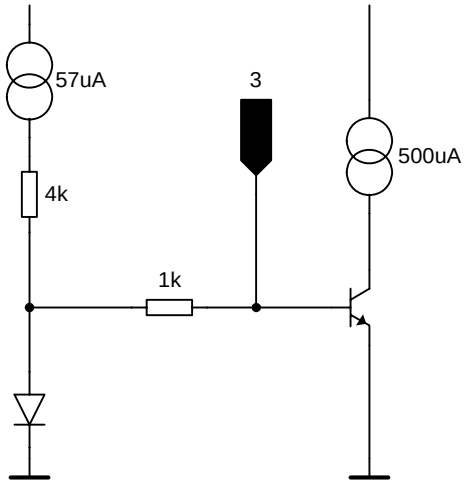
Figure 3-1 IC Pin Configuration

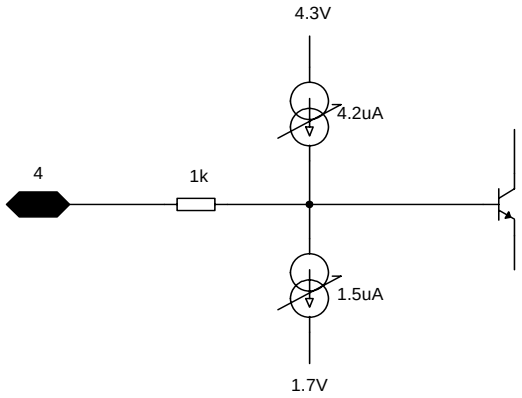
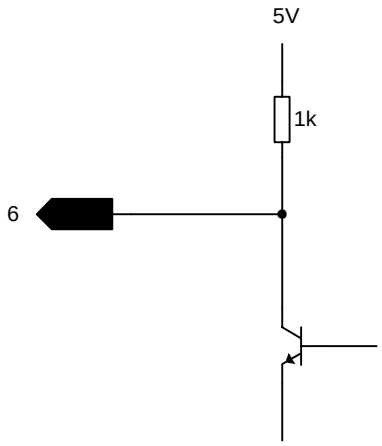
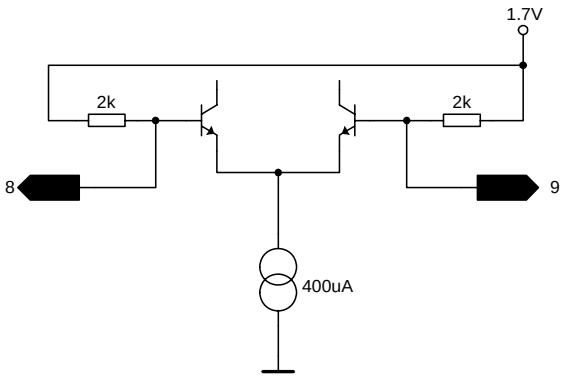
3.2 Pin Definition and Function

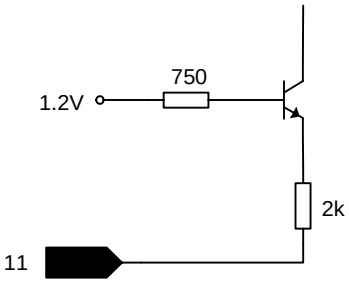
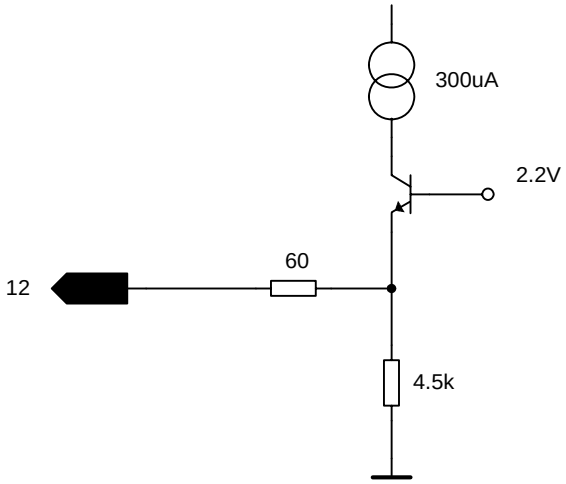
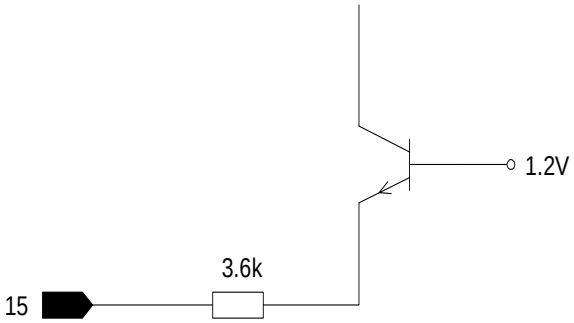
In the subsequent table the internal circuits connected to the pins of the device are shown. ESD-protection circuits are omitted to ease reading.

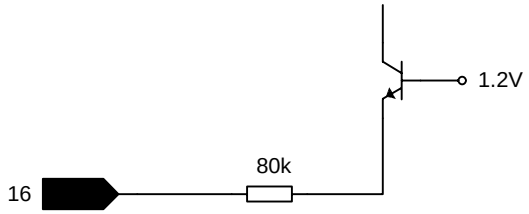
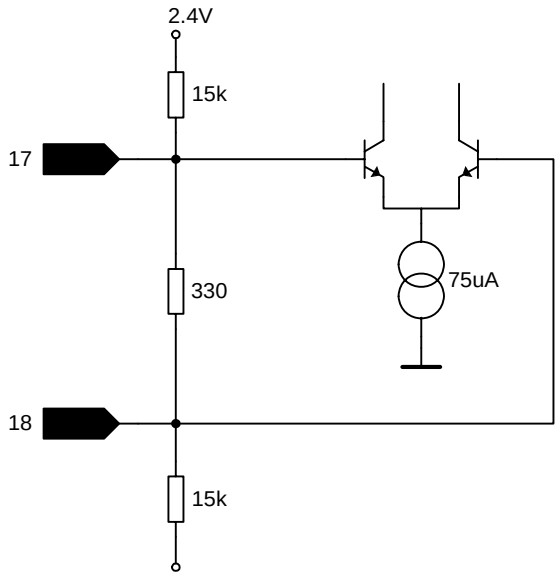
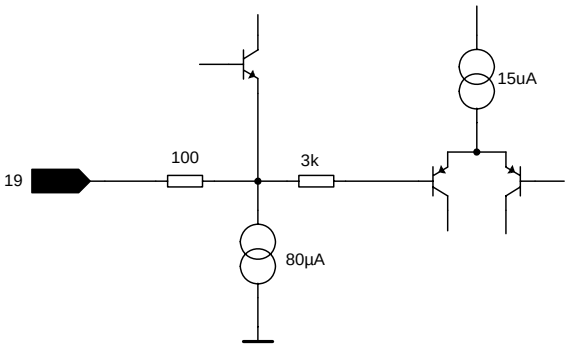
.

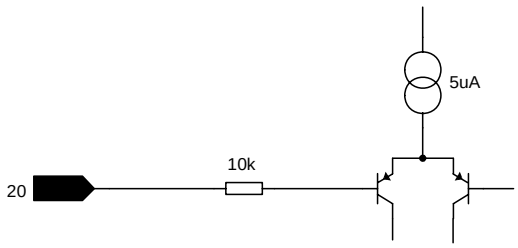
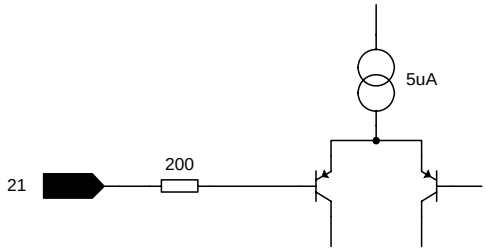
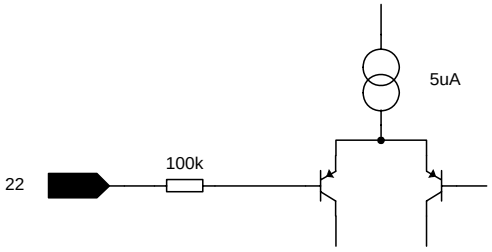
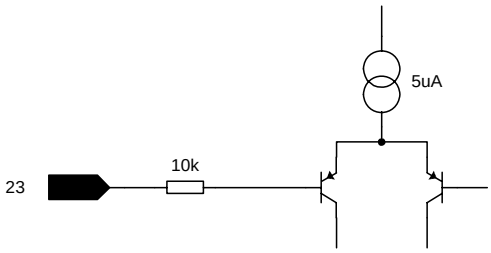
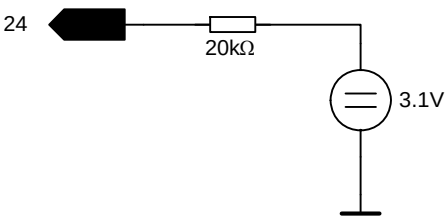
Table 3-1 Pin Definition and Function

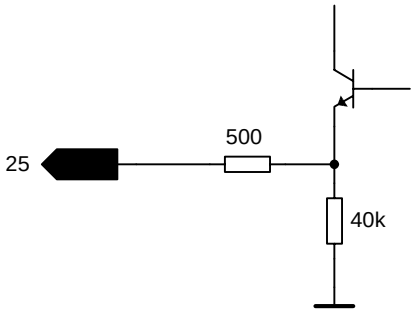
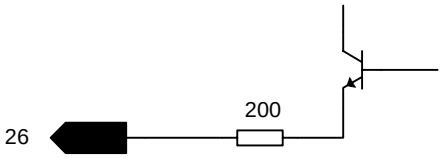
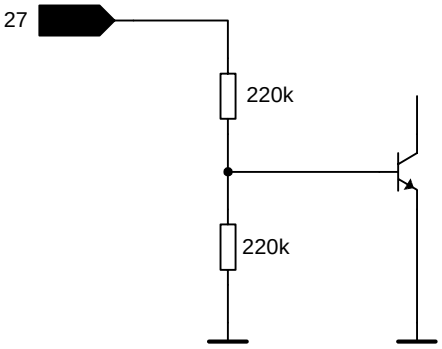
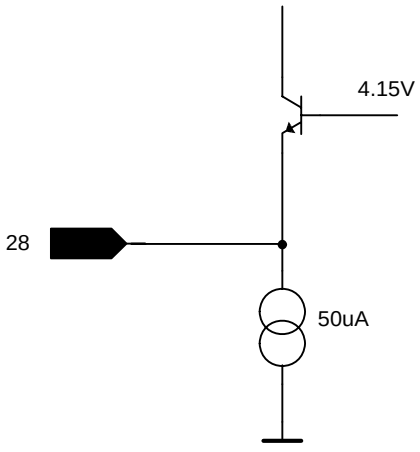
Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	CRST1		External Crystal Connector 1
2	VCC		5V Supply
3	LNI		LNA Input

4	TAGC		AGC Time Constant Control
5	AGND		Analogue Ground Return
6	LNO		LNA Output
7	VCC		5V Supply
8	MI		Mixer Input
9	MIX		Complementary Mixer Input
10	AGND		Analogue Ground Return

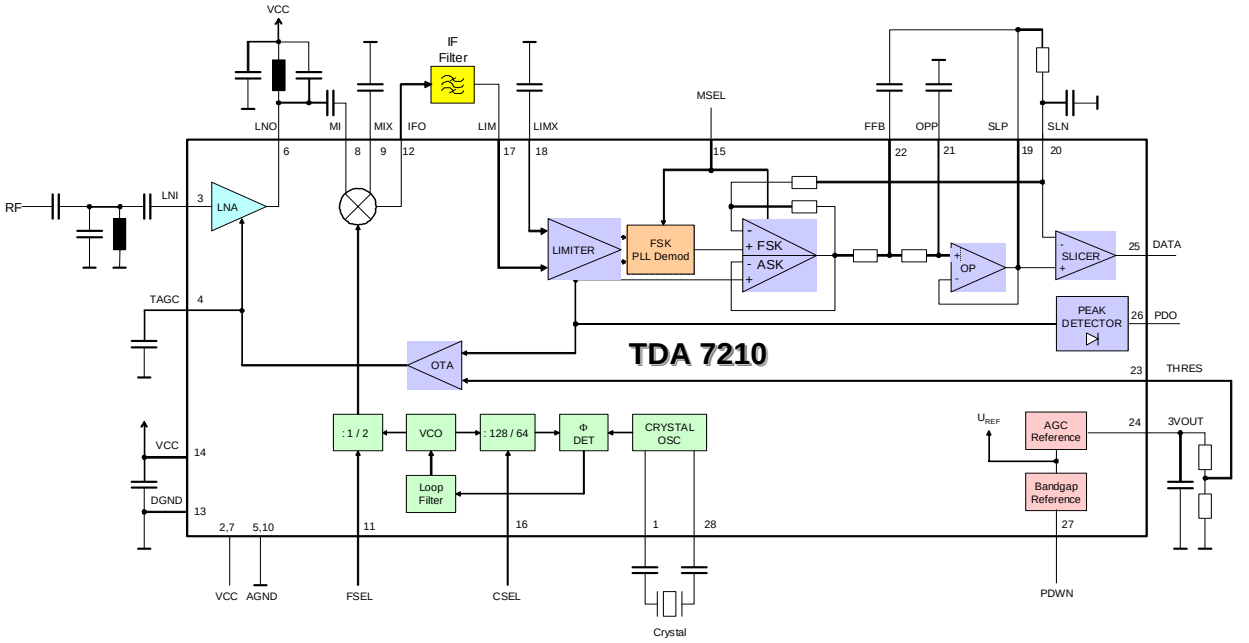
11	FSEL		868/434 MHz Operating Frequency Selector
12	IFO		10.7 MHz IF Mixer Output
13	DGND		Digital Ground Return
14	VDD		5V Supply (PLL Counter Circuitry)
15	MSEL		ASK/FSK Modulation Format Selector

16	CSEL		6.xx or 13.xx MHz Quartz Selector
17	LIM		Limiter Input
18	LIMX		Complementary Limiter Input
19	SLP		Data Slicer Positive Input

20	SLN		Data Slicer Negative Input
21	OPP		OpAmp Noninverting Input
22	FFB		Data Filter Feedback Pin
23	THRES		AGC Threshold Input
24	3VOUT		3V Reference Output

25	DATA		Data Output
26	PDO		Peak Detector Output
27	PDWN		Power Down Input
28	CRST2		External Crystal Connector 2

3.3 Functional Block Diagram



Function_7200.wmf

Figure 3-2 Main Block Diagram

3.4 Functional Blocks

3.4.1 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 to 20dB. The gain figure is determined by the external matching networks situated ahead of LNA and between the LNA output **LNO** (Pin 6) and the Mixer Inputs **MI** and **MIX** (Pins 8 and 9). The noise figure of the LNA is approximately 3dB, the current consumption is 500µA. The gain can be reduced by approximately 18dB. The switching point of this AGC action can be determined externally by applying a threshold voltage at the **THRES** pin (Pin 23). This voltage is compared internally with the received signal (RSSI) level generated by the limiter circuitry. In case that the RSSI level is higher than the threshold voltage the LNA gain is reduced and vice versa. The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin as described in Section 4.1. The time constant of the AGC action can be determined by connecting a capacitor to the **TAGC** pin (Pin 4) and should be chosen along with the appropriate threshold voltage according to the intended operating case and interference scenario to be expected during operation. The optimum choice of AGC time constant and the threshold voltage is described in Section 4.1.

3.4.2 Mixer

The Double Balanced Mixer downconverts the input frequency (RF) in the range of 400-440MHz/810-870MHz to the intermediate frequency (IF) at 10.7MHz with a voltage gain of approximately 21dB by utilising either high- or low-side injection of the local oscillator signal. In case the mixer is interfaced only single-ended, the unused mixer input has to be tied to ground via a capacitor. The mixer is followed by a low pass filter with a corner frequency of 20MHz in order to suppress RF signals to appear at the IF output (**IFO** pin). The IF output is internally consisting of an emitter follower that has a source impedance of approximately 330 Ω to facilitate interfacing the pin directly to a standard 10.7MHz ceramic filter without additional matching circuitry.

3.4.3 PLL Synthesizer

The Phase Locked Loop synthesiser consists of a VCO, an asynchronous divider chain, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCO is including on-chip spiral inductors and varactor diodes. It's nominal centre frequency is 840MHz, the operating range guaranteed over the temperature range specified is 820 to 860MHz. Depending on whether high- or low-side injection of the local oscillator is used the receive frequency ranges are 810 to 840 and 840 to 870MHz or 400 to 420 and 420 to 440MHz (see also Section 4.4). No additional external components are neces-

sary.
The oscillator signal is fed both to the synthesiser divider chain and to the down-converting mixer. In case of operation in the 400 to 440 MHz range, the signal is divided by two before it is fed to the mixer. This is controlled by the selection pin **FSEL** (Pin 11) as described in the following table. The overall division ratio of the divider chain can be selected to be either 128 or 64, depending on the frequency of the reference oscillator quartz (see below and Section 4.4). The loop filter is also realised fully on-chip.

Table 3-2 FSEL Pin Operating States

FSEL	RF Frequency
Open	400-440 MHz
Shorted to ground	810-870 MHz

3.4.4 Crystal Oscillator

The on-chip crystal oscillator circuitry allows for utilisation of quartzes both in the 6 and 13MHz range as the overall division ratio of the PLL can be switched between 64 and 128 via the **CSEL** (Pin 16) pin according to the following table.

Table 3-3 CSEL Pin Operating States

CSEL	Crystal Frequency
Open	6.xx MHz
Shorted to ground	13.xx MHz

The calculation of the value of the necessary quartz load capacitance is shown in Section 4.3, the quartz frequency calculation is explained in Section 4.4.

3.4.5 Limiter

The Limiter is an AC coupled multistage amplifier with a cumulative gain of approximately 80 dB that has a bandpass-characteristic centred around 10.7 MHz. It has a typical input impedance of 330 Ω to allow for easy interfacing to a 10.7 MHz ceramic IF filter. The limiter circuit also acts as a Receive Signal Strength Indicator (RSSI) generator which produces a DC voltage that is directly proportional to the input signal level as can be seen in Figure 4-2. This signal is used to demodulate ASK-modulated receive signals in the subsequent baseband circuitry. The RSSI output is applied to the modulation format switch, to the Peak Detector input and to the AGC circuitry.

In order to demodulate ASK signals the MSEL pin has to be left open as described in the next chapter.

3.4.6 FSK Demodulator

To demodulate frequency shift keyed (FSK) signals a PLL circuit is used that is contained fully on chip. The Limiter output differential signal is fed to the linear phase detector as is the output of the 10.7 MHz center frequency VCO. The demodulator gain is typically 200µV/kHz. The passive loop filter output that is comprised fully on chip is fed to both the VCO and the modulation format switch described in more detail below. This signal is representing the demodulated signal with high frequencies applied to the demodulator demodulated to logic ones and low frequencies demodulated to logic zeroes. Please note that due to this behaviour a sign inversion of the data occurs in case of high-side injection of the local oscillator at receive frequencies below 840 or 420MHz, respectively. See also .

The modulation format switch is actually a switchable amplifier with an AC gain of 11 that is controlled by the **MSEL** pin (Pin 15) as shown in the following table. This gain was chosen to facilitate detection in the subsequent circuits. The DC gain is 1 in order not to saturate the subsequent Data Filter wih the DC offset produced by the demodulator in case of large frequency offsets of the IF signal. The resulting frequency characteristic and details on the principle of operation of the switch are described in Section 4.6.

Table 3-4 MSEL Pin Operating States

MSEL	Modulation Format
Open	ASK
Shorted to ground	FSK

The demodulator circuit is switched off in case of reception of ASK signals.

3.4.7 Data Filter

The data filter comprises an OP-Amp with a bandwidth of 100kHz used as a voltage follower and two 100kΩ on-chip resistors. Along with two external capacitors a 2nd order Sallen-Key low pass filter is formed. The selection of the capacitor values is described in Section 4.2.

3.4.8 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz. This allows for a maximum receive data rate of up to 100kBaud. The maximum achievable data rate also depends on the IF Filter bandwidth and the local oscillator tolerance values. Both inputs are accessible. The output delivers a digital data signal (CMOS-like levels) for sbsequent circuits. The self-adjusting threshold on pin 20 its generated by RC-term or peak detector depending on the baseband coding scheme. The data slicer threshold generation alternatives are described in more detail in Section 4.5.

3.4.9 Peak Detector

The peak detector generates a DC voltage which is proportional to the peak value of the receive data signal. An external RC network is necessary. The input is connected to the output of the RSSI-output of the Limiter, the output is connected to the **PDO** pin (Pin 26). This output can be used as an indicator for the received signal strength to use in wake-up circuits and as a reference for the data slicer in ASK mode. Note that the RSSI level is also output in case of FSK mode.

3.4.10 Bandgap Reference Circuitry

A Bandgap Reference Circuit provides a temperature stable reference voltage for the device. A power down mode is available to switch off all subcircuits which is controlled by the PWDN pin (Pin 27) as shown in the following table. The supply current drawn in this case is typically 50nA.

Table 3-5 PDWN Pin Operating States

PDWN	Operating State
Open or tied to ground	Powerdown Mode
Tied to Vs	Receiver On

4 Applications

Contents of this Chapter

4.1 Choice of LNA Threshold Voltage and Time Constant

In the following figure the internal circuitry of the LNA automatic gain control is shown.

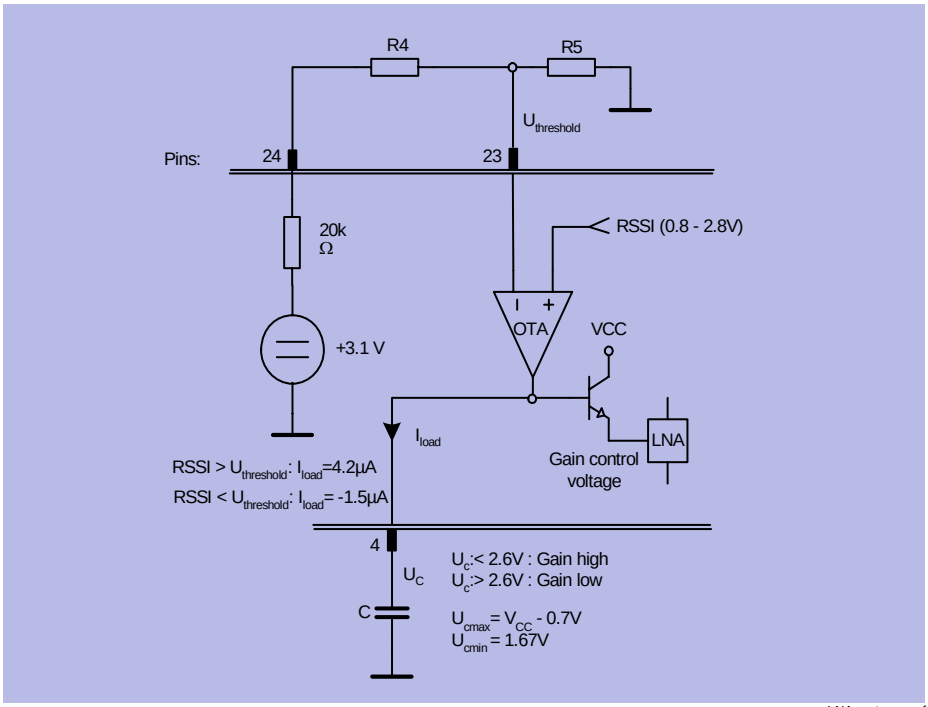


Figure 4-1 LNA Automatic Gain Control Circuitry

The LNA automatic gain control circuitry consists of an operational transimpedance amplifier that is used to compare the received signal strength signal (RSSI) generated by the Limiter with an externally provided threshold voltage U_{thres}. As shown in the following figure the threshold voltage can have any value between approximately 0.8 and 2.8V to provide a switching point within the receive signal dynamic range.

This voltage U_{thres} is applied to the **THRES** pin (Pin 23) The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin. If the RSSI level generated by the Limiter is higher than U_{thres}, the OTA generates a positive current I_{load}. This yields a voltage rise on the **TAGC** pin (Pin 4). Otherwise, the OTA generates a negative current. These currents do not have the same values in order to achieve a fast-attack and slow-release action of the AGC and are used to charge an external capacitor which finally generates the LNA gain control voltage.

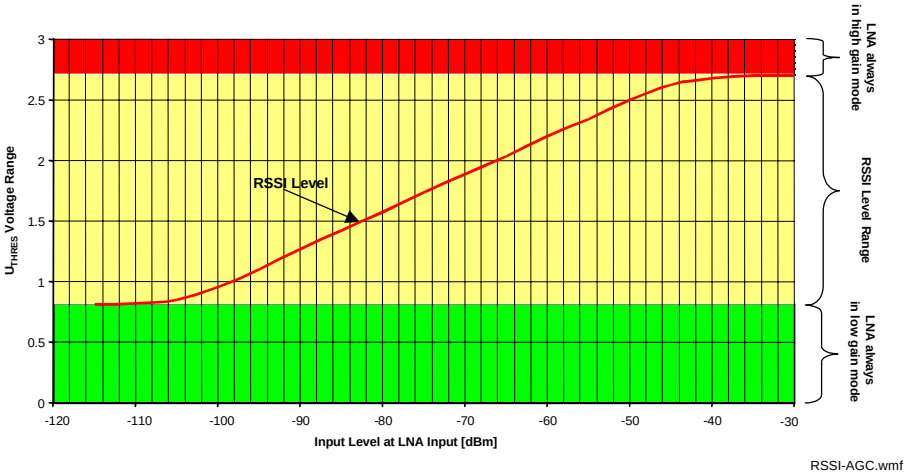


Figure 4-2 RSSI Level and Permissive AGC Threshold Levels

The switching point should be chosen according to the intended operating scenario. The determination of the optimum point is described in the accompanying Application Note, a threshold voltage level of 1.8V is apparently a viable choice. It should be noted that the output of the **3VOUT** pin is capable of driving up to 50µA, but that the **THRES** pin input current is only in the region of 40nA. As the current drawn out of the **3VOUT** pin is directly related to the receiver power consumption, the power divider resistors should have high impedance values. The sum of R1 and R2 has to be 600kΩ in order to yield 3V at the **3VOUT** pin. R1 can thus be chosen as 240kΩ, R2 as 360kΩ to yield an overall **3VOUT** output current of 5µA[1] and a threshold voltage of 1.8V

Note: If the LNA gain shall be kept in either high or low gain mode this has to be accomplished by tying the **THRES** pin to a fixed voltage. In order to achieve always high gain mode operation, a voltage higher than 3.3V shall be applied to the **THRES** pin. A short to the **3VOLT** pin will keep the LNA in high gain mode at least over a large RF-input level range. But to switch the LNA reliable into high gain mode over the whole RF-input level range, either a voltage higher than 3.3V has to be applied on pin 23 as mentioned above or, as alternative, a 330k resistor in parallel with a 47nF capacitor can be connected between pin 4 and GND. Whereas the capacitor should be placed as close as possible to pin 4. In order to achieve low gain mode operation a voltage lower than 0.7V shall be applied to the **THRES**, such as a short to ground.

As stated above the capacitor connected to the **TAGC** pin is generating the gain control voltage of the LNA due to the charging and discharging currents of the OTA and thus is also responsible for the AGC time constant. As the charging and discharging currents are not equal two different time constants will result. The time constant corresponding to the charging process of the capacitor shall be chosen according to the data rate. According to measurements performed at Infineon the capacitor value should be greater than 47nF.

1. note the 20kΩ resistor in series with the 3.1V internal voltage source

4.2 Data Filter Design

Utilising the on-board voltage follower and the two 100kΩ on-chip resistors a 2nd order Sallen-Key low pass data filter can be constructed by adding 2 external capacitors between pins 19 (SLP) and 22 (FFB) and to pin 21 (OPP) as depicted in the following figure and described in the following formulas[1].

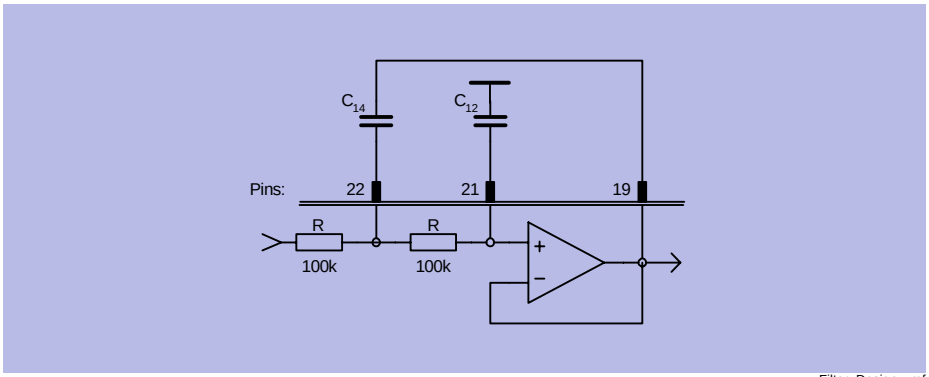


Figure 4-3 Data Filter Design

$$C14 = \frac{2Q\sqrt{b}}{R2\pi f_{3dB}} \qquad C12 = \frac{\sqrt{b}}{4QR\pi f_{3dB}}$$

with

$$Q = \frac{\sqrt{b}}{a}$$

the quality factor of the poles

where

in case of a Bessel filter a = 1.3617, b = 0.618

and thus Q = 0.577

and in case of a Butterworth filter a = 1.414, b = 1

and thus Q = 0.71

Example: Butterworth filter with f_{3dB} = 5kHz and R = 100kΩ:

C_{14} = 450pF, C_{12} = 225pF

1. taken from Tietze/Schenk: Halbleiterschaltungstechnik, Springer Berlin, 1999

4.3 Quartz Load Capacitance Calculation

The value of the capacitor necessary to achieve that the quartz oscillator is operating at the intended frequency is determined by the reactive part of the negative resistance of the oscillator circuit as shown in Section 5.1.3 and by the quartz specifications given by the quartz manufacturer.

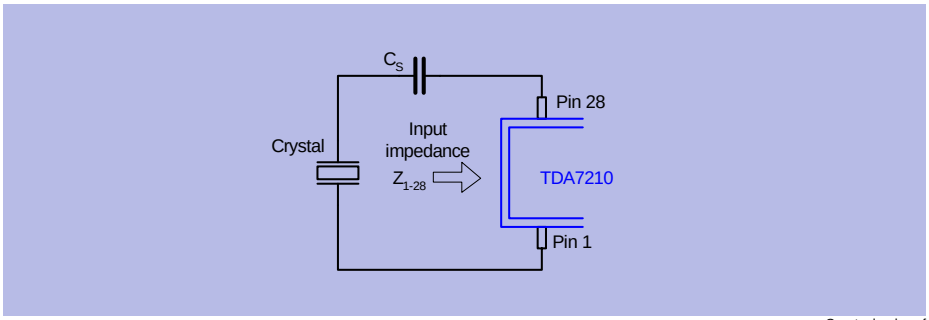


Figure 4-4 Determination of Series Capacitance Value for the Quartz Oscillator

Crystal specified with load capacitance

$$C_S = \frac{1}{\frac{1}{C_L} + 2\pi f X_L}$$

with C_L the load capacitance (refer to the quartz crystal specification).

Examples:

6.7 MHz: C_L = 12 pFX_L=695ΩC_S = 8.9 pF

13.4 MHz: C_L = 12 pFX_L=1010 ΩC_S = 5.9 pF

These values may be obtained in high accuracy by putting two capacitors in series to the quartz, such as 22pF and 15pF in the 6.7MHz case and 22pF and 8.2pF in the 13.4MHz case.

But please note that the calculated value of C_S includes the parasitic capacitors also.

4.4 Quartz Frequency Calculation

As described in Section 3.4.3 the operating range of the on-chip VCO is 820 to 860 MHz with a nominal center frequency of 840MHz. This signal is divided by 2 before applied to the mixer in case of operation at 434 MHz. This local oscillator signal can be used to downconvert the RF signals both with high- or low-side injection at the mixer. The resulting receive frequency ranges then extend between 810 and 870MHz or between 400 and 440MHz. Low-side injection of the local oscillator has to be used for receive frequencies between 840 and 870MHz as well as high-side injection for receive frequencies below 840MHz. Corresponding to that in the 400MHz region low-side injection is applicable for receive frequencies above 420MHz, high-side injection below this frequency. Therefore for operation both in the 868 and the 434 MHz ISM bands low-side injection of the local oscillator has to be used. Then the local oscillator frequency is calculated by subtracting the IF frequency (10.7 MHz) from the RF frequency (434 or 868 MHz). Please note that no sign-inversion occurs in case of reception and demodulation of FSK-modulated signals.

The overall division ratios in the PLL are 64 or 128 in case of operation at 868 MHz or 32 and 64 in case of operation at 434 MHz, depending on the crystal frequency used as shown below. The quartz frequency in case of low-side injection may be calculated by using the following formula:

$$f_{QU} = \frac{f_{RF} \pm 10.7}{r}$$

with f_{RF} receive frequency

f_{LO} local oscillator (PLL) frequency (f_{RF} ± 10.7)

f_{QU} quartz oscillator frequency

r ratio of local oscillator (PLL) frequency and quartz frequency as shown in the subsequent table

Table 4-1 Dependence of PLL Overall Division Ratio on FSEL and CSEL

FSEL	CSEL	Ratio r = (f_{LO}/f_{QU})
open	open	64
open	GND	32
GND	open	128
GND	GND	64

Example (low-side injection mode):

$$f_{QU} = (868.4MHz - 10.7MHz)/64 = 13.40156MHz$$

$$f_{QU} = (868.4MHz - 10.7MHz)/128 = 6.7008\,MHz$$

$$f_{QU} = (434.2\,MHz - 10.7MHz)/32 = 13.23437\,MHz$$

$$f_{QU} = (434.2\,MHz - 10.7MHz)/64 = 6.6172\,MHz$$

4.5 Data Slicer Threshold Generation

The threshold of the data slicer, especially for a coding scheme without DC-content, can be generated using an external R-C integrator as shown in Figure 4-5. The time constant T_A of the R-C integrator has to be significantly larger than the longest period of no signal change T_L within the data sequence. For the calculation of the time constant T_A please see Application Note „TDA521x-ANV1.1“, chapter „4.11 Data Slicer“. In order to keep distortion low, the minimum value for R1 is 20kΩ.

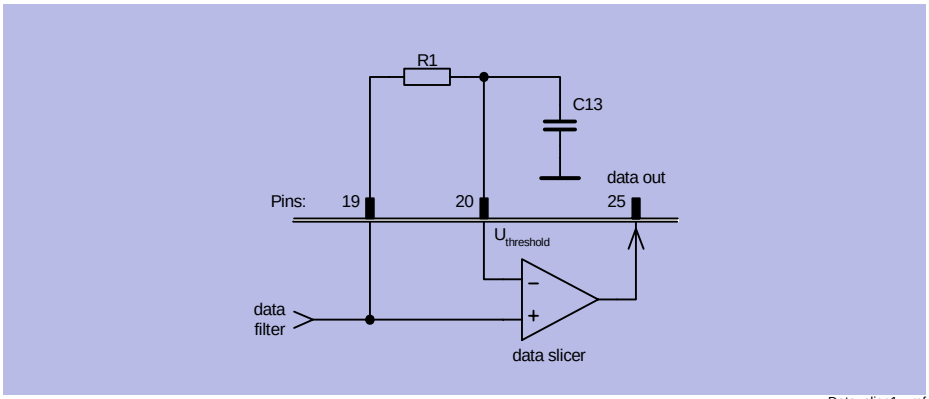


Figure 4-5 Data Slicer Threshold Generation with External R-C Integrator

In case of ASK operation another possibility for threshold generation is to use the peak detector in connection with two resistors and one capacitor as shown in the following figure. The component values are depending on the coding scheme and the protocol used.

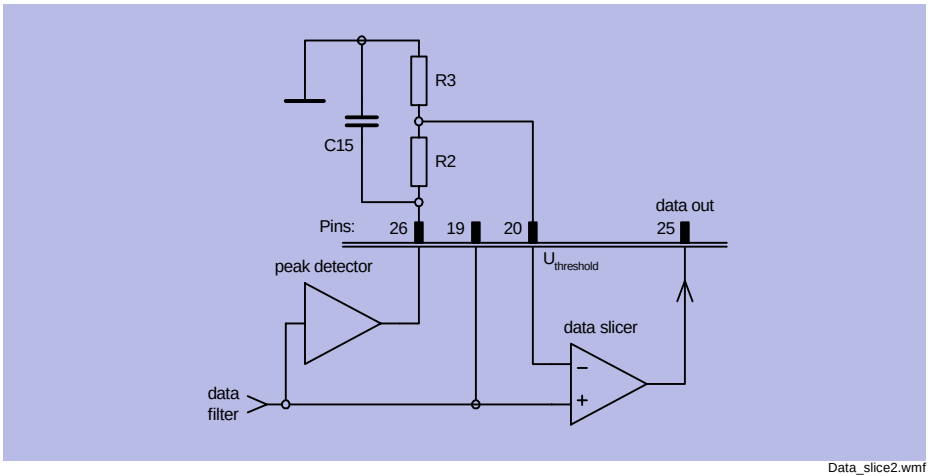


Figure 4-6 Data Slicer Threshold Generation Utilising the Peak Detector

4.6 ASK/FSK Switch Functional Description

The TDA7210 is containing an ASK/FSK switch which can be controlled via Pin 15 (MSEL). This switch is actually consisting of 2 operational amplifiers that are having a gain of 1 in case of the ASK amplifier and a gain of 11 in case of the FSK amplifier in order to achieve an appropriate demodulation gain characteristic. In order to compensate for the DC-offset generated especially in case of the FSK PLL demodulator there is a feedback connection between the threshold voltage of the bit slicer comparator (Pin 20) to the negative input of the FSK switch amplifier. This is shown in the following figure.

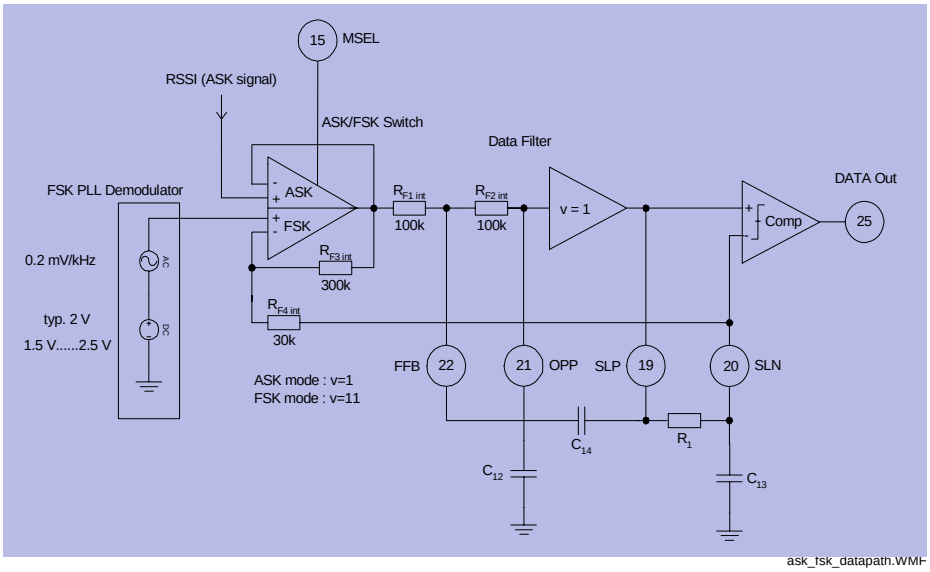


Figure 4-7 ASK/FSK mode datapath

4.6.1 FSK Mode

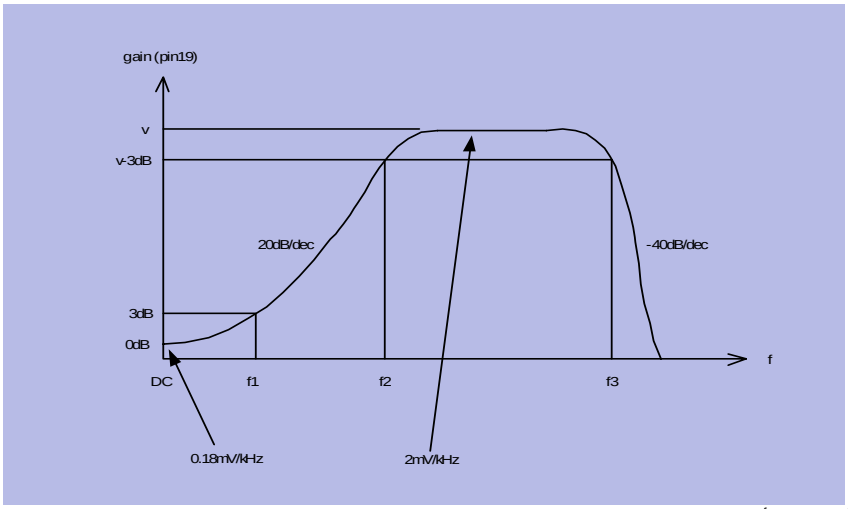
The FSK datapath has a bandpass characterisitc due to the feedback shown above (highpass) and the data filter (lowpass). The lower cutoff frequency f2 is determined by the external RC-combination. The upper cutoff frequency f3 is determined by the data filter bandwidth.

The demodulation gain of the FSK PLL demodulator is 200µV/kHz. This gain is increased by the gain v of the FSK switch, which is 11. Therefore the resulting dynamic gain of this circuit is 2.2mV/kHz within the bandpass. The gain for the DC content of FSK signal remains at 200µV/kHz. The cutoff frequencies of the bandpass have to be chosen such that the spectrum of the data signal is influenced in an acceptable amount.

In case that the user data is containing long sequences of logical zeroes the effect of the drift-off of the bit slicer threshold voltage can be lowered if the offset voltage inherent at the negative input of the slicer comparator (Pin20) is used. The comparator has no hysteresis built in.

This offset voltage is generated by the bias current of the negative input of the comparator (i.e. 20nA) running over the external resistor R1. This voltage raises the voltage appearing at pin 20 (e.g. 1mV with R1 = 100kΩ). In order to obtain benefit of this asymmetrical offset for the demodulation of long zeros the lower of the two FSK frequencies should be chosen in the transmitter as the zero-symbol frequency.

In the following figure the shape of the above mentioned bandpass is shown.



frequenzgang.WMF

Figure 4-8 Frequency characterstic in case of FSK mode

The cutoff frequencies are calculated with the following formulas:

$$f_1 = \frac{1}{2\pi \frac{R1 \cdot 330\,k\Omega}{R1 + 330\,k\Omega} \cdot C13}$$

$$f_2 = v \cdot f_1 = 11 \cdot f_1$$

$$f_3 = f_{3dB}$$

f_3 is the 3dB cutoff frequency of the data filter - see Section 4.2.

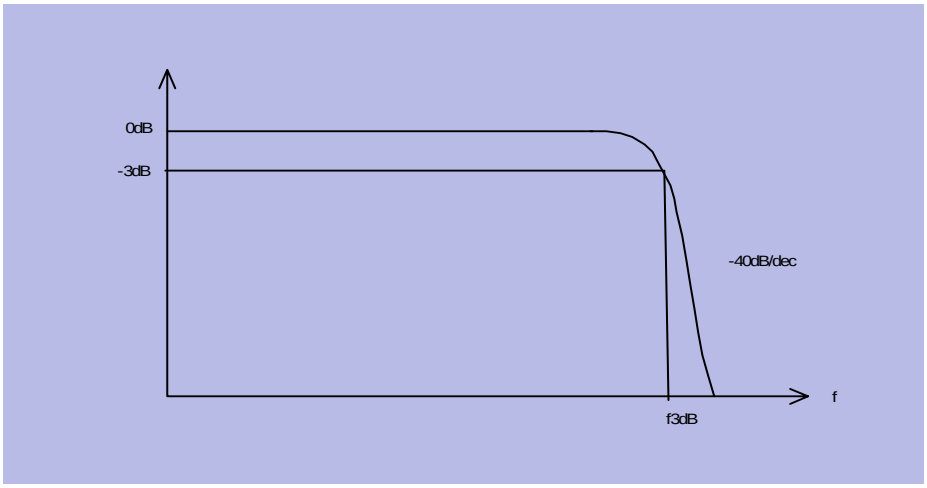
Example:

R1 = 100kΩ, C13 = 47nF

This leads to f_1 = 44Hz and f_2 = 485Hz

4.6.2 ASK Mode

In case the receiver is operated in ASK mode the datapath frequency charactersitic is dominated by the data filter alone, thus it is lowpass shaped.The cutoff frequency is determined by the external capacitors C12 and C14 and the internal 100k resistors as described in Section 4.2



freq_ask.WMF

Figure 4-9 Frequency charcteristic in case of ASK mode

4.7 Principle of the Precharge Circuit

In case the data slicer threshold shall be generated with an external RC network as described in Section 4.5 it is necessary to use large values for the capacitor C13 attached to the **SLN** pin (pin 20) in order to achieve long time constants. This results also from the fact that the choice of the value for R1 connected between the **SLP** and **SLN** pins (pins 19 and 20) is limited by the 330kΩ resistor appearing in parallel to R1 as can be seen in Figure 4-7. Apart from this a resistor value of 100kΩ leads to a voltage offset of 1mV at the comparator input as described in Section 4.6.1. The resulting startup time constant τ_1 can be calculated with:

$$\tau_1 = \left(R1 \parallel 330\ k\Omega\right) \times C13$$

In case R1 is chosen to be 100kΩ and C13 is chosen as 47nF this leads to

$$\tau_1 = \left(100k\Omega \parallel 330k\Omega\right) \times 47nF = 77k\Omega \times 47nF = 3.6ms$$

When the device is turned on this time constant dominates the time necessary for the device to be able to demodulate data properly. In the powerdown mode the capacitor is only discharged by leakage currents.

In order to reduce the turn-on time in the presence of large values of C13 a precharge circuit was included in the TDA7210 as shown in the following figure.

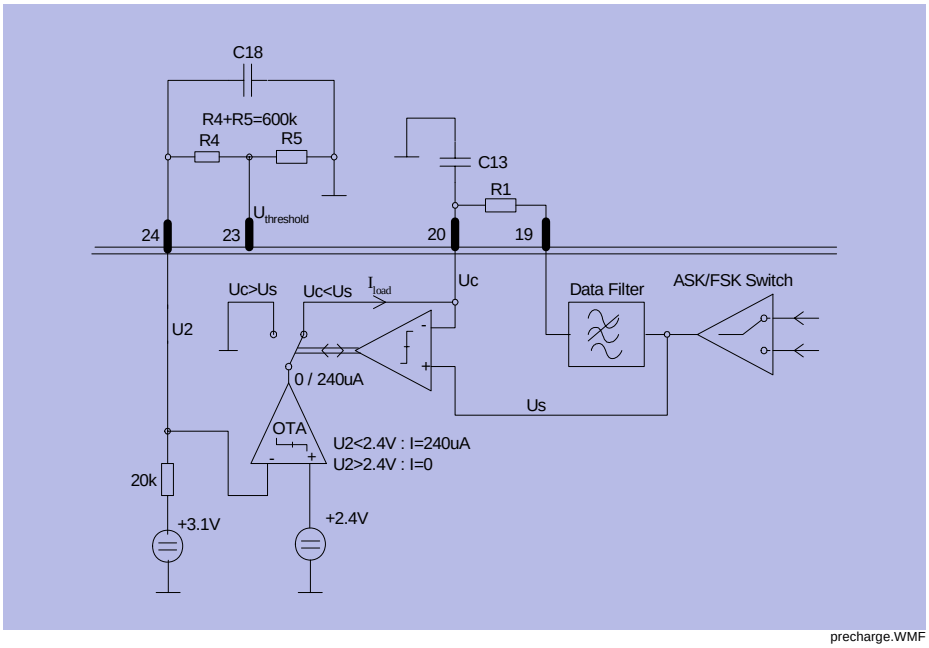


Figure 4-10 Principle of the precharge circuit

This circuit charges the capacitor C13 with an inrush current I_{load} of typically 220µA for a duration of T_2 until the voltage U_c appearing on the capacitor is equal to the voltage U_s at the input of the data filter. This voltage is limited to 2.5V. As soon as these voltages are equal or the duration T_2 is exceeded the precharge circuit is disabled.

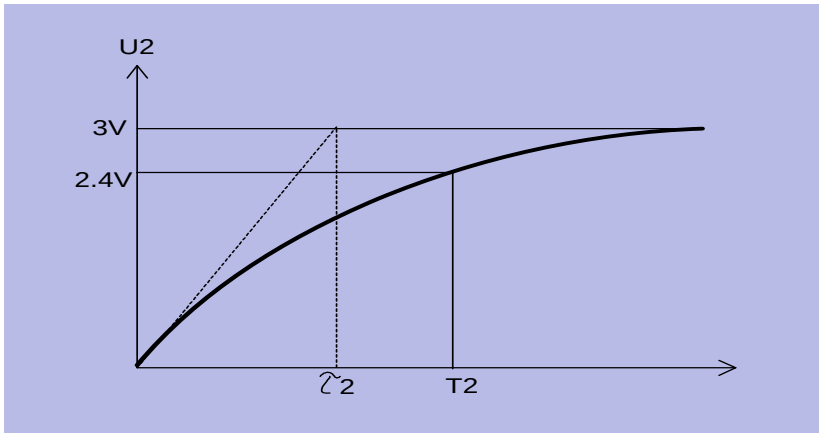
τ_2 is the time constant of the charging process of C18 which can be calculated as

$$\tau_2 = 20k\Omega \times C18$$

as the sum of R4 and R5 is sufficiently large and thus can be neglected. T2 can then be calculated according to the following formula:

$$T_l = \tau_2 \ln\left(\frac{1}{1-\frac{2.4V}{3V}}\right) \approx \tau_2 \times 1.6$$

The voltage transient during the charging of C18 is shown in the following figure:

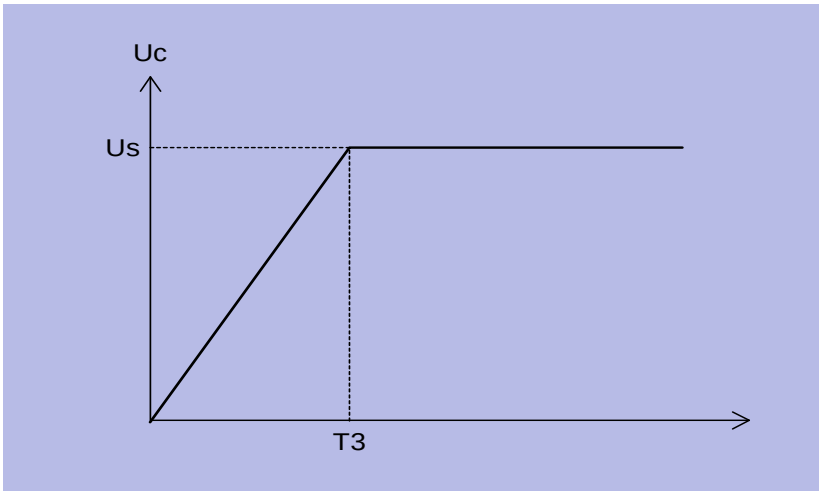


e-fkt1.WMF

Figure 4-11 Voltage appearing on C18 during precharging process

The voltage appearing on the capacitor C13 connected to pin 20 is shown in the following figure. It can be seen that due to the fact that it is charged by a constant current source it exhibits is a linear increase in voltage which is limited to U_{Smax} = 2.5V which is also the approximate operating point of the data filter input. The time constant appearing in this case can be denoted as T3, which can be calculated with

$$T3 = \frac{U_{Smax} \cdot C13}{220\mu A} = \frac{2{,}5V}{220\mu A} \cdot C13$$



e-Fkt2.WMF

Figure 4-12 Voltage transient on capacitor C13 attached to pin 20

As an example the choice of C18 = 22nF and C13 = 47nF yields

τ_2 = 0.44ms

T_2 = 0.71ms

T_3 = 0.53ms

This means that in this case the inrush current could flow for a duration of 0.64ms but stops already after 0.49ms when the U_{Smax} limit has been reached. T3 should always be chosen to be shorter than T2.

It has to be noted finally that during the turn-on duration T2 the overall device power consumption is increased by the 220µA needed to charge C13.

The precharge circuit may be disabled if C18 is not equipped. This yields a T2 close to zero. Note that the sum of R4 and R5 has to be 600kΩ in order to produce 3V at the THRES pin as this voltage is internally used also as the reference for the FSK demodulator.

5 Reference

Contents of this Chapter

5.1 Electrical Data

5.1.1 Absolute Maximum Ratings

WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Table 5-1 Absolute Maximum Ratings, Ambient temperature T_{AMB}=-40°C ... + 85°C

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min	max		
1	Supply Voltage	V_S	-0.3	5.5	V	
2	Junction Temperature	T_j	-40	+125	°C	
3	Storage Temperature	T_S	-40	+150	°C	
4	Thermal Resistance	R_{thJA}		114	K/W	
5	ESD integrity, all pins excl. Pins 1,3, 6, 28 ESD integrity Pins 1,3,6,28	V_{ESD}		+2 +1.5	kV kV	HBM according to MIL STD 883D, method 3015.7

5.1.2 Operating Range

Within the operational range the IC operates as explained in the circuit description. The AC/DC characteristic limits are not guaranteed. Currents flowing into the device are denoted as positive currents and v.v.

Supply voltage: V_{CC} = 4.5V .. 5.5V

Table 5-2 Operating Range, Ambient temperature T_{AMB}= -40°C ... + 85°C

#	Parameter	Symbol	Limit Values		Unit	Test Conditions / Notes	L	Item
			min	max				
1	Supply Current	$I_{SF\ 868}$ $I_{SF\ 434}$ $I_{SA\ 868}$ $I_{SA\ 434}$	4.1 3.9 3.4 3.2	7.7 7.5 7 6.8	mA mA mA mA	f_{RF} = 868MHz, FSK Mode f_{RF} = 434MHz, FSK Mode f_{RF} = 868MHz, ASK Mode f_{RF} = 434MHz, ASK Mode		
2	Receiver Input Level ASK FSK, frequ. dev. ± 50kHz	RF_{in}	 -106 -100	 -13 -13	 dBm dBm	@ source impedance 50Ω, BER 2E-3, average power level, Manchester encoded datarate 4kBit, 280kHz IF Bandwidth	■	
3	LNI Input Frequency	f_{RF}	400/ 810	440/ 870	MHz			
4	MI/X Input Frequency	f_{MI}	400/ 810	440/ 870	MHz			
5	3dB IF Frequency Range ASK FSK	$f_{IF\ -3dB}$	 5 10.4	 23 11	MHz		■	
6	Powerdown Mode On	$PWDN_{ON}$	0	0.8	V			
7	Powerdown Mode Off	$PWDN_{OFF}$	2	V_{CC}	V			
8	Gain Control Voltage, LNA high gain state	V_{THRES}	2.8	V_{CC}-1	V			
9	Gain Control Voltage, LNA low gain state	V_{THRES}	0	0.7	V			

■ Not part of the production test - either verified by design or measured in an Infineon Evalboard as described in 2.

5.1.3 AC/DC Characteristics at T_{AMB} = 25°C

AC/DC characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production. Currents flowing into the device are denoted as positive currents and vice versa. The device performance parameters marked with ■ are not part of the production test, but verified by design or measusured in an Infineon Evalboard as described in 2.

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{CC} = 4.5 ... 5.5 V

	Parameter	Symbol	Limit Values			Unit	Test Conditions / Notes	L	Item
			min	typ	max				
Supply									
Supply Current									
1	Supply current, standby mode	$I_{S\ PDWN}$		50	100	nA	Pin 27 (PDWN) open or tied to 0 V		
2	Supply current, device operating in 868 MHz range, FSK mode	$I_{SF\ 868}$	5.1	5.9	6.7	mA	Pin 11 (FSEL) tied to GND, Pin 15 (MSEL) tied to GND		
3	Supply current, device operating in 434 MHz range, FSK mode	$I_{SF\ 434}$	4.9	5.7	6.5	mA	Pin 11 (FSEL) open, Pin 15 (MSEL) tied to GND		
4	Supply current, device operating in 868 MHz range, ASK mode	$I_{SA\ 868}$	4.4	5.2	6	mA	Pin 11 (FSEL) tied to GND, Pin 15 (MSEL) open		
5	Supply current, device operating in 434 MHz range, ASK mode	$I_{SA\ 434}$	4.2	5	5.8	mA	Pin 11 (FSEL) open, Pin 15 (MSEL) open		
LNA									
Signal Input LNI (PIN 3), V_{THRES} > 3.3V, high gain mode									
1	Average Power Level at BER = 2E-3 (Sensitivity) ASK	RF_{in}		-110		dBm	Manchester encoded datarate 4kBit, 280kHz IF Bandwidth	■	
2	Average Power Level at BER = 2E-3 (Sensitivity) FSK	RF_{in}		-103		dBm	Manchester enc. datarate 4kBit, 280kHz IF Bandw., ± 50kHz pk. dev.	■	
3	Input impedance, f_{RF}=434 MHz	$S_{11\ LNA}$		0.873 / -34.7 deg				■	
4	Input impedance, f_{RF}=869 MHz	$S_{11\ LNA}$		0.738 / -73.5 deg				■	
5	Input level @ 1dB compression	$P1dB_{LNA}$		-15		dBm		■	
6	Input 3rd order intercept point f_{RF}=434 MHz	$IIP3_{LNA}$		-10		dBm	matched input	■	
7	Input 3rd order intercept point f_{RF}=869 MHz	$IIP3_{LNA}$		-14		dBm	matched input	■	

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{CC} = 4.5 ... 5.5 V (continued)

	Parameter	Symbol	Limit Values			Unit	Test Conditions / Notes	L	Item
			min	typ	max				
8	LO signal feedthrough at antenna port	LO_{LNI}			-73	dBm		■	
Signal Output LNO (PIN 6), V_{THRES} > 3.3V, high gain mode									
1	Gain f_{RF}=434 MHz	$S_{21\ LNA}$		1.509 / 138.2 deg				■	
2	Gain f_{RF}=869 MHz	$S_{21\ LNA}$		1.419 / 101.7 deg				■	
3	Output impedance, f_{RF}=434 MHz	$S_{22\ LNA}$		0.886 / -12.9 deg				■	
4	Output impedance, f_{RF}=869 MHz	$S_{22\ LNA}$		0.866 / -24.2 deg				■	
Signal Input LNI, V_{THRES} = GND, low gain mode									
1	Input impedance, f_{RF}=434 MHz	$S_{11\ LNA}$		0.899 / -35.4 deg				■	
2	Input impedance, f_{RF}=869 MHz	$S_{11\ LNA}$		0.772 / -80.2 deg				■	
3	Input level @ 1dB C. P f_{RF} = 434 MHz	$P1dB_{LNA}$		-18		dBm	matched input	■	
4	Input level @ 1dB C. P f_{RF} = 869 MHz	$P1dB_{LNA}$		-6		dBm	matched input	■	
5	Input 3rd order intercept point f_{RF}=434 MHz	$IIP3_{LNA}$		-10		dBm	matched input	■	
6	Input 3rd order intercept point f_{RF}=869 MHz	$IIP3_{LNA}$		-5		dBm	matched input	■	
Signal Output LNO, V_{THRES} = GND, low gain mode									
1	Gain f_{RF}=434 MHz	$S_{21\ LNA}$		0.183 / 140.6 deg				■	
2	Gain f_{RF}=869 MHz	$S_{21\ LNA}$		0.179 / 109.1deg				■	
3	Output impedance, f_{RF}=434 MHz	$S_{22\ LNA}$		0.897 / -13.6 deg				■	
4	Output impedance, f_{RF}=869 MHz	$S_{22\ LNA}$		0.868 / -26.3 deg				■	
Antenna to IFO, V_{THRES} > 3.3V, high gain mode									
1	Voltage Gain Antenna to IFO f_{RF}=434 MHz	$G_{Ant\text{-}IFO}$		42		dB			
2	Voltage Gain Antenna to IFO f_{RF}=869 MHz	$G_{Ant\text{-}IFO}$		40		dB			

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{CC} = 4.5 ... 5.5 V (continued)

	Parameter	Symbol	Limit Values			Unit	Test Conditions / Notes	L	Item
			min	typ	max				
Antenna to IFO, V_{THRES} = GND, low gain mode									
1	Voltage Gain Antenna to IFO f_{RF}=434 MHz	$G_{Ant-IFO}$		22		dB			
2	Voltage Gain Antenna to IFO f_{RF}=869 MHz	$G_{Ant-IFO}$		19		dB			
Signal 3VOUT (PIN 24)									
1	Output voltage	V_{3VOUT}	2.9	3.1	3.3	V	3VOUT Pin open		
2	Current out	I_{3VOUT}	-3	-5	-10	µA	see 2		
Signal THRES (PIN 23)									
1	Input Voltage range	V_{THRES}	0		V_{CC}-1	V	see 2		
2	LNA low gain mode	V_{THRES}	0			V			
3	LNA high gain mode	V_{THRES}	2.8[1]	3[1]	3.3[1]	V	voltage must not be higher than V_{CC}-1V		
4	Current in	I_{THRES_in}		5		nA		■	
Signal TAGC (PIN 4)									
1	Current out, LNA low gain state	I_{TAGC_out}	-3.6	-4.2	-5	µA	RSSI > V_{THRES}		
2	Current in, LNA high gain state	I_{TAGC_in}	1	1.5	2.2	µA	RSSI<V_{THRES}		
MIXER									
Signal Input MI/MIX (PINS 8/9)									
1	Input impedance, f_{RF}=434 MHz	$S_{11\ MIX}$	0.942 / -14.4 deg					■	
2	Input impedance, f_{RF}=869 MHz	$S_{11\ MIX}$	0.918 / -28.1 deg					■	
3	Input 3rd order intercept point f_{RF}=434 MHz	$IIP3_{MIX}$		-28		dBm		■	
4	Input 3rd order intercept point f_{RF}=869 MHz	$IIP3_{MIX}$		-26		dBm		■	
Signal Output IFO (PIN 12)									
1	Output impedance	Z_{IFO}		330		Ω		■	
2	Conversion Voltage Gain f_{RF}=434 MHz	G_{MIX}		+19		dB			
3	Conversion Voltage Gain f_{RF}=869 MHz	G_{MIX}		+18		dB			

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{CC} = 4.5 ... 5.5 V (continued)

	Parameter	Symbol	Limit Values			Unit	Test Conditions / Notes	L	Item
			min	typ	max				
LIMITER									
Signal Input LIM/X (PINS 17/18)									
1	Input Impedance	Z_{LIM}	264	330	396	Ω		■	
2	RSSI dynamic range	DR_{RSSI}	60		80	dB			
3	RSSI linearity	LIN_{RSSI}		±1		dB		■	
4	Operating frequency (3dB points)	f_{LIM}	5	10.7	23	MHz		■	
DATA FILTER									
1	Useable bandwidth	$BW_{BB\ FILT}$			100	kHz		■	
2	RSSI Level at Data Filter Output SLP, RF_{IN}=-103dBm	$RSSI_{low}$		1.1		V	LNA in high gain mode RF=868MHz		
3	RSSI Level at Data Filter Output SLP, RF_{IN}=-30dBm	$RSSI_{high}$		2.65		V	LNA in high gain mode RF=868MHz		
Slicer, Signal Output DATA (PIN 25)									
1	Maximum Datarate	DR_{max}			100	kBps	NRZ, 20pF capacitive loading	■	
2	LOW output voltage	V_{SLIC_L}	0		0.1	V			
3	HIGH output voltage	V_{SLIC_H}	V_{CC} -1.3	V_{CC}-1	V_{CC} -0.7	V	Output current =200µA		
Slicer, Signal SLN (PIN 20)									
1	Precharge Current Out	I_{PCH_SLN}	-100	-220	-300	µA	see 2		
PEAK DETECTOR									
Signal Output PDO (PIN 26)									
1	Load current	I_{load}	-500			µA	static load current must not exceed -500µA		
2	Leakage current	$I_{leakage}$	0	200	1000	nA			
CRYSTAL OSCILLATOR									
Signals CRSTL1, CRSTL 2, (PINS 1/28)									
1	Operating frequency	f_{CRSTL}	6		14	MHz	fundamental mode, series resonance		
2	Input Impedance @ ~6MHz	$Z_{1\text{-}28}$		-825 +j695		Ω		■	
3	Input Impedance @ ~13MHz	$Z_{1\text{-}28}$		-600 +j1010		Ω		■	
4	Serial Capacity @ ~6MHz	$C_{S\ 6}$=C1		8.9		pF			
5	Serial Capacity @ ~13MHz	C_{S13}=C1		5.9		pF			

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{CC} = 4.5 ... 5.5 V (continued)

	Parameter	Symbol	Limit Values			Unit	Test Conditions / Notes	L	Item
			min	typ	max				
ASK/FSK Signal Switch									
Signal MSEL (PIN 15)									
1	ASK Mode	V_{MSEL}	1.4		4[2]	V	or open		
2	FSK Mode	V_{MSEL}	0		0.2	V			
FSK DEMODULATOR									
1	Demodulation Gain	G_{FMDEM}		200		µV/ kHz			
2	Useable IF Bandwidth	BW_{IFPLL}	10.2	10.7	11.2	MHz			
POWER DOWN MODE									
Signal PDWN (PIN 27)									
1	Powerdown Mode On	$PWDN_{ON}$	2.8		V_{CC}	V			
2	Powerdown Mode Off	$PWDN_{Off}$	0		0.8	V			
3	Input bias current PDWN	I_{PDWN}		19		uA	Power On Mode		
4	Start-up Time until valid signal is detected at IF	T_{SU}		<1		ms	depends on the used crystal		
VCO MULTIPLEXER									
Signal FSEL (PIN 11)									
1	f_{RF} range 434 MHz	V_{FSEL}	1.4		4[2]	V	or open		
2	f_{RF} range 869 MHz	V_{FSEL}	0		0.2	V			
3	Output bias current FSEL	I_{FSEL}	-160	-200	-240	µA	FSEL tied to GND		
PLL DIVIDER									
Signal CSEL (PIN 16)									
1	f_{CRSTL} range 6.xxMHz	V_{CSEL}	1.4		4[2]	V	or open		
2	f_{CRSTL} range 13.xxMHz	V_{CSEL}	0		0.2	V			
3	Input bias current CSEL	I_{CSEL}	-3	-5	-7	µA	CSEL tied to GND		

■ Not part of the production test - either verified by design or measured in an Infineon Evalboard as described in 2.

1) 2.8V is the voltage which is at least required that the LNA of a device is in high gain mode over the whole RF-input level range. 3.3V is required that the LNA of each device is reliable in high gain mode over the whole RF-input level range (considering also the production spread).

2) Maximum voltage in Power-On state is 4V, but in PDWN-state the maximum voltage is 2.8V.

5.1.4 AC/DC Characteristics at T_{AMB} = -40 to 85°C

Currents flowing into the device are denoted as positive currents and vice versa

Table 5-4 AC/DC Characteristics with T_{AMB}= -40°C ... + 85°C, V_{CC} = 4.5 ... 5.5 V

	Parameter	Symbol	Limit Values			Unit	Test Conditions / Notes	L	Item
			min	typ	max				
Supply									
Supply Current									
1	Supply current, standby mode	$I_{S\ PDWN}$		50	400	nA	Pin 27 (PDWN) open or tied to 0 V		
2	Supply current, device operating in 868 MHz range, FSK mode	$I_{SF\ 868}$	4.1	5.9	7.7	mA	Pin 11 (FSEL) tied to GND, Pin 15 (MSEL) tied to GND		
3	Supply current, device operating in 434 MHz range, FSK mode	$I_{SF\ 434}$	3.9	5.7	7.5	mA	Pin 11 (FSEL) open, Pin 15 (MSEL) tied to GND		
4	Supply current, device operating in 868 MHz range, ASK mode	$I_{SA\ 868}$	3.4	5.2	7	mA	Pin 11 (FSEL) tied to GND, Pin 15 (MSEL) open		
5	Supply current, device operating in 434 MHz range, ASK mode	$I_{SA\ 434}$	3.2	5	6.8	mA	Pin 11 (FSEL) open, Pin 15 (MSEL) open		
Signal 3VOUT (PIN 24)									
1	Output voltage	V_{3VOUT}	2.9	3.1	3.3	V	3VOUT Pin open		
2	Current out	I_{3VOUT}	-3	-5	-10	µA	see 2		
Signal THRES (PIN 23)									
1	Input Voltage range	V_{THRES}	0		V_{CC}-1	V	see 2		
2	LNA low gain mode	V_{THRES}	0		0.3	V			
3	LNA high gain mode	V_{THRES}	2.8[1]	3[1]	3.3[1]	V	voltage must not be higher than V_{CC}-1V		
4	Current in	I_{THRES_in}		5		nA		■	
Signal TAGC (PIN 4)									
1	Current out, LNA low gain state	I_{TAGC_out}	-1	-4.2	-8	µA	RSSI > V_{THRES}		
2	Current in, LNA high gain state	I_{TAGC_in}	0.5	1.5	5	µA	RSSI < V_{THRES}		
MIXER									
1	Conversion Voltage Gain f_{RF}=434 MHz	G_{MIX}		+19		dB			
2	Conversion Voltage Gain f_{RF}=869 MHz	G_{MIX}		+18		dB			

Table 5-4 AC/DC Characteristics with T_{AMB}= -40°C ... + 85°C, V_{CC} = 4.5 ... 5.5 V

	Parameter	Symbol	Limit Values			Unit	Test Conditions / Notes	L	Item
			min	typ	max				
LIMITER									
Signal Input LIM/X (PINS 17/18)									
1	RSSI dynamic range	DR_{RSSI}	60		80	dB			
DATA FILTER									
2	RSSI Level at Data Filter Output SLP, RF_{IN}=-103dBm	$RSSI_{low}$		1.1		V	LNA in high gain mode		
3	RSSI Level at Data Filter Output SLP, RF_{IN}=-30dBm	$RSSI_{high}$		2.65		V	LNA in high gain mode		
Slicer, Signal Output DATA (PIN 25)									
1	Maximum Datarate	DR_{max}			100	kBps	NRZ, 20pF capacitive loading	■	
2	LOW output voltage	V_{SLIC_L}	0		0.1	V			
3	HIGH output voltage	V_{SLIC_H}	V_{CC} -1.5	V_{CC}-1	V_{CC} -0.5	V	Output current =200µA		
Slicer, Signal SLN (PIN 20)									
1	Precharge Current Out	I_{PCH_SLN}	-100	-220	-300	µA	see 2		
PEAK DETECTOR									
Signal Output PDO (PIN 26)									
1	Load current	I_{load}	-400			µA	static load current must not exceed -500µA		
2	Leakage current	$I_{leakage}$	0	700	2000	nA			
CRYSTAL OSCILLATOR									
Signals CRSTL1, CRSTL 2, (PINS 1/28)									
1	Operating frequency	f_{CRSTL}	6		14	MHz	fundamental mode, series resonance		
ASK/FSK Signal Switch									
Signal MSEL (PIN 15)									
1	ASK Mode	V_{MSEL}	1.4		4^2	V	or open		
2	FSK Mode	V_{MSEL}	0		0.2	V			
FSK DEMODULATOR									
1	Demodulation Gain	G_{FMDEM}		200		µV/ kHz			
2	Useable IF Bandwidth	BW_{IFPLL}	10.2	10.7	11.2	MHz			

Table 5-4 AC/DC Characteristics with T_{AMB}= -40°C ... + 85°C, V_{CC} = 4.5 ... 5.5 V

	Parameter	Symbol	Limit Values			Unit	Test Conditions / Notes	L	Item
			min	typ	max				
POWER DOWN MODE									
Signal PDWN (PIN 27)									
1	Powerdown Mode On	$PWDN_{ON}$	2.8		V_{CC}	V			
2	Powerdown Mode Off	$PWDN_{Off}$	0		0.8	V			
3	Start-up Time until valid signal is detected at IF	T_{SU}		<1		ms	depends on the used crystal		
VCO MULTIPLEXER									
Signal FSEL (PIN 11)									
1	f_{RF} range 434 MHz	V_{FSEL}	1.4		4[2]	V	or open		
2	f_{RF} range 869 MHz	V_{FSEL}	0		0.2	V			
3	Output bias current FSEL	I_{FSEL}	-110	-200	-340	µA	FSEL tied to GND		
PLL DIVIDER									
Signal CSEL (PIN 16)									
1	f_{CRSTL} range 6.xxMHz	V_{CSEL}	1.4		4[2]	V	or open		
2	f_{CRSTL} range 13.xxMHz	V_{CSEL}	0		0.2	V			
3	Input bias current CSEL	I_{CSEL}	-3	-5	-7	µA	CSEL tied to GND		

■ Not part of the production test - either verified by design or measured in an Infineon Evalboard as described in 2.

1) 2.8V is the voltage which is at least required that the LNA of a device is in high gain mode over the whole RF-input level range. 3.3V is required that the LNA of each device is reliable in high gain mode over the whole RF-input level range (considering also the production spread).

2) Maximum voltage in Power-On state is 4V, but in PDWN-state the maximum voltage is 2.8V.

5.2 Test Circuit

The device performance parameters marked with ■ in 2 were either verified by design or measured on an Infineon evaluation board. This evaluation board can be obtained together with evaluation boards of the accompanying transmitter device TDA7110 in an evaluation kit that may be ordered on the INFINEON Webpage www.infineon.com. In case a matching codeword is received, decoded and accepted by the decoder the on-board LED will turn on. This signal is also accessible on a 2-pole pin connector and can be used for simple remote-control applications. More information on the kit is available on request.

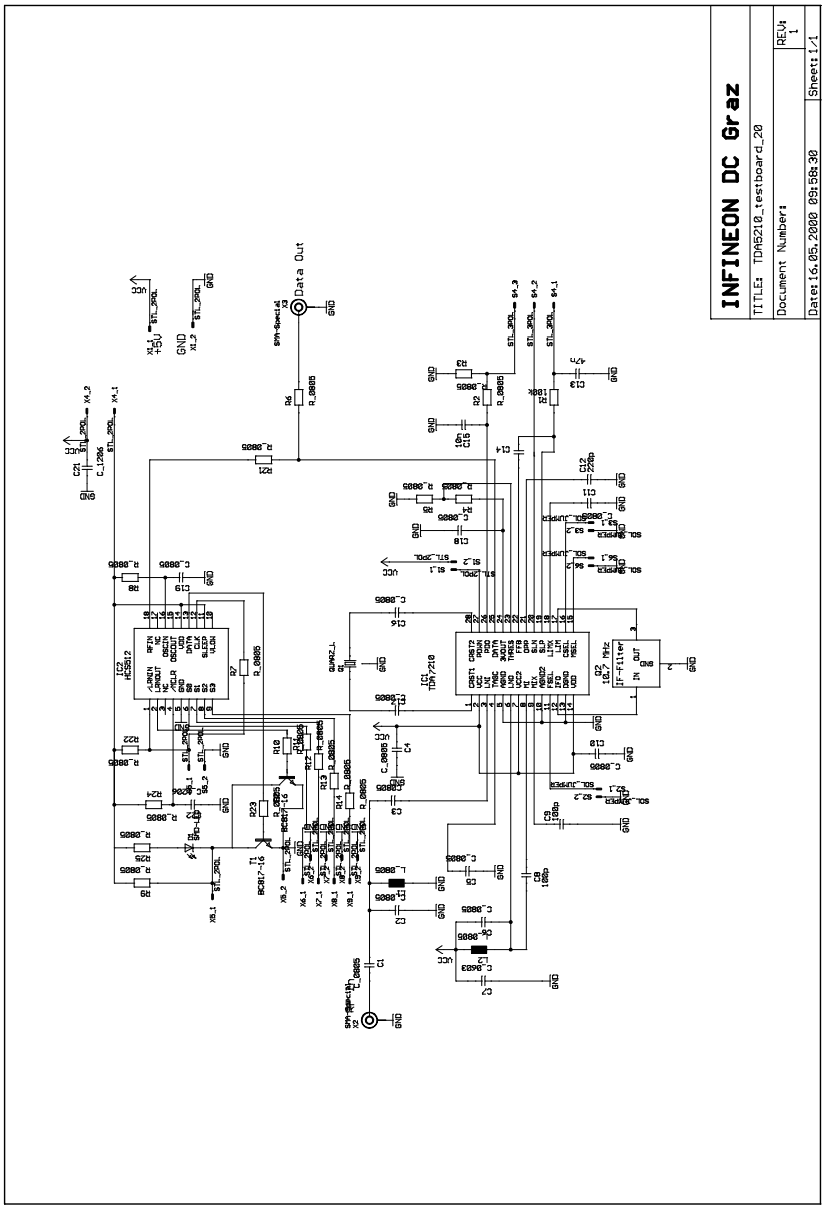
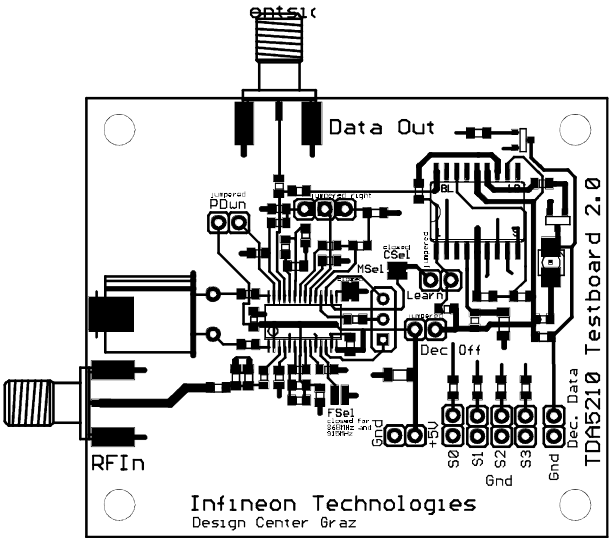


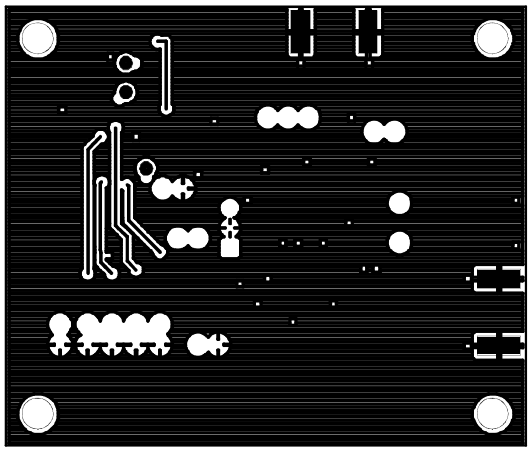
Figure 5-1 Schematic of the Evaluation Board

5.3 Test Board Layouts



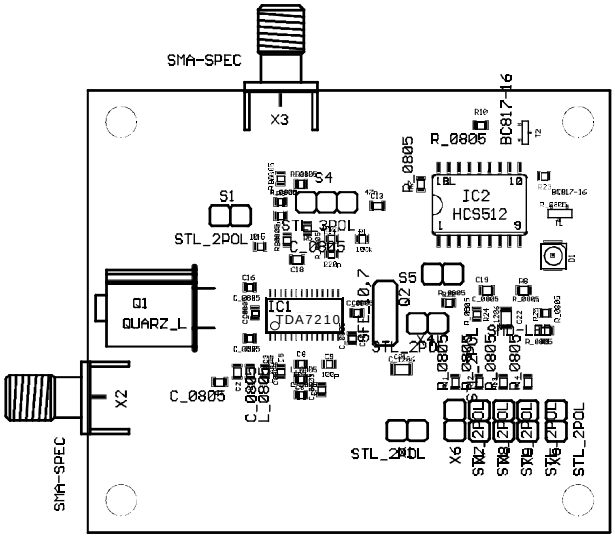
tda5210_testboard_20_top.WMF

Figure 5-2 Top Side of the Evaluation Board



tda5210_testboard_20_bot.WMF

Figure 5-3 Bottom Side of the Evaluation Board



tda5210_testboard_20_plc.EMF

Figure 5-4 Component Placement on the Evaluation Board

5.4 Bill of Materials

The following components are necessary for evaluation of the TDA7210 without use of a Microchip HCS512 decoder.

Table 5-5 Bill of Materials

Ref	Value	Specification
R1	100kΩ	0805, ± 5%
R2	100kΩ	0805, ± 5%
R3	820kΩ	0805, ± 5%
R4	240kΩ	0805, ± 5%
R5	360kΩ	0805, ± 5%
R6	10kΩ	0805, ± 5%
L1	434 MHz: 15nH 869 MHz: 3.3nH	Toko, PTL2012-F15N0G Toko, PTL2012-F3N3C
L2	434 MHz: 8.2pF 869 MHz: 3.9nH	0805, COG, ± 0.1pF Toko, PTL2012-F3N9C
C1	1pF	0805, COG, ± 0.1pF
C2	434 MHz: 4.7pF 869 MHz: 3.9pF	0805, COG, ± 0.1pF 0805, COG, ± 0.1pF
C3	434 MHz: 6.8pF 869 MHz: 5.6pF	0805, COG, ± 0.1pF 0805, COG, ± 0.1pF
C4	100pF	0805, COG, ± 5%
C5	47nF	1206, X7R, ± 10%
C6	434 MHz: 10nH 869 MHz: 3.9pF	Toko, PTL2012-F10N0G 0805, COG, ± 0.1pF
C7	100pF	0805, COG, ± 5%
C8	434 MHz: 33pF 869 MHz: 22pF	0805, COG, ± 5% 0805, COG, ± 5%
C9	100pF	0805, COG, ± 5%
C10	10nF	0805, X7R, ± 10%
C11	10nF	0805, X7R, ± 10%
C12	220pF	0805, COG, ± 5%
C13	47nF	0805, X7R, ± 10%
C14	470pF	0805, COG, ± 5%
C15	47nF	0805, X7R, ± 5%
C16	8.2pF	0805, COG, ± 0.1pF
C17	22pF	0805, COG, ± 1%
C18	22nF	0805, X7R, ± 5%
Q1	(f_{RF} – 10.7MHz)/32 or (f_{RF} – 10.7MHz)/64	HC49/U, fundamental mode, CL = 12pF, e.g. 434.2MHz: Jauch Q 13,23437-S11-1323-12-10/20 e.g. 868.4MHz: Jauch Q 13,40155-S11-1323-12-10/20

Q2	SFE10.7MA5-A or SKM107M1-A20-10	Murata Toko
X2, X3	142-0701-801	Johnson
S1-S3, S6 X1, X3		2-pole pin connector
S4		3-pole pin connector, or not equipped
IC1	TDA7210	Infineon

Please note that in case of operation at 434 MHz a capacitor has to be soldered in place L2 and an inductor in place C6.

The following components are necessary in addition to the above mentioned ones for evaluation of the TDA7210 in conjunction with a Microchip HCS512 decoder.

Table 5-6 Bill of Materials Addendum

Ref	Value	Specification
R7	100kΩ	0805, ± 5%
R8	10kΩ	0805, ± 5%
R9	100kΩ	0805, ± 5%
R10	22kΩ	0805, ± 5%
R11	100Ω	0805, ± 5%
R12	100Ω	0805, ± 5%
R13	100Ω	0805, ± 5%
R14	100Ω	0805, ± 5%
R21	22kΩ	0805, ± 5%
R22	10kΩ	0805, ± 5%
R23	22kΩ	0805, ± 5%
R24	820kΩ	0805, ± 5%
R25	560Ω	0805, ± 5%
C19	10pF	0805, COG, ± 5%
C21	100nF	1206, X7R, ± 10%
C22	100nF	1206, X7R, ± 10%
IC2	HCS512	Microchip
S5, X4-X9		2-pole pin connector
T1, T2	BC 847B	Infineon
D1	LS T670-JL	Infineon

List of Figures

List of Tables