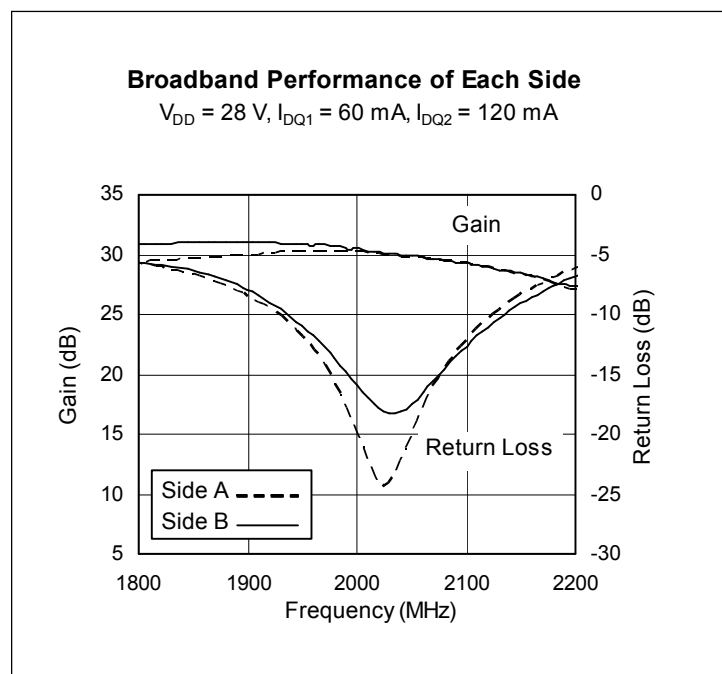


Dual Wideband RF LDMOS Power Amplifier 40 W, 1800 – 2200 MHz

Description

The PTMA210404FL integrates two wideband, 20-watt, 2-stage LDMOS integrated amplifiers into an open-cavity, ceramic package. It is designed for use in cellular amplifier applications in the 1800-2200 MHz frequency band. Manufactured with Infineon's advanced LDMOS process, this amplifier offers excellent thermal performance and superior reliability.

PTMA210404FL
Package H-34248-12



Features

- Designed for wide RF and modulation bandwidths and low memory effects
- Typical channel isolation = 26 dB
- Typical single channel performance CW, 2018 MHz, 28 V
 - Output power at P-1dB = 20 W
 - Linear Gain = 30.5 dB
 - Efficiency = 54%
- Typical Doherty performance with six-carrier TD-SCDMA signal, $V_{DD} = 28\text{ V}$, $I_{DQ1A} = I_{DQ1B} = 55\text{ mA}$, $I_{DQ2B} = 110\text{ mA}$, $V_{GS2A} = 1.06\text{ V}$, $f = 2018\text{ MHz}$
 - Average output power = 10 W
 - Linear Gain = 27 dB
 - Efficiency = 35%
 - ACLR1 = -33 dBc
 - ACLR2 = -34 dBc
- Capable of handling 10:1 VSWR @ 28 V, 50 W (CW) output power
- Integrated ESD protection. Meets HBM Class 1B (minimum), per JESD22-A114F
- High-performance, thermally-enhanced package, Pb-free and RoHS compliant, with low-gold plating

RF Characteristics

Six-carrier TD-SCDMA Measurements in Doherty Circuit (tested in Infineon test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ1A} = I_{DQ1B} = 55\text{ mA}$, $I_{DQ2B} = 110\text{ mA}$, $V_{GS2A} = 1.05\text{ V}$, $P_{OUT} = 10\text{ W}$ average, $f = 2018\text{ MHz}$, input PAR = 9.8 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	26	27	—	dB
Drain Efficiency	η_D	33	35	—	%
Adjacent Channel Power Ratio	ACPR	—	-33	-30	dBc
Alternate Channel Power Ratio	Alt	—	-34	-31	dBc

All published data at $T_{CASE} = 25^\circ\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

CW Measurements (tested in Infineon test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ1A} = I_{DQ1B} = 55\text{ mA}$, $I_{DQ2B} = 110\text{ mA}$, $V_{GS2A} = 1.05\text{ V}$, $f = 2018\text{ MHz}$

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Gain Flatness	1 W / 15 MHz	ΔG	—	0.30	—	dB
Gain Compression	40 W	—	—	-0.4	-1.0	dB

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	$V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1.0	μA
	$V_{DS} = 63\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	10.0	μA
Final Stage On-state Resistance	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)1}$	—	3.6	—	Ω
		$R_{DS(on)2}$	—	0.6	—	Ω
Operating Gate Voltage	$V_{DS} = 28\text{ V}$, $I_{DQ1} = 50\text{ mA}$, $I_{DQ2} = 120\text{ mA}$	V_{GS}	2.0	2.4	3.0	V
Gate Leakage Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}	—	—	1.0	μA

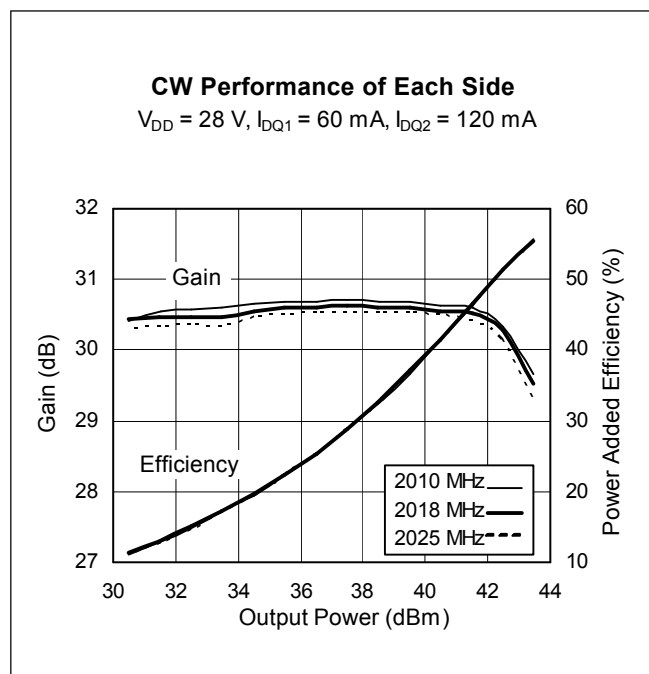
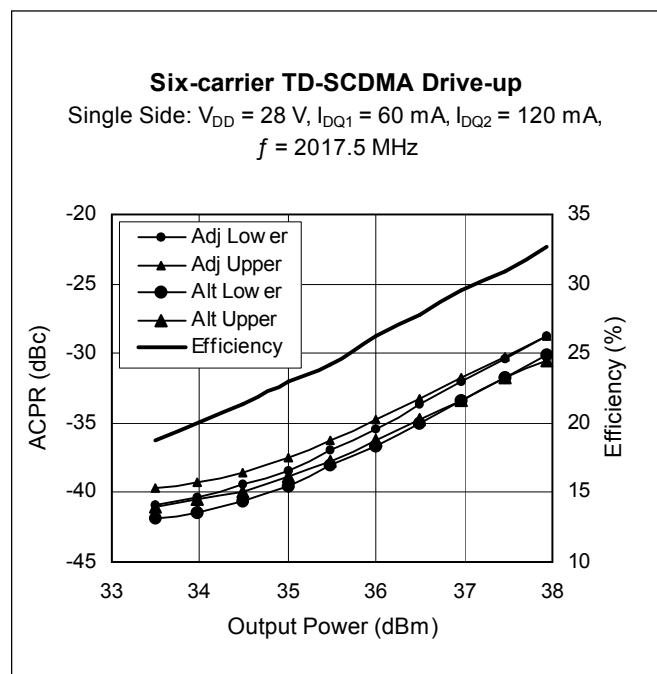
Maximum Ratings

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	65	V
Gate-Source Voltage		V_{GS}	-0.5 to +12	V
Junction Temperature		T_J	200	$^{\circ}\text{C}$
Input Power for CW - each side		P_{IN}	< 20	dBm
Total Device Dissipation	Stage 1	P_D	29	W
	Above 25 $^{\circ}\text{C}$ derate by		0.167	W/ $^{\circ}\text{C}$
	Stage 2	P_D	110	W
	Above 25 $^{\circ}\text{C}$ derate by		0.625	W/ $^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-40 to +150	$^{\circ}\text{C}$
Thermal Resistance ($T_{CASE} = 70^{\circ}\text{C}$)	Stage 1	$R_{\theta JC}$	6.0	$^{\circ}\text{C/W}$
	Stage 2	$R_{\theta JC}$	1.6	$^{\circ}\text{C/W}$

Ordering Information

Type and Version	Package Outline	Flange Type	Shipping	Marking
PTMA210404FL V1	H-34248-12	Earless flange	Tray	PTMA210404FL
PTMA210404FL V1 R250	H-34248-12	Earless flange	Tape & Reel 250 pcs	PTMA210404FL

Typical Performance (data taken in a production test fixture)

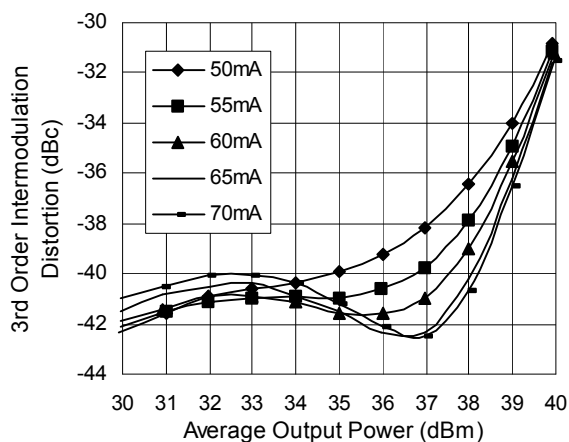


Typical Performance (cont.)

Two-tone Performance at Various I_{DQ1}

Single Side, $f = 2018$ MHz

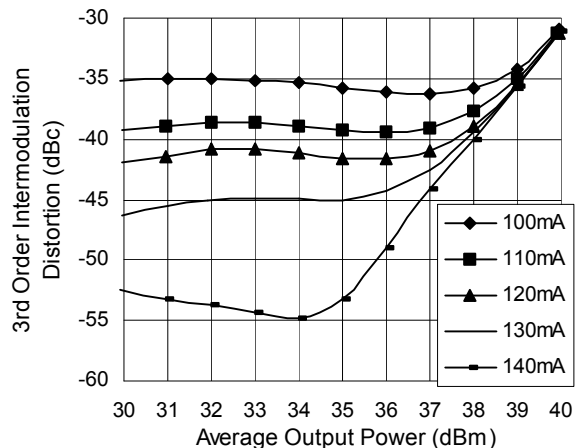
$V_{DD} = 28$ V, $I_{DQ1} = \text{Varying}$, $I_{DQ2} = 120$ mA



Two-tone Performance at Various I_{DQ2}

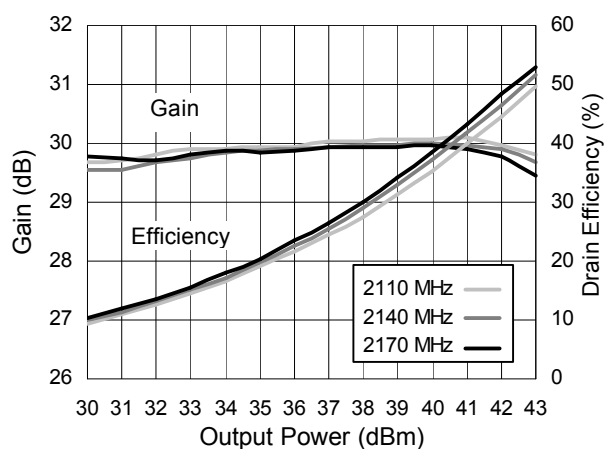
Single Side, $f = 2018$ MHz

$V_{DD} = 28$ V, $I_{DQ1} = 60$ mA, $I_{DQ2} = \text{Varying}$



CW Sweep at P_{-1dB}

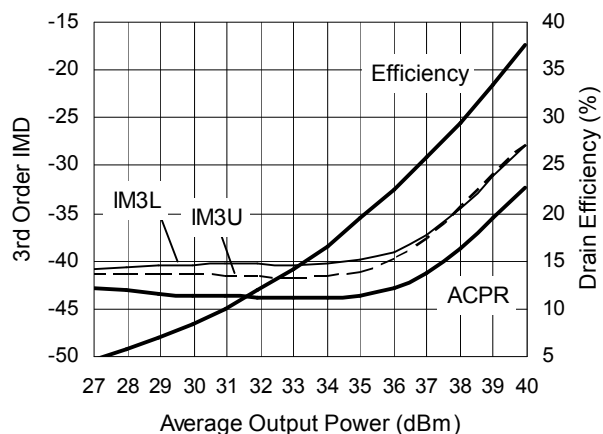
$V_{DD1} = V_{DD2} = 28$ V, $I_{DQ1} = 50$ mA, $I_{DQ2} = 120$ mA



Two-carrier WCDMA Performance

$V_{DD1} = V_{DD2} = 28$ V, $I_{DQ1} = 60$ mA, $I_{DQ2} = 260$ mA

10 MHz Spacing, 8 dB PAR, $f = 2140$ MHz

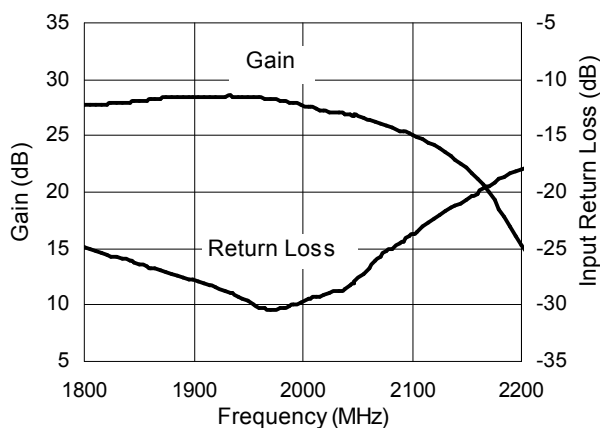


Typical Performance (cont.)

Broadband Performance

Doherty Circuit

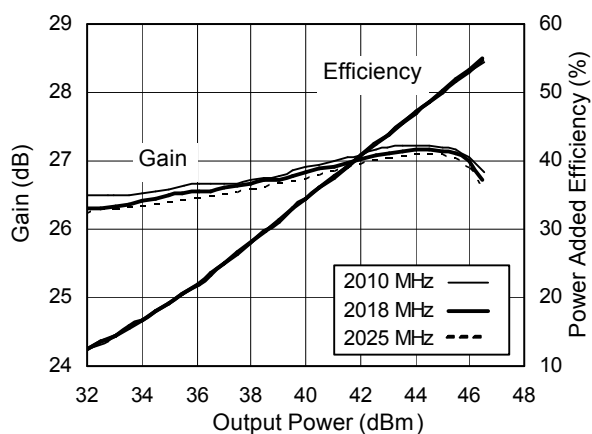
Carrier: $V_{DD} = 28\text{ V}$, $I_{DQ1} = 55\text{ mA}$, $I_{DQ2} = 120\text{ mA}$

Peak: $V_{DD} = 28\text{ V}$, $I_{DQ1} = 55\text{ mA}$, $V_{GS2} = 1.07\text{ V}$


CW Performance

Doherty Circuit,

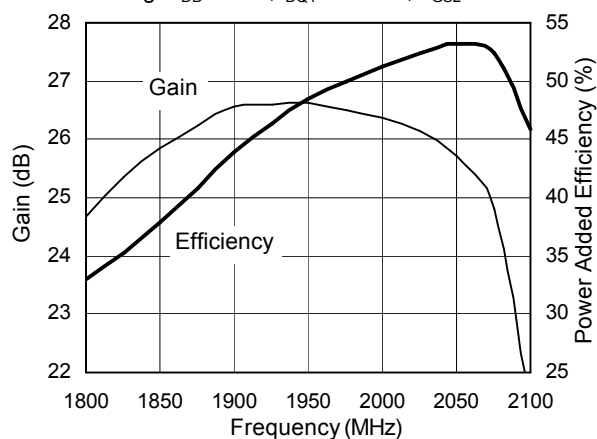
Carrier: $V_{DD} = 28\text{ V}$, $I_{DQ1} = 55\text{ mA}$, $I_{DQ2} = 120\text{ mA}$

Peaking: $V_{DD} = 28\text{ V}$, $I_{DQ1} = 55\text{ mA}$, $V_{GS2} = 1.07\text{ V}$


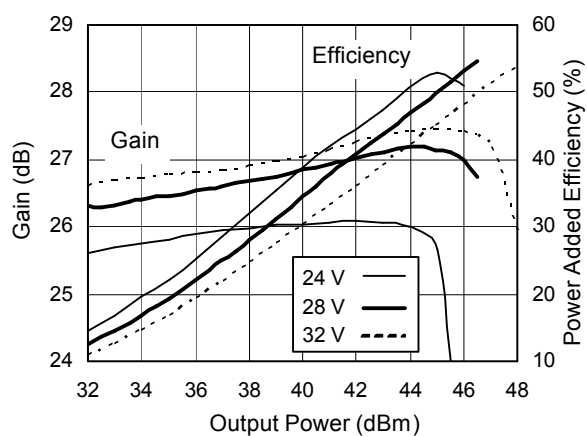
Power Gain vs Frequency

Doherty Circuit, CW, 40W

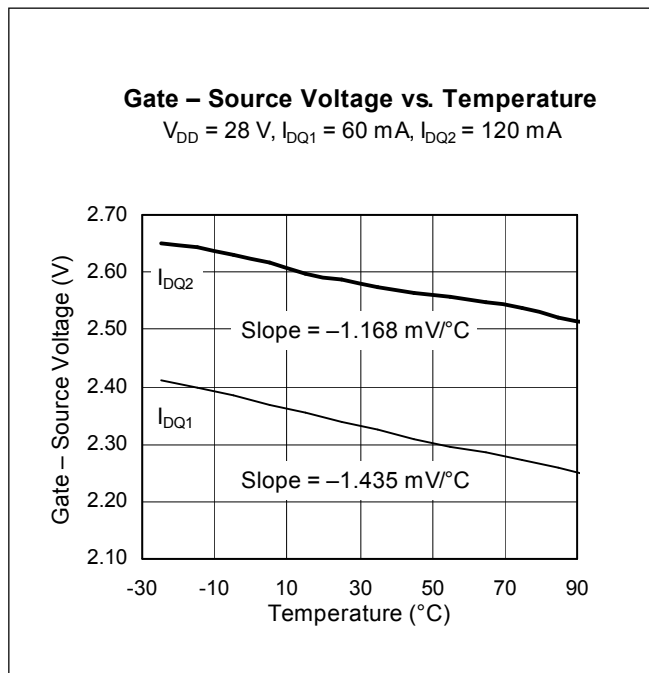
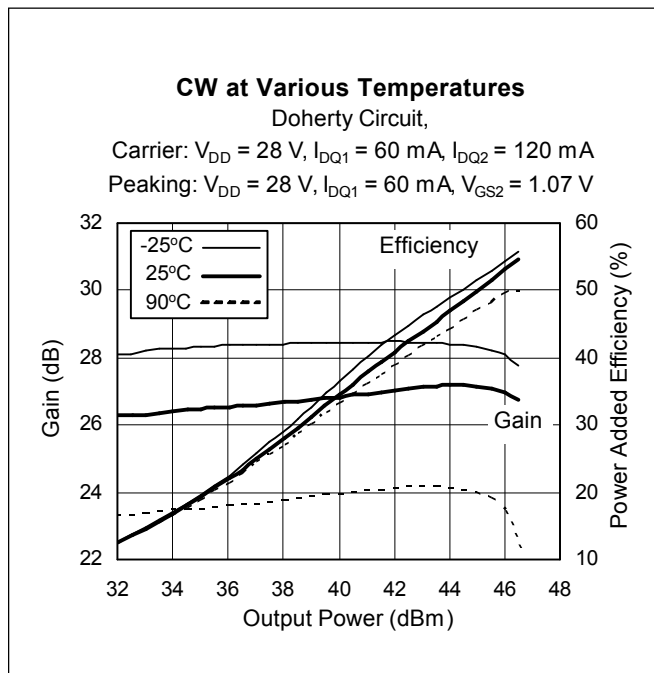
Carrier: $V_{DD} = 28\text{ V}$, $I_{DQ1} = 60\text{ mA}$, $I_{DQ2} = 120\text{ mA}$

Peaking: $V_{DD} = 28\text{ V}$, $I_{DQ1} = 60\text{ mA}$, $V_{GS2} = 1.07\text{ V}$


CW at Various Drain Voltage

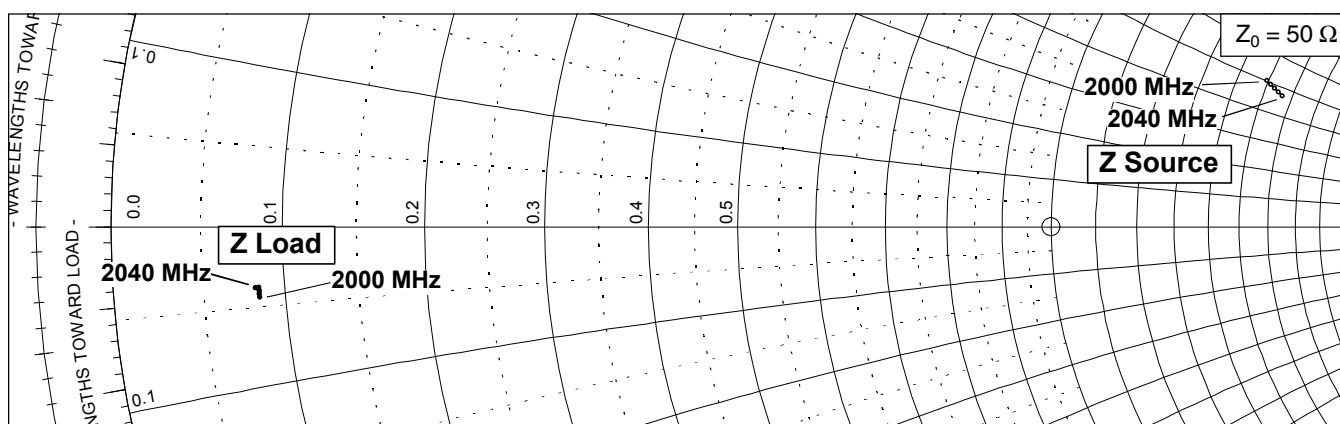
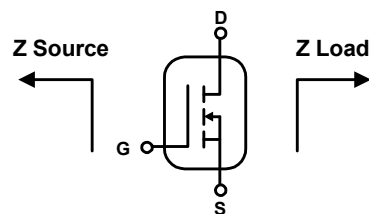
Doherty Circuit, $f = 2018\text{ MHz}$


Typical Performance (cont.)

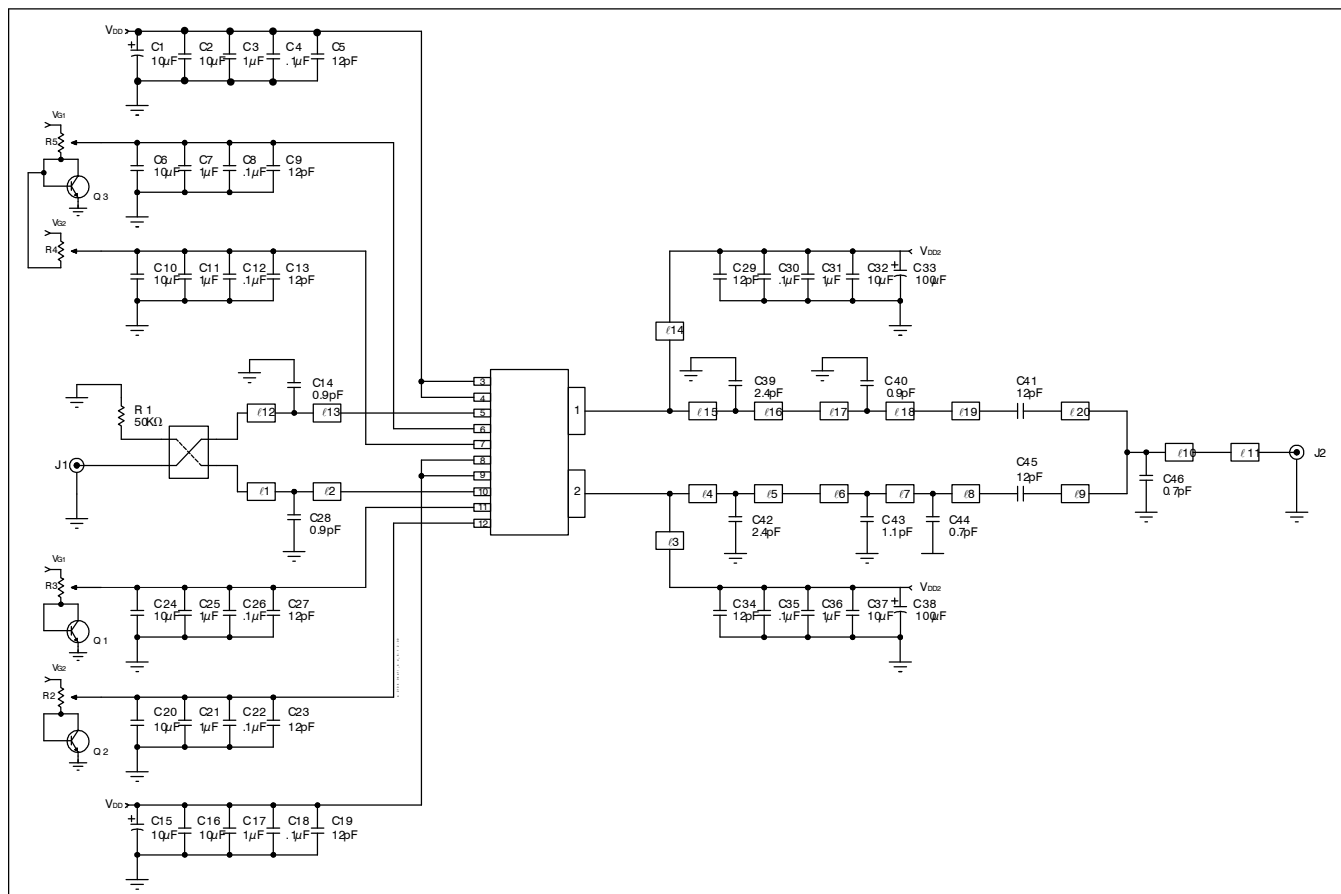


Broadband Circuit Impedance

Frequency MHz	Z Source W		Z Load W	
	R	jX	R	jX
2000	74.7	25.2	4.2	-2.2
2010	75.6	24.9	4.2	-2.1
2020	76.5	24.5	4.2	-2.0
2030	77.4	24.1	4.2	-1.9
2040	78.3	23.7	4.1	-1.9



Reference Circuit



Reference circuit block diagram for $f = 2017.5 \text{ MHz}$

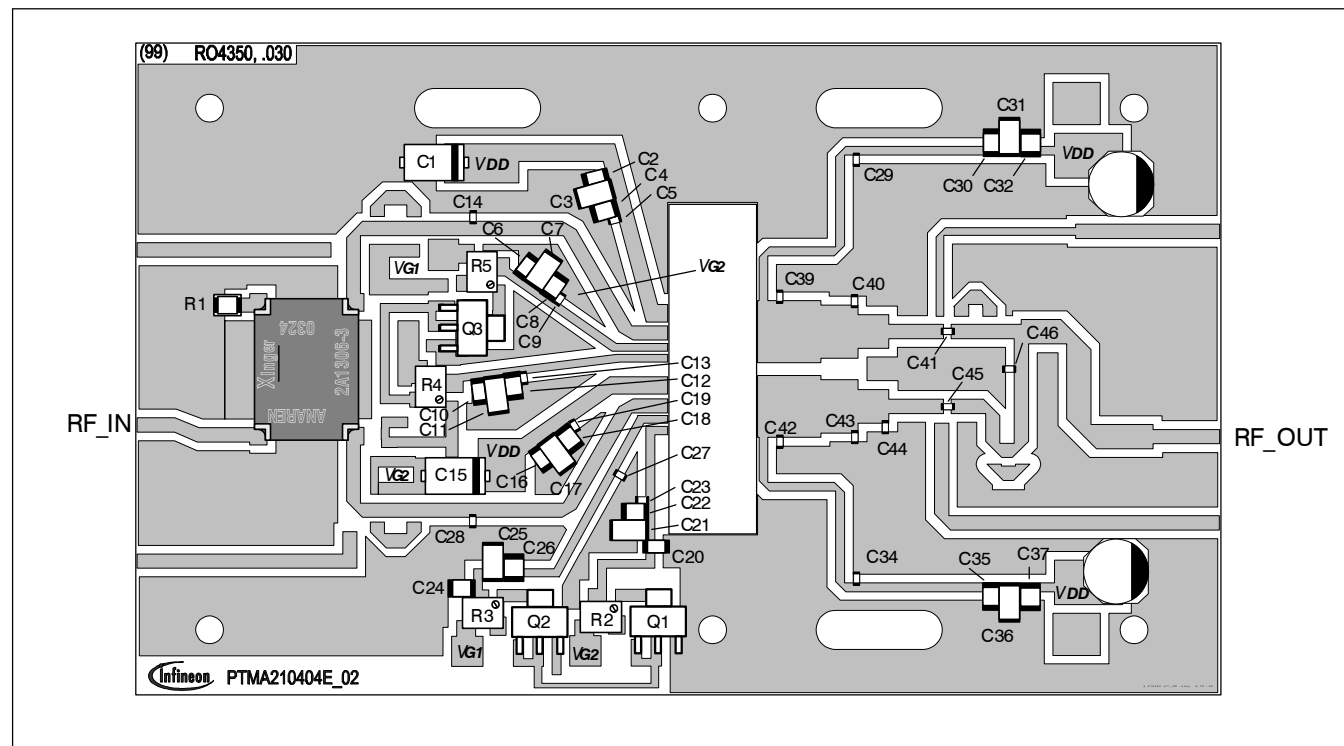
Reference Circuit (cont.)

Circuit Assembly Information

DUT	PTMA210404FL	LDMOS IC	
PCB	0.76 mm [.030"] thick, $\epsilon_r = 3.48$	Rogers RO4350	1 oz. copper

Microstrip	Electrical Characteristics at 2017.5 MHz	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ_1	0.285 λ , 51.0 Ω	25.68 x 1.63	1.011 x 0.064
ℓ_2	0.302 λ , 51.0 Ω	27.23 x 1.63	1.072 x 0.064
ℓ_3	0.311 λ , 67.0 Ω	28.58 x 1.02	1.125 x 0.040
ℓ_4	0.031 λ , 17.2 Ω	2.59 x 7.24	0.102 x 0.285
ℓ_5	0.056 λ , 17.2 Ω	4.75 x 7.24	0.187 x 0.285
ℓ_6	0.051 λ , 19.5 Ω	4.29 x 6.22	0.169 x 0.245
ℓ_7	0.043 λ , 28.0 Ω	3.71 x 3.94	0.146 x 0.155
ℓ_8	0.071 λ , 51.0 Ω	6.43 x 1.63	0.253 x 0.064
ℓ_9	0.239 λ , 51.0 Ω	21.54 x 1.63	0.848 x 0.064
ℓ_{10}	0.289 λ , 33.0 Ω	24.54 x 3.15	0.966 x 0.124
ℓ_{11}	0.086 λ , 51.0 Ω	7.75 x 1.63	0.305 x 0.064
ℓ_{12}	0.285 λ , 51.0 Ω	25.68 x 1.63	1.011 x 0.064
ℓ_{13}	0.302 λ , 51.0 Ω	27.23 x 1.63	1.072 x 0.064
ℓ_{14}	0.311 λ , 67.0 Ω	28.58 x 1.02	1.125 x 0.040
ℓ_{15}	0.031 λ , 17.2 Ω	2.59 x 7.24	0.102 x 0.285
ℓ_{16}	0.056 λ , 17.2 Ω	4.75 x 7.24	0.187 x 0.285
ℓ_{17}	0.051 λ , 19.5 Ω	4.29 x 6.22	0.169 x 0.245
ℓ_{18}	0.043 λ , 28.0 Ω	3.71 x 3.94	0.146 x 0.155
ℓ_{19}	0.071 λ , 51.0 Ω	6.43 x 1.63	0.253 x 0.064
ℓ_{20}	0.140 λ , 51.0 Ω	12.65 x 1.63	0.498 x 0.064

Reference Circuit (cont.)



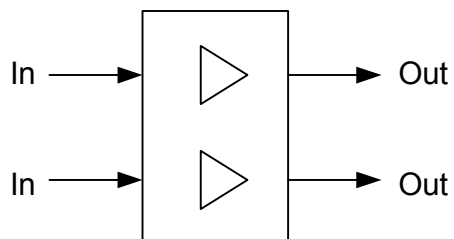
Reference circuit assembly diagram (not to scale)*

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C15	Tantalum Capacitor, 10 μ F, 35 V	Digi-Key	399-1655-2-ND
C2, C6, C10, C15, C20, C24, C32, C37	Ceramic Capacitor, 10 μ F	Digi-Key	490-1891-2-ND
C3, C7, C11, C17, C21, C25, C31, C36	Ceramic Capacitor, 1 μ F	Digi-Key	445-1411-2-ND
C4, C8, C12, C18, C22, C26, C30, C35	Capacitor, 0.1 μ F	Digi-Key	399-1267-2-ND
C5, C9, C13, C19, C23, C27, C29, C34, C41, C45	Ceramic Capacitor, 12 pF	ATC	600S120JT
C14, C28, C40	Ceramic Capacitor, 0.9 pF	ATC	600S0R9BT
C33, C38	Electrolytic Capacitor, 100 μ F, 35 V	Digi-Key	PCE3373TR-ND
C39, C42	Ceramic Capacitor, 2.4 pF	ATC	600S2R4BT
C43	Ceramic Capacitor, 1.1 pF	ATC	600S1R1BT
C44, C46	Ceramic Capacitor, 0.7 pF	ATC	600S0R7BT
Q1, Q2, Q3	Transistor	Infineon Technologies	BCP56
R1	Chip Resistor, 50 ohms	Digi-Key	RFP100200-4Y502
R2, R3, R4, R5	Potentiometer, 2 k-ohms	Digi-Key	3224W-202ETR-ND

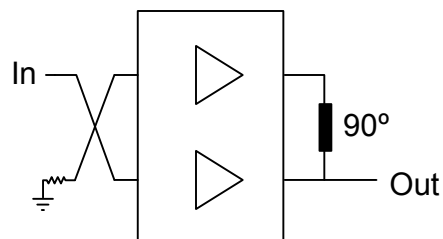
*Gerber Files for this circuit available on request

Application Examples

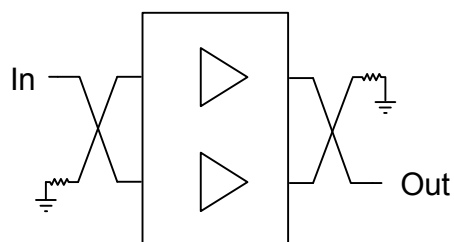
Single - ended



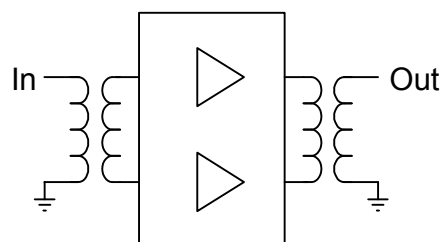
Doherty



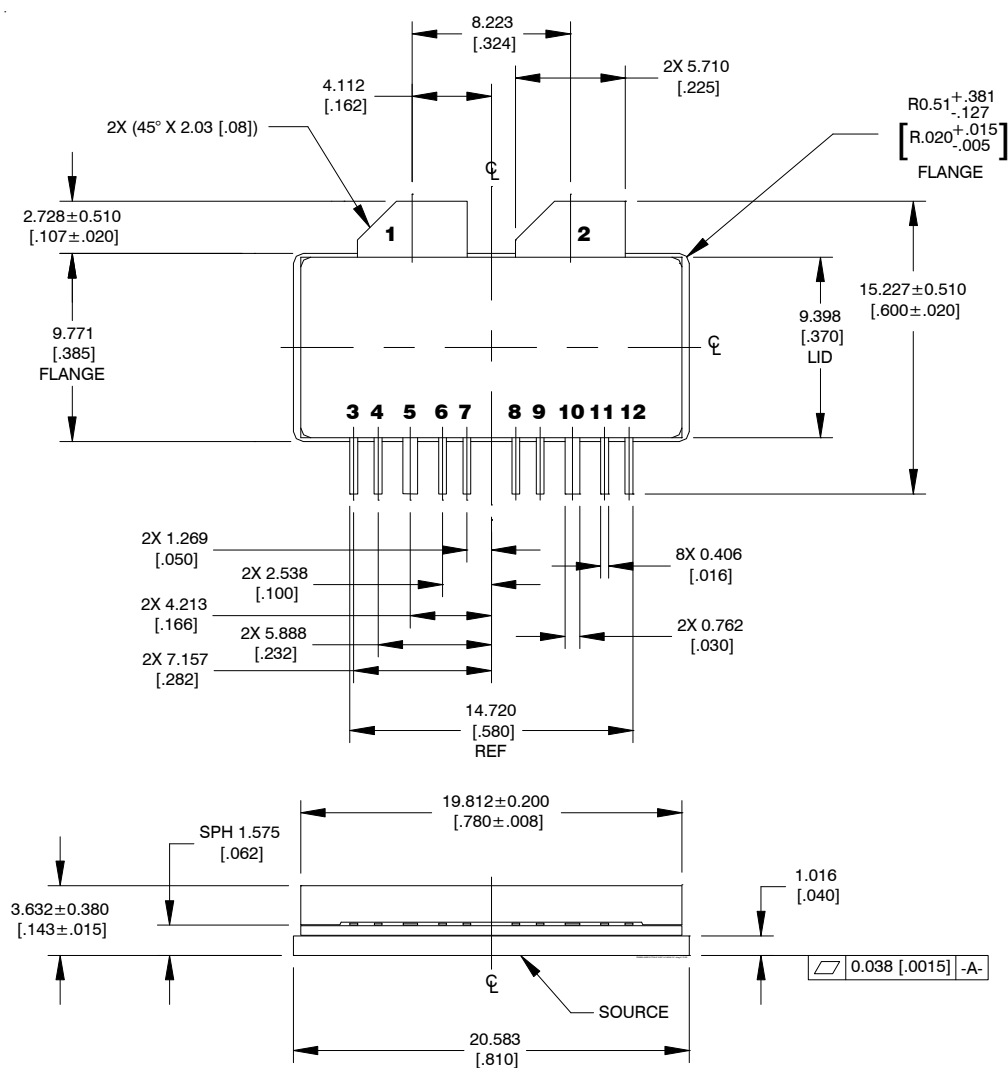
Quadrature Combined



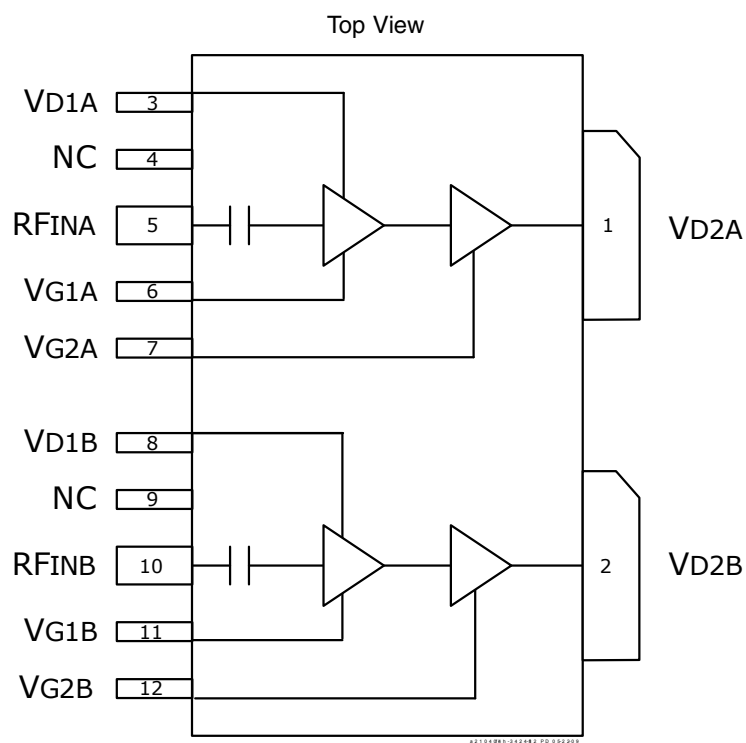
Push-pull



Package H-34248-12 Outline



1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
7. All tolerances ± 0.127 [.005] unless specified otherwise.
4. Lead thickness: $0.102 +0.051/-0.025$ [.004 +.002/-.001].
5. Gold plating thickness: 0.254 micron [10 microinch] max.

Package Specifications (cont.)
Package H-34248-12 Pinout


Source: Package Flange

Find the latest and most complete information about products and packaging at the Infineon Internet page
<http://www.infineon.com/rfpower>

Revision History: 2009-06-16 Data Sheet
Previous Version: 2009-06-05, Preliminary Data Sheet

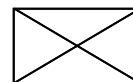
Page	Subjects (major changes since last revision)
all	Remove Preliminary designation
7, 8, 9	Add reference circuit information
11	Finalize package information

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Any information within this document that you feel is wrong, unclear or missing at all?
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Please send your proposal (including a reference to this document) to:

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