STGIPL14K60

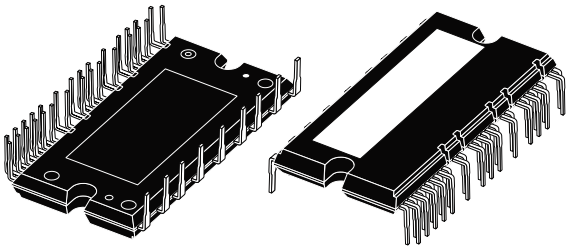
IGBT intelligent power module (IPM)
14 A, 600 V, DBC isolated SDIP-38L molded

Features

- 14 A, 600 V 3-phase IGBT inverter bridge including control ICs for gate driving and free-wheeling diodes
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull down/pull up resistors
- Internal bootstrap diode
- Interlocking function
- 5 kΩ NTC for temperature control
- $V_{CE(sat)}$ negative temperature coefficient
- Short-circuit rugged IGBTs
- Under-voltage lockout
- DBC fully isolated package
- Isolation rating of 2500 Vrms/min
- Smart shut down function
- Op-amps for advanced current sensing
- Comparators for fault protection against over current and short-circuit

Applications

- 3-phase inverters for motor drives
- Home appliances, such as washing machines, refrigerators, air conditioners



SDIP-38L

AM01193v1

Description

The STGIPL14K60 intelligent power module provides a compact, high performance AC motor drive for a simple and rugged design. It mainly targets low power inverters for applications such as home appliances and air conditioners. It combines ST proprietary control ICs with the most advanced short circuit rugged IGBT system technology. Please refer to dedicated technical note TN0107 for mounting instructions.

Table 1. Device summary

Order code	Marking	Package	Packaging
STGIPL14K60	GIPL14K60	SDIP-38L	Tube

Contents

1 Internal block diagram and pin configuration 3

2 Electrical ratings 6

2.1 Absolute maximum ratings 6

2.2 Thermal data 7

3 Electrical characteristics 8

3.1 Control part 10

3.1.1 NTC thermistor 13

3.1.2 Dead time 14

4 Smart shutdown function 15

5 Applications information 16

5.1 Recommendations 17

6 Package mechanical data 18

7 Revision history 20

1 Internal block diagram and pin configuration

Figure 1. Internal block diagram

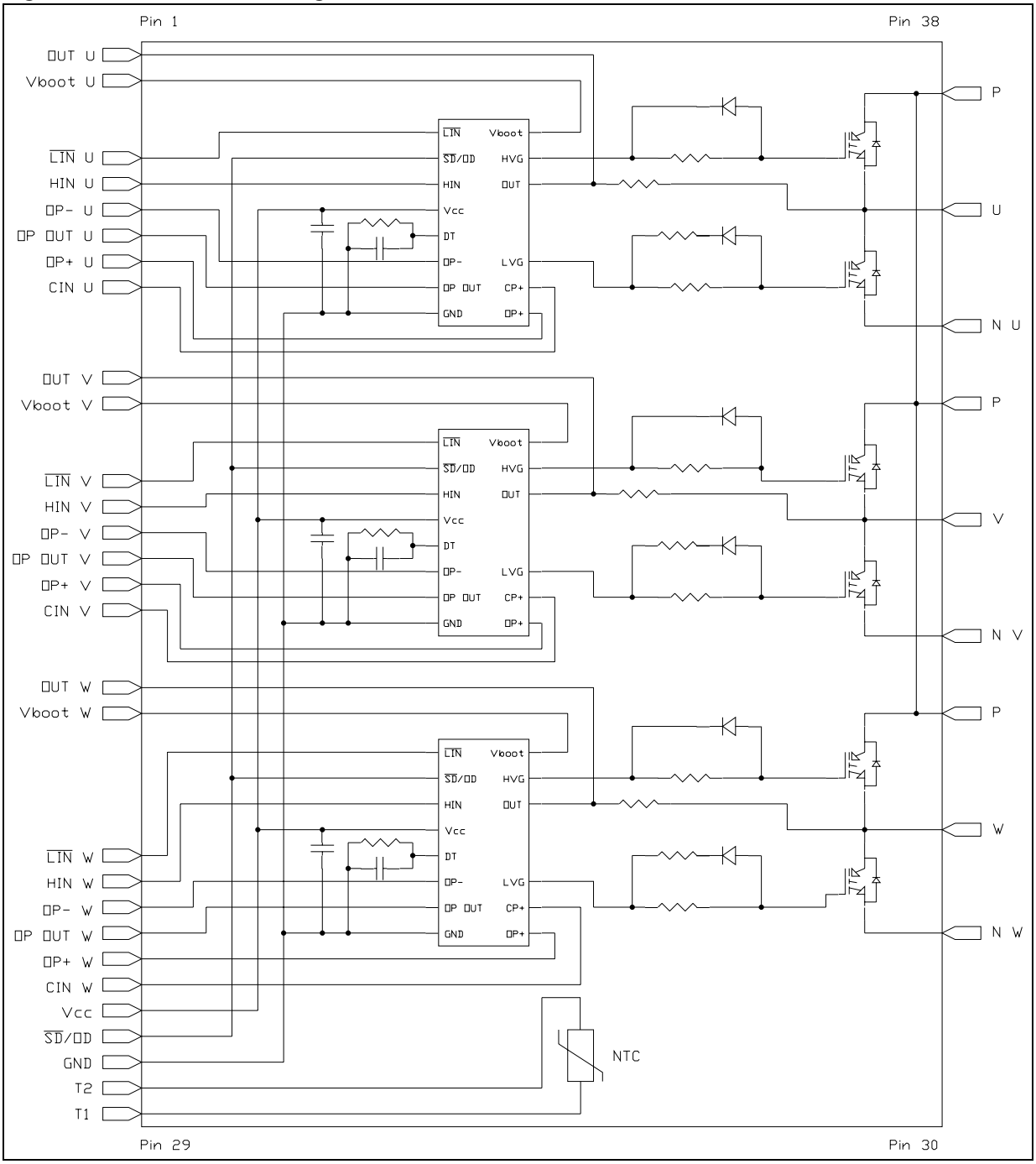


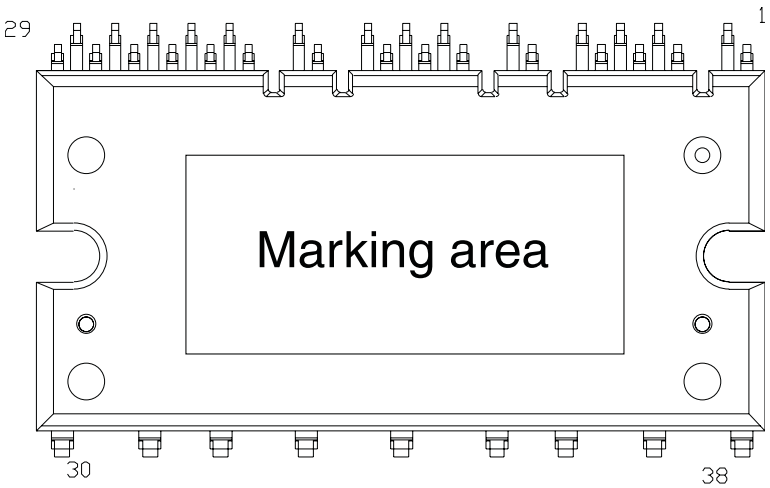
Table 2. Pin description

Pin	Symbol	Description
1	OUT_U	High side reference output for U phase
2	$V_{boot\ U}$	Bootstrap voltage for U phase
3	$\overline{LIN}_U$	Low side logic input for U phase
4	HIN_U	High side logic input for U phase
5	$OP\text{-}_U$	Opamp inverting input for U phase
6	$OP_{OUT\ U}$	Opamp output for U phase
7	$OP+_U$	Opamp non inverting input for U phase
8	CIN_U	Comparator input for U phase
9	OUT_V	High side reference output for V phase
10	$V_{boot\ V}$	Bootstrap voltage for V phase
11	$\overline{LIN}_V$	Low side logic input for V phase
12	HIN_V	High side logic input for V phase
13	$OP\text{-}_V$	Opamp inverting input for V phase
14	$OP_{OUT\ V}$	Opamp output for V phase
15	$OP+_V$	Opamp non inverting input for V phase
16	CIN_V	Comparator input for V phase
17	OUT_W	High side reference output for W phase
18	$V_{boot\ W}$	Bootstrap voltage for W phase
19	$\overline{LIN}_W$	Low side logic input for W phase
20	HIN_W	High side logic input for W phase
21	$OP\text{-}_W$	Opamp inverting input for W phase
22	$OP_{OUT\ W}$	Opamp output for W phase
23	$OP+_W$	Opamp non inverting input for W phase
24	CIN_W	Comparator input for W phase
25	V_{CC}	Low voltage power supply
26	$\overline{SD}$ / OD	Shut down logic input (active low) / open drain (comparator output)
27	GND	Ground
28	T_2	NTC thermistor terminal 2
29	T_1	NTC thermistor terminal 1
30	N_W	Negative DC input for W phase
31	W	W phase output
32	P	Positive DC input
33	N_V	Negative DC input for V phase
34	V	V phase output

Table 2. Pin description (continued)

Pin	Symbol	Description
35	P	Positive DC input
36	N_U	Negative DC input for U phase
37	U	U phase output
38	P	Positive DC input

Figure 2. Pin layout (bottom view)



2 Electrical ratings

2.1 Absolute maximum ratings

Table 3. Inverter part

Symbol	Parameter	Value	Unit
V_{PN}	Supply voltage applied between P-N_U, N_V, N_W	450	V
$V_{PN(surge)}$	Supply voltage (surge) applied between P-N_U, N_V, N_W	500	V
V_{CES}	Collector emitter voltage (V_{IN}(1) = 0)	600	V
± I_C(2)	Each IGBT continuous collector current at T_C = 25°C	14	A
± I_{CP} (3)	Each IGBT pulsed collector current	30	A
P_{TOT}	Each IGBT total dissipation at T_C = 25°C	35	W
t_{scw}	Short circuit withstand time, V_{CE} = 0.5 $V_{(BR)CES}$ T_j = 125 °C, V_{CC} = V_{boot}= 15 V, V_{IN} (1)= 0÷5 V	5	µs

1. Applied between HIN_i, $\overline{LIN_i}$ and GND for i = U, V, W
2. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

3. Pulse width limited by max junction temperature

Table 4. Control part

Symbol	Parameter	Value	Unit
V_{OUT}	Output voltage applied between OUT_U, OUT_V, OUT_W - GND (V_{CC} = 15 V)	V_{boot} - 21 to V_{boot} + 0.3	V
V_{CC}	Low voltage power supply	-0.3 to +21	V
V_{CIN}	Comparator input voltage	-0.3 to V_{CC} +0.3	V
V_{boot}	Bootstrap voltage applied between $V_{boot\,i}$ - OUT_i for i = U, V, W	-0,3 to 620	V
V_{IN}	Logic input voltage applied between HIN, $\overline{LIN}$ and GND	-0.3 to 15	V
$V_{\overline{SD}/OD}$	Open drain voltage	-0.3 to 15	V
dV_{out}/dt	Allowed output slew rate	50	V/ns

Table 5. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60sec.)	2500	V
T_j	Operating junction temperature	-40 to 125	°C

2.2 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Thermal resistance junction-case single IGBT	2.8	°C/W
	Thermal resistance junction-case single diode	5	°C/W

3 Electrical characteristics

(T_j = 25 °C unless otherwise specified)

Table 7. Inverter part

Symbol	Parameter	Test condition	Value			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{CC} = V_{Boot} = 15 V, V_{IN}(1)= 0 ÷ 5 V, I_C = 7 A	-	2.1	2.5	V
		V_{CC} = V_{Boot} = 15 V, V_{IN}(1)= 0 ÷ 5 V, I_C = 7 A, T_j= 125 °C	-	1.8		
I_{CES}	Collector-cut off current (V_{IN}(1)=0 “logic state”)	V_{CE} = 600 V V_{CC} = V_{boot} = 15 V	-		100	µA
V_F	Diode forward voltage	V_{IN}(1) = 0 “logic state”, I_C = 7 A	-		2.1	V
Inductive load switching time and energy						
t_{on}	Turn-on time	V_{DD} = 300 V, V_{CC} = V_{boot} = 15 V, V_{IN}(1)= 0 ÷ 5 V, I_C = 7 A (see *Figure 3*)	-	270		ns
$t_{c(on)}$	Crossover time (on)		-	130		
t_{off}	Turn-off time		-	320		
$t_{c(off)}$	Crossover time (off)		-	110		
t_{rr}	Reverse recovery time		-	130		
E_{on}	Turn-on switching losses		-	150		µJ
E_{off}	Turn-off switching losses		-	90		

1. Applied between HIN_i $\overline{LIN_i}$ and GND for i = U, V, W ($\overline{LIN}$ inputs are active-low).

Note: t_{on} and t_{off} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.

Figure 3. Switching time test circuit

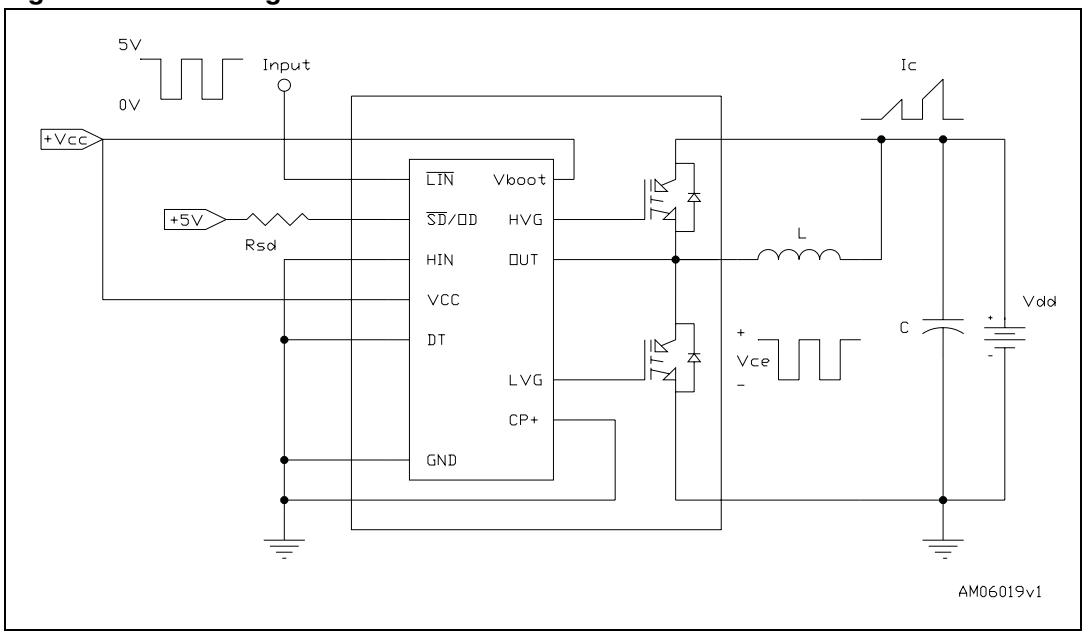
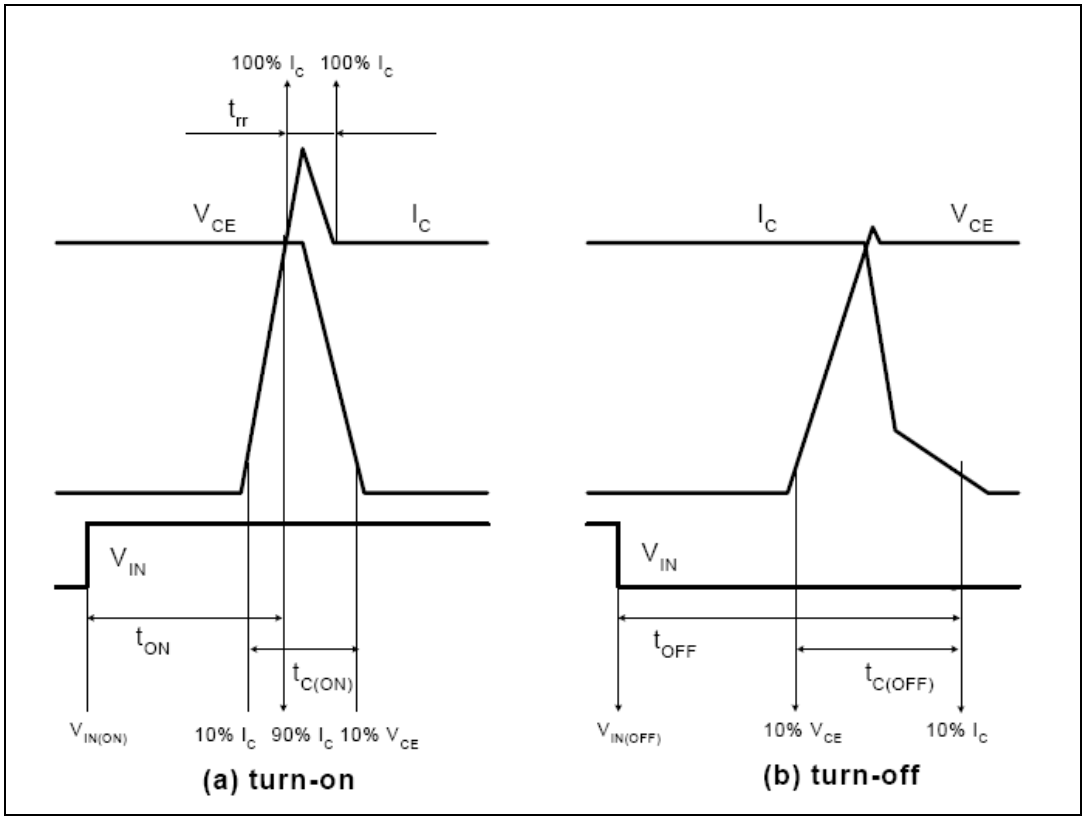


Figure 4. Switching time definition



3.1 Control part

Table 8. Low voltage power supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{cc_hys}	V_{cc} UV hysteresis		1.2	1.5		V
V_{cc_thON}	V_{cc} UV turn ON threshold		11.5	12.0		V
V_{cc_thOFF}	V_{cc} UV turn OFF threshold		10	10.5		V
I_{qccu}	Undervoltage quiescent supply current	V_{CC} = 10 V $\overline{SD}$/OD = 5 V; $\overline{LIN}$ = 5 V; HIN = 0, CIN = 0			450	µA
I_{qcc}	Quiescent current	V_{cc} = 15 V $\overline{SD}$/OD = 5 V; $\overline{LIN}$ = 5 V HIN = 0, CIN = 0			3.5	mA
V_{ref}	Internal comparator (CIN) reference voltage		0.5	0.54	0.58	mV

Table 9. Bootstrapped voltage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BS_hys}	V_{BS} UV hysteresis		1.2	1.5		V
V_{BS_thON}	V_{BS} UV turn ON threshold		10.6	11.5		V
V_{BS_thOFF}	V_{BS} UV turn OFF threshold		9.0	10.0		V
I_{QBSU}	Undervoltage V_{BS} quiescent current	V_{BS} = 10 V $\overline{SD}$/OD = 5 V; $\overline{LIN}$ and HIN = 5 V; CIN = 0		70	110	µA
I_{QBS}	V_{BS} quiescent current	V_{BS} = 15 V $\overline{SD}$/OD = 5 V; $\overline{LIN}$ and HIN = 5 V; CIN = 0		150	210	µA
$R_{DS(on)}$	Bootstrap driver on resistance	LVG ON		120		Ω

Table 10. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low logic level voltage				0.8	V
V_{ih}	High logic level voltage		2.2			V
I_{HINh}	HIN logic “1” input bias current	HIN = 15 V		175	260	µA
I_{HINl}	HIN logic “0” input bias current	HIN = 0 V			1	µA
I_{LINl}	$\overline{LIN}$ logic “0” input bias current	$\overline{LIN}$ = 0 V		6	20	µA
I_{LINh}	$\overline{LIN}$ logic “1” input bias current	$\overline{LIN}$ = 15 V			1	µA
I_{SDh}	$\overline{SD}$ logic “1” input bias current	$\overline{SD}$ = 15 V		120	300	µA

Table 10. Logic inputs (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SDI}	$\overline{SD}$ logic "0" input bias current	$\overline{SD}$ = 0 V			3	µA
Dt	Dead time	see *Figure 8*		600		ns

Table 11. OPAMP characteristics (V_{CC} = 15 V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	V_{ic} = 0 V, V_o = 7.5 V			6	mV
I_{io}	Input offset current	V_{ic} = 0 V, V_o = 7.5 V		4	40	nA
I_{ib}	Input bias current (1)			100	200	nA
V_{icm}	Input common mode voltage range		0			V
V_{OL}	Low level output voltage	R_L = 10 kΩ to V_{CC}		75	150	mV
V_{OH}	High level output voltage	R_L = 10 kΩ to GND	14	14.7		V
I_o	Output short circuit current	Source, V_{id} = +1; V_o = 0 V	16	30		mA
		Sink, V_{id} = -1; V_o = V_{CC}	50	80		mA
SR	Slew rate	V_i = 1 ÷ 4 V; C_L = 100 pF; unity gain	2.5	3.8		V/µs
GBWP	Gain bandwidth product	V_o = 7.5 V	8	12		MHz
A_{vd}	Large signal voltage gain	R_L = 2 kΩ	70	85		dB
SVR	Supply voltage rejection ratio	vs. V_{CC}	60	75		dB
CMRR	Common mode rejection ratio		55	70		dB

1. The direction of input current is out of the IC.

Table 12. Sense comparator characteristics (V_{CC} = 15 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{io}	Input bias current	V_{CP+} = 1 V	-		3	µA
V_{ol}	Open-drain low-level output voltage	I_{od} = - 3 mA	-		0.5	V
t_{d_comp}	Comparator delay	$\overline{SD}$/OD pulled to 5 V through 100 kΩ resistor	-	90	130	ns
SR	Slew rate	C_L = 180 pF; R_{pu} = 5 kΩ	-	60		V/µsec

Table 13. Truth table

Condition	Logic input (V_I)			Output	
	$\overline{SD}$/OD	$\overline{LIN}$	HIN	LVG	HVG
Shutdown enable half-bridge tri-state	L	X	X	L	L
Interlocking half-bridge tri-state	H	L	H	L	L
0 ‘’logic state” half-bridge tri-state	H	H	L	L	L
1 “logic state” low side direct driving	H	L	L	H	L
1 “logic state” high side direct driving	H	H	H	L	H

Note: X: don’t care.

Figure 5. Maximum $I_{C(RMS)}$ current vs. switching frequency (1)

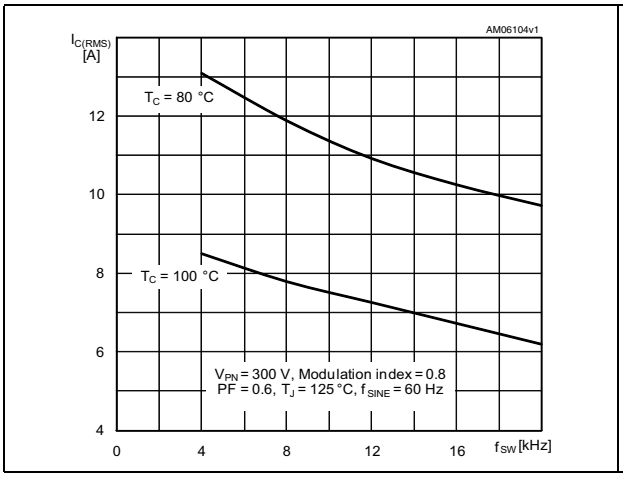
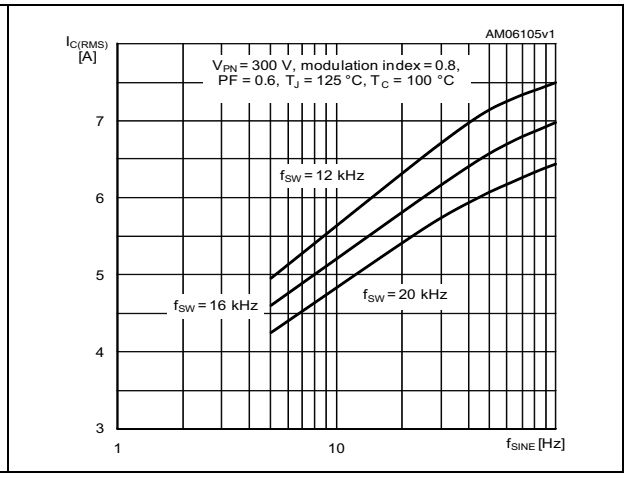


Figure 6. Maximum $I_{C(RMS)}$ current vs. f_{sine} (1)



1. Simulated curves refer to typical IGBT parameters and maximum $R_{thj\text{-}c}$.

3.1.1 NTC thermistor

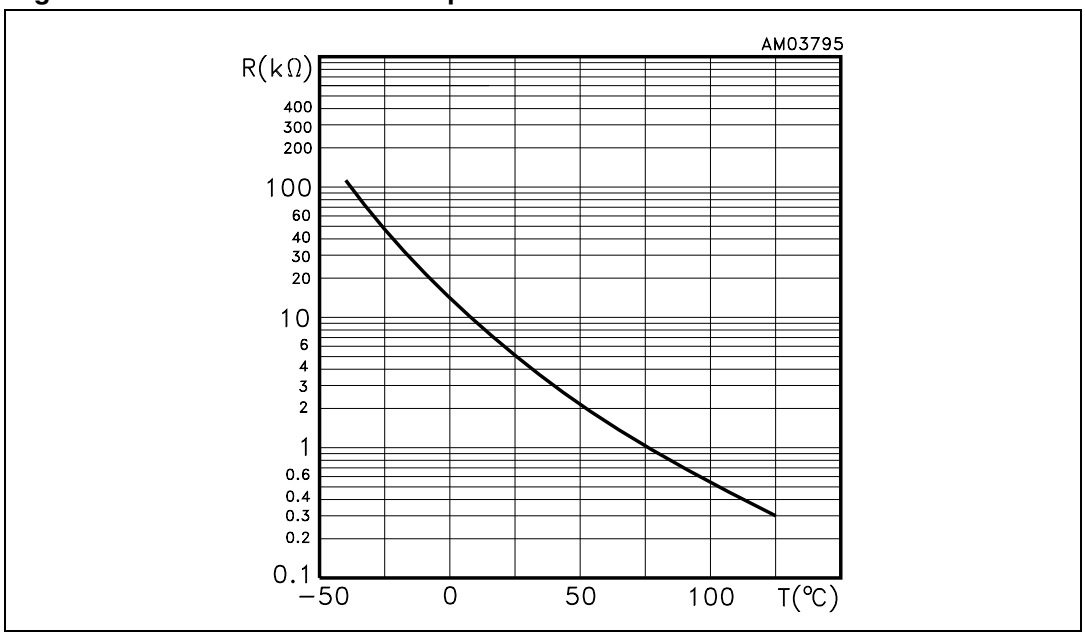
Table 14. NTC thermistor

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
R_{25}	Resistance	T_C = 25°C		5		kΩ
R_{125}	Resistance	T_C = 125°C		300		Ω
B	B-constant	T_C = 25°C		3435		k
T	Operating temperature		-40		125	°C

Equation 1: resistance variation vs temperature

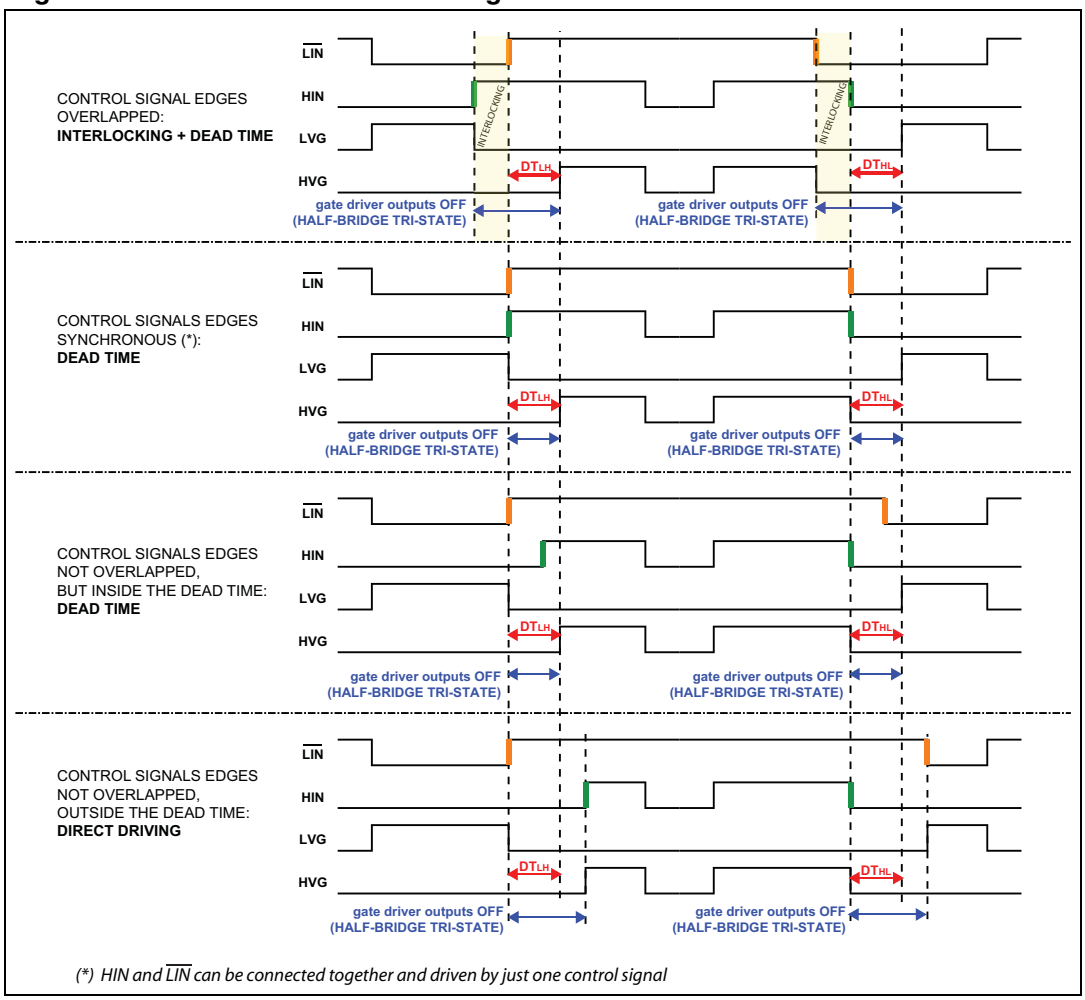
$$R(T) = R_{25} \cdot e^{B\left(\frac{1}{T} - \frac{1}{298k}\right)}$$

Figure 7. NTC resistance vs temperature



3.2 Waveforms definitions

Figure 8. Dead time and interlocking waveforms definitions

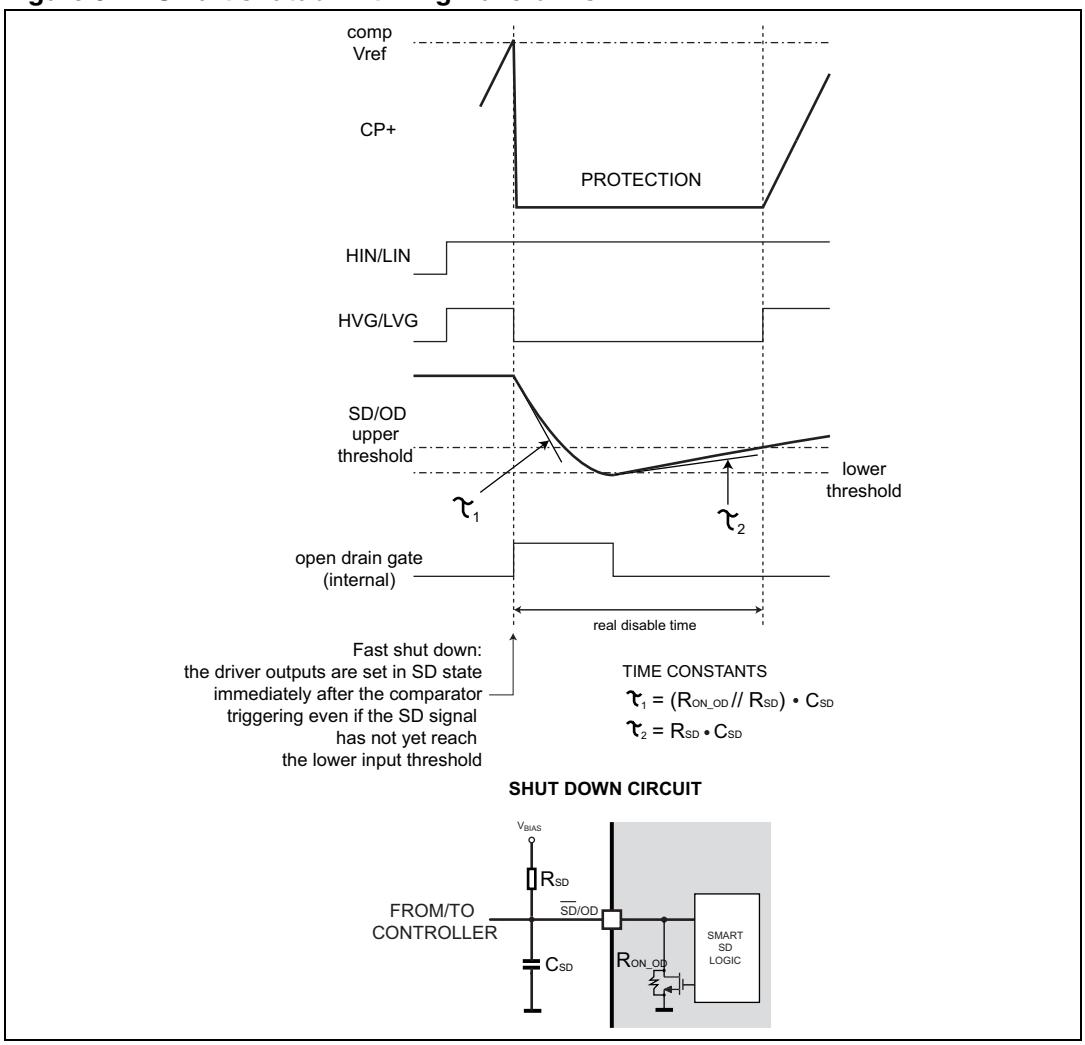


(*) HIN and $\overline{LIN}$ can be connected together and driven by just one control signal

4 Smart shutdown function

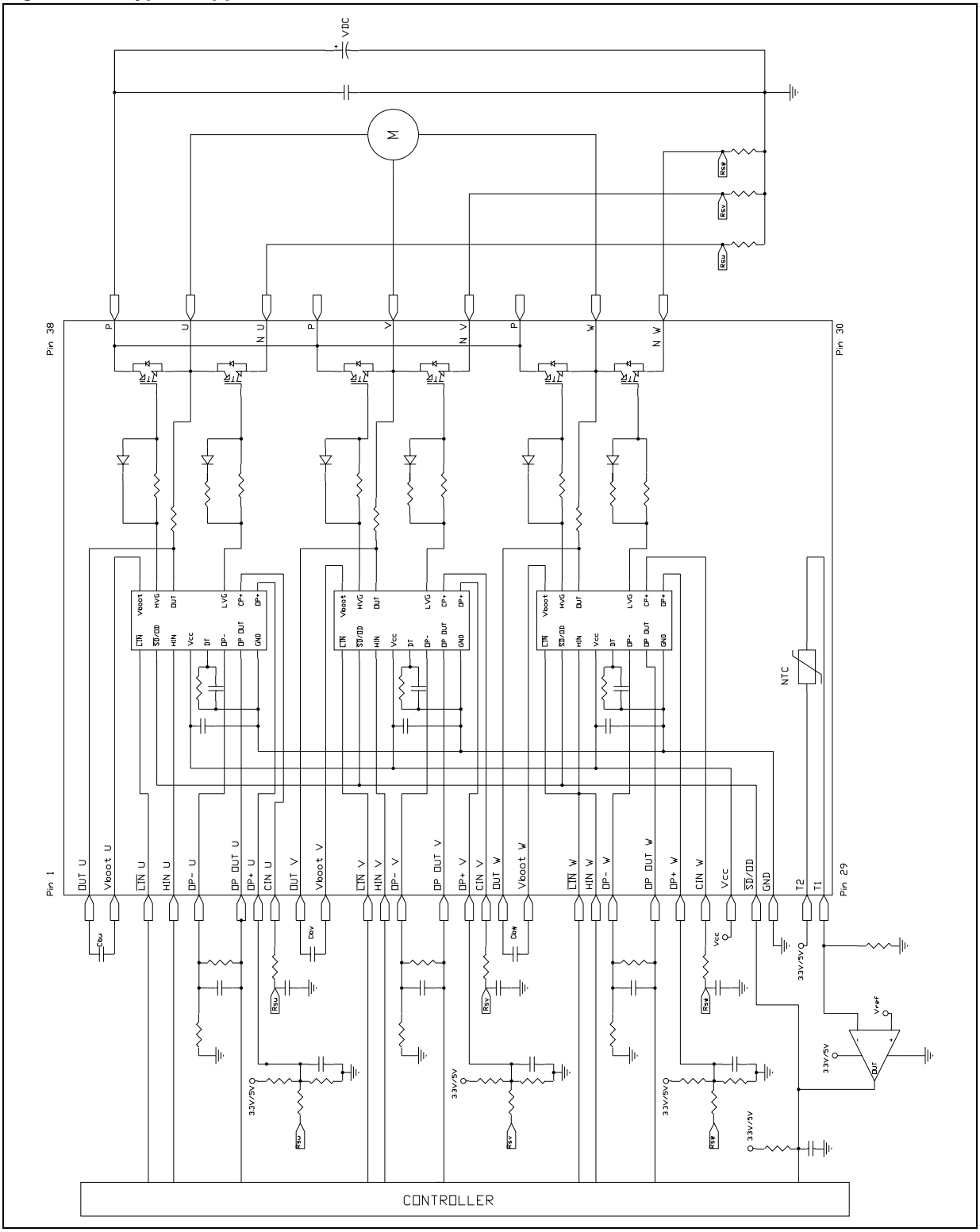
The STGIPL14K60 integrates a comparator for fault sensing purposes. The comparator non-inverting input (CIN) can be connected to an external shunt resistor in order to implement a simple over-current protection function. When the comparator triggers, the device is set in shutdown state and both its outputs are set to low-level leading the half-bridge in tri-state. In the common overcurrent protection architectures the comparator output is usually connected to the shutdown input through a RC network, in order to provide a mono-stable circuit, which implements a protection time that follows the fault condition. Our smart shutdown architecture allows to immediately turn-off the output gate driver in case of overcurrent, the fault signal has a preferential path which directly switches off the outputs. The time delay between the fault and the outputs turn-off is no more dependent on the RC values of the external network connected to the shutdown pin. At the same time the internal logic turns on the open-drain output and holds it on until the shutdown voltage goes below the logic input lower threshold. Finally the smart shutdown function provides the possibility to increase the real disable time without increasing the constant time of the external RC network.

Figure 9. Smart shutdown timing waveforms



5 Applications information

Figure 10. Typical application circuit



5.1 Recommendations

- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
- The $\overline{SD}$/OD signal should be pulled up to 5 V / 3.3 V with an external resistor (see *Section 4: Smart shutdown function* for detailed info).

Table 15. Recommended operating conditions

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{PN}	Supply Voltage	Applied between P-Nu,Nv,Nw		300	400	V
V_{CC}	Control supply voltage	Applied between V_{CC}-GND	13.5	15	18	V
V_{BS}	High side bias voltage	Applied between V_{BOOTi}-OUT_i for i=U,V,W			18	V
t_{dead}	Blanking time to prevent Arm-short	For each input signal	1			µs
f_{PWM}	PWM input signal	-40°C < T_c < 100°C -40°C < T_j < 125°C			20	kHz

6 Package mechanical data

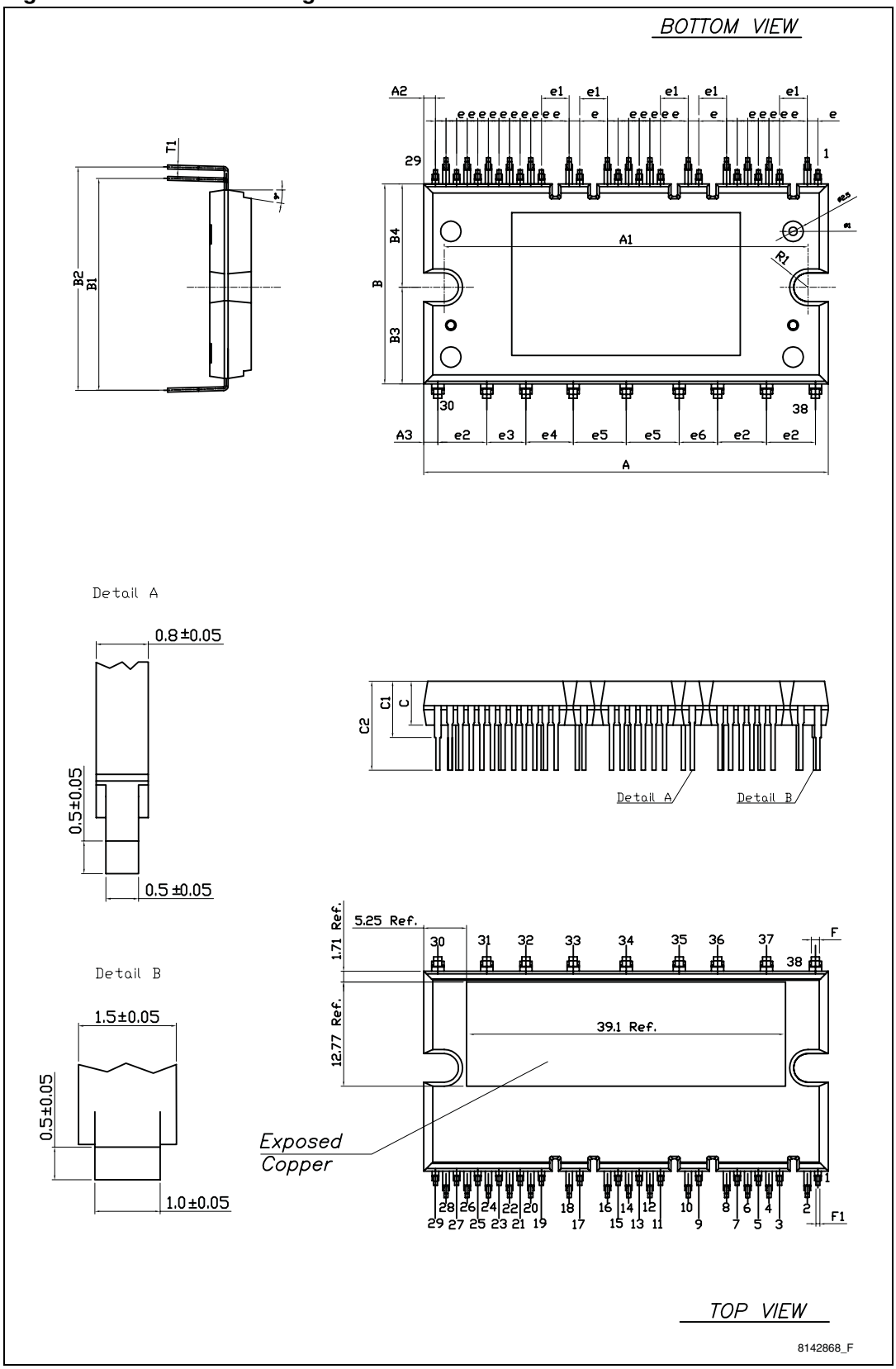
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.

Table 16. SDIP-38L mechanical data

Dimensions	mm		
	Min.	Typ.	Max.
A	49.1		50.1
A1	44.1		45.1
A2	1.37		1.47
A3	1.23		2.23
B	24		25
B1	27.1	27.6	28.1
B2	28.6	29.1	29.6
B3	11.25		12.45
B4	12.05		13.25
C	5		6
C1	6.40		7.40
C2	10.41		11.41
e	1.1	1.3	1.5
e1	3.2	3.4	3.6
e2	5.8	6.0	6.2
e3	4.6	4.8	5.0
e4	5.6	5.8	6.0
e5	6.3	6.5	6.7
e6	4.5	4.7	4.9
F	0.8	1.0	1.2
F1	0.35	0.5	0.65
R1	1.3		2.1
T1	0.45	0.55	0.65

Figure 11. SDIP-38L drawing dimensions



7 Revision history

Table 17. Document revision history

Date	Revision	Changes
16-Apr-2009	1	Initial release
29-Mar-2010	2	Inserted *Figure 5*, *Figure 6* and *Section 4: Smart shutdown function*. Updated *Section 3.1: Control part* and package mechanical data, *Section 6*. Minor text changes to improve readability.
14-Jun-2010	3	Document status promoted from preliminary data to datasheet. Updated *Table 7: Inverter part*, *Figure 5: Maximum IC(RMS) current vs. switching frequency* and *Figure 6: Maximum IC(RMS) current vs. fsine(1)*.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com