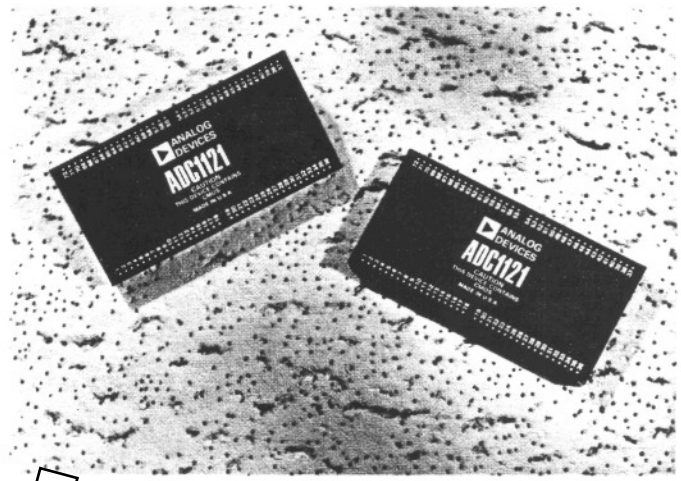
Low Power Analog to Digital Converter

ADC1121

FEATURES
- 12 Bit Resolution and Accuracy
- CMOS Compatible
- Very Low Power Consumption
- Exceptional Power Supply Rejection
- Can Operate From Single Battery
- No Missing Codes, 0 to +70°C



GENERAL DESCRIPTION

The CMOS compatible ADC1121 requires less than 6 microjoules of energy to perform a complete, 12 bit analog-to-digital conversion. In addition, it has ±0.01% relative accuracy, a 70μs maximum conversion time, a maximum power consumption of 100mW for continuous conversions, and no missing codes from 0 to +70°C. Power may be supplied by a single +12V to +15V source, but the logic portions of the converter may also be powered by a separate +5V to +15V supply to permit logic level matching. If batteries are used as a power source, the resulting voltage droop will have little effect on the ADC1121 accuracy due to its excellent power supply rejection.

The ADC1121 accepts analog inputs in the range of 0 to +5V, 0 to +10V, ±5V, or ±10V and produces both parallel and serial digital outputs. Parallel outputs are binary, offset binary, or two's complement coded; serial outputs are binary or offset binary coded.

The special combination of high performance and low power exhibited by this 2″ x 4″ x 0.4″ (51 x 102 x 10mm) module makes it ideal for use in applications such as remote and portable instrumentation, and large data handling networks.

TIMING

When the convert command is set to logic "1", the internal clock starts to run. The first '1' to '0' clock transition sets the STATUS output to logic '1' and sets the MSB through LSB and SERIAL output lines to logic '0'. The CONVERT COMMAND input may be returned to logic '0' 100ns after this clock transition but may also remain at logic '1' until 500ns before the sixth clock transition. The MSB decision process starts on the second negative-going clock edge and concludes one clock period later. The bit decisions continue at the rate of one per clock cycle until the LSB decision has finally been made. After the LSB decision, the clock returns to logic '1' and the STATUS output returns to logic '0'.

The serial data output is of the non-return-to-zero (NRZ) type. The data is available, MSB first, at the third and subsequent positive-going clock transitions.

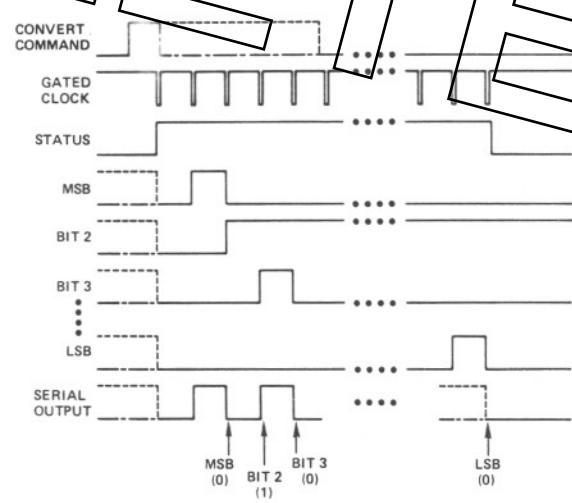


Figure 1. Timing Diagram

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577

West Coast	Mid-West	Texas
213/595-1783	312/894-3300	214/231-5094

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

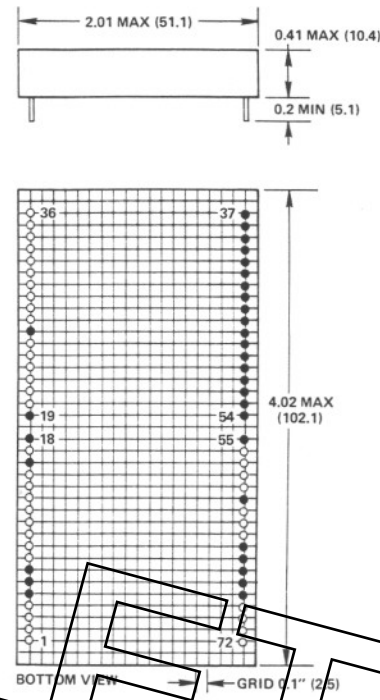
RESOLUTION	12 Bits
ACCURACY	
Error Relative to Full Scale	±½LSB max
Differential Nonlinearity Error	±½LSB max
Missing Codes	No Missing Codes from 0 to +70°C
TEMPERATURE COEFFICIENT	
Gain	±20ppm/°C of Reading, max [1]
Unipolar Zero	±8ppm/°C of Range, max[2]
Bipolar Offset	±20ppm/°C of Range, max[2]
Differential Nonlinearity	±5ppm/°C of Range, max[2]
CONVERSION TIME[3]	
+5V Logic Supply	63μs (70μs max)
+10V Logic Supply	54μs (61μs max)
+15V Logic Supply	52μs (59μs max)
INPUT VOLTAGE RANGES	0 to +5V, 0 to +10V, ±5V, ±10V
INPUT IMPEDANCE	
0 to +5V Range	400kΩ min
0 to +10V Range	144kΩ min
±5V Range	144kΩ min
±10V Range	120kΩ min
DIGITAL OUTPUTS	
Logic Levels	CMOS Compatible (see pg. 4)
Parallel Output Codes	
Unipolar	Positive True Binary
Bipolar	Positive True Offset Binary or Two's Complement
Serial Output Codes	
Unipolar	Positive True Binary, NRZ Format, MSB First
Bipolar	Positive True Offset Binary, NRZ Format, MSB First
Status Output	Logic '1' During Conversion
CONVERT COMMAND INPUT	
Logic Levels	CMOS Compatible (see pg. 4)
Pulse Width	6μs min, 15μs max;
Rise and Fall Times	1μs max
POWER SUPPLY REQUIREMENTS[4]	
Analog Supply (V_S)	+12V to +15V
Logic Supply (V_{DD})	+5V to +15V
POWER CONSUMPTION	See Graphs on pg. 3
POWER SUPPLY SENSITIVITY[5]	
Gain	±¼LSB
Unipolar Zero	±¼LSB
Bipolar Offset	±¼LSB
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55 to +125°C
ADJUSTMENT RANGES	
Gain	±0.2% of Range[2]
Offset	±0.2% of Range[2]
PRICE (1–9)	$229

[1] Reading for bipolar operation is defined as: Actual Reading – (-Full Scale)
[2] Range for unipolar operation is defined as: + Full Scale
Range for bipolar operation is defined as: 2 (+ Full Scale)
[3] Conversion time is measured from the rising edge of the convert command pulse to the falling edge of the STATUS output. A graph showing conversion time as a function of logic supply voltage is shown on page 3.
[4] Power supply current for both the analog and logic supplies is very transient in nature; peak current for both is less than 100mA.
[5] Maximum change as analog supply voltage varies from +12V to +15V.

Specifications subject to change without notice.

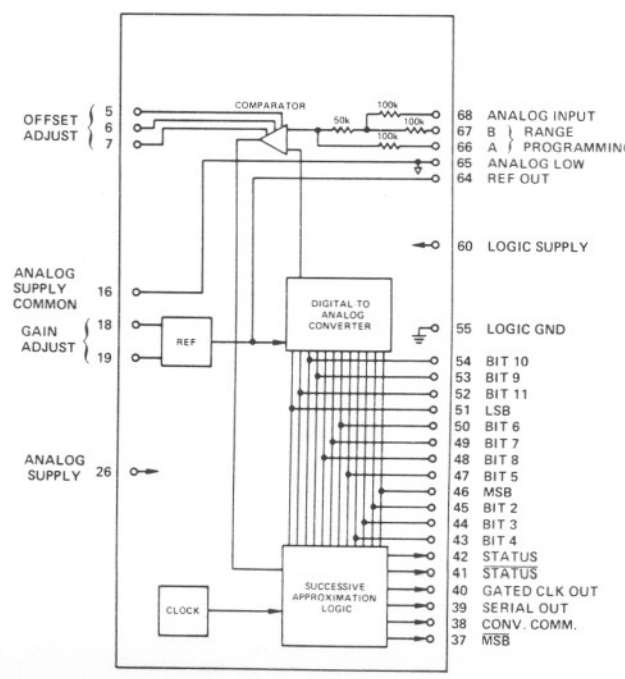
OUTLINE DIMENSIONS AND PIN DESIGNATIONS

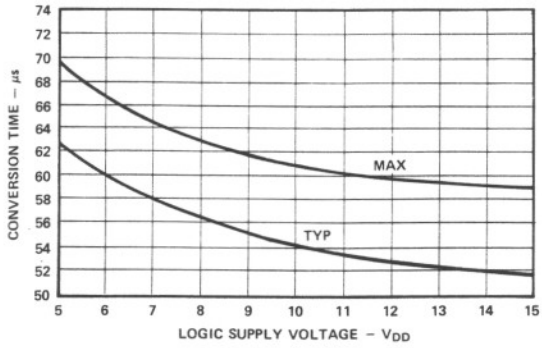
Dimensions shown in inches and (mm).



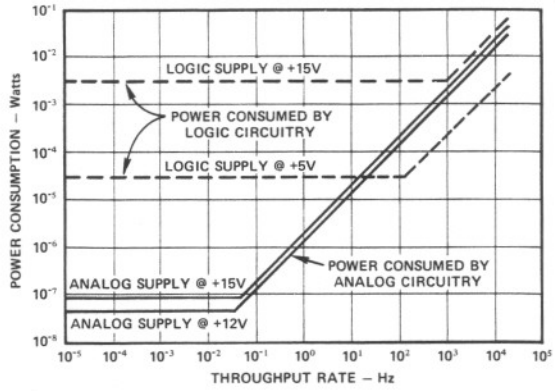
NOTE:
Terminal pins installed only in shaded hole locations.
All pins are gold plated half-hard brass (MIL-G-45204), 0.019" ±0.001" (0.48 ±0.03mm) dia.
For plug-in mounting card order Board No. AC1521, $33.00 (1–9)

BLOCK DIAGRAM

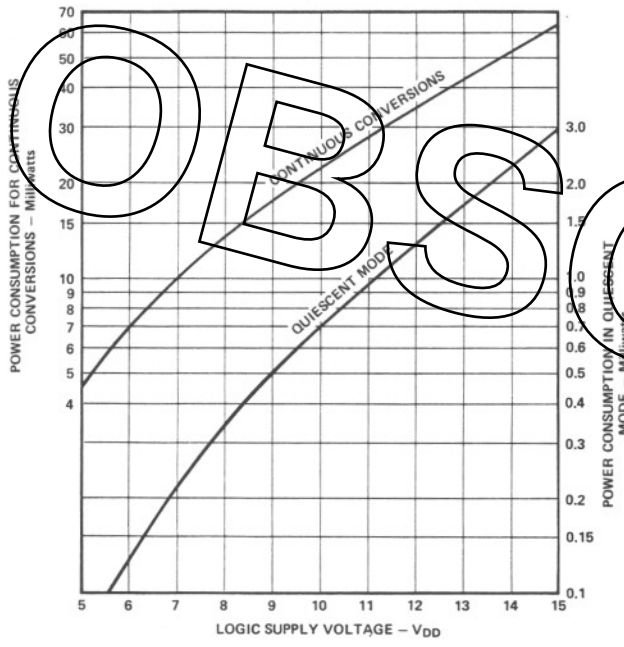




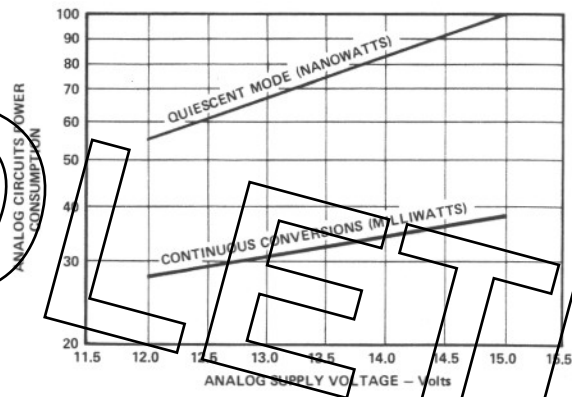
Conversion Time Vs. Logic Supply Voltage



Power Consumption Vs. Throughput Rate and Supply Voltages



Logic Circuits Power Consumption



Analog Circuits Power Consumption

ANALOG INPUT CHARACTERISTICS

The input circuit of the ADC1121 is shown below in block diagram form.

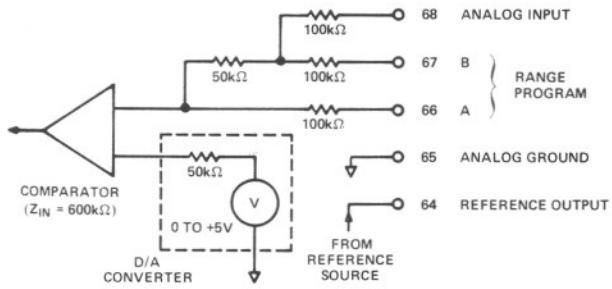


Figure 2. Analog Input Configuration

Analog signals in the range of 0 to +5V, 0 to +10V, ±5V, or ±10V are applied between pins 68 and 65. The range programming circuitry serves to offset and divide these signals as necessary to provide the comparator with a 0 to +5V input which is then compared to the 0 to +5V D/A converter output. Table I, below, shows the range programming connections required for the various input ranges and also shows the resulting input impedances.

INPUT RANGE	CONNECTIONS PIN 66 TO:	CONNECTIONS PIN 67 TO:	INPUT IMPEDANCE
0 to +5V	68	68	500kΩ min
0 to +10V	65	68	180kΩ min
±5V	64	68	180kΩ min
±10V	64	65	150kΩ min

Table I. Range Programming

PARALLEL DATA OUTPUTS

The ADC1121 produces natural binary coded outputs when configured as a unipolar device; as a bipolar device it can produce either offset binary or two's complement output codes.

The most significant bit is represented by pin 46 (the MSB output) for binary and offset binary codes and by pin 37 (the $\overline{\text{MSB}}$ output) for the two's complement code. Tables II and III, below, illustrate the relationship between the analog input and digital output for all three codes.

ANALOG INPUT		DIGITAL OUTPUT
0 TO +5V RANGE	0 TO +10V RANGE	BINARY CODE
+4.9988V	+9.9976V	111111111111
+2.5000V	+5.0000V	100000000000
+0.6250V	+1.2500V	001000000000
+0.0012V	+0.0024V	000000000001
+0.0000V	+0.0000V	000000000000

Table II. Nominal Unipolar Input-Output Relationships

ANALOG INPUT		DIGITAL OUTPUT	
±5V RANGE	±10V RANGE	OFFSET BINARY CODE	TWO'S COMPLEMENT CODE
+4.9976V	+9.9951V	111111111111	011111111111
+2.5000V	+5.0000V	110000000000	010000000000
+0.0024V	+0.0049V	100000000001	000000000001
+0.0000V	+0.0000V	100000000000	000000000000
-5.0000V	-10.0000V	000000000000	100000000000

Table III. Nominal Bipolar Input-Output Relationships

SERIAL DATA OUTPUTS

The serial data output, available at pin 39, is of the non-return-to-zero format. The data, which is transmitted MSB first, is binary coded for unipolar units and offset binary coded for bipolar units.

Figure 3, below, indicates one method for transmitting data serially using only three wires (plus a digital ground). The data is clocked into a receiving shift register by the positive-going transitions of the gated clock output. Since these clock transitions occur typically 250 to 550ns after each bit of serial output data becomes valid, ample time is allowed for shift register set-up.

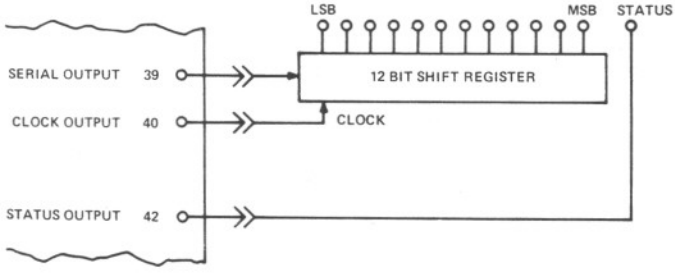


Figure 3. Serial Data Transmission

The STATUS output goes from logic '1' to logic '0' approximately 100 to 450ns after the last '0' to '1' clock transition. If the shift register's propagation delay exceeds this CLOCK output to STATUS output delay, the parallel output data appearing at its terminals will not be stable when end-of-conversion is signalled. The introduction of a suitable delay into the STATUS output line will readily circumvent this problem.

LOGIC LEVELS

The logic levels of the ADC1121's CMOS digital outputs are as shown below:

$V_{DD} \geqslant$ Logic "1" $\geqslant V_{DD}$ - 0.1V; where V_{DD} is the logic supply voltage.

0.1V $\geqslant$ Logic "0" $\geqslant$ 0.0V

The logic power supply voltage (which is independent of the analog supply voltage) can be varied from +5V to +15V. This allows the user to match the converter's logic levels to the logic levels of other CMOS devices in his system.

Although TTL logic levels can be achieved by setting the logic supply voltage to +5V, the MSB through LSB output gates do not have sufficient current sink capability to drive standard TTL logic. They can, however, readily drive low power TTL such as the series 74L devices. The remaining digital outputs (STATUS, $\overline{\text{STATUS}}$, SERIAL OUT, CLOCK OUT, and $\overline{\text{MSB}}$) have a 4mA current sink capability and, thus, can be used directly with standard TTL logic.

CONVERT COMMAND, the only digital input, will respond to logic levels of:

$V_{DD} \geqslant$ Logic "1" $\geqslant 0.7\ V_{DD}$

$0.3\ V_{DD} \geqslant$ Logic "0" $\geqslant$ 0.0V

However, for minimum logic power supply consumption, Logic '1' should be kept as close to V_{DD} as possible and Logic '0' as close to 0.0V as possible.

GAIN AND OFFSET ADJUSTMENTS

The potentiometers used for making gain and offset adjustments are connected as shown in Figure 4. These potentiometers should be small 10 or 20 turn cermet type devices mounted as close to the module pins as possible.

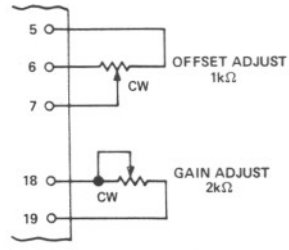


Figure 4. Adjustment Potentiometer Connections

Proper gain and offset calibration requires great care and the use of sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable. It should be capable of being set to within ±1/10LSB of the desired value at both ends of its range.

The gain and offset calibrations will be independent of each other if the offset adjustment is made first. These adjustments are not made with zero and full scale input signals and it may be helpful to understand why. An A/D converter will produce a given digital word output for a small range of input signals, the nominal width of the range being 1LSB. If the input test signal is set to a value which should cause the converter to be on the verge of switching between two adjacent digital outputs, the unit can be calibrated so that it does, in fact, switch at just that point. With a high speed convert command rate and a visu-

al display, these adjustments can be performed in a very accurate and sensitive way. Analog Devices' Conversion Handbook gives more detailed information on testing and calibrating A/D converters.

OFFSET CALIBRATION

For 0 to +5V units set the input voltage precisely to +0.0006V; for 0 to +10V units set it to +0.0012V. Adjust the offset potentiometer until the converter is just on the verge of switching from 000000000000 to 000000000001.

For ±5V units set the input voltage precisely to +0.0012V; for ±10V units set it to +0.0024V. Adjust the offset potentiometer until offset binary coded units are just on the verge of switching from 100000000000 to 100000000001 and two's complement coded units are just on the verge of switching from 000000000000 to 000000000001.

GAIN CALIBRATION

Set the input voltage precisely to +4.9982V for 0 to +5V units, to +9.9963V for 0 to +10V units, to +4.9963V for ±5V units, or to +9.9927V for ±10V units. Note that these values are 1½LSB's less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 111111111110 to 111111111111 and two's complement coded units are just on the verge of switching from 011111111110 to 011111111111.

POWER SUPPLY AND GROUNDING CONNECTIONS

The ADC1121 has independent analog and logic supply inputs which may be powered from a single source or from separate sources. Figures 5 and 6, below, show the proper connections for both cases. The analog supply ground, pin 16, and the digital supply ground, pin 55, are not connected internally but should be jumpered together close to the module pins. Although the analog supply ground and analog signal ground, pin 65, are joined inside the module, pin 65 should never be used as a power supply return. Due to the transient nature of the supply currents encountered in a device of this type, it is recommended that 15μF, 35V tantalum bypass capacitors be added across the analog and digital supplies at a location close to the module pins.

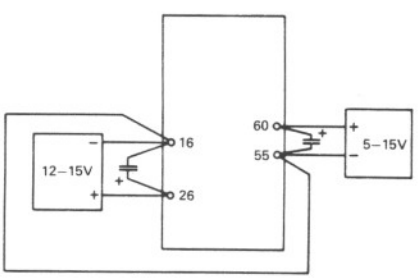


Figure 5. Two Source Connection

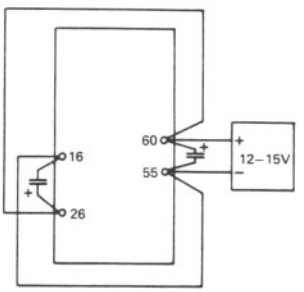


Figure 6. Single Source Connection

Since battery-powered equipment is one of the prime areas of application for the ADC1121, excellent power supply rejection has been provided. The ADC1121 will have less than a ±¼LSB gain shift and less than a ±¼LSB offset shift as the analog supply voltage changes from +15V to +12V during the course of a battery discharge cycle.

REPETITIVE CONVERSIONS

When making repetitive conversions, a new convert command pulse may be initiated any time after the '1' to '0' transition of the STATUS output. If the STATUS output is connected to the CONVERT COMMAND input, a new conversion will automatically begin as soon as the conversion in progress has been completed. The STATUS line will remain in the logic '1' state for approximately 4μs between conversions in this mode of operation.

HANDLING CONSIDERATIONS

Care must be taken in the handling of the ADC1121 to prevent electrostatic damage to its CMOS logic. The unit should be transported on conductive foam or other suitable material and should be handled only by properly grounded personnel. Ground connections must be made before power is applied. Electrostatic damage, should it occur, would be manifested by excessive logic current drain and/or complete failure of one or more logic IC's.

THE AC1521 MOUNTING CARD

The AC1521 mounting card is available to assist in the application of the ADC1121. This 4.5″ x 4.4″ (114 x 111mm) printed circuit card, shown in Figure 7, has sockets which allow an ADC1121 to be plugged directly onto it. It includes the necessary gain and offset adjustment potentiometers and bypass capacitors; it mates with a Cinch 251-22-30-160 (or equivalent) dual 22 pin edge connector which is supplied with every card.

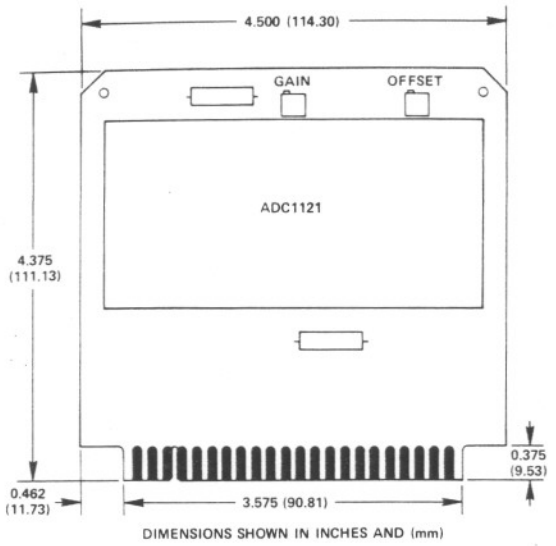
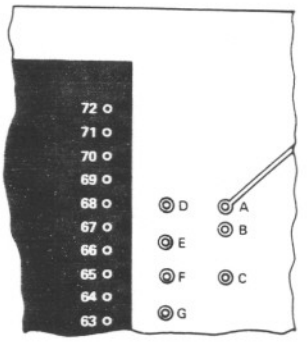


Figure 7. AC1521 Outline Drawing

The input voltage range is programmed by means of jumpers which the user installs as shown in Figure 8. The pin connections are as shown in Table IV.



INPUT VOLTAGE RANGE	JUMPER CONNECTIONS
0 to +5V	E-D, B-A
0 to +10V	E-F, B-A
±5V	E-G, B-A
±10V	E-G, B-C

Figure 8. AC1521 Range Programming

PIN	FUNCTION	PIN	FUNCTION
A	MSB	1	$\overline{\text{MSB}}$
B	Bit 2	2	Convert Command
C	Bit 3	3	Serial Output
D	Bit 4	4	Gated Clock Out
E	Bit 5	5	$\overline{\text{Status}}$
F	Bit 6	6	Status
H	Bit 7	7	N.C.
J	Bit 8	8	
K	Bit 9	9	
L	Bit 10	10	
M	Bit 11	11	
N	LSB	12	Logic Supply
P	Logic Ground	13	N.C.
R	N.C.	14	Analog Supp. Comm.
S	+ Analog Supply	15	N.C.
T	N.C.	16	
U		17	
V		18	
W		19	
X		20	
Y		21	
Z	Analog Low	22	Analog Input

Table IV. AC1521 Pin Designations

C387–8–8/76

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