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Fax: 886-2-29174598
URL: http://www.princeton.com.tw

DESCRIPTION

PT8300 is an I/O expander utilizing CMOS technology providing 16 bits serial input-parallel output and 8 bits parallel input-serial output shift register function. 8 input pins or 16 output pins can be configured to a cascading or parallel structure. Reading of serial data during the parallel to serial data conversion is enabled by the built-in independent registers for serial input to parallel output and parallel input to serial output. Housed in 28 pins, SOP Package, PT8300 provides 8 input or 16 output pins which can be configured into a cascading structure. Pin assignments and application circuits are optimized for easy PCB layout and cost saving benefits.

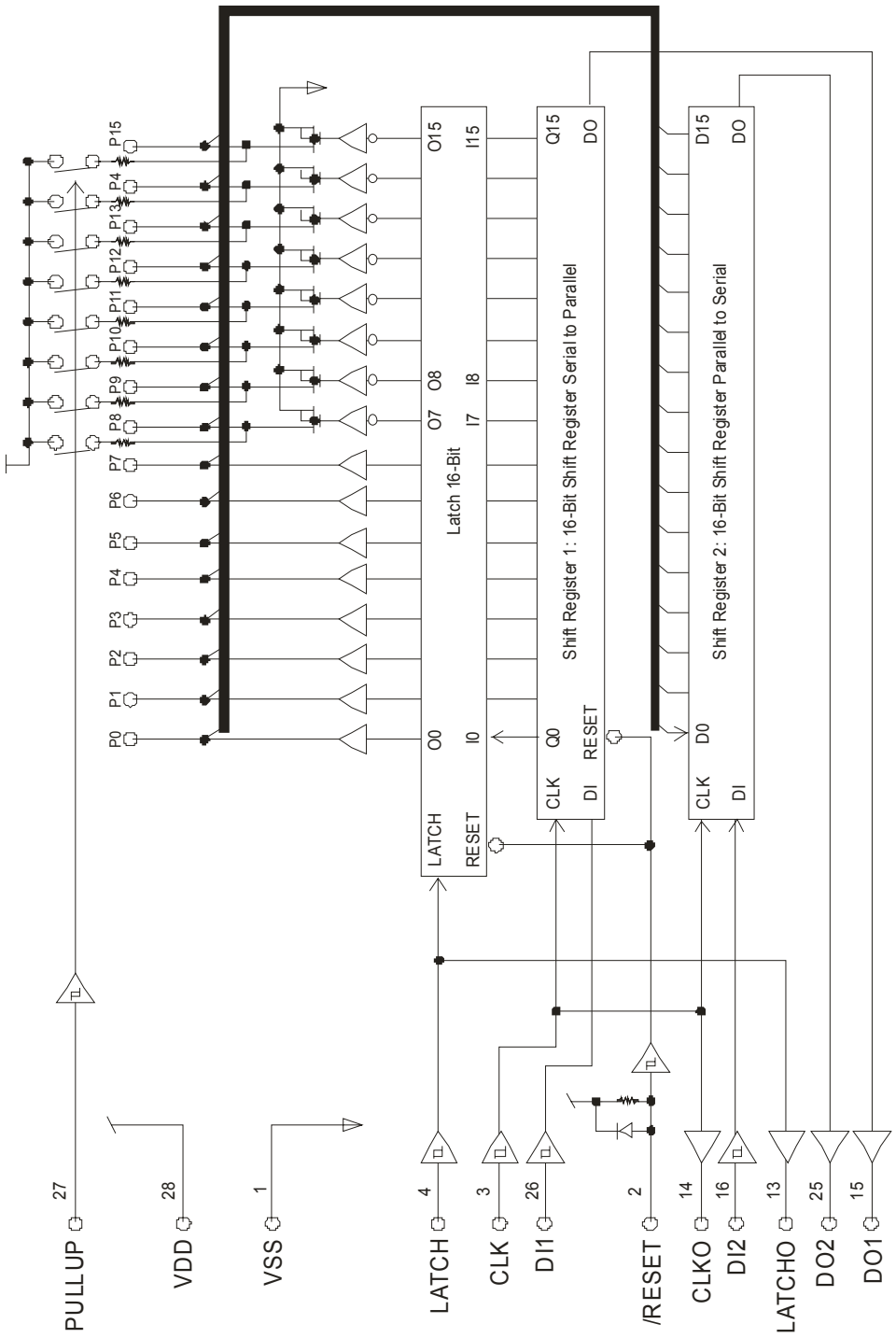
FEATURES

- CMOS technology
- Low power consumption:
  - Wide operating supply voltage range: V_{DD}=3 to 5.5V
  - Wide operating temperature range: Ta=-20 to +75℃
- Reading of the serial data during parallel to serial data conversion
- 8 output pins or 8 input/output pins provided
- Schmitt triggered inputs (DI1,DI2,CLK,LATCH, /RESET,PULLUP)
- Parallel data inputs provided (P8 to P15)
- Open drain with selectable pull up resistance ports provided (P8 to P15)
- Normal output ports provided (P0 to P7)
- Port extension is supported

APPLICATIONS

- MCU peripheral device
- Serial bus system data communication

BLOCK DIAGRAM



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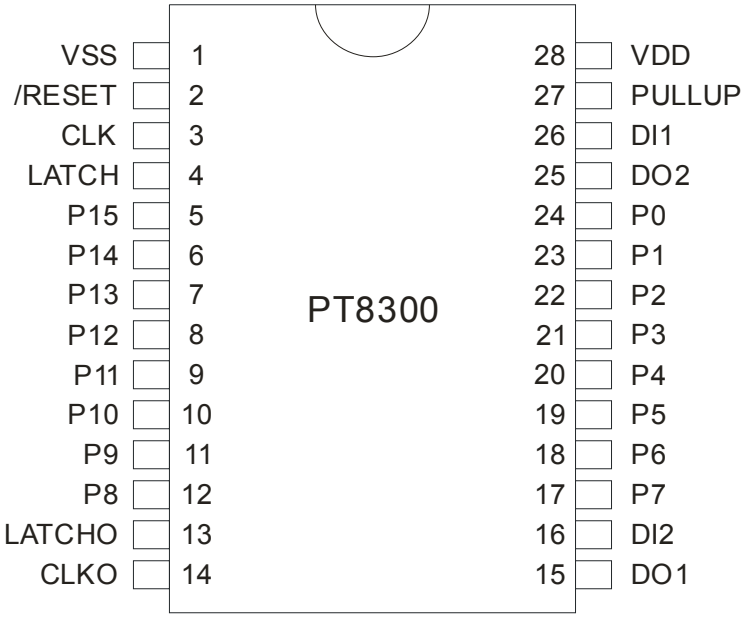
PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
VSS	-	Ground	1
/RESET	I	Reset pin (Active: Low)	2
CLK	I	Clock input pin	3
LATCH	I	Latch input pin	4
P15 ~ P8	I/O	Parallel data input/output pins	5 ~ 12
LATCHO	O	Latch output pin	13
CLKO	O	Clock output pin	14
DO1, DO2	O	Serial data output pins	15, 25
DI1, DI2	I	Serial data input pins	26, 16
P7 ~ P0	O	Parallel data output pins	17 ~ 24
PULLUP	I	P8 to P15 control pin for internal resistor When P8 to P15 are in the output state, the PULLUP pin must be connected to VDD. When P8 to P15 are in the input state, the PULLUP pin must be connected to VSS.	27
VDD	-		28

FUNCTION DESCRIPTION

PT8300 is an I/O Expander IC which independently generates a 16-bit serial input-to-parallel output shift register and a parallel input-to-serial output shift register for the purpose of reading the serial input data that is generated during the parallel to serial data output conversion.

When the /RESET Pin is connected to VSS, the outputs of pins -- P0 to P7 are 0. If the PULLUP pin is connected to VSS or open, the outputs of pins -- P8 to P15 are floating. If the PULLUP pin is connected to VDD, the P8 to P15 pins are 1.

NO USED PINS

If any of the Input, Output or I/O (P8 to P15) pins are not used, then the following conditions listed in the table must be carefully followed.

When an output pin is not used, it must keep OPEN. The unused input pin must only be set to either HIGH or LOW. It should be noted that when an input pin is not used, it cannot be OPEN.

When the I/O Pins -- P8 to P15 -- are not used, certain conditions must be followed. If any of these pins, P8 to P15 are connected to VSS, the PULLUP Pin must also be connected to VSS. If any of these pins -- P8 to P15 -- are connected to VDD, then the Internal Shift Register 1 (Q8 to Q15) must be set to 1. If these pins -- P8 to P15 -- are not connected to either VSS or VDD, then any one of the following conditions must be followed:
1) PULLUP pin must be connected to VDD and the Shift Register 1 (Q8 to Q15) must be set to 1, or

2) PULLUP pin must be connected to VSS and the Shift Register 1 (Q8 to Q15) must be set to 0.

It must be noted that when P8 to P15 are not in used, they must be set to HIGH or LOW.

Type of Pin Not Used	Condition	
Output pin	The unused output pin must be kept OPEN or not connected	
Input pin	The unused input pin must either be set to HIGH or LOW. It cannot be kept OPEN.	
I/O pin (P8 to P15)	Connected to VSS	PULLUP pin must be connected to VSS
	Connected to VDD	Shift register 1 (Q1 to Q15) is set to 1
	No Connection	Any one of the conditions must be followed: 1. PULLUP pin is connected to VDD and shift register 1 (Q1 to Q15) is set to 1. 2. PULLUP pin is connected to VSS, and shift register 1 (Q8 to Q15) is set to 0. 3. When P8 to P15 are not in used, they must either be set to HIGH or LOW.

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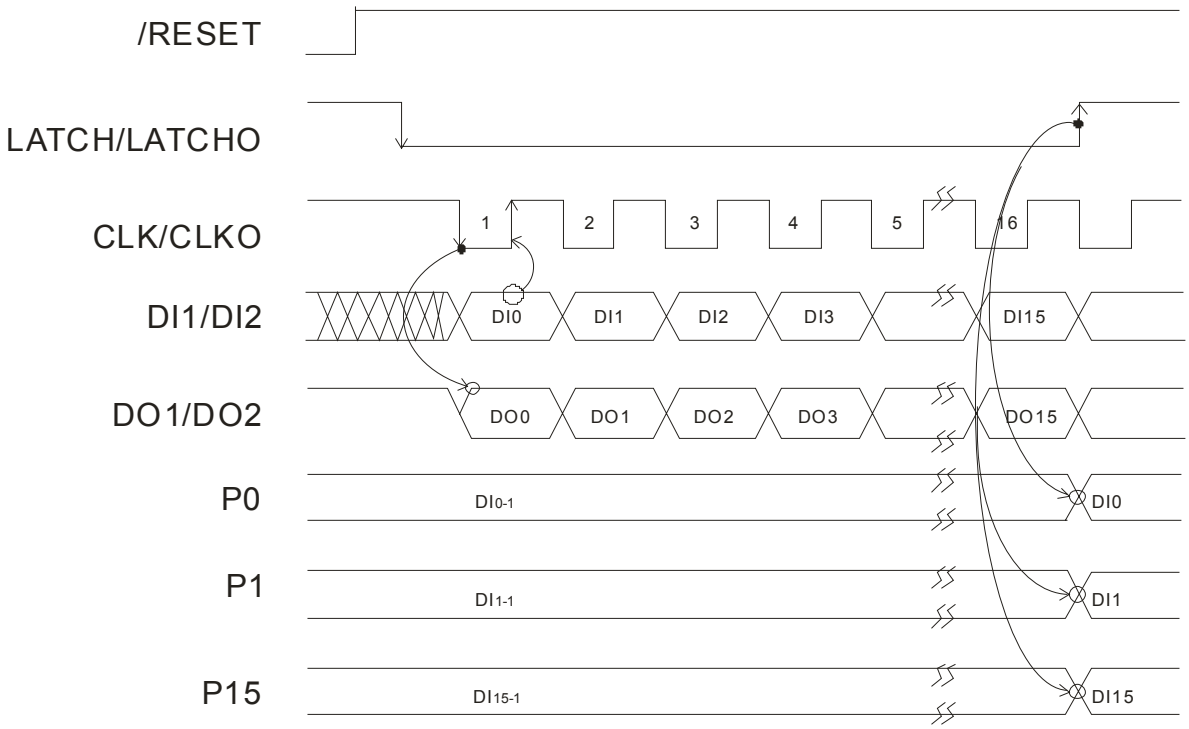
OPERATION

1. P0 to P15 are undefined when power is turned ON, but if /RESET is set to LOW, P0 to P7 are in LOW state. If PULLUP pin is connected to VSS, P8 to P15 are floating. If PULLUP pin is connected to VDD, P8 to P15 are in HIGH State.
2. The status of P0 to P15 is loaded to the Shift register 1 at the falling edge of LATCH/LATCHO.
3. At the falling edge of the CLK, the 16-bit serial output of the data loaded to the Shift register 1 (Shift register 2) is sequentially performed from DO1(DO2).
4. At the rising edge of CLK, 16-bit serial data is written into the Shift register 1 (Shift register 2) from DI1(DI2).
5. At the rising edge of the LATCH/LATCHO, the data written is outputted in a parallel manner to the P0 to P15.
6. Shift Register 1 loads the data that is to be applied externally and the data with the latched content. to the parallel output latch.
7. When the LATCH/LATCHO is activated after the arrival of CLK's 16th bit, the parallel output latch sends out P0 to P15 by storing the data that has been written into the Shift register 2. The Shift Registers 1 and 2 continue the shift operation until the CLK's 16th bit and the DO1 (DO2) output serial data arrive.
8. Serial data is used to control the switching mode operation (input ↔ output) of P8 to P15. When P8 to P15 operate as Output Pins, the PULLUP must be set to HIGH.

OPERATION TIMING DIAGRAM



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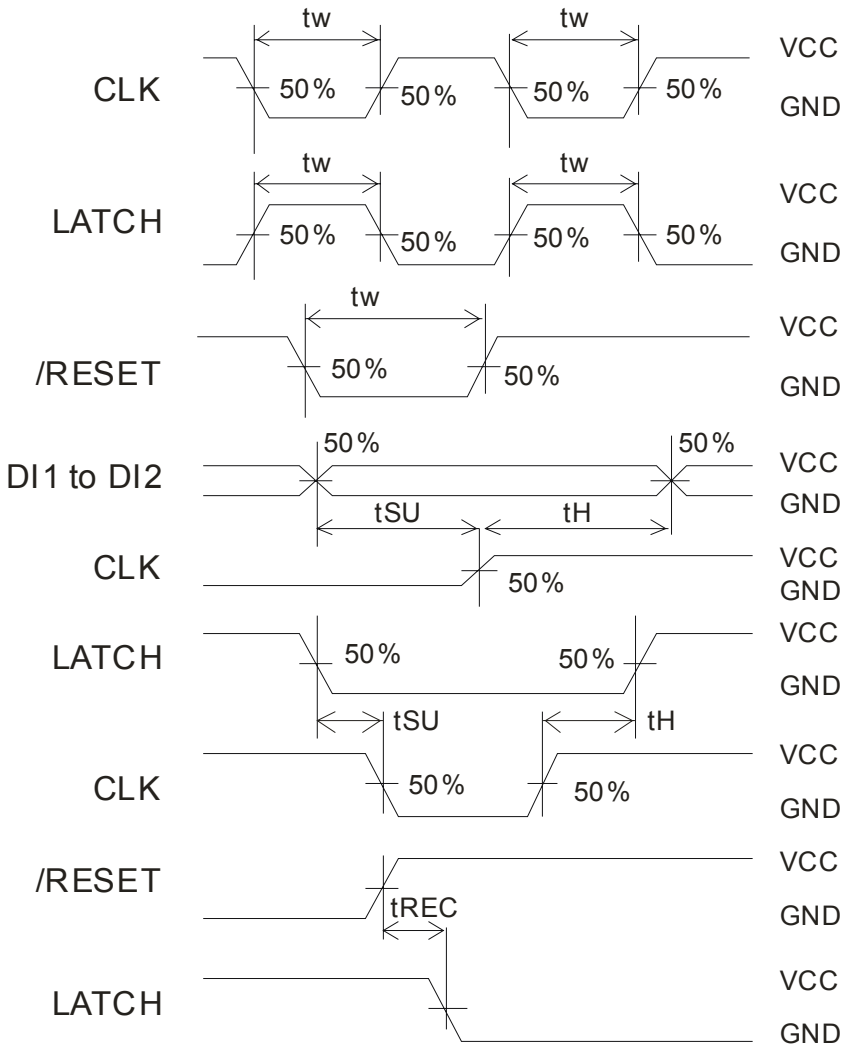
TIMING REQUIRMENTS

(Unless otherwise stated, VCC=5V)

Parameter	Symbol	Limits						Unit
		Ta=25℃, Ta=-40 ~ +85℃						
		Min.	Typ.	Max.	Min.	Typ.	Max.	
CLK, LATCH, /RESET pulse width	tw	100	-	-	150	-	-	ns
DI1/DI2 setup time for CLK	tSU	50	-	-	100	-	-	ns
Latch setup time for LK		50	-	-	100	-	-	ns
DI1/DI2 hold time for CLK	tH	50	-	-	100	-	-	ns
LATCH hold time for CLK		50	-	-	100	-	-	ns
LATCH recovery time	tREC	50	-	-	100	-	-	ns

TIMING DIRGRAM



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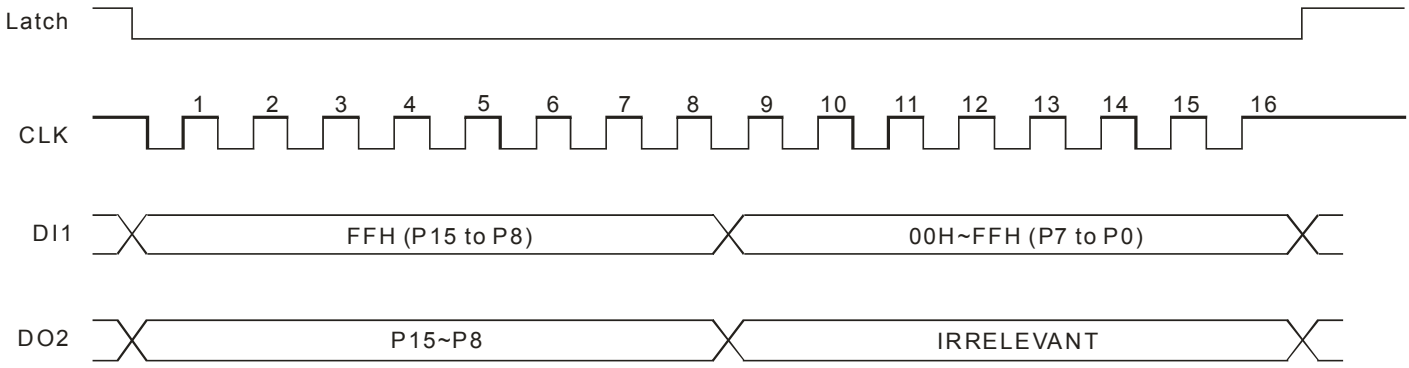
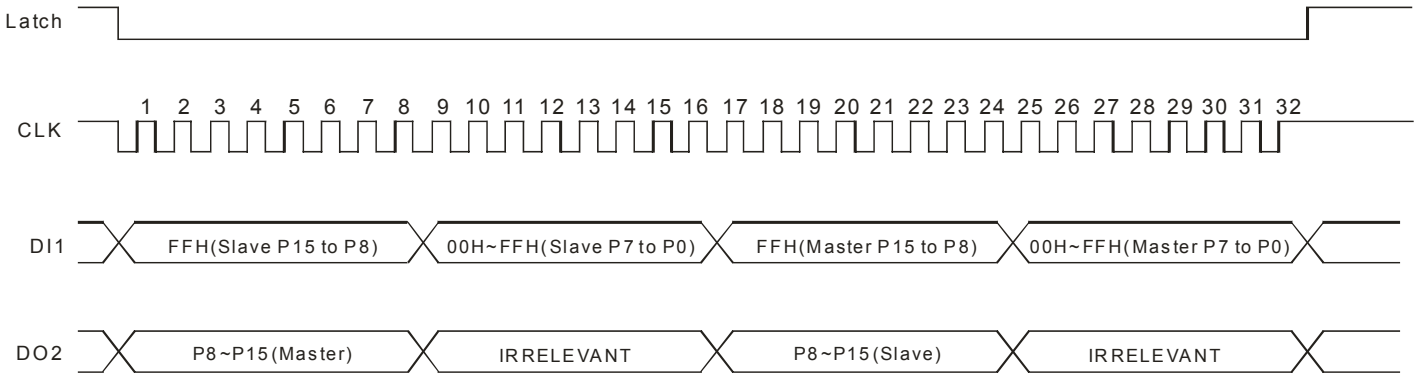
DATA TIMING DIAGRAM

READ

SINGLE MODE (P0-P7 = Output [Write], P8-P15 = Input [Read])



CASCADE MODE (P0-P7 [Master] = Output [Write], P8-P15 [Master] = Input [Read], P0-P7 [Slave] = Output [Write], P8-P15 [Slave] = Input [Read])



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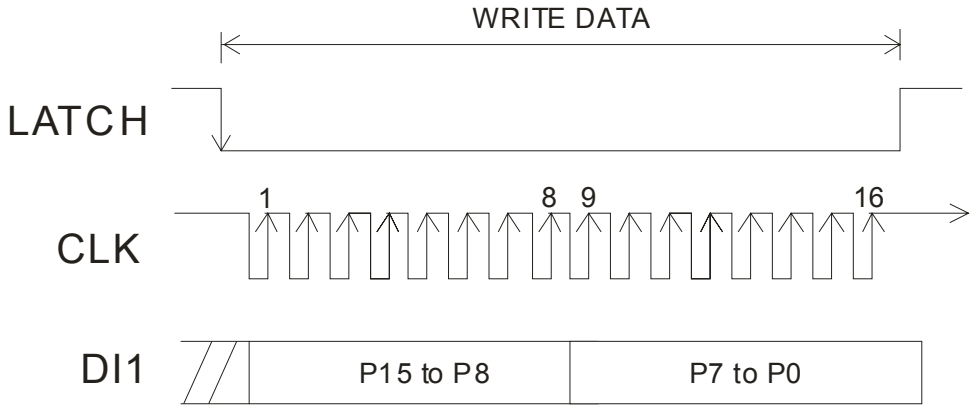
WRITE



ABSOLUTE MAXIMUM RATING

(Unless otherwise specified, Topr=-40~+85℃)

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	VDD		-0.3 ~ 7.0	V
Input voltage	VI	-	-0.3 ~ VCC+0.3	V
Output voltage	VO	-	-0.3 ~ VCC+0.3	V
Operation temperature	Topr	-	-40 ~ +85	℃
Storage temperature	Tstg	-	-65 ~ +150	℃

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, VCC=2V to 6V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	VCC	-	3.0	-	5.5	V
Stand-by current	ISB	-	-	-	1	μA
Operating current	IDD	VCC=3V, CLK=1MHz LATCH, /RESET connected to VDD. PULLUP, DI1, DI2 connected to GND	-	50	-	μA
		VCC=5V, CLK=1MHz LATCH, /RESET connected to VDD. PULLUP, DI1, DI2 connected to GND	-	85	-	μA
High level input voltage	VIH	VCC=5V (CLK, LATCH, DI1, DI2, PULLUP)	0.7VDD	-	VDD	V
Low level input voltage	VIL	VCC=5V (CLK, LATCH, DI1, DI2, PULLUP)	VSS	-	0.2VDD	V
High level output current	IOH	VCC=5V (Output Pins other than P0 to P7, VOH=4.7V)	2.5	-	-	mA
		VCC=5V (P8 to P15, VOH=4.7V)	0.5	-	-	mA
Low level output current	IOL	VCC=5V (Output Pins other than P0 to P7, VOH=0.3V)	3.5	-	-	mA
		VCC=5V (P8 to P15, VOH=0.8V)	13	-	-	mA

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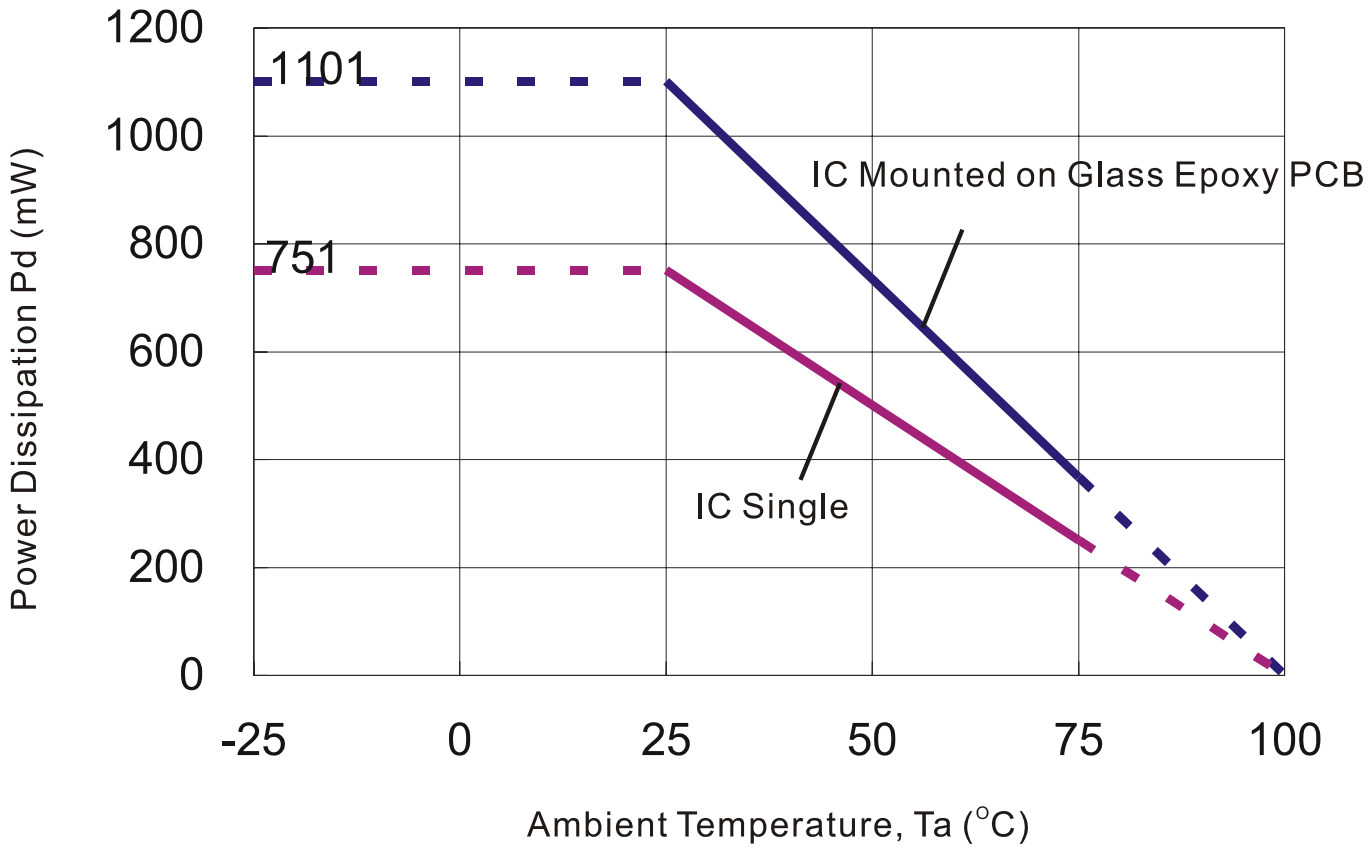
SOP28 300 MIL THERMAL PERFORMANCE IN STILL AIR AT TJ=100°C



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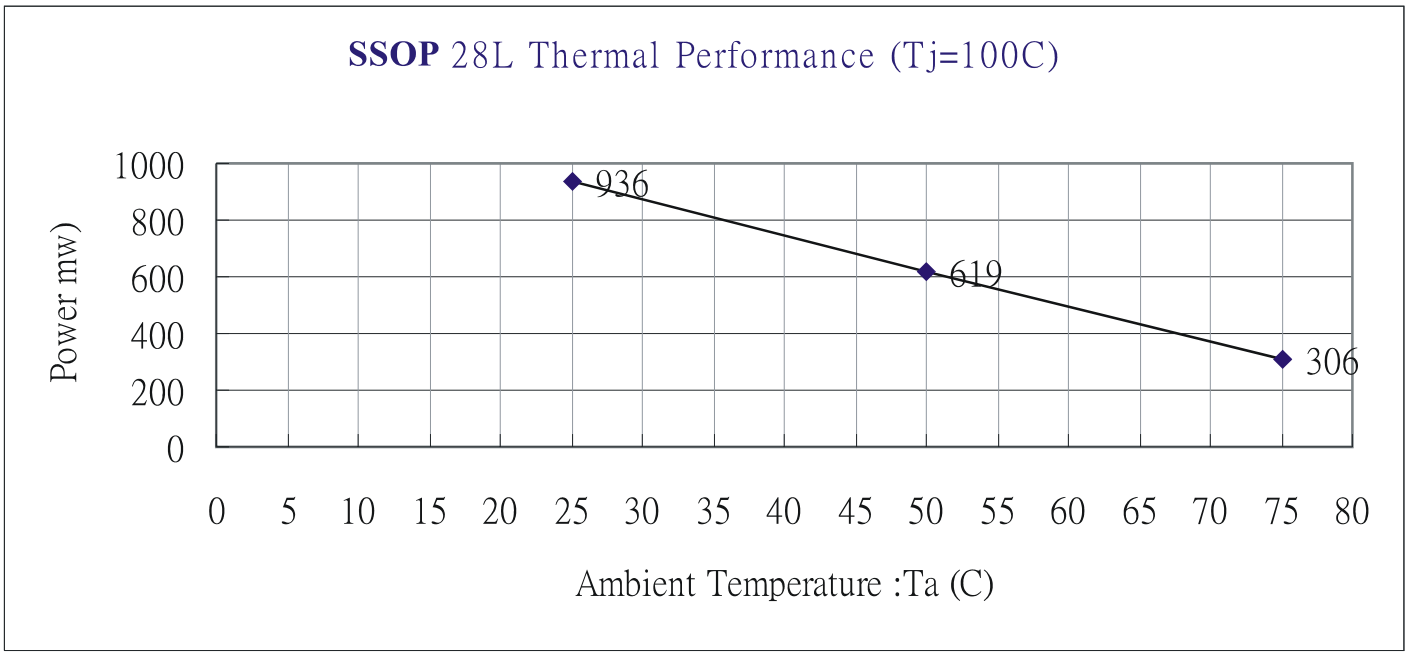
SSOP28 150 MIL THERMAL PERFORMANCE IN STILL AIR AT TJ=100°C



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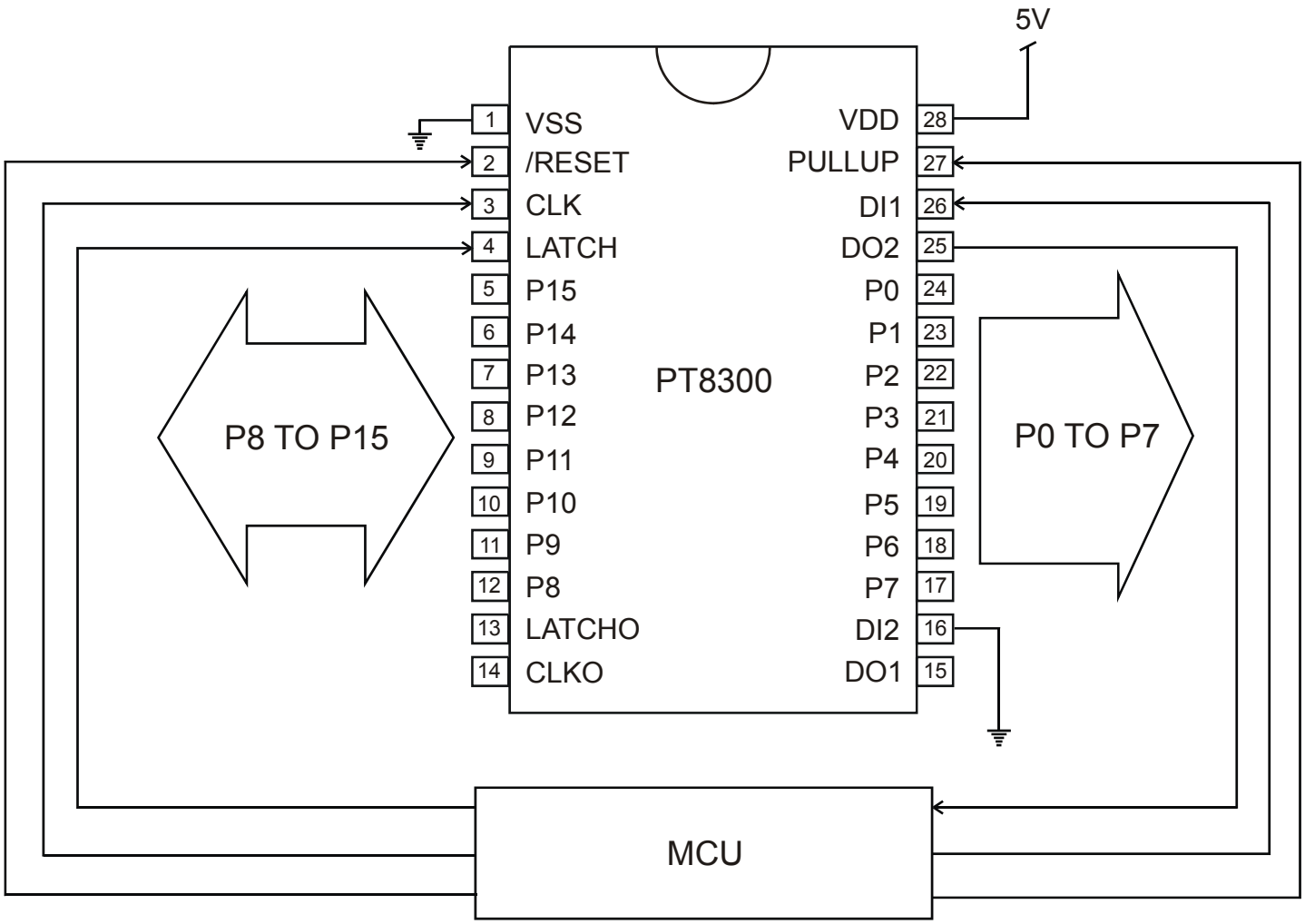
APPLICATION CIRCUIT 1



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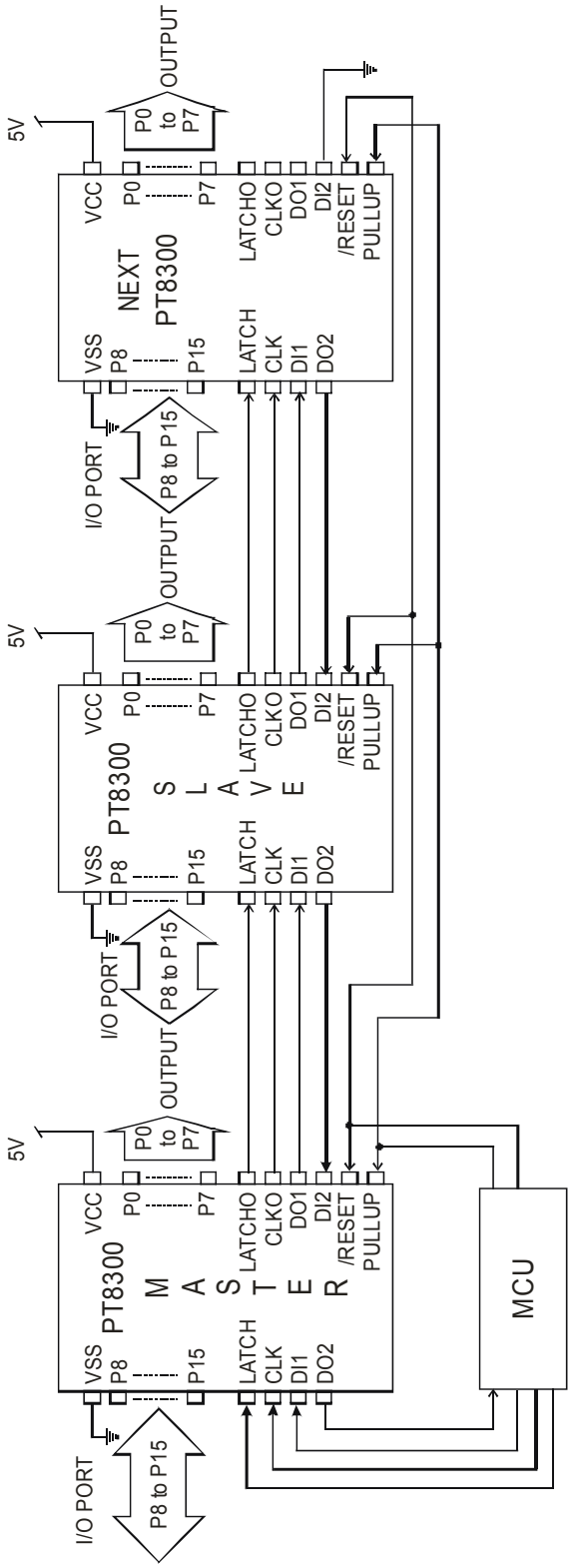
APPLICATION CIRCUIT 2



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ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT8300	28 Pins, SOP, 300mil	PT8300
PT8300-R	28 Pins, SSOP, 150mil	PT8300-R

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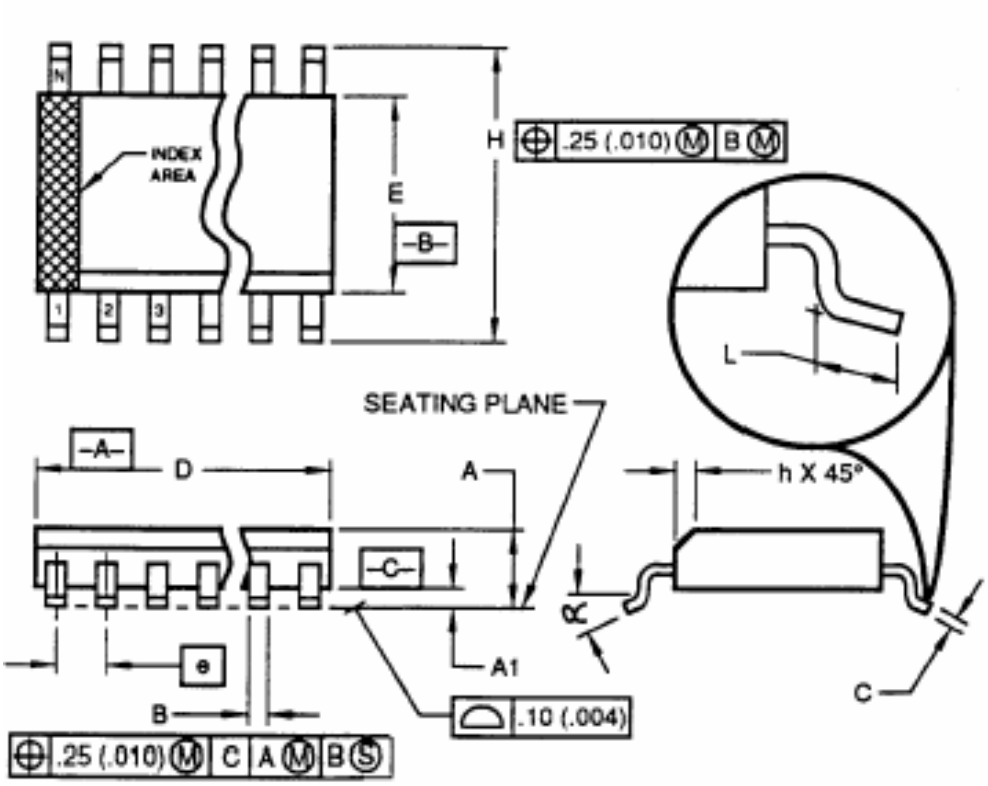
PACKAGE INFORMATION

28 PINS, SOP, 300MIL



Symbol	Min.	Max
A	2.35	2.65
A1	0.10	0.30
B	0.33	0.51
C	0.23	0.32
D	17.70	18.10
E	7.40	7.60
e	1.27 bsc	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0^o	8^o

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5-1982.
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.15mm (0.006 in) per side.
3. Dimension E does not include interlead flash or protrusions. Interlead flash and protrusion shall not exceed 0.15mm (0.016in) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. L is the length of terminal for soldering to a substrate.
6. N is the number of terminal positions (N=28).
7. The lead width B as measured 0.36mm (0.014in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024 in).
8. Controlling dimension: MILLIMETER
9. Refer to JEDEC MS-013 Variation AE.

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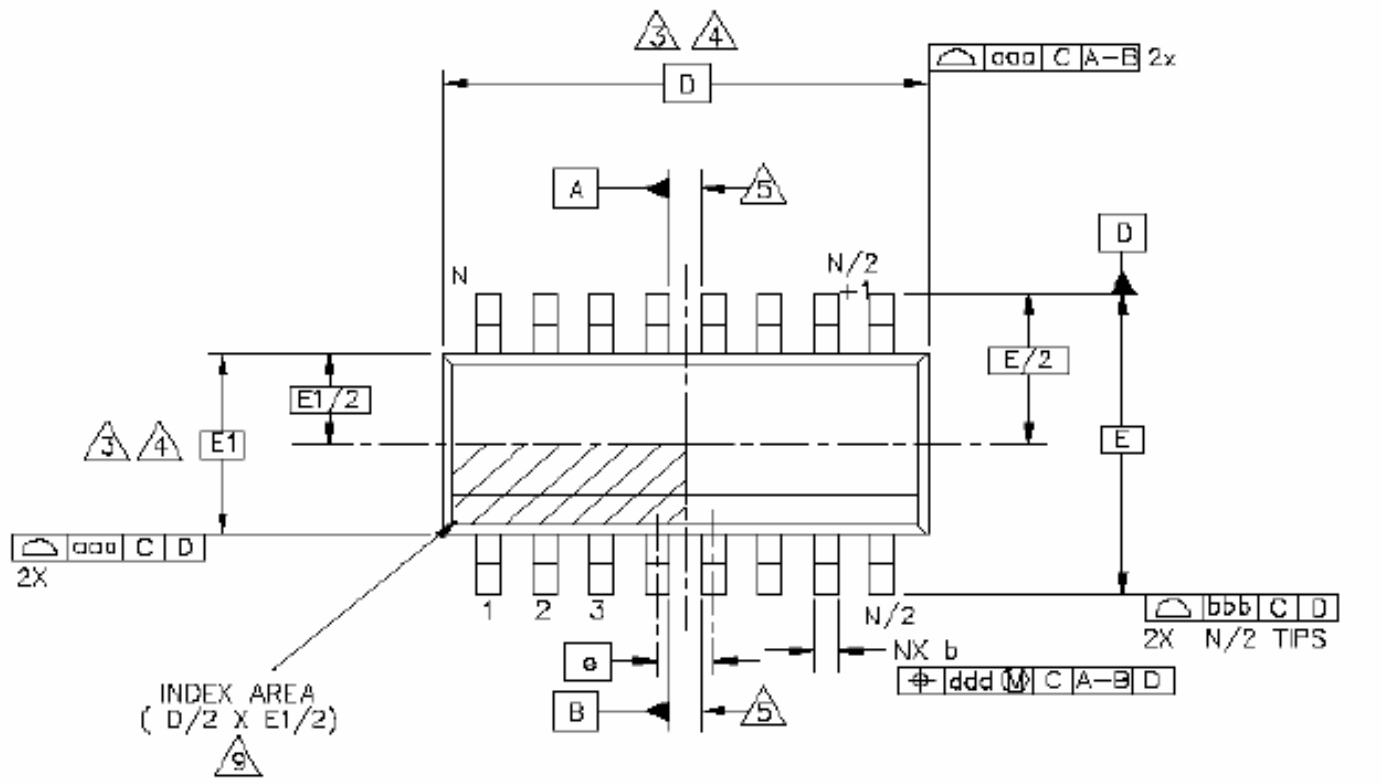
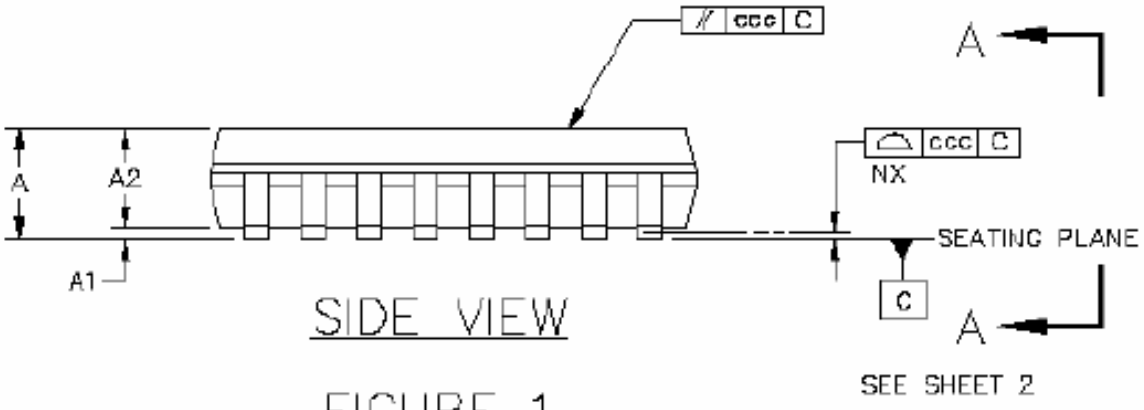
28 PINS, SSOP, 150MIL





SEE SHEET 2

FIGURE 1

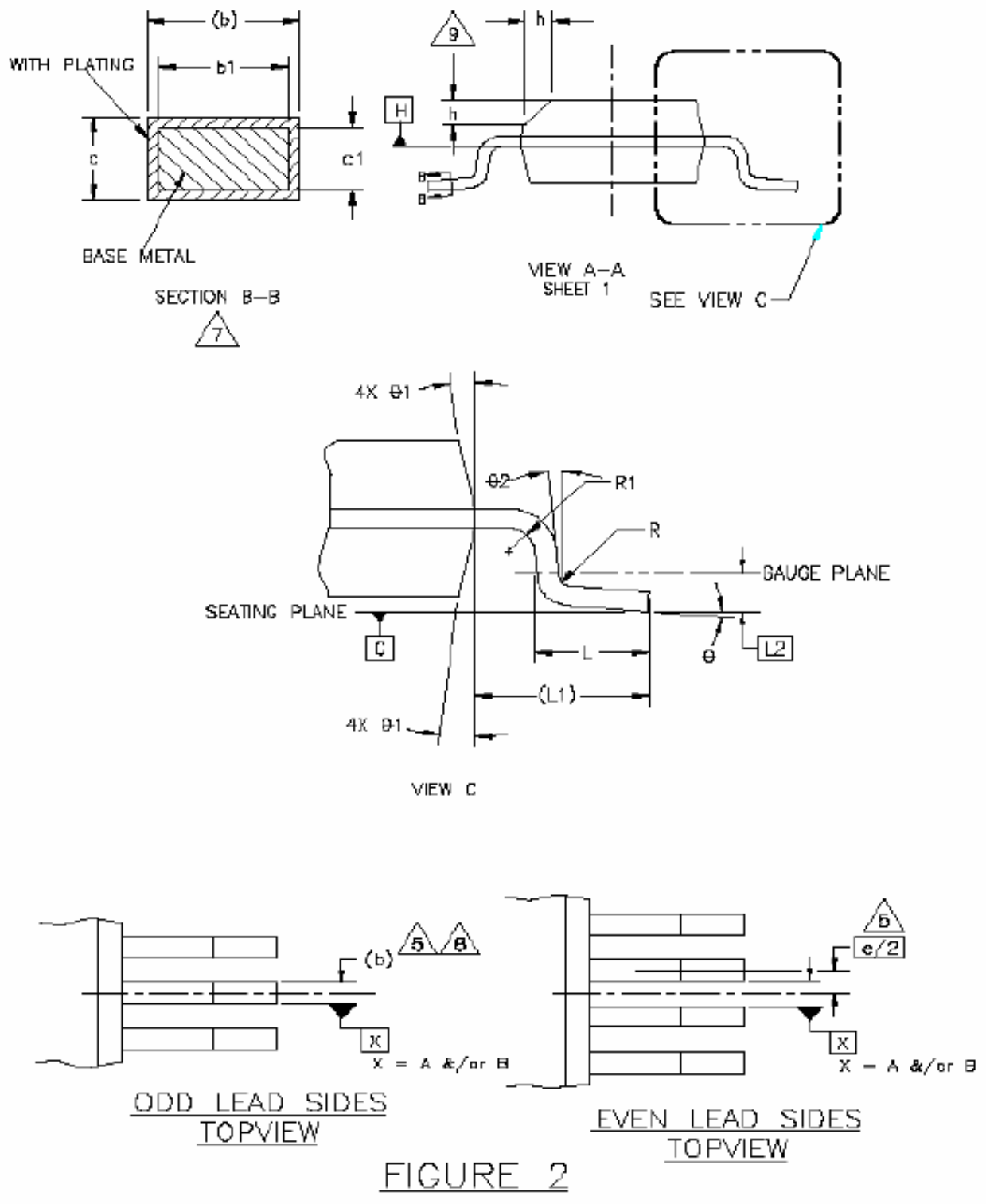

(b)
WITH PLATING
b1
c
c1
BASE METAL
SECTION B–B
7
9
h
H
h
VIEW A–A
SHEET 1
SEE VIEW C
4X θ1
θ2
R1
R
GAUGE PLANE
SEATING PLANE
C
L
θ
L2
(L1)
4X θ1
VIEW C
(b)
5
8
X
X = A &/or B
ODD LEAD SIDES
TOPVIEW
5
e/2
X
X = A &/or B
EVEN LEAD SIDES
TOPVIEW

FIGURE 2

Symbol	Dimension in Inches		
	Min.	Typ.	Max.
A	0.053	-	0.069
A1	0.004	-	0.010
A2	0.049	-	0.065
b	0.008	-	0.012
c	0.006	-	0.010
D	0.390 BSC.		
E	0.236 BSC.		
E1	0.154 BSC.		
e	0.025 BSC.		
L	0.016	-	0.050
L1	0.041 REF.		
R	0.003	-	-
R1	0.003	-	-
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions in Inches (Angles in Degrees)
3. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.006 inches per end. Dimension E1 does not include interlead flashor protrusion. Interlead flash or protrusion shall not exceed 0.006 inches per side. D and E1 dimensions are determined at datum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
5. Datums A & B to be determined at datum H.
6. The dimensions apply to the flat section of the lead between 0.004 to 0.010 inches from the lead tip.
7. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.004 inches total in excess of the b dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.
8. Refer to JEDEC MO-137 Variation AF

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