NETWORK SEARCH ENGINE
32K x 72 Entries

To request the full IDT75N42102 datasheet, please contact your local IDT Sales Representative or call 1-800-345-7015

Device Description

IDT provides proven, industry-leading network search engines (NSEs) that enable and accelerate the intelligent processing of network services in communications equipment. As a part of the complete IDT classification subsystem that includes content inspection engines, the IDT family of NSEs delivers high-performance, feature-rich, easy-to-use, integrated search accelerators.

The IDT 75N42102 NSE is a high performance, low cost, full-ternary 32K x 72 entry device. Each entry location in the NSE has both a Data entry and an associated Mask entry. The NSE devices integrate content addressable memory (CAM) technology with high-performance logic. The device can perform Lookup operations plus Read and Write maintenance operations.

The IDT 75N42102 NSE device has a bi-directional bus that is a multiplexed address and data bus that can support up to 200 million sustained searches per second. This device offers the ability to simultaneously search in mutually exclusive databases substantially increasing the NSE search rate. This device can be configured to enable multiple width lookups from 40 to 288 bits wide. The IDT 75N42102 requires a 1.5-volt V_{DD1} supply and a 2.5-volt V_{DD2} supply.

The IDT 75N42102 NSE utilizes the latest high-performance 1.5V CMOS processing technology and is packaged in a JEDEC Standard, thermally enhanced, 304 pin low profile Ball Grid Array.

Block Diagram
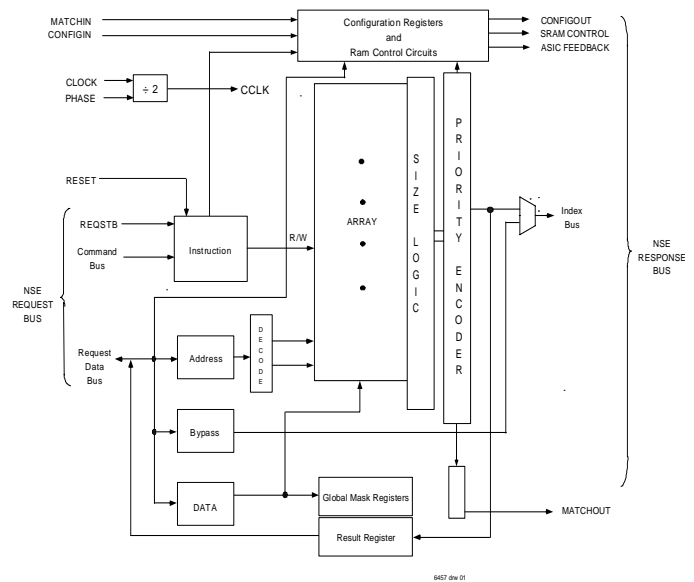
System Configurations

The IDT NSEs are designed to fulfill the needs of various types of networking systems. In solutions requiring data searching such as routers, a system configuration as shown in Figure 1.0 may be realized. In this configuration, the NSE interfaces directly to an ASIC/FPGA for lookups and routes an Index to an associated SRAM device, which supplies the next hop address via an SRAM Data Bus to the ASIC. The NSE provides the required control signals to directly hookup to ZBT™ or Synchronous Pipeline Burst SRAM. Lookup results can also be fed directly back to the ASIC/FPGA without the use of external SRAM. Control of the associated handshake signals is provided by all NSEs to adapt to either configuration.

Figure 1.0 ASIC / Compatible NSE / SRAM configuration


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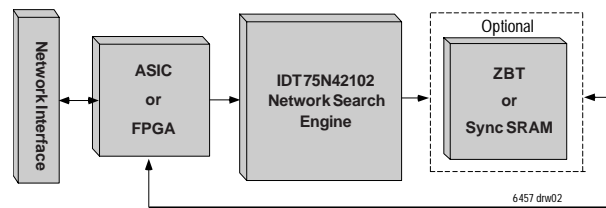
Features

- Full Ternary 32K x 72 bit content addressable memory
- Global Mask Registers
- 40/72/144/288 multiple width lookups
- 200M sustained lookups per second at 72 and 144 width lookups
- Dual bus interface
- Cascadable to 8 devices with no glue logic or latency penalty
- Glueless interface to standard ZBT™ or Synchronous Pipelined Burst SRAMs
- Boundary Scan JTAG Interface (IEEE 1149.1 compliant)
- 1.5V match power supply
- 2.5V core and I/O power supply

Functional Highlights

Data and Mask Array

The NSE has Data cell entries and associated Mask cell entries as shown in Fig. 1.1. This combination of Data and Mask cell entries enables the NSE to store 0, 1 or X, making it a full ternary Network Search Engine. During a lookup operation, both arrays are used along with a Global Mask Register to find a match to a requested data word.

Figure 1.1
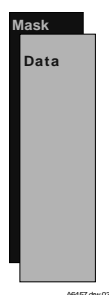
Bus Interface

The NSE utilizes a dual bus interface consisting of the NSE Request Bus and the NSE Response Bus.

The NSE Request Bus is comprised of the Command Bus and the Request Data Bus. The Command Bus handles the instruction to the NSE while the Request Data Bus is the main data path to the NSE.

The 72 bit bi-directional Request Data Bus functions as a multiplexed address and data bus, which performs the writing and reading of NSE entries, as well as presenting lookup data to the device.

The NSE Response Bus is comprised of an independent unidirectional Index Bus which drives the result of the lookup (or index) to either an SRAM device or an ASIC. In addition to driving the Index, the NSE Response Bus also drives the associated SRAM control signals ($\overline{CE}/\overline{OE}$, and $\overline{WE}$) for either ZBT™ or Synchronous Pipeline Burst SRAM devices.

Command Bus

The Command Bus loads the specific instructions into the NSE. These include:

- Read or Write

A Read or Write instruction operates on a specified data entry, mask entry, register or external SRAM.

- SRAM No Wait Read

An SRAM No Wait Read is a Read instruction to an external SRAM that can be pipelined within a series of operations and does not require the user to wait for the Read to complete before loading the next instruction.

- Lookup

A lookup can be requested in 40-bit, 72-bit, 144-bit or 288-bit widths.

- SMDL Lookup

The three SMDL Lookup instructions offer the ability to simultaneously search in mutually exclusive databases which increases the search rate up to 200 MSPS.

SRAM Interface

The NSE provides all required address and control signals for a glueless SRAM interface. The NSE provides a pipelined bypass path for reads or writes to the external SRAM. The ASIC/FPGA handles the pipelining of the data to and from the SRAM.

Registers

There are four basic types of registers supported:

- Configuration Registers are used at initialization to define the segmentation of the entries, timing of outputs and the SRAM interface.
- Global Mask Registers are provided to support Lookup instructions by masking individual bits during a search.
- Search Result Registers are used to store the resulting index of a search from a Lookup operation.
- Reply Width Registers are used with Lookup operations.

Signal Descriptions

Pin Function	I/O	Description
NSE Request Bus:		
Request Strobe	Input	This input signifies a valid input request and signals the start of an NSE operation cycle.
Command Bus	Input	Defines the instruction to be performed by the NSE and selects Global Mask registers and Search Result registers.
Request Data Bus	Input/Output Three State	The Request Data Bus is a multiplexed address/data bus used to perform reads (and writes) from (to) the NSE, and to present search data for lookups.
NSE Response Bus:		
Index Bus	Output Three State	This bus is used to drive the address of an external SRAM, or feedback Lookup result information directly to the NSE's ASIC/FPGA. The Index Bus contains the encoded location at which the compare was found.
Chip Enable/ Output Enable	Output Three State	This signal is driven along with the Index Bus. It is connected to the $\overline{CE}$ input pin of a ZBT SRAM or to the $\overline{OE}$ pin of a PBSRAM.
Write Enable	Output Three State	This signal is driven along with the Index bus. It is used to assert the $\overline{WE}$ pin of an external SRAM. It is active for SRAM write operations.
Read Acknowledge	Output	This signal is sent back when the data is read from the NSE on the Request Data Bus, or when the data being read from the associated external SRAM.
Match Acknowledge	Output	This is signal is sent with the Index. It will be driven low if there was no match, high if a match was found.
Valid Lookup Bit	Output	This signal is sent with the Index. It will be driven high upon the completion of a lookup, even if the lookup did not result in a hit.
Clock and Initialization:		
Clock Input	Input	All inputs and outputs are referenced to the positive edge of this clock.
Clock Phase Enable	Input	This signal is used to generate an internal clock at ½ the frequency of the input clock.
Reset	Input	This pin will force all outputs to a high impedance condition, as well as clearing the NSE enable bit.
Depth Expansion:		
Configuration In	Input	Configures the Device ID at power up.
Configuration Out	Output	Configures the Device ID at power up.
Match Input	Input	The Match Input signal is driven by all upstream Match Output signals. This indicates to all down stream NSEs that a hit in a higher priority NSE has occurred.
Match Output	Output	The Match Output signal signifies that a match has occurred in the NSE. The signal is fed into a Match Input line of all lower priority NSE(s).

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