

**Radiation Hardened 3.3V Quad Differential Line Receiver**

The Intersil HS-26CLV32RH is a radiation hardened 3.3V quad differential line receiver designed for digital data transmission over balanced lines, in low voltage, RS-422 protocol applications. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26CLV32RH has an input sensitivity of 200mV (Typ) over a common mode input voltage range of -4V to +7V. The receivers are also equipped with input fail safe circuitry, which causes the outputs to go to a logic “1” when the inputs are open. The device has unique inputs that remain high impedance when the receiver is disabled or powered-down, maintaining signal integrity in multi-receiver applications.

**Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.**

**Detailed Electrical Specifications for these devices are contained in SMD 5962-95689. A “hot-link” is provided on our homepage for downloading.**  
[www.intersil.com/military/](http://www.intersil.com/military/)

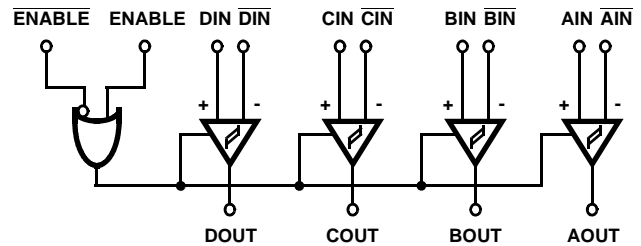
**Features**

- Electrically Screened to SMD # 5962-95689
- QML Qualified per MIL-PRF-38535 Requirements
- 1.2 Micron Radiation Hardened CMOS
  - Total Dose. . . . . 300 krad(Si)(Max)
  - Single Event Upset LET . . . . . 100MeV/mg/cm<sup>2</sup>
  - Single Event Latch-up Immune
- Low Stand-by Current . . . . . 13mA(Max)
- Operating Supply Range . . . . . 3.0V to 3.6V
- Enable Input Levels . . .  $V_{IH} > (0.7)(V_{DD})$ ;  $V_{IL} < (0.3)(V_{DD})$
- CMOS Output Levels . . . . .  $V_{OH} > 2.55V$ ;  $V_{OL} < 0.4V$
- Input Fail Safe Circuitry
- High Impedance Inputs when Disabled or Powered-down
- Full -55°C to +125°C Military Temperature Range
- Pb-Free (RoHS Compliant)

**Applications**

- Line Receiver for MIL-STD-1553 Serial Data Bus

**Logic Diagram**

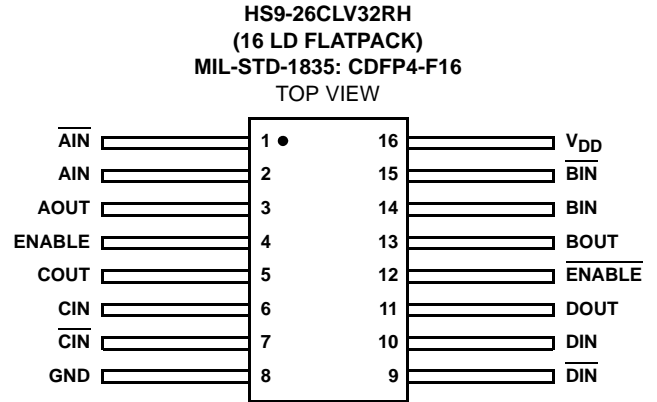
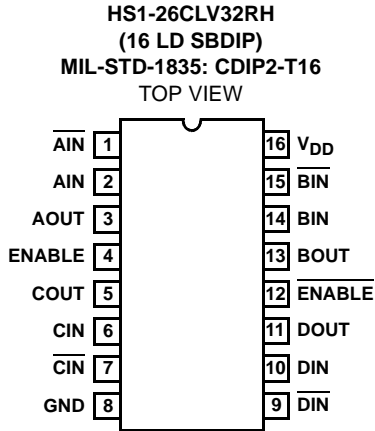


**Ordering Information**

ORDERING NUMBER (Note)	INTERNAL MKT. NO.	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
5962F9568902QEC	HS1-26CLV32RH-8	Q 5962F95 68902QEC	-55 to +125	16 Ld SBDIP	D16.3
5962F9568902QXC	HS9-26CLV32RH-8	Q 5962F95 68902QXC	-55 to +125	16 Ld FLATPACK	K16.A
5962F9568902VEC	HS1-26CLV32RH-Q	Q 5962F95 68902VEC	-55 to +125	16 Ld SBDIP	D16.3
5962F9568902VXC	HS9-26CLV32RH-Q	Q 5962F95 68902VXC	-55 to +125	16 Ld FLATPACK	K16.A
HS1-26CLV32RH/PROTO	HS1-26CLV32RH/PROTO	HS1- 26CLV32RH /PROTO	-55 to +125	16 Ld SBDIP	D16.3
HS9-26CLV32RH/PROTO	HS9-26CLV32RH/PROTO	HS9- 26CLV32RH /PROTO	-55 to +125	16 Ld FLATPACK	K16.A

NOTE: These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Pinouts



All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.  
Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)

**Die Characteristics**

**DIE DIMENSIONS:**

84 mils x 130 mils x 21 mils  
(2140µm x 3290µm)

**INTERFACE MATERIALS:**

**Glassivation:**

Type: PSG (Phosphorus Silicon Glass)  
Thickness: 8kÅ ±1kÅ

**Substrate:**

AVLS11RA, Silicon backside, V<sub>DD</sub> backside potential

**Metallization:**

Bottom: Mo/Tiw  
Thickness: 5800Å ±1kÅ  
Top: Al/Si/Cu  
Thickness: 10kÅ ±1kÅ

**Worst Case Current Density:**

<2.0 x 10<sup>5</sup>A/cm<sup>2</sup>

**Bond Pad Size:**

110µm x 100µm

**Metallization Mask Layout**

HS-26CLV32RH

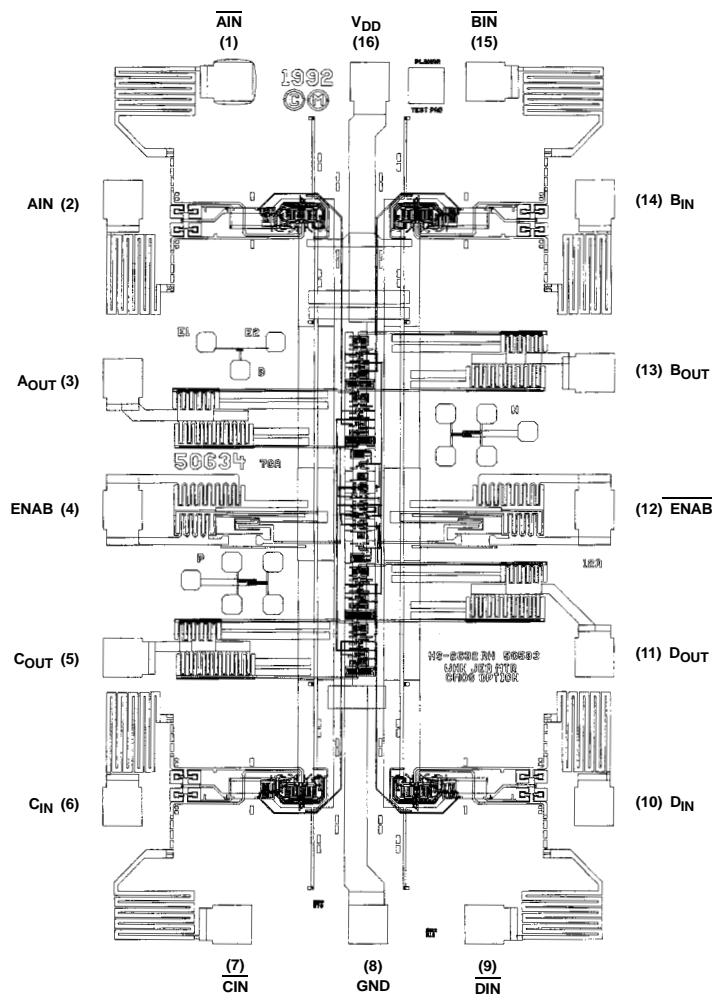


TABLE 1. HS26CLV32RH PAD COORDINATES

PIN NUMBER	PAD NAME	RELATIVE TO PIN 1	
		X COORDINATES	Y COORDINATES
1	AIN	0	0
2	AIN	-337.1	-362
3	AOUT	-337.1	-912.5
4	ENABLE	-337.1	-1319.3
5	COUT	-337.1	-1774.4
6	CIN	-337.1	-2233.7
7	CIN	0	-2595.7
8	GND	418.4	-2596.7
9	DIN	776.4	-2595.7
10	DIN	1113.5	-2233.7
11	DOUT	1113.5	-1774.4
12	ENABLE	1113.5	-1319.3
13	BOUT	1113.5	-898.4
14	BIN	1113.5	-362
15	BIN	776.4	0
16	VDD	420.2	1

NOTE: Dimensions in microns