Freescale Semiconductor
Data Sheet: Advance Information

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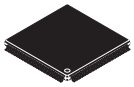
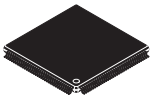
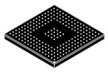
MPC5634M


144 LQFP
20 x 20 mm

100 LQFP
14 x 14 mm


176 LQFP
24 x 24 mm


208 MAPBGA
17 x 17 mm

MPC5634M Microcontroller Data Sheet

- Operating Parameters
  - Fully static operation, 0 MHz – 80 MHz (plus 2% frequency modulation - 82 MHz)
  - –40 °C to 150 °C junction temperature operating range
  - Low power design
    - Less than 400 mW power dissipation (nominal)
    - Designed for dynamic power management of core and peripherals
    - Software controlled clock gating of peripherals
    - Low power stop mode, with all clocks stopped
  - Fabricated in 90 nm process
  - 1.2 V internal logic
  - Single power supply with 5.0 V –10% / +5% (4.5 V to 5.25 V) with internal regulator to provide 3.3 V and 1.2 V for the core
  - Input and output pins with 5.0 V –10% / +5% (4.5 V to 5.25 V) range
    - 35%/65% V_{DDE} CMOS switch levels (with hysteresis)
    - Selectable hysteresis
    - Selectable slew rate control
  - Nexus pins powered by 3.3 V supply
  - Designed with EMI reduction techniques
    - Phase-locked loop
    - Frequency modulation of system clock frequency
    - On-chip bypass capacitance
    - Selectable slew rate and drive strength
- High performance e200z335 core processor
  - 32-bit *Power Architecture Book E* programmer's model
  - Variable Length Encoding Enhancements
    - Allows Power Architecture instruction set to be optionally encoded in a mixed 16 and 32-bit instructions
    - Results in smaller code size
  - Single issue, 32-bit *Power Architecture Book E* compliant CPU
  - In-order execution and retirement
  - Precise exception handling
  - Branch processing unit
    - Dedicated branch address calculation adder
    - Branch acceleration using Branch Lookahead Instruction Buffer
  - Load/store unit
    - One-cycle load latency
    - Fully pipelined
    - Big and Little Endian support
    - Misaligned access support
    - Zero load-to-use pipeline bubbles
  - Thirty-two 64-bit general purpose registers (GPRs)
  - Memory management unit (MMU) with 16-entry fully-associative translation look-aside buffer (TLB)
  - Separate instruction bus and load/store bus
  - Vectored interrupt support
  - Interrupt latency < 120 ns @ 80 MHz (measured from interrupt request to execution of first instruction of interrupt exception handler)
  - Non-maskable interrupt (NMI) input for handling external events that must produce an immediate response, e.g., power down detection. On this device, the NMI input is connected to the Critical Interrupt Input. (May not be recoverable)
  - Critical Interrupt input. For external interrupt sources that are higher priority than provided by the Interrupt Controller. (Always recoverable)
  - New 'Wait for Interrupt' instruction, to be used with new low power modes
  - Reservation instructions for implementing read-modify-write accesses
  - Signal processing extension (SPE) APU

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- Operating on all 32 GPRs that are all extended to 64 bits wide
- Provides a full compliment of vector and scalar integer and floating point arithmetic operations (including integer vector MAC and MUL operations) (SIMD)
- Provides rich array of extended 64-bit loads and stores to/from extended GPRs
- Fully code compatible with e200z6 core

— Floating point
- IEEE 754 compatible with software wrapper
- Scalar single precision in hardware, double precision with software library
- Conversion instructions between single precision floating point and fixed point
- Fully code compatible with e200z6 core

— Long cycle time instructions, except for guarded loads, do not increase interrupt latency
— Extensive system development support through Nexus debug port

• Advanced microcontroller bus architecture (AMBA) crossbar switch (XBAR)
— Three master ports, four slave ports
- Masters: CPU Instruction bus; CPU Load/store bus (Nexus); eDMA
- Slave: Flash; SRAM; Peripheral Bridge; calibration EBI

— 32-bit internal address bus, 64-bit internal data bus

• Enhanced direct memory access (eDMA) controller
— 32 channels support independent 8-bit, 16-bit, or 32-bit single value or block transfers
— Supports variable sized queues and circular queues
— Source and destination address registers are independently configured to post-increment or remain constant
— Each transfer is initiated by a peripheral, CPU, or eDMA channel request
— Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer

• Interrupt controller (INTC)
— 191 peripheral interrupt request sources
— 8 software settable interrupt request sources
— 9-bit vector
- Unique vector for each interrupt request source
- Provided by hardware connection to processor or read from register

— Each interrupt source can be programmed to one of 16 priorities
— Preemption
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority. Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.

— Low latency—three clocks from receipt of interrupt request from peripheral to interrupt request to processor

• Frequency Modulating Phase-locked loop (FMPLL)
— Reference clock pre-divider (PREDIV) for finer frequency synthesis resolution
— Reduced frequency divider (RFD) for reducing the FMPLL output clock frequency without forcing the FMPLL to re-lock
— System clock divider (SYSDIV) for reducing the system clock frequency in normal or bypass mode
— Input clock frequency range from 4 MHz to 20 MHz before the pre-divider, and from 4 MHz to 16 MHz at the FMPLL input
— Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz

- VCO free-running frequency range from 25 MHz to 125 MHz
- Four bypass modes: crystal or external reference with PLL on or off
- Two normal modes: crystal or external reference
- Programmable frequency modulation
  - Triangle wave modulation
  - Register programmable modulation frequency and depth
- Lock detect circuitry reports when the FMPLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
  - User-selectable ability to generate an interrupt request upon loss of lock
  - User-selectable ability to generate a system reset upon loss of lock
- Clock quality monitor (CQM) module provides loss-of-clock detection for the FMPLL reference and output clocks
  - User-selectable ability to generate an interrupt request upon loss of clock
  - User-selectable ability to generate a system reset upon loss of clock
  - Backup clock (reference clock or FMPLL free-running) can be applied to the system in case of loss of clock

- Calibration bus interface (EBI)
  - Available only in the calibration package
  - 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
  - Memory controller with support for various memory types
  - 16-bit data bus, up to 22-bit address bus
  - Selectable drive strength
  - Configurable bus speed modes
  - Bus monitor
  - Configurable wait states
- System integration unit (SIU)
  - Centralized GPIO control of 80 I/O pins
  - Centralized pad control on a per-pin basis
    - Pin function selection
    - Configurable weak pull-up or pull-down
    - Drive strength
    - Slew rate
    - Hysteresis
  - System reset monitoring and generation
  - External interrupt inputs, filtering and control
  - Critical Interrupt control
  - Non-Maskable Interrupt control
  - Internal multiplexer subblock (IMUX)
    - Allows flexible selection of eQADC trigger inputs (eTPU, eMIOS and external signals)
    - Allows selection of interrupt requests between external pins and DSPI
- Error correction status module (ECSM)
  - Configurable error-correcting codes (ECC) reporting
  - Single-bit error correction reporting
- On-chip flash memory
  - Up to 1.5 MB flash memory, accessed via a 64-bit wide bus interface
  - 16 KB shadow block

- Fetch Accelerator
  - Provide single cycle flash access at 80 MHz
  - Quadruple 128-bit wide prefetch/burst buffers
  - Prefetch buffers can be configured to prefetch code or data or both
- Censorship protection scheme to prevent flash content visibility
- Flash divided into two independent arrays, allowing reading from one array while erasing/programming the other array (used for EEPROM emulation)
- Memory block:
  - For MPC5634M: 18 blocks (4 × 16 KB, 2 × 32 KB, 2 × 64 KB, 10 × 128 KB)
  - For MPC5633M: 14 blocks (4 × 16 KB, 2 × 32 KB, 2 × 64 KB, 6 × 128 KB)
  - For MPC5632M: 12 blocks (4 × 16 KB, 2 × 32 KB, 2 × 64 KB, 4 × 128 KB)
- Hardware programming state machine

- On-chip static RAM
  - For MPC5634M: 94 KB general purpose RAM of which 32 KB are on standby power supply
  - For MPC5633M: 64 KB general purpose RAM of which 24 KB are on standby power supply
  - For MPC5632M: 48 KB general purpose RAM of which 24 KB are on standby power supply
- Boot assist module (BAM)
  - Enables and manages the transition of MCU from reset to user code execution in the following configurations:
    - Execution from internal flash memory
    - Execution from external memory on the calibration bus
    - Download and execution of code via FlexCAN or eSCI
- Periodic interrupt timer (PIT)
  - 32-bit wide down counter with automatic reload
  - Four channels clocked by system clock
  - One channel clocked by crystal clock
  - Each channel can produce periodic software interrupt
  - Each channel can produce periodic triggers for eQADC queue triggering
  - One channel out of the five can be used as wake-up timer to wake device from low power stop mode
- System timer module (STM)
  - 32-bit up counter with 8-bit prescaler
  - Clocked from system clock
  - Four-channel timer compare hardware
  - Each channel can generate a unique interrupt request
  - Designed to address AutoSAR task monitor function
- Software watchdog timer (SWT)
  - 32-bit timer
  - Clock by system clock or crystal clock
  - Can generate either system reset or non-maskable interrupt followed by system reset
  - Enabled out of reset
- Enhanced modular I/O system (eMIOS)
  - 16 timer channels (up to 14 channels in 144 LQFP)
  - 24-bit timer resolution
  - Supports a subset of the timer modes found in eMIOS on MPC5554
  - 3 selectable time bases plus shared time or angle counter bus from eTPU2
  - DMA and interrupt request support

— Motor control capability

- Second-generation enhanced time processor unit (eTPU2)
  - — Object-code compatible with eTPU—no changes are required to hardware or software if only eTPU features are used
  - — Intelligent co-processor designed for timing control
  - — High level tools, assembler and compiler available
  - — 32 channels (each channel has dedicated I/O pin in all packages)
  - — 24-bit timer resolution
  - — 14 KB code memory and 3 KB data memory
  - — Double match and capture on all channels
  - — Angle clock hardware support
  - — Shared time or angle counter bus with eMIOS
  - — DMA and interrupt request support
  - — Nexus Class 1 debug support
  - — eTPU2 enhancements
    - – Counters and channels can run at full system clock speed
    - – Software watchdog
    - – Real-time performance monitor
    - – Instruction set enhancements for smaller more flexible code generation
    - – Programmable channel mode for customization of channel operation
- Enhanced queued A/D converter (eQADC)
  - — Two independent on-chip RSD Cyclic ADCs
    - – 8-, 10-, and 12-bit resolution
    - – Differential conversions
    - – Targets up to 10-bit accuracy at 500 KSample/s (ADC_CLK = 7.5 MHz) and 8-bit accuracy at 1 MSample/s (ADC_CLK = 15 MHz) for differential conversions
    - – Differential channels include variable gain amplifier for improved dynamic range (×1; ×2; ×4)
    - – Differential channels include programmable pull-up and pull-down resistors for biasing and sensor diagnostics (200 kΩ; 100 kΩ; low value of 5 kΩ)
    - – Single-ended signal range from 0 to 5 V
    - – Sample times of 2 (default), 8, 64 or 128 ADC clock cycles
    - – Provides time stamp information when requested
    - – Parallel interface to eQADC command FIFOs (CFIFOs) and result FIFOs (RFIFOs)
    - – Supports both right-justified unsigned and signed formats for conversion results
    - – Temperature sensor to enable measurement of die temperature
    - – Ability to measure all power supply pins directly
  - — Automatic application of ADC calibration constants
    - – Provision of reference voltages (25% VREF and 75% VREF) for ADC calibration purposes
  - — Up to 34[1] input channels available to the two on-chip ADCs
  - — Four pairs of differential analog input channels
  - — Full duplex synchronous serial interface to an external device
    - – Has a free-running clock for use by the external device
    - – Supports a 26-bit message length

1. 176-pin and 208-pin packages have 34 input channels; 144-pin package has 32.

- Transmits a null message when there are no triggered CFIFOs with commands bound for external CBuffers, or when there are triggered CFIFOs with commands bound for external CBuffers but the external CBuffers are full

— Parallel Side Interface to communicate with an on-chip companion module
— Zero jitter triggering for queue 0. (Queue 0 trigger causes current conversion to be aborted and the queued conversions in the CBUFFER to be bypassed. Delay from Trigger to start of conversion is 13 system clocks + 1 ADC clock.)
— eQADC Result Streaming. Generation of a continuous stream of ADC conversion results from a single eQADC command word. Controlled by two different trigger signals; one to define the rate at which results are generated and the other to define the beginning and ending of the stream. Used to digitize waveforms during specific time/angle windows, e.g., engine knock sensor sampling.
— Angular Decimation. The ability of the eQADC to sample an analog waveform in the time domain, perform FIR/IIR filtering also in the time domain, but to down sample the results in the angle domain. Resulting in a time domain filtered result at a given engine angle.
— Priority Based CFIFOs
  - Supports six CFIFOs with fixed priority. The lower the CFIFO number, the higher its priority. When commands of distinct CFIFOs are bound for the same CBuffer, the higher priority CFIFO is always served first.
  - Supports software and several hardware trigger modes to arm a particular CFIFO
  - Generates interrupt when command coherency is not achieved
— External Hardware Triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter
— Supports four external 8-to-1 muxes which can expand the input channel number from 34[1] to 59

- Two deserial serial peripheral interface modules (DSPI)
  — SPI
    - Full duplex communication ports with interrupt and DMA request support
    - Supports all functional modes from QSPI subblock of QSMCM (MPC5xx family)
    - Support for queues in RAM
    - 6 chip selects, expandable to 64 with external demultiplexers
    - Programmable frame size, baud rate, clock delay and clock phase on a per frame basis
    - Modified SPI mode for interfacing to peripherals with longer setup time requirements
    - LVDS option for output clock and data to allow higher speed communication
  — Deserial serial interface (DSI)
    - Pin reduction by hardware serialization and deserialization of eTPU, eMIOS channels and GPIO
    - 32 bits per DSPI module
    - Triggered transfer control and change in data transfer control (for reduced EMI)
    - Compatible with Microsecond Bus Version 1.0 downlink
- Two enhanced serial communication interface (eSCI) modules
  — UART mode provides NRZ format and half or full duplex interface
  — eSCI bit rate up to 1 Mbps
  — Advanced error detection, and optional parity generation and detection
  — Word length programmable as 8, 9, 12 or 13 bits
  — Separately enabled transmitter and receiver
  — LIN support

1. 176-pin and 208-ball packages.

- DMA support
- Interrupt request support
- Programmable clock source: system clock or oscillator clock
- Support Microsecond Bus (Timed Serial Bus - TSB) uplink Version 1.0

- Two FlexCAN
  - One with 32 message buffers; the second with 64 message buffers
  - Full implementation of the CAN protocol specification, Version 2.0B
  - Based on and including all existing features of the Freescale TouCAN module
  - Programmable acceptance filters
  - Short latency time for high priority transmit messages
  - Arbitration scheme according to message ID or message buffer number
  - Listen only mode capabilities
  - Programmable clock source: system clock or oscillator clock
  - Message buffers may be configured as mailboxes or as FIFO
- Nexus port controller (NPC)
  - Per IEEE-ISTO 5001-2003
  - Real time development support for Power Architecture core and eTPU engine through Nexus class 2/1
  - Read and write access (Nexus class 3 feature that is supported on this device)
    - Run-time access of entire memory map
    - Calibration
  - Support for data value breakpoints / watchpoints
    - Run-time access of entire memory map
    - Calibration

      Table constants calibrated using MMU and internal and external RAM

      Scalar constants calibrated using cache line locking
  - Configured via the IEEE 1149.1 (JTAG) port
- IEEE 1149.1 JTAG controller (JTAGC)
  - IEEE 1149.1-2001 Test Access Port (TAP) interface
  - 5-bit instruction register that supports IEEE 1149.1-2001 defined instructions
  - 5-bit instruction register that supports additional public instructions
  - Three test data registers: a bypass register, a boundary scan register, and a device identification register
  - Censorship disable register. By writing the 64-bit serial boot password to this register, Censorship may be disabled until the next reset
  - TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- On-chip Voltage Regulator for single 5 V supply operation
  - On-chip regulator 5 V to 3.3 V for internal supplies
  - On-chip regulator controller 5 V to 1.2 V (with external bypass transistor) for core logic
- Low-power modes
  - SLOW Mode. Allows device to be run at very low speed (approximately 1 MHz), with modules (including the PLL) selectively disabled in software
  - STOP Mode. System clock stopped to all modules including the CPU. Wake-up timer used to restart the system clock after a predetermined time

1 Introduction

1.1 Document overview

This document provides an overview and describes the features of the MPC5634M series of microcontroller units (MCUs). For functional characteristics, refer to the device reference manual. Electrical specifications and package mechanical drawings are included in this device data sheet. Pin assignments can be found in both the reference manual and data sheet.

1.2 Description

These 32-bit automotive microcontrollers are a family of system-on-chip (SoC) devices that contain all the features of the MPC5500 family and many new features coupled with high performance 90 nm CMOS technology to provide substantial reduction of cost per feature and significant performance improvement. The advanced and cost-efficient host processor core of this automotive controller family is built on Power Architecture® technology. This family contains enhancements that improve the architecture's fit in embedded applications, includes additional instruction support for digital signal processing (DSP), integrates technologies—such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system—that are important for today's lower-end powertrain applications. This device family is a completely compatible extension to Freescale's MPC5500 family. The device has a single level of memory hierarchy consisting of up to 94 KB on-chip SRAM and up to 1.5 MB of internal flash memory. The device also has an external bus interface (EBI) for 'calibration'. This external bus interface has been designed to support most of the standard memories used with the MPC5xx and MPC55xx families.

2 Overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5634M series of microcontroller units (MCUs). For functional characteristics, refer to the *MPC5634M Microcontroller Reference Manual.*

The MPC5634M series microcontrollers are system-on-chip devices that are built on Power Architecture® technology and:

- Are 100% user-mode compatible with the Power Architecture instruction set
- Contain enhancements that improve the architecture's fit in embedded applications
- Include additional instruction support for digital signal processing (DSP)
- Integrate technologies such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system

2.1 Device comparison

Table 1. MPC5634M family device summary

Feature	MPC5634M	MPC5633M	MPC5632M
Flash memory size (KB)	1536	1024	768
Total SRAM size (KB)	94	64	48
Standby SRAM size (KB)	32	24	24
Processor core	32-bit e200z335 with SPE support	32-bit e200z335 with SPE support	32-bit e200z335 with SPE support
Core frequency (MHz)	60/80	40/60/80	40/60
Calibration bus width[1]	16 bits	16 bits	—
DMA (direct memory access) channels	32	32	32
eMIOS (enhanced modular input-output system) channels	16	16	8
eQADC (enhanced queued analog-to-digital converter) channels (on-chip)	Up to 34[2]	Up to 34[2]	Up to 32[2]
eSCI (serial communication interface)	2	2	2
DSPI (deserial serial peripheral interface)	2	2	2
Microsecond Bus compatible interface	2	2	2
eTPU (enhanced time processor unit)	Yes	Yes	Yes
Channels	32	32	32
Code memory (KB)	14	14	14
Parameter RAM (KB)	3	3	3
FlexCAN (controller area network)[3]	2	2	2
FMPLL (frequency-modulated phase-locked loop)	Yes	Yes	Yes
INTC (interrupt controller) channels	364[4]	364[4]	364[4]
JTAG controller	Yes	Yes	Yes
NDI (Nexus development interface) level	Class 2+	Class 2+	Class 2+
Non-maskable interrupt and critical interrupt	Yes	Yes	Yes
PIT (peripheral interrupt timers)	5	5	5
Task monitor timer	4 channels	4 channels	4 channels
Temperature sensor	Yes	Yes	Yes
Windowing software watchdog	Yes	Yes	Yes
Packages	144 LQFP 176 LQFP 208 MAPBGA	144 LQFP 176 LQFP 208 MAPBGA	144 LQFP

1 Calibration package only.

2 The 176-pin and 208-pin packages have 34 input channels; 144-pin package has 32.

3 One FlexCAN module has 64 message buffers; the other has 32 message buffers.

[4] 165 interrupt channels are reserved for compatibility with future devices. This device has 191 peripheral interrupt sources plus 8 software interrupts available to the user.

2.2 MPC5634M features

- Operating Parameters
  - Fully static operation, 0 MHz – 80 MHz (plus 2% frequency modulation - 82 MHz)
  - –40 °C to 150 °C junction temperature operating range
  - Low power design
    - Less than 400 mW power dissipation (nominal)
    - Designed for dynamic power management of core and peripherals
    - Software controlled clock gating of peripherals
    - Low power stop mode, with all clocks stopped
  - Fabricated in 90 nm process
  - 1.2 V internal logic
  - Single power supply with 5.0 V –10% / +5% (4.5 V to 5.25 V) with internal regulator to provide 3.3 V and 1.2 V for the core
  - Input and output pins with 5.0 V –10% / +5% (4.5 V to 5.25 V) range
    - 35%/65% V_{DDE} CMOS switch levels (with hysteresis)
    - Selectable hysteresis
    - Selectable slew rate control
  - Nexus pins powered by 3.3 V supply
  - Designed with EMI reduction techniques
    - Phase-locked loop
    - Frequency modulation of system clock frequency
    - On-chip bypass capacitance
    - Selectable slew rate and drive strength
- High performance e200z335 core processor
  - 32-bit *Power Architecture Book E* programmer's model
  - Variable Length Encoding Enhancements
    - Allows Power Architecture instruction set to be optionally encoded in a mixed 16 and 32-bit instructions
    - Results in smaller code size
  - Single issue, 32-bit *Power Architecture Book E* compliant CPU
  - In-order execution and retirement
  - Precise exception handling
  - Branch processing unit
    - Dedicated branch address calculation adder
    - Branch acceleration using Branch Lookahead Instruction Buffer
  - Load/store unit
    - One-cycle load latency
    - Fully pipelined
    - Big and Little Endian support
    - Misaligned access support
    - Zero load-to-use pipeline bubbles
  - Thirty-two 64-bit general purpose registers (GPRs)

- Memory management unit (MMU) with 16-entry fully-associative translation look-aside buffer (TLB)
- Separate instruction bus and load/store bus
- Vectored interrupt support
- Interrupt latency < 120 ns @ 80 MHz (measured from interrupt request to execution of first instruction of interrupt exception handler)
- Non-maskable interrupt (NMI) input for handling external events that must produce an immediate response, e.g., power down detection. On this device, the NMI input is connected to the Critical Interrupt Input. (May not be recoverable)
- Critical Interrupt input. For external interrupt sources that are higher priority than provided by the Interrupt Controller. (Always recoverable)
- New 'Wait for Interrupt' instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
  - Operating on all 32 GPRs that are all extended to 64 bits wide
  - Provides a full compliment of vector and scalar integer and floating point arithmetic operations (including integer vector MAC and MUL operations) (SIMD)
  - Provides rich array of extended 64-bit loads and stores to/from extended GPRs
  - Fully code compatible with e200z6 core
- Floating point
  - IEEE 754 compatible with software wrapper
  - Scalar single precision in hardware, double precision with software library
  - Conversion instructions between single precision floating point and fixed point
  - Fully code compatible with e200z6 core
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port

- Advanced microcontroller bus architecture (AMBA) crossbar switch (XBAR)
  - Three master ports, four slave ports
    - Masters: CPU Instruction bus; CPU Load/store bus (Nexus); eDMA
    - Slave: Flash; SRAM; Peripheral Bridge; calibration EBI
  - 32-bit internal address bus, 64-bit internal data bus
- Enhanced direct memory access (eDMA) controller
  - 32 channels support independent 8-bit, 16-bit, or 32-bit single value or block transfers
  - Supports variable sized queues and circular queues
  - Source and destination address registers are independently configured to post-increment or remain constant
  - Each transfer is initiated by a peripheral, CPU, or eDMA channel request
  - Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- Interrupt controller (INTC)
  - 191 peripheral interrupt request sources
  - 8 software settable interrupt request sources
  - 9-bit vector
    - Unique vector for each interrupt request source
    - Provided by hardware connection to processor or read from register
  - Each interrupt source can be programmed to one of 16 priorities
  - Preemption
    - Preemptive prioritized interrupt requests to processor

        - ISR at a higher priority preempts ISRs or tasks at lower priorities
        - Automatic pushing or popping of preempted priority to or from a LIFO
        - Ability to modify the ISR or task priority. Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
    - Low latency—three clocks from receipt of interrupt request from peripheral to interrupt request to processor
- Frequency Modulating Phase-locked loop (FMPLL)
    - Reference clock pre-divider (PREDIV) for finer frequency synthesis resolution
    - Reduced frequency divider (RFD) for reducing the FMPLL output clock frequency without forcing the FMPLL to re-lock
    - System clock divider (SYSDIV) for reducing the system clock frequency in normal or bypass mode
    - Input clock frequency range from 4 MHz to 20 MHz before the pre-divider, and from 4 MHz to 16 MHz at the FMPLL input
    - Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz
    - VCO free-running frequency range from 25 MHz to 125 MHz
    - Four bypass modes: crystal or external reference with PLL on or off
    - Two normal modes: crystal or external reference
    - Programmable frequency modulation
        - Triangle wave modulation
        - Register programmable modulation frequency and depth
    - Lock detect circuitry reports when the FMPLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
        - User-selectable ability to generate an interrupt request upon loss of lock
        - User-selectable ability to generate a system reset upon loss of lock
    - Clock quality monitor (CQM) module provides loss-of-clock detection for the FMPLL reference and output clocks
        - User-selectable ability to generate an interrupt request upon loss of clock
        - User-selectable ability to generate a system reset upon loss of clock
        - Backup clock (reference clock or FMPLL free-running) can be applied to the system in case of loss of clock
- Calibration bus interface (EBI)
    - Available only in the calibration package
    - 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
    - Memory controller with support for various memory types
    - 16-bit data bus, up to 22-bit address bus
    - Selectable drive strength
    - Configurable bus speed modes
    - Bus monitor
    - Configurable wait states
- System integration unit (SIU)
    - Centralized GPIO control of 80 I/O pins
    - Centralized pad control on a per-pin basis
        - Pin function selection
        - Configurable weak pull-up or pull-down
        - Drive strength
        - Slew rate
        - Hysteresis
    - System reset monitoring and generation

- External interrupt inputs, filtering and control
- Critical Interrupt control
- Non-Maskable Interrupt control
- Internal multiplexer subblock (IMUX)
  - Allows flexible selection of eQADC trigger inputs (eTPU, eMIOS and external signals)
  - Allows selection of interrupt requests between external pins and DSPI

- Error correction status module (ECSM)
  - Configurable error-correcting codes (ECC) reporting
  - Single-bit error correction reporting
- On-chip flash memory
  - Up to 1.5 MB flash memory, accessed via a 64-bit wide bus interface
  - 16 KB shadow block
  - Fetch Accelerator
    - Provide single cycle flash access at 80 MHz
    - Quadruple 128-bit wide prefetch/burst buffers
    - Prefetch buffers can be configured to prefetch code or data or both
  - Censorship protection scheme to prevent flash content visibility
  - Flash divided into two independent arrays, allowing reading from one array while erasing/programming the other array (used for EEPROM emulation)
  - Memory block:
    - For MPC5634M: 18 blocks (4 × 16 KB, 2 × 32 KB, 2 × 64 KB, 10 × 128 KB)
    - For MPC5633M: 14 blocks (4 × 16 KB, 2 × 32 KB, 2 × 64 KB, 6 × 128 KB)
    - For MPC5632M: 12 blocks (4 × 16 KB, 2 × 32 KB, 2 × 64 KB, 4 × 128 KB)
  - Hardware programming state machine
- On-chip static RAM
  - For MPC5634M: 94 KB general purpose RAM of which 32 KB are on standby power supply
  - For MPC5633M: 64 KB general purpose RAM of which 24 KB are on standby power supply
  - For MPC5632M: 48 KB general purpose RAM of which 24 KB are on standby power supply
- Boot assist module (BAM)
  - Enables and manages the transition of MCU from reset to user code execution in the following configurations:
    - Execution from internal flash memory
    - Execution from external memory on the calibration bus
    - Download and execution of code via FlexCAN or eSCI
- Periodic interrupt timer (PIT)
  - 32-bit wide down counter with automatic reload
  - Four channels clocked by system clock
  - One channel clocked by crystal clock
  - Each channel can produce periodic software interrupt
  - Each channel can produce periodic triggers for eQADC queue triggering
  - One channel out of the five can be used as wake-up timer to wake device from low power stop mode
- System timer module (STM)
  - 32-bit up counter with 8-bit prescaler
  - Clocked from system clock
  - Four-channel timer compare hardware
  - Each channel can generate a unique interrupt request

- Designed to address AutoSAR task monitor function
- Software watchdog timer (SWT)
  - 32-bit timer
  - Clock by system clock or crystal clock
  - Can generate either system reset or non-maskable interrupt followed by system reset
  - Enabled out of reset
- Enhanced modular I/O system (eMIOS)
  - 16 timer channels (up to 14 channels in 144 LQFP)
  - 24-bit timer resolution
  - Supports a subset of the timer modes found in eMIOS on MPC5554
  - 3 selectable time bases plus shared time or angle counter bus from eTPU2
  - DMA and interrupt request support
  - Motor control capability
- Second-generation enhanced time processor unit (eTPU2)
  - Object-code compatible with eTPU—no changes are required to hardware or software if only eTPU features are used
  - Intelligent co-processor designed for timing control
  - High level tools, assembler and compiler available
  - 32 channels (each channel has dedicated I/O pin in all packages)
  - 24-bit timer resolution
  - 14 KB code memory and 3 KB data memory
  - Double match and capture on all channels
  - Angle clock hardware support
  - Shared time or angle counter bus with eMIOS
  - DMA and interrupt request support
  - Nexus Class 1 debug support
  - eTPU2 enhancements
    - Counters and channels can run at full system clock speed
    - Software watchdog
    - Real-time performance monitor
    - Instruction set enhancements for smaller more flexible code generation
    - Programmable channel mode for customization of channel operation
- Enhanced queued A/D converter (eQADC)
  - Two independent on-chip RSD Cyclic ADCs
    - 8-, 10-, and 12-bit resolution
    - Differential conversions
    - Targets up to 10-bit accuracy at 500 KSample/s (ADC_CLK = 7.5 MHz) and 8-bit accuracy at 1 MSample/s (ADC_CLK = 15 MHz) for differential conversions
    - Differential channels include variable gain amplifier for improved dynamic range (×1; ×2; ×4)
    - Differential channels include programmable pull-up and pull-down resistors for biasing and sensor diagnostics (200 kΩ; 100 kΩ; low value of 5 kΩ)
    - Single-ended signal range from 0 to 5 V
    - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles
    - Provides time stamp information when requested
    - Parallel interface to eQADC command FIFOs (CFIFOs) and result FIFOs (RFIFOs)
    - Supports both right-justified unsigned and signed formats for conversion results

- Temperature sensor to enable measurement of die temperature
- Ability to measure all power supply pins directly

— Automatic application of ADC calibration constants
- Provision of reference voltages (25% VREF and 75% VREF) for ADC calibration purposes

— Up to 34[1] input channels available to the two on-chip ADCs
— Four pairs of differential analog input channels
— Full duplex synchronous serial interface to an external device
- Has a free-running clock for use by the external device
- Supports a 26-bit message length
- Transmits a null message when there are no triggered CFIFOs with commands bound for external CBuffers, or when there are triggered CFIFOs with commands bound for external CBuffers but the external CBuffers are full

— Parallel Side Interface to communicate with an on-chip companion module
— Zero jitter triggering for queue 0. (Queue 0 trigger causes current conversion to be aborted and the queued conversions in the CBUFFER to be bypassed. Delay from Trigger to start of conversion is 13 system clocks + 1 ADC clock.)
— eQADC Result Streaming. Generation of a continuous stream of ADC conversion results from a single eQADC command word. Controlled by two different trigger signals; one to define the rate at which results are generated and the other to define the beginning and ending of the stream. Used to digitize waveforms during specific time/angle windows, e.g., engine knock sensor sampling.
— Angular Decimation. The ability of the eQADC to sample an analog waveform in the time domain, perform FIR/IIR filtering also in the time domain, but to down sample the results in the angle domain. Resulting in a time domain filtered result at a given engine angle.
— Priority Based CFIFOs
- Supports six CFIFOs with fixed priority. The lower the CFIFO number, the higher its priority. When commands of distinct CFIFOs are bound for the same CBuffer, the higher priority CFIFO is always served first.
- Supports software and several hardware trigger modes to arm a particular CFIFO
- Generates interrupt when command coherency is not achieved

— External Hardware Triggers
- Supports rising edge, falling edge, high level and low level triggers
- Supports configurable digital filter

— Supports four external 8-to-1 muxes which can expand the input channel number from 34[2] to 59

- Two deserial serial peripheral interface modules (DSPI)

— SPI
- Full duplex communication ports with interrupt and DMA request support
- Supports all functional modes from QSPI subblock of QSMCM (MPC5xx family)
- Support for queues in RAM
- 6 chip selects, expandable to 64 with external demultiplexers
- Programmable frame size, baud rate, clock delay and clock phase on a per frame basis
- Modified SPI mode for interfacing to peripherals with longer setup time requirements
- LVDS option for output clock and data to allow higher speed communication

— Deserial serial interface (DSI)
- Pin reduction by hardware serialization and deserialization of eTPU, eMIOS channels and GPIO
- 32 bits per DSPI module

1. 176-pin and 208-pin packages have 34 input channels; 144-pin package has 32.
2. 176-pin and 208-ball packages.

- Triggered transfer control and change in data transfer control (for reduced EMI)
- Compatible with Microsecond Bus Version 1.0 downlink

- Two enhanced serial communication interface (eSCI) modules
  - UART mode provides NRZ format and half or full duplex interface
  - eSCI bit rate up to 1 Mbps
  - Advanced error detection, and optional parity generation and detection
  - Word length programmable as 8, 9, 12 or 13 bits
  - Separately enabled transmitter and receiver
  - LIN support
  - DMA support
  - Interrupt request support
  - Programmable clock source: system clock or oscillator clock
  - Support Microsecond Bus (Timed Serial Bus - TSB) uplink Version 1.0
- Two FlexCAN
  - One with 32 message buffers; the second with 64 message buffers
  - Full implementation of the CAN protocol specification, Version 2.0B
  - Based on and including all existing features of the Freescale TouCAN module
  - Programmable acceptance filters
  - Short latency time for high priority transmit messages
  - Arbitration scheme according to message ID or message buffer number
  - Listen only mode capabilities
  - Programmable clock source: system clock or oscillator clock
  - Message buffers may be configured as mailboxes or as FIFO
- Nexus port controller (NPC)
  - Per IEEE-ISTO 5001-2003
  - Real time development support for Power Architecture core and eTPU engine through Nexus class 2/1
  - Read and write access (Nexus class 3 feature that is supported on this device)
    - Run-time access of entire memory map
    - Calibration
  - Support for data value breakpoints / watchpoints
    - Run-time access of entire memory map
    - Calibration
      Table constants calibrated using MMU and internal and external RAM
      Scalar constants calibrated using cache line locking
  - Configured via the IEEE 1149.1 (JTAG) port
- IEEE 1149.1 JTAG controller (JTAGC)
  - IEEE 1149.1-2001 Test Access Port (TAP) interface
  - 5-bit instruction register that supports IEEE 1149.1-2001 defined instructions
  - 5-bit instruction register that supports additional public instructions
  - Three test data registers: a bypass register, a boundary scan register, and a device identification register
  - Censorship disable register. By writing the 64-bit serial boot password to this register, Censorship may be disabled until the next reset
  - TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- On-chip Voltage Regulator for single 5 V supply operation

— On-chip regulator 5 V to 3.3 V for internal supplies
— On-chip regulator controller 5 V to 1.2 V (with external bypass transistor) for core logic

- Low-power modes
  — SLOW Mode. Allows device to be run at very low speed (approximately 1 MHz), with modules (including the PLL) selectively disabled in software
  — STOP Mode. System clock stopped to all modules including the CPU. Wake-up timer used to restart the system clock after a predetermined time

2.3 MPC5634M feature details

2.3.1 e200z335 core

The e200z335 processor utilizes a four stage pipeline for instruction execution. The Instruction Fetch (stage 1), Instruction Decode/Register file Read/Effective Address Calculation (stage 2), Execute/Memory Access (stage 3), and Register Writeback (stage 4) stages operate in an overlapped fashion, allowing single clock instruction execution for most instructions.

The integer execution unit consists of a 32-bit Arithmetic Unit (AU), a Logic Unit (LU), a 32-bit Barrel shifter (Shifter), a Mask-Insertion Unit (MIU), a Condition Register manipulation Unit (CRU), a Count-Leading-Zeros unit (CLZ), a 32×32 Hardware Multiplier array, result feed-forward hardware, and support hardware for division.

Most arithmetic and logical operations are executed in a single cycle with the exception of the divide instructions. A Count-Leading-Zeros unit operates in a single clock cycle. The Instruction Unit contains a PC incrementer and a dedicated Branch Address adder to minimize delays during change of flow operations. Sequential prefetching is performed to ensure a supply of instructions into the execution pipeline. Branch target prefetching is performed to accelerate taken branches. Prefetched instructions are placed into an instruction buffer capable of holding six instructions.

Branches can also be decoded at the instruction buffer and branch target addresses calculated prior to the branch reaching the instruction decode stage, allowing the branch target to be prefetched early. When a branch is detected at the instruction buffer, a prediction may be made on whether the branch is taken or not. If the branch is predicted to be taken, a target fetch is initiated and its target instructions are placed in the instruction buffer following the branch instruction. Many branches take zero cycle to execute by using branch folding. Branches are folded out from the instruction execution pipe whenever possible. These include unconditional branches and conditional branches with condition codes that can be resolved early.

Conditional branches which are not taken and not folded execute in a single clock. Branches with successful target prefetching which are not folded have an effective execution time of one clock. All other taken branches have an execution time of two clocks. Memory load and store operations are provided for byte, halfword, and word (32-bit) data with automatic zero or sign extension of byte and halfword load data as well as optional byte reversal of data. These instructions can be pipelined to allow effective single cycle throughput. Load and store multiple word instructions allow low overhead context save and restore operations. The load/store unit contains a dedicated effective address adder to allow effective address generation to be optimized. Also, a load-to-use dependency does not incur any pipeline bubbles for most cases.

The Condition Register unit supports the condition register (CR) and condition register operations defined by the Power Architecture. The condition register consists of eight 4-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching. Vectored and autovectored interrupts are supported by the CPU. Vectored interrupt support is provided to allow multiple interrupt sources to have unique interrupt handlers invoked with no software overhead.

The hardware floating-point unit utilizes the IEEE-754 single-precision floating-point format and supports single-precision floating-point operations in a pipelined fashion. The general purpose register file is used for source and destination operands, thus there is a unified storage model for single-precision floating-point data types of 32 bits and the normal integer type. Single-cycle floating-point add, subtract, multiply, compare, and conversion operations are provided. Divide instructions are multi-cycle and are not pipelined.

The Signal Processing Extension (SPE) Auxiliary Processing Unit (APU) provides hardware SIMD operations and supports a full complement of dual integer arithmetic operation including Multiply Accumulate (MAC) and dual integer multiply (MUL)

in a pipelined fashion. The general purpose register file is enhanced such that all 32 of the GPRs are extended to 64 bits wide and are used for source and destination operands, thus there is a unified storage model for 32×32 MAC operations which generate greater than 32-bit results.

The majority of both scalar and vector operations (including MAC and MUL) are executed in a single clock cycle. Both scalar and vector divides take multiple clocks. The SPE APU also provides extended load and store operations to support the transfer of data to and from the extended 64-bit GPRs. This SPE APU is fully binary compatible with e200z6 SPE APU used in MPC5554 and MPC5553.

The CPU includes support for Variable Length Encoding (VLE) instruction enhancements. This enables the classic Power Architecture instruction set to be represented by a modified instruction set made up from a mixture of 16- and 32-bit instructions. This results in a significantly smaller code size footprint without noticeably affecting performance. The classic Power Architecture instruction set and VLE instruction set are available concurrently. Regions of the memory map are designated as PPC or VLE using an additional configuration bit in each of Table Look-aside Buffers (TLB) entries in the MMU.

The CPU core is enhanced by the addition of two additional interrupt sources; Non-Maskable Interrupt and Critical Interrupt. These two sources are routed directly from package pins, via edge detection logic in the SIU to the CPU, bypassing completely the Interrupt Controller. Once the edge detection logic is programmed, it cannot be disabled, except by reset. The non-maskable Interrupt is, as the name suggests, completely un-maskable and when asserted will always result in the immediate execution of the respective interrupt service routine. The non-maskable interrupt is not guaranteed to be recoverable. The Critical Interrupt is very similar to the non-maskable interrupt, but it can be masked by other exceptional interrupts in the CPU and is guaranteed to be recoverable (code execution may be resumed from where it stopped).

The CPU core has an additional ‘Wait for Interrupt’ instruction that is used in conjunction with low power STOP mode. When Low Power Stop mode is selected, this instruction is executed to allow the system clock to be stopped. An external interrupt source or the system wake-up timer is used to restart the system clock and allow the CPU to service the interrupt.

2.3.2 Crossbar

The XBAR multi-port crossbar switch supports simultaneous connections between three master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows three concurrent transactions to occur from the master ports to any slave port; but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- 3 master ports:
  - e200z335 core complex Instruction port
  - e200z335 core complex Load/Store port
  - eDMA
- 4 slave ports
  - FLASH
  - calibration bus
  - SRAM
  - Peripheral bridge A/B (eTPU2, eMIOS, SIU, DSPI, eSCI, FlexCAN, eQADC, BAM, decimation filter, PIT, STM and SWT)
- 32-bit internal address, 64-bit internal data paths

2.3.3 eDMA

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 32 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size. The eDMA module provides the following features:

- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses, transfer size, plus support for enhanced addressing modes
- Transfer control descriptor organized to support two-deep, nested transfer operations
- An inner data transfer loop defined by a “minor” byte transfer count
- An outer data transfer loop defined by a “major” iteration count
- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests (one per channel)
- Support for fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- 1 interrupt per channel, optionally asserted at completion of major iteration count
- Error termination interrupts are optionally enabled
- Support for scatter/gather DMA processing
- Channel transfers can be suspended by a higher priority channel

2.3.4 Interrupt controller

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC allows interrupt request servicing from up to 191 peripheral interrupt request sources, plus 165 sources reserved for compatibility with other family members).

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

Multiple processors can assert interrupt requests to each other through software settable interrupt requests. These same software settable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion. The high priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software settable interrupt request to finish the servicing in a lower priority ISR. Therefore these software settable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS.

The INTC provides the following features:

- 356 peripheral interrupt request sources
- 8 software settable interrupt request sources
- 9-bit vector addresses
- Unique vector for each interrupt request source
- Hardware connection to processor or read from register

- Each interrupt source can be programmed to one of 16 priorities
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts executing ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority to implement the priority ceiling protocol for accessing shared resources
- Low latency—three clocks from receipt of interrupt request from peripheral to interrupt request to processor

This device also includes a non-maskable interrupt (NMI) pin that bypasses the INTC and multiplexing logic.

2.3.5 FMPLL

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 20 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency from 4 MHz to 20 MHz
- Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz, resulting in system clock frequencies from 16 MHz to 80 MHz with granularity of 4 MHz or better
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- 3 modes of operation
  - Bypass mode with PLL off
  - Bypass mode with PLL running (default mode out of reset)
  - PLL normal mode
- Each of the three modes may be run with a crystal oscillator or an external clock reference
- Programmable frequency modulation
  - Modulation enabled/disabled through software
  - Triangle wave modulation up to 100 kHz modulation frequency
  - Programmable modulation depth (0% to 2% modulation depth)
  - Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock Quality Module
  - detects the quality of the crystal clock and cause interrupt request or system reset if error is detected
  - detects the quality of the PLL output clock. If an error is detected, causes a system reset or switches the system clock to the crystal clock and causes an interrupt request
- Programmable interrupt request or system reset on loss of lock

2.3.6 Calibration EBI

The Calibration EBI controls data transfer across the crossbar switch to/from memories or peripherals attached to the VertiCal connector in the calibration address space. The Calibration EBI is only available in the VertiCal Calibration System. The Calibration EBI includes a memory controller that generates interface signals to support a variety of external memories. The Calibration EBI memory controller supports legacy flash, SRAM, and asynchronous memories. In addition, the calibration EBI supports up to three regions via chip selects (two chip selects are multiplexed with two address bits), along with programmed region-specific attributes. The calibration EBI supports the following features:

- 22-bit address bus (two most significant signals multiplexed with two chip selects)
- 16-bit data bus
- Multiplexed mode with addresses and data signals present on the data lines

NOTE

The calibration EBI must be configured in multiplexed mode when the extended Nexus trace is used on the VertiCal Calibration System. This is because Nexus signals and address lines of the calibration bus share the same balls in the calibration package.

- Memory controller with support for various memory types:
  - Asynchronous/legacy flash and SRAM
  - Most standard memories used with the MPC5xx or MPC55xx family
- Bus monitor
  - User selectable
  - Programmable time-out period (with 8 external bus clock resolution)
- Configurable wait states (via chip selects)
- 3 chip-select (Cal_$\overline{CS}$[0], Cal_$\overline{CS}$[2:3]) signals (Multiplexed with 2 most significant address signals)
- 2 write/byte enable (WE[0:1]/BE[0:1]) signals
- Configurable bus speed modes
  - system frequency
  - 1/2 of system frequency
  - 1/4 of system frequency
- Optional automatic CLKOUT gating to save power and reduce EMI
- Compatible with MPC5xx external bus (with some limitations)
- Selectable drive strengths; 10 pF, 20 pF, 30 pF, 50 pF

2.3.7 SIU

The MPC5634M SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the $\overline{RSTOUT}$ pin. Communication between the SIU and the e200z335 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control for each pad
  - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software
  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - 11 interrupt requests
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical Interrupt request
  - Non-Maskable Interrupt request
- GPIO
  - GPIO function on 80 I/O pins

- Virtual GPIO on 64 I/O pins via DSPI serialization (requires external deserialization device)
- Dedicated input and output registers for setting each GPIO and Virtual GPIO pin

- Internal multiplexing
  - Allows serial and parallel chaining of DSPIs
  - Allows flexible selection of eQADC trigger inputs
  - Allows selection of interrupt requests between external pins and DSPI

2.3.8 ECSM

The error correction status module provides status information regarding platform memory errors reported by error-correcting codes.

2.3.9 Flash

Devices in the MPC5634M family provide up to 1.5 MB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash module includes a Fetch Accelerator, that optimizes the performance of the flash array to match the CPU architecture and provides single cycle random access to the flash @ 80 MHz. The flash module interfaces the system bus to a dedicated flash memory array controller. For CPU 'loads', DMA transfers and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains a four-entry, 128-bit prefetch buffer and a prefetch controller which prefetches sequential lines of data from the flash array into the buffer. Prefetch buffer hits allow no-wait responses. Normal flash array accesses are registered and are forwarded to the system bus on the following cycle, incurring three wait-states. Prefetch operations may be automatically controlled, and are restricted to instruction fetch.

The flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch Accelerator
  - Architected to optimize the performance of the flash with the CPU to provide single cycle random access to the flash up to 80 MHz system clock speed
  - Configurable read buffering and line prefetch support
  - Four line read buffers (128 bits wide) and a prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis
- Interface to the flash array controller is pipelined with a depth of one, allowing overlapped accesses to proceed in parallel for interleaved or pipelined flash array designs
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0-31 additional cycles) allowing use for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (four words)
- ECC with single-bit correction, double-bit detection
- Program page size of 128 bits (four words) to accelerate programming
- ECC single-bit error corrections are visible to software
- Minimum program size is two consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Shadow information stored in non-volatile shadow block

- Independent program/erase of the shadow block

2.3.10 SRAM

The MPC5634M SRAM module provides a general-purpose up to 94 KB memory block. The SRAM controller includes these features:

- Supports read/write accesses mapped to the SRAM memory from any master
- 32 KB or 24 KB block powered by separate supply for standby operation
- Byte, halfword, word and doubleword addressable
- ECC performs single-bit correction, double-bit detection on 32-bit data element

2.3.11 BAM

The BAM (Boot Assist Module) is a block of read-only memory that is programmed once by Freescale and is identical for all MPC5634M MCUs. The BAM program is executed every time the MCU is powered-on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (A program is downloaded into RAM via eSCI or the FlexCAN and then executed)
- Booting from external memory on calibration bus

The BAM also reads the reset configuration half word (RCHW) from internal flash memory and configures the MPC5634M hardware accordingly. The BAM provides the following features:

- Sets up MMU to cover all resources and mapping all physical address to logical addresses with minimum address translation
- Sets up the MMU to allow user boot code to execute as either Power Architecture code (default) or as Freescale VLE code
- Detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid
- Supports user programmable 64-bit password protection for serial boot mode
- Supports serial bootloading via FlexCAN bus and eSCI using Freescale protocol
- Supports serial bootloading via FlexCAN bus and eSCI with auto baud rate sensing
- Supports serial bootloading of either Power Architecture code (default) or Freescale VLE code
- Supports booting from calibration bus interface
- Supports censorship protection for internal flash memory
- Provides an option to enable the core watchdog timer
- Provides an option to disable the system watchdog timer

2.3.12 eMIOS

The eMIOS (Enhanced Modular Input Output System) module provides the functionality to generate or measure time events. The channels on this module provide a range of operating modes including the capability to perform dual input capture or dual output compare as well as PWM output.

The eMIOS provides the following features:

- 16 channels (24-bit timer resolution)
- For compatibility with other family members selected channels and timebases are implemented:
  - Channels 0 to 6, 8 to 15, and 23
  - Timebases A, B and C

- Channels 1, 3, 5 and 6 support modes:
  - General Purpose Input/Output (GPIO)
  - Single Action Input Capture (SAIC)
  - Single Action Output Compare (SAOC)
- Channels 2, 4, 11 and 13 support all the modes above plus:
  - Output Pulse Width Modulation Buffered (OPWMB)
- Channels 0, 8, 9, 10, 12, 14, 15, 23 support all the modes above plus:
  - Input Period Measurement (IPM)
  - Input Pulse Width Measurement (IPWM)
  - Double Action Output Compare (set flag on both matches) (DAOC)
  - Modulus Counter Buffered (MCB)
  - Output Pulse Width and Frequency Modulation Buffered (OPWFMB)
- Three 24-bit wide counter buses
  - Counter bus A can be driven by channel 23 or by the eTPU2 and all channels can use it as a reference
  - Counter bus B is driven by channel 0 and channels 0 to 6 can use it as a reference
  - Counter bus C is driven by channel 8 and channels 8 to 15 can use it as a reference
- Shared time bases with the eTPU through the counter buses
- Synchronization among internal and external time bases

2.3.13 eTPU2

The eTPU2 is an enhanced co-processor designed for timing control. Operating in parallel with the host CPU, eTPU2 processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. A powerful timer subsystem is formed by combining the eTPU2 with its own instruction and data RAM. High-level assembler/compiler and documentation allows customers to develop their own functions on the eTPU2.

The eTPU2 includes these distinctive features:

- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.
- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.

- 32 channels, each channel is associated with one input and one output signal
  - Enhanced input digital filters on the input pins for improved noise immunity.
  - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality.
  - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators
  - Input and output signal states visible from the host
- 2 independent 24-bit time bases for channel synchronization:
  - First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler
  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host
- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
  - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
  - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
  - Automatic channel context switch when a “task switch” occurs, i.e., one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel
  - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
  - Dual-parameter coherency hardware support allows atomic access to two parameters by host
- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test (MISC — multiple input signature calculator), runs concurrently with eTPU2 normal operation

For MPC5634M, the eTPU2 has been further enhanced with these features:

- System enhancements
  - Timebases and channels are run at full system clock speed
  - Software watchdog with programmable timeout
  - Real-time performance information
- Channel enhancements

— Programmable channel mode allows customization of channel function
— Channels 1 and 2 can optionally drive angle clock hardware

- Programming enhancements
  — Engine relative addressing mode
  — More flexibility in requesting DMA and interrupt service
  — Channel flags can be tested

2.3.14 eQADC

The enhanced queued analog to digital converter (eQADC) block provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog to digital converters (ADC), and a single master to single slave serial interface to an off-chip external device. Both on-chip ADCs have access to all the analog channels.

The eQADC prioritizes and transfers commands from six command conversion command 'queues' to the on-chip ADCs or to the external device. The block can also receive data from the on-chip ADCs or from an off-chip external device into the six result queues, in parallel, independently of the command queues. The six command queues are prioritized with Queue_0 having the highest priority and Queue_5 the lowest. Queue_0 also has the added ability to bypass all buffering and queuing and abort a currently running conversion on either ADC and start a Queue_0 conversion. This means that Queue_0 will always have a deterministic time from trigger to start of conversion, irrespective of what tasks the ADCs were performing when the trigger occurred. The eQADC supports software and external hardware triggers from other blocks to initiate transfers of commands from the queues to the on-chip ADCs or to the external device. It also monitors the fullness of command queues and result queues, and accordingly generates DMA or interrupt requests to control data movement between the queues and the system memory, which is external to the eQADC.

The ADCs also support features designed to allow the direct connection of high impedance acoustic sensors that might be used in a system for detecting engine knock. These features include differential inputs; integrated variable gain amplifiers for increasing the dynamic range; programmable pull-up and pull-down resistors for biasing and sensor diagnostics.

The eQADC also integrates a programmable decimation filter capable of taking in ADC conversion results at a high rate, passing them through a hardware low pass filter, then down-sampling the output of the filter and feeding the lower sample rate results to the result FIFOs. This allows the ADCs to sample the sensor at a rate high enough to avoid aliasing of out-of-band noise; while providing a reduced sample rate output to minimize the amount DSP processing bandwidth required to fully process the digitized waveform.

The eQADC provides the following features:

- Dual on-chip ADCs
  — 2 × 12-bit ADC resolution
  — Programmable resolution for increased conversion speed (12 bit, 10 bit, 8 bit)
    – 12-bit conversion time – 1 μs (1M sample/sec)
    – 10-bit conversion time – 867 ns (1.2M sample/second)
    – 8-bit conversion time – 733 ns (1.4M sample/second)
  — Up to 10-bit accuracy at 500 KSample/s and 9-bit accuracy at 1 MSample/s
  — Differential conversions
  — Single-ended signal range from 0 to 5 V
  — Variable gain amplifiers on differential inputs (×1, ×2, ×4)
  — Sample times of 2 (default), 8, 64 or 128 ADC clock cycles
  — Provides time stamp information when requested
  — Parallel interface to eQADC CFIFOs and RFIFOs
  — Supports both right-justified unsigned and signed formats for conversion results
- Up to 34[1] input channels (accessible by both ADCs)

1. 176-pin and 208-pin packages have 34 input channels; 144-pin package has 32; 100-pin package has 23.

- 23 additional internal channels for measuring control and monitoring voltages inside the device
  - Including Core voltage, I/O voltage, LVI voltages, etc.
- An internal bandgap reference to allow absolute voltage measurements
- 4 pairs of differential analog input channels
  - Programmable pull-up/pull-down resistors on each differential input for biasing and sensor diagnostic (200 kΩ, 100 kΩ, 5 kΩ)
- Silicon die temperature sensor
  - provides temperature of silicon as an analog value
  - read using an internal ADC analog channel
  - may be read with either ADC
- Decimation Filter
  - Programmable decimation factor (2 to 16)
  - Selectable IIR or FIR filter
  - Up to 4th order IIR or 8th order FIR
  - Programmable coefficients
  - Saturated or non-saturated modes
  - Programmable Rounding (Convergent; Two's Complement; Truncated)
  - Pre-fill mode to pre-condition the filter before the sample window opens
- Full duplex synchronous serial interface to an external device
  - Free-running clock for use by an external device
  - Supports a 26-bit message length
- Priority based Queues
  - Supports six Queues with fixed priority. When commands of distinct Queues are bound for the same ADC, the higher priority Queue is always served first
  - Queue_0 can bypass all prioritization, buffering and abort current conversions to start a Queue_0 conversion a deterministic time after the queue trigger
  - Supports software and hardware trigger modes to arm a particular Queue
  - Generates interrupt when command coherency is not achieved
- External hardware triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter
- Supports four external 8-to-1 muxes which can expand the input channels to 56 channels total

2.3.15 DSPI

The deserial serial peripheral interface (DSPI) block provides a synchronous serial interface for communication between the MPC5634M MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU and eMIOS channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. This SPI-like protocol is completely configurable for baud rate, polarity and phase, frame length, chip select assertion, etc. Each bit in the frame may be configured to serialize either eTPU channels, eMIOS channels or GPIO signals. The DSPI can be configured to serialize data to an external device that implements the Microsecond Bus protocol. There are two identical DSPI blocks on the MPC5634M MCU. The DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) to improve high speed operation.

The DSPIs have three configurations:

- Serial peripheral interface (SPI) configuration where the DSPI operates as an up to 16-bit SPI with support for queues
- Enhanced deserial serial interface (DSI) configuration where DSPI serializes up to 32 bits with three possible sources per bit

- eTPU, eMIOS, new virtual GPIO registers as possible bit source
- Programmable inter-frame gap in continuous mode
- Bit source selection allows microsecond bus downlink with command or data frames up to 32 bits
- Microsecond bus dual receiver mode

- Combined serial interface (CSI) configuration where the DSPI operates in both SPI and DSI configurations interleaving DSI frames with SPI frames, giving priority to SPI frames

For queued operations, the SPI queues reside in system memory external to the DSPI. Data transfers between the memory and the DSPI FIFOs are accomplished through the use of the eDMA controller or through host software.

The DSPI supports these SPI features:

- Full-duplex, synchronous transfers
- Selectable LVDS Pads working at 40 MHz for SOUT, SIN and SCK pins
- Master and Slave Mode
- Buffered transmit operation using the TX FIFO with parameterized depth of 1 to 16 entries
- Buffered receive operation using the RX FIFO with parameterized depth of 1 to 16 entries
- TX and RX FIFOs can be disabled individually for low-latency updates to SPI queues
- Visibility into the TX and RX FIFOs for ease of debugging
- FIFO Bypass Mode for low-latency updates to SPI queues
- Programmable transfer attributes on a per-frame basis:
  - Parameterized number of transfer attribute registers (from two to eight)
  - Serial clock with programmable polarity and phase
  - Various programmable delays:
    - PCS to SCK delay
    - SCK to PCS delay
    - Delay between frames
  - Programmable serial frame size of 4 to 16 bits, expandable with software control
  - Continuously held chip select capability
- 6 Peripheral Chip Selects, expandable to 64 with external demultiplexer
- Deglitching support for up to 32 Peripheral Chip Selects with external demultiplexer
- DMA support for adding entries to TX FIFO and removing entries from RX FIFO:
  - TX FIFO is not full (TFFF)
  - RX FIFO is not empty (RFDF)
- 6 Interrupt conditions:
  - End of queue reached (EOQF)
  - TX FIFO is not full (TFFF)
  - Transfer of current frame complete (TCF)
  - Attempt to transmit with an empty Transmit FIFO (TFUF)
  - RX FIFO is not empty (RFDF)
  - FIFO Underrun (slave only and SPI mode, the slave is asked to transfer data when the TxFIFO is empty)
  - FIFO Overrun (serial frame received while RX FIFO is full)
- Modified transfer formats for communication with slower peripheral devices
- Continuous Serial Communications Clock (SCK)
- Power savings via support for Stop Mode
- Enhanced DSI logic to implement a 32-bit Timed Serial Bus (TSB) configuration, supporting the Microsecond Bus downstream frame format

The DSPIs also support these features unique to the DSI and CSI configurations:

- 2 sources of the serialized data:
  - eTPU_A and eMIOS output channels
  - Memory-mapped register in the DSPI
- Destinations for the deserialized data:
  - eTPU_A and eMIOS input channels
  - SIU External Interrupt Request inputs
  - Memory-mapped register in the DSPI
- Deserialized data is provided as Parallel Output signals and as bits in a memory-mapped register
- Transfer initiation conditions:
  - Continuous
  - Edge sensitive hardware trigger
  - Change in data
- Pin serialization/deserialization with interleaved SPI frames for control and diagnostics
- Continuous serial communications clock
- Support for parallel and serial chaining of up to four DSPI blocks

2.3.16 eSCI

The enhanced serial communications interface (eSCI) allows asynchronous serial communications with peripheral devices and other MCUs. It includes special support to interface to Local Interconnect Network (LIN) slave devices. The eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit, data format
- Programmable 12-bit or 13-bit data format for Timed Serial Bus (TSB) configuration to support the Microsecond bus standard
- Automatic parity generation
- LIN support
  - Autonomous transmission of entire frames
  - Configurable to support all revisions of the LIN standard
  - Automatic parity bit generation
  - Double stop bit after bit error
  - 10- or 13-bit break support
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- 2 receiver wake up methods:
  - Idle line wake-up
  - Address mark wake-up
- Interrupt-driven operation with flags
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- DMA support for both transmit and receive data
  - Global error bit stored with receive data in system RAM to allow post processing of errors

2.3.17 FlexCAN

The MPC5634M MCU contains two controller area network (FlexCAN) blocks. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. FlexCAN module 'A' contains 64 message buffers (MB); FlexCAN module 'C' contains 32 message buffers.

The FlexCAN module provides the following features:

- Based on and including all existing features of the Freescale TouCAN module
- Full Implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - Zero to eight bytes data length
  - Programmable bit rate up to 1 Mbit/s
- Content-related addressing
- 64 / 32 message buffers of zero to eight bytes data length
- Individual Rx Mask Register per message buffer
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Includes 1056 / 544 bytes of embedded memory for message buffer storage
- Includes a 256-byte and a 128-byte memories for storing individual Rx mask registers
- Full featured Rx FIFO with storage capacity for six frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous FlexCAN versions
- Programmable clock source to the CAN Protocol Interface, either system clock or oscillator clock
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- 3 programmable Mask Registers
- Programmable transmit-first scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Warning interrupts when the Rx and Tx Error Counters reach 96
- Independent of the transmission medium (an external transceiver is assumed)
- Multi master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wake-up on bus activity

2.3.18 System timers

The system timers provide two distinct types of system timer:

- Periodic interrupts/triggers using the Peripheral Interrupt Timer (PIT)
- Operating system task monitors using the System Timer Module (STM)

2.3.18.1 Peripheral Interrupt Timer (PIT)

The PIT provides five independent timer channels, capable of producing periodic interrupts and periodic triggers. The PIT has no external input or output pins and is intended to be used to provide system ‘tick’ signals to the operating system, as well as periodic triggers for eQADC queues. Of the five channels in the PIT, four are clocked by the system clock, one is clocked by the crystal clock. This one channel is also referred to as Real Time Interrupt (RTI) and is used to wakeup the device from low power stop mode.

The following features are implemented in the PIT:

- 5 independent timer channels
- Each channel includes 32-bit wide down counter with automatic reload
- 4 channels clocked from system clock
- 1 channel clocked from crystal clock (wake-up timer)
- Wake-up timer remains active when System STOP mode is entered. Used to restart system clock after predefined time-out period
- Each channel can optionally generate an interrupt request or a trigger event (to trigger eQADC queues) when the timer reaches zero

2.3.18.2 System Timer Module (STM)

The System Timer Module (STM) is designed to implement the software task monitor as defined by AUTOSAR (see http://www.autosar.org). It consists of a single 32-bit counter, clocked by the system clock, and four independent timer comparators. These comparators produce a CPU interrupt when the timer exceeds the programmed value.

The following features are implemented in the STM:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

2.3.19 Software Watchdog Timer (SWT)

The Software Watchdog Timer (SWT) is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. The SWT is a 32-bit modulus counter, clocked by the system clock or the crystal clock, that can provide a system reset or interrupt request when the correct software key is not written within the required time window.

The following features are implemented:

- 32-bit modulus counter
- Clocked by system clock or crystal clock
- Optional programmable watchdog window mode
- Can optionally cause system reset or interrupt request on timeout
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Configuration is protected by a software key or a write-once register

2.3.20 Debug features

2.3.20.1 Nexus port controller

The NPC (Nexus Port Controller) block provides real-time development support capabilities for the MPC5634M Power Architecture-based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NPC block is an integration of several individual Nexus blocks that are selected to provide the development support interface for the MPC5634M. The NPC block interfaces to the host processor (e200z335), eTPU, and internal buses to provide development support as per the IEEE-ISTO 5001-2003 standard. The development support provided includes program trace and run-time access to the MCUs internal memory map and access to the Power Architecture and eTPU internal registers during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins. MPC5634M in the production 144 LQFP supports a 3.3 V reduced (4-bit wide) Auxiliary port. These Nexus port pins can also be used as 5 V I/O signals to increase usable I/O count of the device. When using this Nexus port as IO, Nexus trace is still possible using VertiCal calibration. In the VertiCal calibration package, the full 12-bit Auxiliary port is available.

NOTE

In the VertiCal package, the full Nexus Auxiliary port shares balls with the addresses of the calibration bus. Therefore multiplexed address/data bus mode must be used for the calibration bus when using full width Nexus trace in VertiCal assembly.

The following features are implemented:

- 5-pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)
  - Always available in production package
  - Supports both JTAG Boundary Scan and debug modes
  - 3.3 V interface
  - Supports Nexus class 1 features
  - Supports Nexus class 3 read/write feature
- 9-pin Reduced Port interface in 144 LQFP production package
  - Alternate function as IO
  - 5 V (in GPIO or alternate function mode), 3.3 V (in Nexus mode) interface
  - Auxiliary Output port
    - 1 MCKO (message clock out) pin
    - 4 MDO (message data out) pins
    - 2 $\overline{\text{MSEO}}$ (message start/end out) pins
    - 1 $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
    - 1 $\overline{\text{EVTI}}$ (event in) pin
- 17-pin Full Port interface in VertiCal calibration package
  - 3.3 V interface
  - Auxiliary Output port
    - 1 MCKO (message clock out) pin
    - 4 (reduced port mode) or 12 (full port mode) MDO (message data out) pins; 8 extra full port pins shared with calibration bus
    - 2 $\overline{\text{MSEO}}$ (message start/end out) pins
    - 1 $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
    - 1 $\overline{\text{EVTI}}$ (event in) pin

- Host processor (e200) development support features
  - IEEE-ISTO 5001-2003 standard class 2 compliant
  - Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus, static code may be traced.
  - Watchpoint trigger enable of program trace messaging
  - Data Value Breakpoints (JTAG feature of the e200z335 core): allows CPU to be halted when the CPU writes a specific value to a memory location
    - 4 data value breakpoints
    - CPU only
    - Detects ‘equal’ and ‘not equal’
    - Byte, half word, word (naturally aligned)

NOTE

This feature is imprecise due to CPU pipelining.

  - Subset of Power Architecture software debug facilities with OnCE block (Nexus class 1 features)
- eTPU development support features
  - IEEE-ISTO 5001-2003 standard class 1 compliant for the eTPU
  - Nexus based breakpoint configuration and single step support (JTAG feature of the eTPU)
- Run-time access to the on-chip memory map via the Nexus read/write access protocol. This feature supports accesses for run-time internal visibility, calibration variable acquisition, calibration constant tuning, and external rapid prototyping for powertrain automotive development systems.
- All features are independently configurable and controllable via the IEEE 1149.1 I/O port
- Power-on-reset status indication during reset via MDO[0] in disabled and reset modes

2.3.20.2 JTAG

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface 4 pins (TDI, TMS, TCK, and TDO)
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC
  - ACCESS_AUX_TAP_ONCE
  - ACCESS_AUX_TAP_eTPU
  - ACCESS_CENSOR
- 3 test data registers to support JTAG Boundary Scan mode
  - Bypass register
  - Boundary scan register
  - Device identification register
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- Censorship Inhibit Register
  - 64-bit Censorship password register

— If the external tool writes a 64-bit password that matches the Serial Boot password stored in the internal flash shadow row, Censorship is disabled until the next system reset

2.4 MPC5634M series architecture

2.4.1 Block diagram

Figure 1 shows a top-level block diagram of the MPC5634M series.

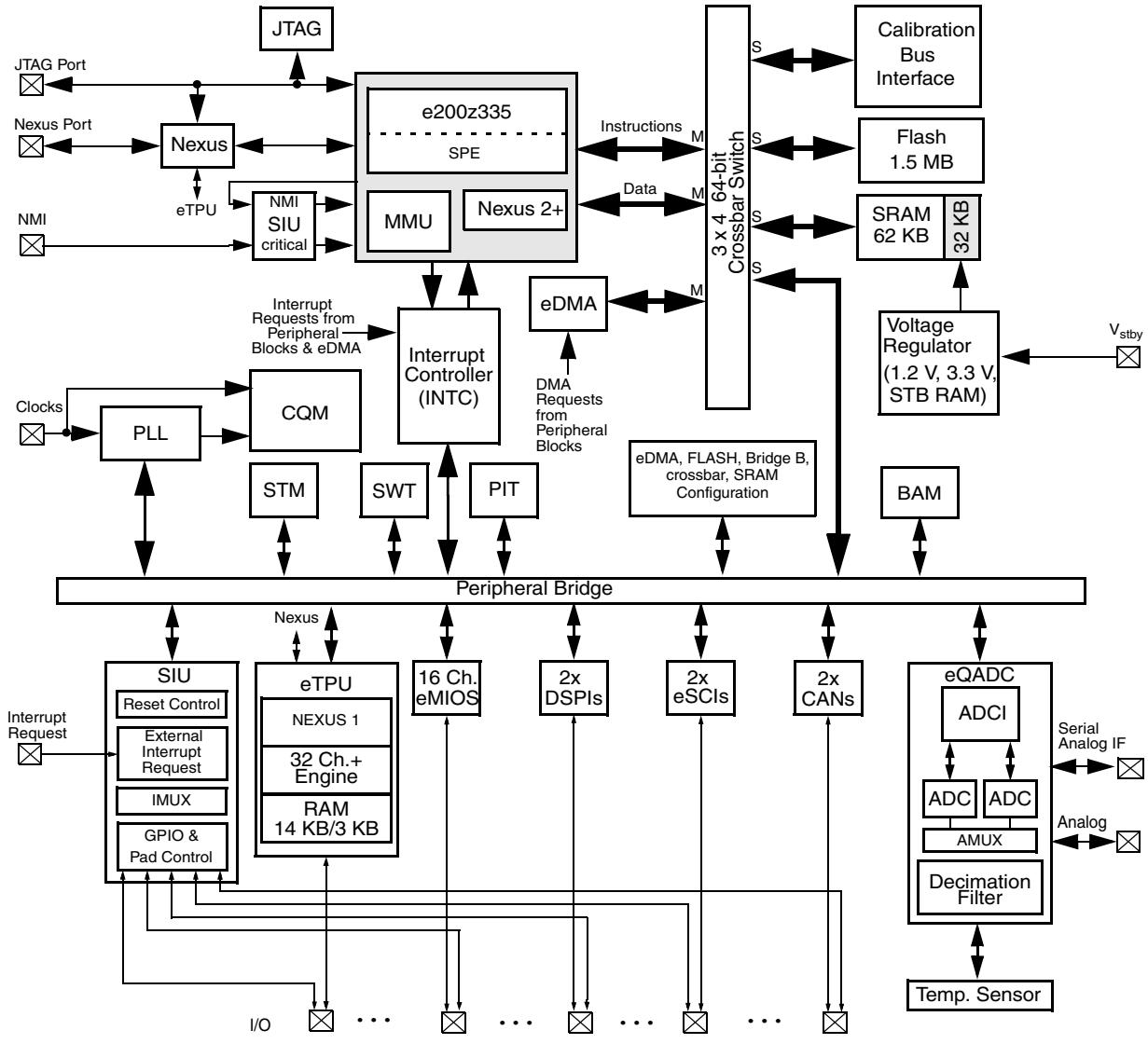


Figure 1. MPC5634M series block diagram

2.4.2 Block summary

Table 2 summarizes the functions of the blocks present on the MPC5634M series microcontrollers.

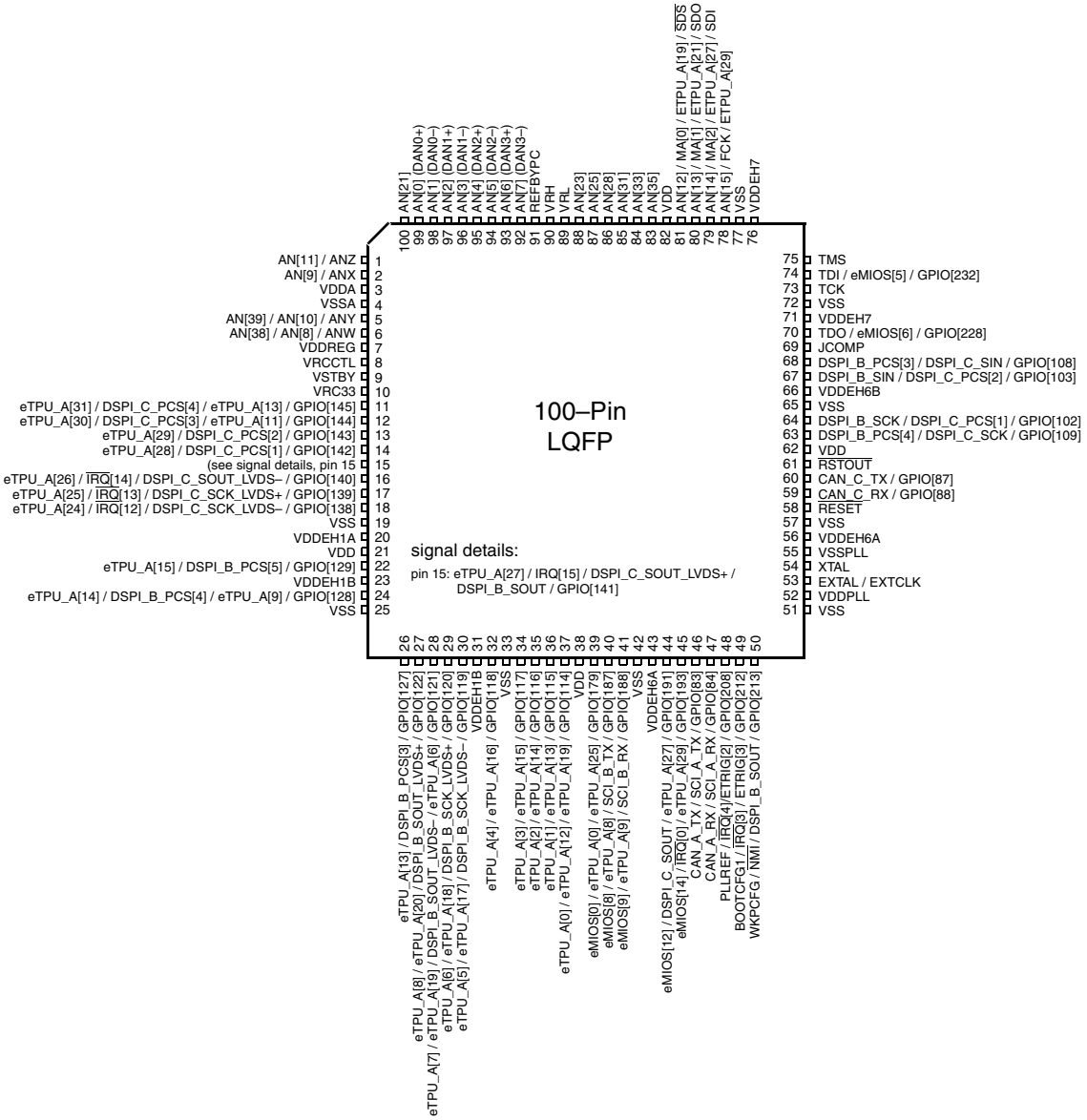
Table 2. MPC5634M series block summary

Block	Function
e200z3 core	Executes programs and interrupt handlers.
Flash memory	Provides storage for program code, constants, and variables
RAM (random-access memory)	Provides storage for program code, constants, and variables
Calibration bus	Transfers data across the crossbar switch to/from peripherals attached to the VertiCal connector
DMA (direct memory access)	Performs complex data movements with minimal intervention from the core
DSPI (deserial serial peripheral interface)	Provides a synchronous serial interface for communication with external devices
eMIOS (enhanced modular input-output system)	Provides the functionality to generate or measure events
eQADC (enhanced queued analog-to-digital converter)	Provides accurate and fast conversions for a wide range of applications
eSCI (serial communication interface)	Allows asynchronous serial communications with peripheral devices and other microcontroller units
eTPU (enhanced time processor unit)	Processes real-time input events, performs output waveform generation, and accesses shared data without host intervention
FlexCAN (controller area network)	Supports the standard CAN communications protocol
FMPLL (frequency-modulated phase-locked loop)	Generates high-speed system clocks and supports the programmable frequency modulation of these clocks
INTC (interrupt controller)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
NPC (Nexus Port Controller)	Provides real-time development support capabilities in compliance with the IEEE-ISTO 5001-2003 standard
PIT (peripheral interrupt timer)	Produces periodic interrupts and triggers
Temperature sensor	Provides the temperature of the device as an analog value
SWT (Software Watchdog Timer)	Provides protection from runaway code
STM (System Timer Module)	Timer providing a set of output compare events to support AutoSAR and operating system tasks

3 Pinout and signal description

This section contains the pinouts for all production packages for the MPC5634M family of devices. Please note the following:

- Pins labeled “NC” are to be left unconnected. Any connection to an external circuit or voltage may cause unpredictable device behavior or damage.
- Pins labeled “NIC” have no internal connection.



3.1 144 LQFP pinout

Figure 2 shows the pinout for the 144-pin LQFP.

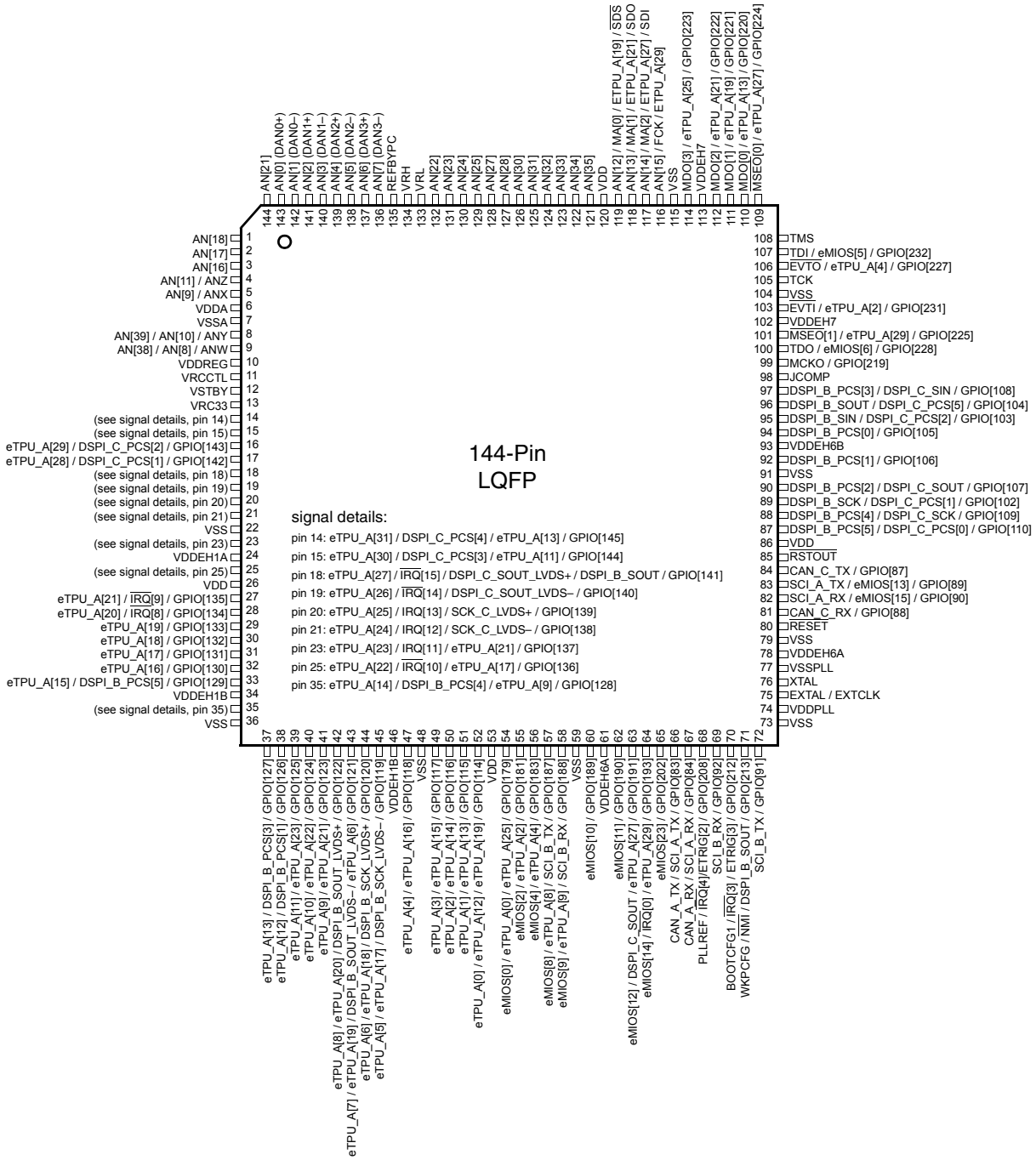
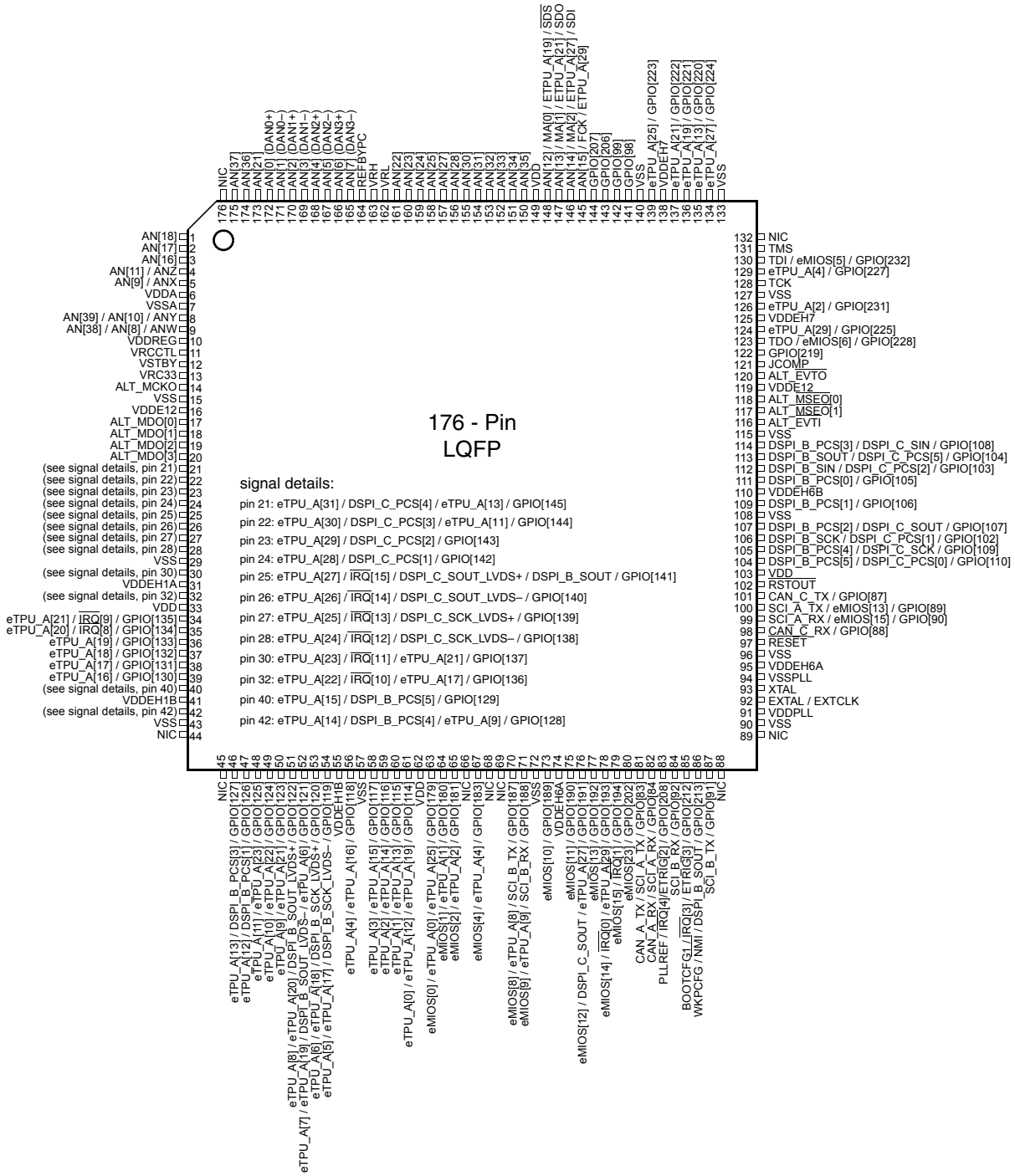


Figure 2. 144-pin LQFP pinout (top view; all 144-pin devices)

3.2 176 LQFP pinout (MPC5634M)

Figure 3 shows the 176-pin LQFP pinout for the MPC5634M (1536 KB flash memory).

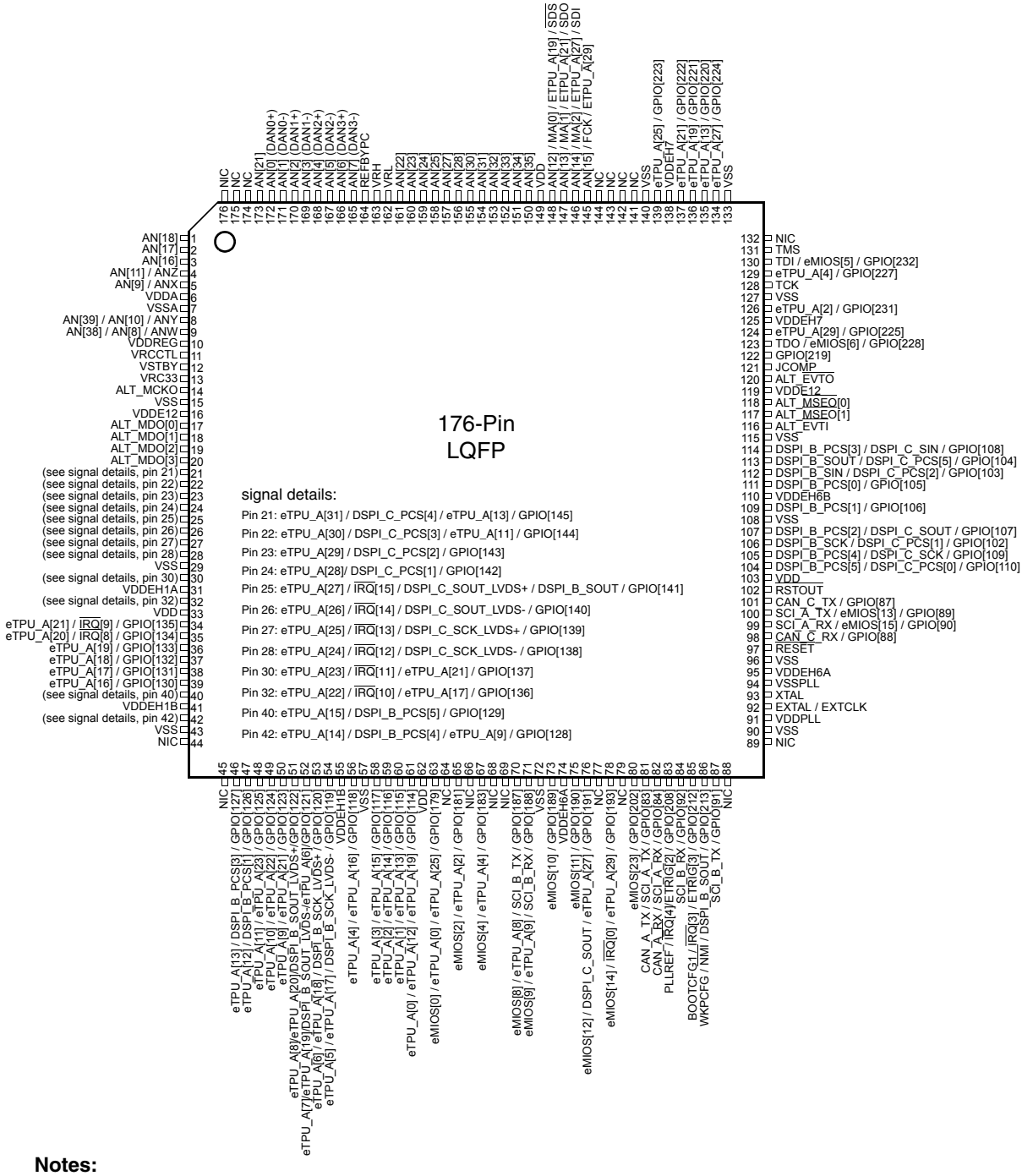


Note: Pins marked “NIC” have no internal connection.

Figure 3. 176-pin LQFP pinout (MPC5634M; top view)

3.3 176 LQFP pinout (MPC5633M)

Figure 4 shows the pinout for the 176-pin LQFP for the MPC5633M (1024 KB flash memory).



Notes:

1. Pins marked “NIC” have no internal connection.
2. Pins marked “NC” are not functional pins but may be connected to internal circuitry. Connections to external circuits or other pins on this device can result in unpredictable system behavior or damage.

Figure 4. 176-pin LQFP pinout (MPC5633M; top view)

3.4 208 MAPBGA ballmap (MPC5634M)

Figure 5 shows the 208-pin MAPBGA ballmap for the MPC5634M (1536 KB flash memory) as viewed from above.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12- $\overline{SDS}$	ALT_ MDO2	ALT_ MDO0	VRC33	VSS
B	VDD	VSS	AN38	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	ALT_ MDO3	ALT_ MDO1	VSS	VDD
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15 FCK	VSS	$\overline{ALT_ MSEO0}$	TCK
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	ALT_$\overline{EVTO}$	NIC[1]
E	ETPUA30	ETPUA31	AN37	VDD									VDDE7	TDI	ALT_$\overline{EVTI}$	$\overline{ALT_ MSEO1}$
F	ETPUA28	ETPUA29	ETPUA26	AN36									VDDEH6	TDO	ALT_MCKO	JCOMP
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_ SOUT	DSPI_B_ PCS3	DSPI_B_ SIN	DSPI_B_ PCS0
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			GPIO99	DSPI_B_ PCS4	DSPI_B_ PCS2	DSPI_B_ PCS1
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_ PCS5	SCI_A_TX	GPIO98	DSPI_B_ SCK
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1			VSS	VSS	VSS	VSS			CAN_C_ TX	SCI_A_RX	$\overline{RSTOUT}$	VDDREG
L	ETPUA12	ETPUA11	ETPUA6	ETPUA0									SCI_B_TX	CAN_C_ RX	WKPCFG	$\overline{RESET}$
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSSPLL
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH1/6[2]	EMIOS12	eTPU_A19[3]	VRC33	VSS	VRCCTL	NIC[1]	EXTAL
P	ETPUA3	ETPUA2	VSS	VDD	GPIO207	VDDE7	NIC[1]	EMIOS8	eTPU_A29[3]	eTPU_A2[3]	eTPU_A21[3]	CAN_A_ TX	VDD	VSS	NIC[1]	XTAL
R	NIC[1]	VSS	VDD	GPIO206	EMIOS4	NIC[1]	EMIOS9	EMIOS11	EMIOS14	eTPU_A27[3]	EMIOS23	CAN_A_ RX	NIC[1]	VDD	VSS	VDDPLL
T	VSS	VDD	NIC[1]	EMIOS0	EMIOS1	GPIO219	eTPU_A25[3]	EMIOS13	EMIOS15	eTPU_A4[3]	eTPU_A13[3]	NIC[1]	VDDE5	CLKOUT	VDD	VSS

1 Pins marked “NIC” have no internal connection.
2 This ball may be changed to “NC” (no connection) in a future revision.
3 eTPU output only channel.

Figure 5. 208-pin MAPBGA ballmap (MPC5634M; top view)

3.5 208 MAPBGA ballmap (MPC5633M only)

Figure 6 shows the 208-pin MAPBGA ballmap for the MPC5633M (1024 KB flash memory) as viewed from above.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12-SDS	ALT_ MDO2	ALT_ MDO0	VRC33	VSS
B	VDD	VSS	AN38	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	ALT_ MDO3	ALT_ MDO1	VSS	VDD
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15 FCK	VSS	ALT_ MSEO0	TCK
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	ALT_ EVTO	NIC[1]
E	ETPUA30	ETPUA31	NC[2]	VDD									VDDE7	TDI	ALT_ EVTI	ALT_ MSEO1
F	ETPUA28	ETPUA29	ETPUA26	NC[2]									VDDEH6	TDO	ALT_MCKO	JCOMP
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_ SOUT	DSPI_B_ PCS3	DSPI_B_ SIN	DSPI_B_ PCS0
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			NC[2]	DSPI_B_ PCS4	DSPI_B_ PCS2	DSPI_B_ PCS1
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_ PCS5	SCI_A_TX	NC[2]	DSPI_B_ SCK
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1			VSS	VSS	VSS	VSS			CAN_C_ TX	SCI_A_RX	RSTOUT	VDDREG
L	ETPUA12	ETPUA11	ETPUA6	ETPUA0									SCI_B_TX	CAN_C_ RX	WKPCFG	RESET
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSSPLL
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH1/6[3]	EMIOS12	eTPUA19[4]	VRC33	VSS	VRCCTL	NIC[1]	EXTAL
P	ETPUA3	ETPUA2	VSS	VDD	NC[2]	VDDE7	NIC[1]	EMIOS8	eTPUA29[3]	eTPUA2[3]	eTPUA21[3]	CAN_A_ TX	VDD	VSS	NIC[1]	XTAL
R	NIC[1]	VSS	VDD	NC[2]	EMIOS4	NIC[1]	EMIOS9	EMIOS11	EMIOS14	eTPUA27[3]	EMIOS23	CAN_A_ RX	NC[2]	VDD	VSS	VDDPLL
T	VSS	VDD	NIC[1]	EMIOS0	NC[2]	GPIO219	eTPUA25[3]	NC[2]	NC[2]	eTPUA4[3]	eTPUA13[3]	NIC[1]	VDDE5	CLKOUT	VDD	VSS

1 Pins marked “NIC” have no internal connection.
2 Pins marked “NC” may be connected to internal circuitry. Connections to external circuits or other pins on this device can result in unpredictable system behavior or damage.
3 This ball may be changed to “NC” (no connection) in a future revision.
4 eTPU output only channel.

Figure 6. 208-pin MAPBGA ballmap (MPC5633M; top view)

3.6 Signal summary

Table 3. MPC563xM signal properties

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]	Pin No.			
									144 LQFP	176 LQFP	208 MAPBGA
Dedicated GPIO											
GPIO[98]	GPIO	PCR[98]	—	I/O	VDDEH7 Slow	– / Up	GPIO[98]/Up		—	141[7]	J15[8]
GPIO[99]	GPIO	PCR[99]	—	I/O	VDDEH7 Slow	– / Up	GPIO[99]/Up		—	142[7]	H13[8]
GPIO[206][9]	GPIO	PCR[206]	—	I/O	VDDEH7 Slow	– / Up	GPIO[206]/Up		—	143[7]	R4[8]
GPIO[207][9]	GPIO	PCR[207]	—	I/O	VDDEH7 Slow	– / Up	GPIO[207]/Up		—	144[7]	P5[8]
Reset / Configuration											
$\overline{\text{RESET}}$	External Reset Input	—	—	I	VDDEH6a Slow	I / Up	$\overline{\text{RESET}}$ / Up		80	97	L16
$\overline{\text{RSTOUT}}$	External Reset Output	PCR[230]	—	O	VDDEH6a Slow	$\overline{\text{RSTOUT}}$/ Low	$\overline{\text{RSTOUT}}$/ High		85	102	K15
PLLREF $\overline{\text{IRQ}}$[4] ETRIG[2] GPIO[208]	FMPLL Mode Selection External Interrupt Request eQADC Trigger Input GPIO	PCR[208]	011 010 100 000	I I I I/O	VDDEH6a Slow	PLLREF / Up	– / Up		68	83	M14
BOOTCFG1 $\overline{\text{IRQ}}$[3] ETRIG[3] GPIO[212]	Boot Config. Input External Interrupt Request eQADC Trigger Input GPIO	PCR[212]	011 010 100 000	I I I I/O	VDDEH6a Slow	BOOTCFG1 / Down	– / Down		70	85	M15
WKPCFG $\overline{\text{NMI}}$ DSPI_B_SOUT GPIO[213]	Weak Pull Config. Input Non-Maskable Interrupt DSPI_B Data Output GPIO	PCR[213]	01 11 10 00	I I O I/O	VDDEH6a Slow	WKPCFG / Up	– / Up		71	86	L15
Calibration[10]											
CAL_ADDR[12:15][11]	Calibration Address Bus	PCR[340]	—	O	VDDE12 Fast	O / Low	CAL_ADDR / Low		—	—	—

Table 3. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPB GA
CAL_ADDR[16][21] ALT_MDO[0][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	MDO / ALT_ADDR[12] / Low		—	17	A14
CAL_ADDR[17][21] ALT_MDO[1][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	ALT_MDO / CAL_ADDR[12] / Low		—	18	B14
CAL_ADDR[18][21] ALT_MDO[2][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	ALT_MDO / CAL_ADDR[12] / Low		—	19	A13
CAL_ADDR[19][21] ALT_MDO[3][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	ALT_MDO / CAL_ADDR[12] / Low		—	20	B13
CAL_ADDR[20:27] ALT_MDO[4:11]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] Fast	O / Low	ALT_MDO / CAL_ADDR[16] / Low		—	—	—
CAL_ADDR[28][21] ALT_$\overline{\text{MSEO}}$[0][12]	Calibration Address Bus Nexus Msg Start/End Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[17]	ALT_$\overline{\text{MSEO}}$[16] / CAL_ADDR[17]/ Low		—	118	C15
CAL_ADDR[29][21] ALT_$\overline{\text{MSEO}}$[1][12]	Calibration Address Bus Nexus Msg Start/End Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[17]	ALT_$\overline{\text{MSEO}}$[16] / CAL_ADDR[17]/ Low		—	117	E16
CAL_ADDR[30][21] ALT_$\overline{\text{EVTI}}$[12]	Calibration Address Bus Nexus Event In	PCR[345]	—	O I	VDDE12[13] VDDE7[14] Fast	—[18]	ALT_$\overline{\text{EVTI}}$ / CAL_ADDR[19]		—	116	E15
ALT_$\overline{\text{EVTO}}$	Nexus Event Out	PCR[344]	—	O	VDDE12[13] VDDE7[14] Fast	O / Low	ALT_$\overline{\text{EVTO}}$ / High		—	120	D15
ALT_MCKO	Nexus Msg Clock Out	PCR[344]	—	O	VDDE12[13] VDDE7[14] Fast	O / Low	ALT_MCKO / Enabled		—	14	F15
NEXUSCFG[11]	Nexus/Calibration bus selector	—	—	I	VDDE12 Fast	I / Down	NEXUSCFG / Down		—	—	—
CAL_$\overline{\text{CS}}$[0][11]	Calibration Chip Selects	PCR[336]	—	O	VDDE12 Fast	O / High	CAL_$\overline{\text{CS}}$ / High		—	—	—
CAL_$\overline{\text{CS}}$[2][11] CAL_ADDR[10]	Calibration Chip Selects Calibration Address Bus	PCR[338]	11 10	O O	VDDE12 Fast	O / High	CAL_$\overline{\text{CS}}$ / High		—	—	—

Table 3. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPB GA
CAL_$\overline{CS}$[3][11] CAL_ADDR[11]	Calibration Chip Selects Calibration Address Bus	PCR[339]	11 10	O O	VDDE12 Fast	O / High	CAL_$\overline{CS}$ / High		—	—	—
CAL_DATA[0:9][11]	Calibration Data Bus	PCR[341]		I/O	VDDE12 Fast	– / Up	– / Up		—	—	—
CAL_DATA[10:15][11]	Calibration Data Bus	PCR[341]		I/O	VDDE12 Fast	– / Up	– / Up		—	—	—
CAL_$\overline{OE}$[11]	Calibration Output Enable	PCR[342]	—	O	VDDE12 Fast	O / High	CAL_$\overline{OE}$ / High		—	—	—
CAL_RD_$\overline{WR}$[11]	Calibration Read/Write	PCR[342]	—	O	VDDE12 Fast	O / High	CAL_RD_$\overline{WR}$ /High		—	—	—
CAL_$\overline{TS}$_ALE[11]	Calibration Transfer Start Address Latch Enable	PCR[343]		O O	VDDE12 Fast	O / High	CAL_$\overline{TS}$ / High		—	—	—
CAL_$\overline{WE}$_BE[0:1][11]	Calibration Write Enable Byte Enable	PCR[342]	—	O	VDDE12 Fast	O / High	CAL_$\overline{WE}$ / High		—	—	—
NEXUS[20]											
$\overline{EVTI}$[21] eTPU_A[2] GPIO[231]	Nexus Event In eTPU A Ch. GPIO	PCR[231]	01 10 00	I O I/O	VDDEH7 Multi-V	– / –	– / –		103	126	P10
$\overline{EVTO}$ [21] eTPU_A[4] GPIO[227]	Nexus Event Out eTPU A Ch. GPIO	PCR[227]	01[22] 10 00	O O I/O	VDDEH7 Multi-V	I / Up	I / Up		106	129	T10
MCKO[21] GPIO[219]	Nexus Msg Clock Out GPIO	PCR[219]	N/A[22] 00	O I/O	VDDEH7 Multi-V	– / –	– / –		99	122	T6
MDO[0][21] eTPU_A[13] GPIO[220]	Nexus Msg Data Out eTPU A Ch. GPIO	PCR[220]	01 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		110	135	T11
MDO[1][21] eTPU_A[19] GPIO[221]	Nexus Msg Data Out eTPU A Ch. GPIO	PCR[221]	01[22] 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		111	136	N11
MDO[2][21] eTPU_A[21] GPIO[222]	Nexus Msg Data Out eTPU A Ch. GPIO	PCR[222]	01[22] 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		112	137	P11

Table 3. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPB GA
MDO[3][21] eTPU_A[25] GPIO[223]	Nexus Msg Data Out eTPU A Ch. GPIO	PCR[223]	01[22] 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		114	139	T7
$\overline{\text{MSEO}}$[0][21] eTPU_A[27] GPIO[224]	Nexus Msg Start/End Out eTPU A Ch. GPIO	PCR[224]	01[22] 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		109	134	R10
$\overline{\text{MSEO}}$[1][21] eTPU_A[29] GPIO[225]	Nexus Msg Start/End Out eTPU A Ch. GPIO	PCR[225]	01[22] 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		101	124	P9
JTAG / TEST											
TCK	JTAG Test Clock Input	—	—	I	VDDEH7 Multi-V	TCK / Down	TCK / Down		105	128	C16
TDI[23] eMIOS[5] GPIO[232]	JTAG Test Data Input eMIOS Ch. GPIO	PCR[232]	01[24] 10 00	I O I/O	VDDEH7 Multi-V	– / –	– / –		107	130	E14
TDO[23] eMIOS[6] GPIO[228]	JTAG Test Data Output eMIOS Ch. GPIO	PCR[228]	01[24] 10 00	O O I/O	VDDEH7 Multi-V	– / –	– / –		100	123	F14
TMS	JTAG Test Mode Select Input	—	—	I	VDDEH7 Multi-V	TMS / Up	TMS / Up		108	131	D14
JCOMP	JTAG TAP Controller Enable	—	—	I	VDDEH7 Multi-V	JCOMP / Down	JCOMP / Down		98	121	F16
CAN											
CAN_A_TX SCI_A_TX GPIO[83]	CAN_A Transmit eSCI_A Transmit GPIO	PCR[83]	01 10 00	O O I/O	VDDEH6a Slow	– / Up	– / Up[25]		66	81	P12
CAN_A_RX SCI_A_RX GPIO[84]	CAN_A Receive eSCI_A Receive GPIO	PCR[84]	01 10 00	I I I/O	VDDEH6a Slow	– / Up	– / Up		67	82	R12
CAN_C_TX GPIO[87]	CAN_C Transmit GPIO	PCR[87]	01 00	O I/O	VDDEH6a Medium	– / Up	– / Up		84	101	K13
CAN_C_RX GPIO[88]	CAN_C Receive GPIO	PCR[88]	01 00	I I/O	VDDEH6a Slow	– / Up	– / Up		81	98	L14

Table 3. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPB GA
eSCI											
SCI_A_TX eMIOS[13] GPIO[89]	eSCI_A Transmit eMIOS Ch. GPIO	PCR[89]	01 10 00	O O I/O	VDDEH6a Slow	– / Up	– / Up		83	100	J14
SCI_A_RX eMIOS[15] GPIO[90]	eSCI_A Receive eMIOS Ch. GPIO	PCR[90]	01 10 00	I O I/O	VDDEH6a Slow	– / Up	– / Up		82	99	K14
SCI_B_TX GPIO[91]	eSCI_B Transmit GPIO	PCR[91]	01 00	I/O I/O	VDDEH6a Slow	– / Up	– / Up		72	87	L13
SCI_B_RX GPIO[92]	eSCI_B Receive GPIO	PCR[92]	01 00	I I/O	VDDEH6a Slow	– / Up	– / Up		69	84	M13
DSPI											
DSPI_B_SCK DSPI_C_PCS[1] GPIO[102]	DSPI_B Clock DSPI_C Periph Chip Select GPIO	PCR[102]	01 10 00	I/O O I/O	VDDEH6b Medium	– / Up	– / Up		89	106	J16
DSPI_B_SIN DSPI_C_PCS[2] GPIO[103]	DSPI_B Data Input DSPI_C Periph Chip Select GPIO	PCR[103]	01 10 00	I O I/O	VDDEH6b Medium	– / Up	– / Up		95	112	G15
DSPI_B_SOUT DSPI_C_PCS[5] GPIO[104]	DSPI_B Data Output DSPI_C Periph Chip Select GPIO	PCR[104]	01 10 00	O O I/O	VDDEH6b Medium	– / Up	– / Up		96	113	G13
DSPI_B_PCS[0] GPIO[105]	DSPI_B Periph Chip Select GPIO	PCR[105]	01 00	O I/O	VDDEH6b Medium	– / Up	– / Up		94	111	G16
DSPI_B_PCS[1] GPIO[106]	DSPI_B Periph Chip Select GPIO	PCR[106]	01 00	O I/O	VDDEH6b Medium	– / Up	– / Up		92	109	H16
DSPI_B_PCS[2] DSPI_C_SOUT GPIO[107]	DSPI_B Periph Chip Select DSPI_C Data Output GPIO	PCR[107]	01 10 00	O O I/O	VDDEH6b Medium	– / Up	– / Up		90	107	H15
DSPI_B_PCS[3] DSPI_C_SIN GPIO[108]	DSPI_B Periph Chip Select DSPI_C Data Input GPIO	PCR[108]	01 10 00	O I I/O	VDDEH6b Medium	– / Up	– / Up		97	114	G14
DSPI_B_PCS[4] DSPI_C_SCK GPIO[109]	DSPI_B Periph Chip Select DSPI_C Clock GPIO	PCR[109]	01 10 00	O I/O I/O	VDDEH6b Medium	– / Up	– / Up		88	105	H14

Table 3. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPB GA
DSPI_B_PCS[5] DSPI_C_PCS[0] GPIO[110]	DSPI_B Periph Chip Select DSPI_C Periph Chip Select GPIO	PCR[110]	01 10 00	O O I/O	VDDEH6b Medium	– / Up	– / Up		87	104	J13
eQADC											
AN[0] DAN0+	Single Ended Analog Input Positive Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[0] / –		143	172	B5
AN[1] DAN0-	Single Ended Analog Input Negative Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[1] / –		142	171	A6
AN[2] DAN1+	Single Ended Analog Input Positive Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[2] / –		141	170	D6
AN[3] DAN1-	Single Ended Analog Input Negative Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[3] / –		140	169	C7
AN[4] DAN2+	Single Ended Analog Input Positive Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[4] / –		139	168	B6
AN[5] DAN2-	Single Ended Analog Input Negative Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[5] / –		138	167	A7
AN[6] DAN3+	Single Ended Analog Input Positive Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[6] / –		137	166	D7
AN[7] DAN3-	Single Ended Analog Input Negative Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[7] / –		136	165	C8
AN[8]	See AN[38]-AN[8]-ANW										
AN[9] ANX	Single Ended Analog Input External Multiplexed Analog Input	—	—	I I	VDDA	I / –	AN[9] / –		5	5	A2
AN[10]	See AN[39]-AN[10]-ANY										
AN[11] ANZ	Single Ended Analog Input External Multiplexed Analog Input	—	—	I I	VDDA	I / –	AN[11] / –		4	4	A3
AN[12] MA[0] ETPU_A[19] $\overline{SDS}$	Single Ended Analog Input Mux Address ETPU_A Ch. eQADC Serial Data Strobe	PCR[215]	011 010 100 000	I O O O	VDDEH7	I / –	AN[12] / –		119	148	A12

Table 3. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]	Pin No.			
									144 LQFP	176 LQFP	208 MAPB GA
AN[13] MA[1] ETPU_A[21] SDO	Single Ended Analog Input Mux Address ETPU_A Ch. eQADC Serial Data Out	PCR[216]	011 010 100 000	I O O O	VDDEH7	I / –	AN[13] / –		118	147	B12
AN[14] MA[2] ETPU_A[27] SDI	Single Ended Analog Input Mux Address ETPU_A Ch. eQADC Serial Data In	PCR[217]	011 010 100 000	I O O I	VDDEH7	I / –	AN[14] / –		117	146	C12
AN[15] FCK ETPU_A[29]	Single Ended Analog Input eQADC Free Running Clock ETPU_A Ch.	PCR[218]	011 010 100	I O O	VDDEH7	I / –	AN[15] / –		116	145	C13
AN[16]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		3	3	C6
AN[17]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		2	2	C4
AN[18]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		1	1	D5
AN[21]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		144	173	B4
AN[22]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		132	161	B8
AN[23]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		131	160	C9
AN[24]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		130	159	D8
AN[25]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		129	158	B9
AN[27]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		128	157	A10
AN[28]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		127	156	B10
AN[30]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		126	155	D9
AN[31]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		125	154	D10
AN[32]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		124	153	C10
AN[33]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		123	152	C11
AN[34]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		122	151	C5
AN[35]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		121	150	D11
AN[36]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		—	174[7]	F4[8]
AN[37]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		—	175[7]	E3[8]

Table 3. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPB GA
AN[38]-AN[8]-ANW	Single Ended Analog Input Multiplexed Analog Input	—	—	I	VDDA	I / –	AN[38] / –		9	9	B3
AN[39]-AN[10]-ANY	Single Ended Analog Input Multiplexed Analog Input	—	—	I	VDDA	I / –	AN[39] / –		8	8	D2
VRH	Voltage Reference High	—	—	I	VDDA	– / –	VRH		134	163	A8
VRL	Voltage Reference Low	—	—	I	VSSA0	– / –	VRL		133	162	A9
REFBYPC	Bypass Capacitor Input	—	—	I	VRL	– / –	REFBYPC		135	164	B7
eTPU2											
eTPU_A[0] eTPU_A[12] eTPU_A[19] GPIO[114]	eTPU_A Ch. eTPU_A Ch. eTPU_A Ch. GPIO	PCR[114]	011 010 100 000	I/O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		52	61	L4, N3
eTPU_A[1] eTPU_A[13] GPIO[115]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[115]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		51	60	M3
eTPU_A[2] eTPU_A[14] GPIO[116]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[116]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		50	59	P2
eTPU_A[3] eTPU_A[15] GPIO[117]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[117]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		49	58	P1
eTPU_A[4] eTPU_A[16] GPIO[118]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[118]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		47	56	N2
eTPU_A[5] eTPU_A[17] DSPI_B_SCK_LVDS- GPIO[119]	eTPU_A Ch. eTPU_A Ch. DSPI_B CLOCK LVDS- GPIO	PCR[119]	001 010 100 000	I/O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		45	54	M4
eTPU_A[6] eTPU_A[18] DSPI_B_SCK_LVDS+ GPIO[120]	eTPU_A Ch. eTPU_A Ch. DSPI_B Clock LVDS+ GPIO	PCR[120]	001 010 100 000	I/O O O I/O	VDDEH1b Medium	– / WKPCFG	– / WKPCFG		44	53	L3

Table 3. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPB GA
eTPU_A[7] eTPU_A[19] DSPI_B_SOUT_LVDS- eTPU_A[6] GPIO[121]	eTPU_A Ch. eTPU_A Ch. DSPI_B Data Output LVDS- eTPU_A Ch. GPIO	PCR[121]	0001 0010 0100 1000 0000	I/O O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		43	52	K3
eTPU_A[8] eTPU_A[20] DSPI_B_SOUT_LVDS+ GPIO[122]	eTPU_A Ch. eTPU_A Ch. DSPI_B Data Output LVDS+ GPIO	PCR[122]	001 010 100 000	I/O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		42	51	N1
eTPU_A[9] eTPU_A[21] GPIO[123]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[123]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		41	50	M2
eTPU_A[10] eTPU_A[22] GPIO[124]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[124]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		40	49	M1
eTPU_A[11] eTPU_A[23] GPIO[125]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[125]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		39	48	L2
eTPU_A[12] DSPI_B_PCS[1] GPIO[126]	eTPU_A Ch. DSPI_B Periph Chip Select GPIO	PCR[126]	01 10 00	I/O O I/O	VDDEH1b Medium	– / WKPCFG	– / WKPCFG		38	47	L1
eTPU_A[13] DSPI_B_PCS[3] GPIO[127]	eTPU_A Ch. DSPI_B Periph Chip Select GPIO	PCR[127]	01 10 00	I/O O I/O	VDDEH1b Medium	– / WKPCFG	– / WKPCFG		37	46	J4
eTPU_A[14] DSPI_B_PCS[4] eTPU_A[9] GPIO[128]	eTPU_A Ch. DSPI_B Periph Chip Select eTPU_A Ch. GPIO	PCR[128]	001 010 100 000	I/O O O I/O	VDDEH1b Medium	– / WKPCFG	– / WKPCFG		35	42	J3
eTPU_A[15] DSPI_B_PCS[5] GPIO[129]	eTPU_A Ch. DSPI_B Periph Chip Select GPIO	PCR[129]	01 10 00	I/O O I/O	VDDEH1b Medium	– / WKPCFG	– / WKPCFG		33	40	K2
eTPU_A[16] GPIO[130]	eTPU_A Ch. GPIO	PCR[130]	01 00	I/O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		32	39	K1
eTPU_A[17] GPIO[131]	eTPU_A Ch. GPIO	PCR[131]	01 00	I/O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		31	38	H3

Table 3. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]	Pin No.			
									144 LQFP	176 LQFP	208 MAPB GA
eTPU_A[18] GPIO[132]	eTPU_A Ch. GPIO	PCR[132]	01 00	I/O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		30	37	H4
eTPU_A[19] GPIO[133]	eTPU_A Ch. GPIO	PCR[133]	01 00	I/O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		29	36	J2
eTPU_A[20] $\overline{\text{IRQ}}$[8] GPIO[134]	eTPU_A Ch. External Interrupt Request GPIO	PCR[134]	01 10 00	I/O I I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		28	35	J1
eTPU_A[21] $\overline{\text{IRQ}}$[9] GPIO[135]	eTPU_A Ch. External Interrupt Request GPIO	PCR[135]	01 10 00	I/O I I/O	VDDEH1a Slow	– / WKPCFG	– / WKPCFG		27	34	G4
eTPU_A[22] $\overline{\text{IRQ}}$[10] eTPU_A[17] GPIO[136]	eTPU_A Ch. External Interrupt Request eTPU_A Ch. External GPIO	PCR[136]	001 010 100 000	I/O I O I/O	VDDEH1a Slow	– / WKPCFG	– / WKPCFG		25	32	H2
eTPU_A[23] $\overline{\text{IRQ}}$[11] eTPU_A[21] GPIO[137]	eTPU_A Ch. External Interrupt Request eTPU_A Ch. External GPIO	PCR[137]	001 010 100 000	I/O I O I/O	VDDEH1a Slow	– / WKPCFG	– / WKPCFG		23	30	H1
eTPU_A[24][26] $\overline{\text{IRQ}}$[12] DSPI_C_SCK_LVDS- GPIO[138]	eTPU_A Ch. External Interrupt Request DSPI_C Clock LVDS- GPIO	PCR[138]	001 010 100 000	I/O I O I/O	VDDEH1a Slow	– / WKPCFG	– / WKPCFG		21	28	G1
eTPU_A[25][26] $\overline{\text{IRQ}}$[13] DSPI_C_SCK_LVDS+ GPIO[139]	eTPU_A Ch. External Interrupt Request DSPI _C Clock LVDS+ GPIO	PCR[139]	001 010 100 000	I/O I O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		20	27	G3
eTPU_A[26][26] $\overline{\text{IRQ}}$[14] DSPI_C_SOUT_LVDS- GPIO[140]	eTPU_A Ch. External Interrupt Request DSPI_C Data Output LVDS- GPIO	PCR[140]	001 010 100 000	I/O I O I/O	VDDEH1a Slow	– / WKPCFG	– / WKPCFG		19	26	F3
eTPU_A[27][26] $\overline{\text{IRQ}}$[15] DSPI_C_SOUT_LVDS+ DSPI_B_SOUT GPIO[141]	eTPU_A Ch. External Interrupt Request DSPI_C Data Output LVDS+ DSPI_B Data Output GPIO	PCR[141]	0001 0010 0100 1000 0000	I/O I O O I/O	VDDEH1a Slow	– / WKPCFG	– / WKPCFG		18	25	G2

Table 3. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPB GA
eTPU_A[28][26] DSPI_C_PCS[1] GPIO[142]	eTPU_A Ch. (Output Only) DSPI_C Periph Chip Select GPIO	PCR[142]	10 01 00	I/O O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		17	24	F1
eTPU_A[29][26] DSPI_C_PCS[2] GPIO[143]	eTPU_A Ch. (Output Only) DSPI_C Periph Chip Select GPIO	PCR[143]	10 01 00	I/O O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		16	23	F2
eTPU_A[30] DSPI_C_PCS[3] eTPU_A[11] GPIO[144]	eTPU_A Ch. DSPI_C Periph Chip Select eTPU_A Ch. GPIO	PCR[144]	011 010 001 000	I/O O O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		15	22	E1
eTPU_A[31] DSPI_C_PCS[4] eTPU_A[13] GPIO[145]	eTPU_A Ch. DSPI_C Periph Chip Select eTPU_A Ch. GPIO	PCR[145]	011 010 001 000	I/O O O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		14	21	E2
eMIOS											
eMIOS[0] eTPU_A[0] eTPU_A[25][27] GPIO[179]	eMIOS Ch. eTPU_A Ch. eTPU_A Ch. GPIO	PCR[179]	001 010 100 000	I/O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		54	63	T4
eMIOS[1] eTPU_A[1] GPIO[180]	eMIOS Ch. eTPU_A Ch. GPIO	PCR[180]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		—	64[7]	T5[8]
eMIOS[2] eTPU_A[2] GPIO[181]	eMIOS Ch. eTPU_A Ch. GPIO	PCR[181]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		55	65	N7
eMIOS[4] eTPU_A[4] GPIO[183]	eMIOS Ch. eTPU_A Ch. GPIO	PCR[183]	01 10 00	I/O O I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		56	67	R5
eMIOS[8] eTPU_A[8][28] SCI_B_TX GPIO[187]	eMIOS Ch. eTPU_A Ch. eSCI_B Transmit GPIO	PCR[187]	001 010 100 000	I/O O O I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		57	70	P8
eMIOS[9] eTPU_A[9][28] SCI_B_RX GPIO[188]	eMIOS Ch. eTPU_A Ch. eSCI_B Receive GPIO	PCR[188]	001 010 100 000	I/O O I I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		58	71	R7

Table 3. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPB GA
eMIOS[10] GPIO[189]	eMIOS Ch. GPIO	PCR[189]	01 00	I/O I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		60	73	N8
eMIOS[11] GPIO[190]	eMIOS Ch. GPIO	PCR[190]	01 00	I/O I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		62	75	R8
eMIOS[12][29] DSPI_C_SOUT eTPU_A[27] GPIO[191]	eMIOS Ch. DSPI C Data Output eTPU_A Ch. GPIO	PCR[191]	001 010 100 000	I/O O O I/O	VDDEH6a Medium	– / WKPCFG	– / WKPCFG		63	76	N10
eMIOS[13] GPIO[192]	eMIOS Ch. GPIO	PCR[192]	01 00	I/O I/O	VDDEH6a	– / WKPCFG	– / WKPCFG		—	77[7]	T8[8]
eMIOS[14] $\overline{\text{IRQ}}$[0] eTPU_A[29] GPIO[193]	eMIOS Ch. External Interrupt Request eTPU_A Ch. GPIO	PCR[193]	001 010 100 000	O I O I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		64	78	R9
eMIOS[15] $\overline{\text{IRQ}}$[1] GPIO[194]	eMIOS Ch. External Interrupt Request GPIO	PCR[194]	01 10 00	O I I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		—	79[7]	T9[8]
eMIOS[23] GPIO[202]	eMIOS Ch. GPIO	PCR[202]	01 00	I/O I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		65	80	R11
Clock Synthesizer											
XTAL	Crystal Oscillator Output	—	—	O	VDDEH6a	O / –	XTAL[30] / –		76	93	P16
EXTAL EXTCLK	Crystal Oscillator Input External Clock Input	—	—	I	VDDEH6a	I / –	EXTAL[31] / –		75	92	N16
CLKOUT	System Clock Output	PCR[229]	—	O	VDDE5 Fast	CLKOUT / Enabled	CLKOUT / Enabled		—	—	T14
Power / Ground											
VDDPLL	PLL Supply Voltage	—	—	I	VDDPLL (1.2 V)	I / –	—		74	91	R16
VSSPLL[32]	PLL Ground	—	—	I	VSSPLL	I / –	—		77	94	M16
VSTBY	Power Supply for Standby RAM	—	—	I	VSTBY	I / –	—		12	12	C1
VRC33	3.3 V Voltage Regulator Bypass Capacitor	—	—	O	VRC33	O / –	—		13	13	A15, D1, N6, N12

Table 3. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]	Pin No.			
									144 LQFP	176 LQFP	208 MAPBGA
VRCCTL	Voltage Regulator Control Output	—	—	O	NA	O / –	—		11	11	N14
VDDA[33]	Analog Power Input for eQADC	—	—	I	VDDA (5.0 V)	I / –	—		6	6	—
VDDA0	Analog Power Input for eQADC	—	—	I	VDDA	I / –	—		—	—	B11
VSSA0	Analog Ground Input for eQADC	—	—	I	VSSA	I / –	—		—	—	A11
VDDA1	Analog Power Input for eQADC	—	—	I	VDDA	I / –	—		—	—	A4
VSSA1	Analog Ground Input for eQADC	—	—	I	VSSA	I / –	—		—	—	A5
VSSA[34]	Analog Ground Input for eQADC	—	—	I	VSSA	I / –	—		7	7	—
VDDREG	Voltage Regulator Supply	—	—	I	VDDREG (5.0 V)	I / –	—		10	10	K16
VDD	Internal Logic Supply Input	—	—	I	VDD (1.2 V)	I / –	—		26, 53, 86, 120	33, 62, 103, 149	B1, B16, C2, D3, E4, N5, P4, P13, R3, R14, T2, T15
VSS	Ground	—	—	–	VSS0	I / –	—		22, 36, 48, 59, 73, 79, 91, 104, 115	15, 29, 43, 57, 72, 90, 96, 108, 115[7], 127, 133, 140	A1, A16, B2, B15, C3, C14, D4, D13, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, N4, N13, P3, P14, R2, R15, T1, T16
VDDEH1A[35] VDDEH1B[35]	I/O Supply Input	—	—	I	VDDEH1[36] (3.3–5.0 V)	I / –	—		24, 34, 46	31, 41 55	K4

Table 3. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]	Pin No.			
									144 LQFP	176 LQFP	208 MAPB GA
VDDE5	I/O Supply Input	—	—	I	VDDE5	I / –	—		—	—	T13
VDDEH6a[37, 38] VDDEH6b[38]	I/O Supply Input	—	—	I	VDDEH6 (3.3–5.0V)	I / –	—		78, 93, 61	95, 110, 74	—
VDDEH6	I/O Supply Input	—	—	I	VDDEH6	I / –	—		—	—	F13
VDDEH7	I/O Supply Input	—	—	I	VDDEH7[39] (3.3–5.0 V)	I / –	—		102, 113	125, 138	D12
VDDE7[40]	I/O Supply Input	—	—	I	VDDE7 (3.3 V)	I / –	—		—	16, 119[7]	E13, P6

1 For each pin in the table, each line in the Function column is a separate function of the pin. For all I/O pins the selection of primary pin function or secondary function or GPIO is done in the SIU except where explicitly noted.

2 Values in this column refer to registers in the System Integration Unit (SIU). The actual register name is “SIU_PCR” suffixed by the PCR number. For example, PCR[190] refers to the SIU register named SIU_PCR190.

3 The Pad Configuration Register (PCR) PA field is used by software to select pin function.

4 The VDDE and VDDEH supply inputs are broken into segments. Each segment of slow I/O pins (VDDEH) may have a separate supply in the 3.3 V to 5.0 V range (–10%/+5%). Each segment of fast I/O (VDDE) may have a separate supply in the 1.8 V to 3.3 V range (+/– 10%).

5 Terminology is O - output, I - input, Up - weak pull up enabled, Down - weak pull down enabled, Low - output driven low, High - output driven high. A dash for the function in this column denotes that both the input and output buffer are turned off.

6 Function after reset of GPI is general purpose input. A dash for the function in this column denotes that both the input and output buffer are turned off.

7 Not available on 1 MB version of 176-pin package.

8 Not available on 1 MB version of 208-pin package.

9 The GPIO functions on GPIO[206] and GPIO[207] can be selected as trigger functions in the SIU for the ADC by making the proper selections in the SIU_ETISR and SIU_ISEL3 registers in the SIU.

10 Some signals in this section are available only on calibration package.

11 These pins are only available in the 496 CSP/MAPBGA calibration/development package.

12 On the calibration package, the Nexus function on this pin is enabled when the NEXUSCFG pin is high and Nexus is configured to full port mode. On the 176-pin and 208-pin packages, the Nexus function on this pin is enabled permanently.

13 In the calibration package, the I/O segment containing this pin is called VDDE12.

14 208-ball BGA package only

15 When configured as Nexus (208-pin package or calibration package with NEXUSCFG=1), and JCOMP is asserted during reset, MDO[0] is driven high until the crystal oscillator becomes stable, at which time it is then negated.

16 The function of this pin is Nexus when NEXUSCFG is high.

17 High when the pin is configured to Nexus, low otherwise.

18 O/Low for the calibration with NEXUSCFG=0; I/Up otherwise.

[19] ALT_ADDR/Low for the calibration package with NEXUSCFG=0; $\overline{\text{EVTI}}$/Up otherwise.

[20] In 176-pin and 208-pin packages, the Nexus function is disabled and the pin/ball has the secondary function

[21] This signal is not available in the 176-pin and 208-pin packages.

[22] The primary function is not selected via the PA field when the pin is a Nexus signal. Instead, it is activated by the Nexus controller.

[23] TDI and TDO are required for JTAG operation.

[24] The primary function is not selected via the PA field when the pin is a JTAG signal. Instead, it is activated by the JTAG controller.

[25] The function and state of the CAN_A and eSCI_A pins after execution of the BAM program is determined by the BOOTCFG1 pin.

[26] ETPUA[24:29] are input and output. The input muxing is controlled by SIU_ISEL8 register.

[27] eTPU_A[25] is an output only function.

[28] Only the output channels of eTPU[8:9] are connected to pins.

[29] Only the output of eMIOS[12] is connected to the pin. The DSPI_C_SOUT is not available in this device.

[30] The function after reset of the XTAL pin is determined by the value of the signal on the PLLCFG[1] pin. When bypass mode is chosen XTAL has no function and should be grounded.

[31] The function after reset of the EXTAL_EXTCLK pin is determined by the value of the signal on the PLLCFG[1] pin. If the EXTCLK function is chosen, the valid operating voltage for the pin is 1.62 V to 3.6 V. If the EXTAL function is chosen, the valid operating voltage is 3.3 V.

[32] VSSPLL and VSSREG are connected to the same pin.

[33] This pin is shared by two pads: VDDA_AN, using pad_vdde_hv, and VDDA_DIG, using pad_vdde_int_hv.

[34] This pin is shared by two pads: VSSA_AN, using pad_vsse_hv, and VSSA_DIG, using pad_vsse_int_hv.

[35] VDDEH1A, VDDEH1B, and VDDEH1AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[36] LVDS pins will not work at 3.3 V.

[37] The VDDEH6 segment may be powered from 3.0 V to 5.0 V for mux address or SSI functions, but must meet the VDDA specifications of 4.5 V to 5.25 V for analog input function.

[38] VDDEH6A and VDDEH6B are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[39] If using JTAG or Nexus, the I/O segment that contains the JTAG and Nexus pins must be powered by a 5 V supply. The 3.3 V Nexus/JTAG signals are derived from the 5 volt power supply.

[40] In the calibration package this signal is named VDDE12.

Table 4. Pad types

Pad Type	Name	Supply Voltage
Slow	pad_ssr_hv	3.0 V – 5.25 V
Medium	pad_msr_hv	3.0 V – 5.25 V
Fast	pad_fc	3.0 V – 3.6 V
MultiV	pad_multv_hv	3.0 V - 5.25 V (high swing mode) 4.5 V - 5.25 V (low swing mode)
Analog	pad_ae_hv	0.0 - 5.25 V
LVDS	pad_lo_lv	—

3.7 Signal details

Table 5 contains details on the multiplexed signals that appear in Table 3, “MPC563xM signal properties”.

Table 5. Signal details

Signal	Module or Function	Description
CLKOUT	Clock Generation	MPC5634M clock output for the external/calibration bus interface
EXTAL	Clock Generation	Input pin for an external crystal oscillator or an external clock source based on the value driven on the PLLREF pin at reset.
EXTCLK	Clock Generation	External clock input
PLLREF	Clock Generation	PLLREF is used to select whether the oscillator operates in xtal mode or external reference mode from reset. PLLREF=0 selects external reference mode.
XTAL	Clock Generation	Crystal oscillator input
SCK_B_LVDS– SCK_B_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission
SOUT_B_LVDS– SOUT_B_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission
SCK_C_LVDS– SCK_C_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission
SOUT_C_LVDS– SOUT_C_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission
PCS_B[0] PCS_C[0]	DSPI_B – DSPI_C	Peripheral chip select when device is in master mode—slave select when used in slave mode
PCS_B[1:5] PCS_C[1:5]	DSPI_B – DSPI_C	Peripheral chip select when device is in master mode—not used in slave mode
SCK_B SCK_C	DSPI_B – DSPI_C	DSPI clock—output when device is in master mode; input when in slave mode
SIN_B SIN_C	DSPI_B – DSPI_C	DSPI data in
SOUT_B SOUT_C	DSPI_B – DSPI_C	DSPI data out
CAL_ADDR[12:30]	Calibration Bus	The CAL_ADDR[12:30] signals specify the physical address of the bus transaction.
CAL_$\overline{\text{CS}}$[0:3]	Calibration Bus	$\overline{\text{CS}}$x is asserted by the master to indicate that this transaction is targeted for a particular memory bank on the Primary external bus.
CAL_DATA[0:15]	Calibration Bus	The CAL_DATA[0:15] signals contain the data to be transferred for the current transaction.
CAL_$\overline{\text{OE}}$	Calibration Bus	$\overline{\text{OE}}$ is used to indicate when an external memory is permitted to drive back read data. External memories must have their data output buffers off when $\overline{\text{OE}}$ is negated. $\overline{\text{OE}}$ is only asserted for chip-select accesses.
CAL_RD_$\overline{\text{WR}}$	Calibration Bus	RD_$\overline{\text{WR}}$ indicates whether the current transaction is a read access or a write access.

Table 5. Signal details (continued)

Signal	Module or Function	Description
CAL_$\overline{TS}$_ALE	Calibration Bus	The Transfer Start signal ($\overline{TS}$) is asserted by the MPC5634M to indicate the start of a transfer. The Address Latch Enable (ALE) signal is used to demultiplex the address from the data bus.
CAL_$\overline{EVTO}$	Calibration Bus	Nexus Event Out
CAL_MCKO	Calibration Bus	Nexus Message Clock Out
NEXUSCFG	Nexus/Calibration Bus	Nexus/Calibration Bus selector
eMIOS[0:23]	eMIOS	eMIOS I/O channels
AN[0:39]	eQADC	Single-ended analog inputs for analog-to-digital converter
FCK	eQADC	eQADC free running clock for eQADC SSI.
MA[0:2]	eQADC	These three control bits are output to enable the selection for an external Analog Mux for expansion channels.
REFBYPC	eQADC	Bypass capacitor input
SDI	eQADC	Serial data in
SDO	eQADC	Serial data out
SDS	eQADC	Serial data select
VRH	eQADC	Voltage reference high input
VRL	eQADC	Voltage reference low input
SCI_A_RX SCI_B_RX	eSCI_A – eSCI_B	eSCI receive
SCI_A_TX SCI_B_TX	eSCI_A – eSCI_B	eSCI transmit
ETPU_A[0:31]	eTPU	eTPU I/O channel
CAN_A_TX CAN_C_TX	FlexCan_A – FlexCAN_C	FlexCAN transmit
CAN_A_RX CAN_C_RX	FlexCAN_A – FlexCAN_C	FlexCAN receive
JCOMP	JTAG	Enables the JTAG TAP controller.
TCK	JTAG	Clock input for the on-chip test and debug logic.
TDI	JTAG	Serial test instruction and data input for the on-chip test and debug logic.
TDO	JTAG	Serial test data output for the on-chip test logic.
TMS	JTAG	Controls test mode operations for the on-chip test and debug logic.
$\overline{EVTI}$	Nexus	$\overline{EVTI}$ is an input that is read on the negation of $\overline{RESET}$ to enable or disable the Nexus Debug port. After reset, the $\overline{EVTI}$ pin is used to initiate program synchronization messages or generate a breakpoint.

Table 5. Signal details (continued)

Signal	Module or Function	Description
$\overline{\text{EVTO}}$	Nexus	Output that provides timing to a development tool for a single watchpoint or breakpoint occurrence.
MCKO	Nexus	MCKO is a free running clock output to the development tools which is used for timing of the MDO and $\overline{\text{MSEO}}$ signals.
MDO[3:0]	Nexus	Trace message output to development tools. This pin also indicates the status of the crystal oscillator clock following a power-on reset, when MDO[0] is driven high until the crystal oscillator clock achieves stability and is then negated.
$\overline{\text{MSEO}}$[1:0]	Nexus	Output pin—Indicates the start or end of the variable length message on the MDO pins
BOOTCFG[1]	SIU – Configuration	The BOOTCFG1 pin is sampled during the assertion of the RSTOUT signal, and the value is used to update the RSR and the BAM boot mode The following values are for BOOTCFG[0:1}: 0 Boot from internal flash memory 1 FlexCAN/eSCI boot
WKPCFG	SIU – Configuration	The WKPCFG pin is applied at the assertion of the internal reset signal (assertion of $\overline{\text{RSTOUT}}$), and is sampled 4 clock cycles before the negation of the $\overline{\text{RSTOUT}}$ pin. The value is used to configure whether the eTPU and eMIOS pins are connected to internal weak pull up or weak pull down devices after reset. The value latched on the WKPCFG pin at reset is stored in the Reset Status Register (RSR), and is updated for all reset sources except the Debug Port Reset and Software External Reset. 0: Weak pulldown applied to eTPU and eMIOS pins at reset 1: Weak pullup applied to eTPU and eMIOS pins at reset.
ETRIG[2:3]	SIU – eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
IRQ[0:15]	SIU – External Interrupts	The IRQ[0:15] pins connect to the SIU IRQ inputs. IMUX Select Register 1 is used to select the IRQ[0:15] pins as inputs to the IRQs.

Table 5. Signal details (continued)

Signal	Module or Function	Description
NMI	SIU – External Interrupts	Non-Maskable Interrupt
GPIO[n]	SIU – GPIO	Configurable general purpose I/O pins. Each GPIO input and output is separately controlled by an 8-bit input (GPDI) or output (GPDO) register. Additionally, each GPIO pins is configured using a dedicated SIU_PCR register. The GPIO pins are generally multiplexed with other I/O pin functions.
$\overline{\text{RESET}}$	SIU – Reset	The $\overline{\text{RESET}}$ pin is an active low input. The $\overline{\text{RESET}}$ pin is asserted by an external device during a power-on or external reset. The internal reset signal asserts only if the $\overline{\text{RESET}}$ pin asserts for 10 clock cycles. Assertion of the $\overline{\text{RESET}}$ pin while the device is in reset causes the reset cycle to start over. The $\overline{\text{RESET}}$ pin has a glitch detector which detects spikes greater than two clock cycles in duration that fall below the switch point of the input buffer logic of the VDDEH input pins. The switch point lies between the maximum VIL and minimum VIH specifications for the VDDEH input pins.
$\overline{\text{RSTOUT}}$	SIU – Reset	The $\overline{\text{RSTOUT}}$ pin is an active low output that uses a push/pull configuration. The $\overline{\text{RSTOUT}}$ pin is driven to the low state by the MCU for all internal and external reset sources. There is a delay between initiation of the reset and the assertion of the RSTOUT pin.

Table 6 gives the power/ground segmentation of the MPC563x MCU. Each segment provides the power and ground for the given set of I/O pins, and can be powered by any of the allowed voltages regardless of the power on the other segments.

Table 6. MPC563x Power/Ground Segmentation

Power Segment		144-LQFP Pin Number	176-LQFP Pin Number	208-BGA Pin Number	Voltage Range[1]	I/O Pins Powered by Segment
VDDA0		6	6	B11	5.0 V	AN[0:7], AN[9], AN[11], AN[16:18], AN[21:25], AN[27:28], AN[30:37], AN38, AN39, VRL, REFBYPC, VRH
VDDE5		—	—	T13	1.8 V – 3.3 V	CLKOUT
VDDEH1 (a,b)		24, 34	31, 41	K4	3.3 V – 5.0 V	PCKCFG[2], eTPU_A[0:31], eMIOS[0:2]

Table 6. MPC563x Power/Ground Segmentation (continued)

Power Segment		144-LQFP Pin Number	176-LQFP Pin Number	208-BGA Pin Number	Voltage Range[1]	I/O Pins Powered by Segment
VDDEH6 (a,b)		78, 93	95, 110	F13	3.3 V – 5.0 V	$\overline{\text{RESET}}$, $\overline{\text{RSTOUT}}$, WKPCFG, BOOTCFG1, PLLREF, SCK_B, PCKCFG[0], CAN_A_TX, CAN_A_RX, CAN_C_TX, CAN_C_RX, SCI_A_TX, SCI_A_RX, SCI_B_TX, SCI_B_RX, SCK_B, SIN_B, SOUT_B, DSPI_B_PCS_B[0:5], eMIOS[4], eMIOS[8:15], eMIOS[23], XTAL, EXTAL
VDDEH7[2]		102, 113	125, 138	D12	3.3 V – 5.0 V	PCKCFG[1], MDO[0:3], $\overline{\text{EVTI}}$, $\overline{\text{EVTO}}$, MCKO, $\overline{\text{MSEO}}$[0:1], TDO, TDI, TMS, TCK, JCOMP, AN[12:15] (GPIO[98:99], GPIO[206:207])
VDDE12[3] VDDE7		—	16, 119	E13, P6	1.8 V – 3.3 V	CAL_ADDR[12:30], CAL_DATA[0:15], CAL_$\overline{\text{CS}}$[0], CAL_$\overline{\text{CS}}$[2:3], CAL_RD_$\overline{\text{WR}}$, CAL_$\overline{\text{WE}}$[0:1], CAL_$\overline{\text{OE}}$, CAL_$\overline{\text{TS}}$, ALT_MCKO, ALT_$\overline{\text{EVTO}}$, NEXUSCFG

1 These are nominal voltages. All VDDE and VDDEH voltages are –5%, +10% (VDDE 1.62 V to 3.6 V, VDDEH 3.0 V to 5.5 V). VDDA is +5%, –10%.

2 The VDDEH7 segment may be powered from 3.0 V to 5.0 V for mux address or SSI functions, but must meet the VDDA specifications of 4.5 V to 5.25 V for analog input function.

3 In the calibration package this signal is named VDDE12; it is named VDDE7 in all other packages.

4 Electrical characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5634M series of MCUs.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol "CC" for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol "SR" for System Requirement is included in the Symbol column.

4.1 Parameter classification

The electrical parameters shown in this document are guaranteed by various methods. To provide a better understanding, the classifications listed in Table 7 are used and the parameters are tagged accordingly in the tables. Note that only controller characteristics ("CC") are classified. System requirements ("SR") are operating conditions that must be provided to ensure normal device operation.

Table 7. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled "C" in the parameter tables where appropriate.

4.2 Maximum ratings

Table 8. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Value		Unit
				min	max	
V_{DD}	SR	1.2 V core supply voltage[2]		– 0.3	1.32	V
V_{FLASH}	SR	Flash core voltage[3,4]		– 0.3	3.6	V
V_{STBY}	SR	SRAM standby voltage[5]		– 0.3	5.5	V
V_{DDPLL}	SR	Clock synthesizer voltage		– 0.3	1.32	V
V_{RC33}[6]	SR	Voltage regulator control input voltage[4]		– 0.3	3.6	V

Table 8. Absolute maximum ratings[1] (continued)

Symbol		Parameter	Conditions	Value		Unit
				min	max	
V_{DDA}	SR	Analog supply voltage[5]	Reference to V_{SSA}	– 0.3	5.5	V
V_{DDE}	SR	I/O supply voltage[4,7]		– 0.3	3.6	V
V_{DDEH}	SR	I/O supply voltage[5]		– 0.3	5.5	V
V_{IN}	SR	DC input voltage[8]	V_{DDEH} powered I/O pads	–1.0[9]	V_{DDEH} + 0.3 V[10]	V
			V_{DDE} powered I/O pads	–1.0[10]	V_{DDE} + 0.3 V[11]	
			V_{DDA} powered I/O pads	–1.0	V_{DDA} + 0.3 V	
V_{DDREG}	SR	Voltage regulator supply voltage[6]		– 0.3	5.5	V
V_{RH}	SR	Analog reference high voltage	Reference to VRL	– 0.3	5.5	V
$V_{SS} – V_{SSA}$	SR	V_{SS} differential voltage		– 0.1	0.1	V
$V_{RH} – V_{RL}$	SR	V_{REF} differential voltage[6]		– 0.3	5.5	V
$V_{RL} – V_{SSA}$	SR	VRL to V_{SSA} differential voltage		– 0.3	0.3	V
$V_{SSPLL} – V_{SS}$	SR	V_{SSPLL} to V_{SS} differential voltage		– 0.1	0.1	V
I_{MAXD}	SR	Maximum DC digital input current[12]	Per pin, applies to all digital pins	– 3	3	mA
I_{MAXA}	SR	Maximum DC analog input current[13]	Per pin, applies to all analog pins	—	5	mA
T_J	SR	Maximum operating temperature range[14] – die junction temperature		– 40.0	150.0	°C
T_{STG}	SR	Storage temperature range		– 55.0	150.0	°C
T_{SDR}	SR	Maximum solder temperature[15]		—	260.0	°C
MSL	SR	Moisture sensitivity level[16]		—	3	—

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Allowed 2 V for 10 hours cumulative time, remaining time at 1.2 V +10%.

3 The V_{FLASH} supply is connected to V_{RC33} in the package substrate. This specification applies to calibration package devices only.

4 Allowed 5.3 V for 10 hours cumulative time, remaining time at 3.3 V +10%.

5 Allowed 6.8 V for 10 hours cumulative time, remaining time at 5 V +10%.

6 The pin named as V_{RC33} is internally connected to the pads V_{FLASH} and V_{RC33} in the 144 LQFP package. These limits apply when the internal regulator is disabled and V_{RC33} power is supplied externally.

7 All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}, or V_{DDEH}.

[8] AC signal overshoot and undershoot of up to 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).

[9] Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met.

[10] Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.

[11] Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.

[12] Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

[13] Total injection current for all analog input pins must not exceed 15 mA.

[14] Lifetime operation at these specification limits is not guaranteed.

[15] Solder profile per CDF-AEC-Q100.

[16] Moisture sensitivity per JEDEC test method A112.

4.3 Thermal characteristics

Table 9. Thermal characteristics for 144-pin LQFP

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[1]	Single layer board – 1s	43	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board – 2s2p	35	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Ambient (@200 ft/min)[2]	Single layer board –1s	34	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Ambient (@200 ft/min)[2]	Four layer board – 2s2p	29	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board[2]		22	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case (Top)[3]		8	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection[4]		2	°C/W

[1] Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

[2] Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

[3] Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

[4] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 10. Thermal characteristics for 176-pin LQFP[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Single layer board - 1s	38	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board - 2s2p	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	@200 ft./min., single layer board - 1s	30	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	@200 ft./min., four layer board - 2s2p	25	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board[3]		20	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case[4]		5	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection[5]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 11. Thermal characteristics for 208-pin MAPBGA[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection[2,3]	One layer board - 1s	39	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-ambient natural convection[2,4]	Four layer board - 2s2p	24	°C/W
$R_{\theta JA}$	CC	D	Junction-to-ambient (@200 ft/min)[2,4]	Single layer board	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-ambient (@200 ft/min)[2,4]	Four layer board 2s2p	20	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[5]	Four layer board - 2s2p	13	°C/W
$R_{\theta JC}$	CC	D	Junction-to-case[6]		6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top natural convection[7]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

[7] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.3.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)
$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)
P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} * P_D) \quad \textit{Eqn. 2}$$

where:

T_B = board temperature for the package perimeter (^oC)
$R_{\theta JB}$ = junction-to-board thermal resistance ($^oC/W$) per JESD51-8S
P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 3}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)
$R_{\theta JC}$ = junction-to-case thermal resistance ($^oC/W$)
$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 4}$$

where:

T_T = thermocouple temperature on top of the package (^oC)
Ψ_{JT} = thermal characterization parameter ($^oC/W$)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134
USA
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at http://www.jedec.org.

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- G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications”, Electronic Packaging and Production, pp. 53-58, March 1998.

- B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

4.4 Electromagnetic Interference (EMI) characteristics

Table 12. EMI testing specifications[1]

Symbol	Parameter	Conditions	f_{OSC}/f_{BUS}	Frequency	Level (Typ)	Unit
Radiated Emissions	V_{EME}	Device Configuration, test conditions and EM testing per standard IEC61967-2; Supply Voltage = 5.0V DC, Ambient Temperature = 25°C, Worst-case Orientation	Oscillator Frequency = 8 MHz; System Bus Frequency = 80 MHz; No PLL Frequency Modulation	150 kHz – 50 MHz	26	dBμV
				50–150 MHz	24	
				150–500 MHz	24	
				500–1000 MHz	21	
				IEC Level	K	—
			Oscillator Frequency = 8 MHz; System Bus Frequency = 80 MHz; 1% PLL Frequency Modulation	150 kHz – 50 MHz	20	dBμV
				50–150 MHz	19	
				150–500 MHz	14	
				500–1000 MHz	7	
				IEC Level	L	—

1 IEC Classification Level: L = 24dBuV; K = 30dBuV.

4.5 Electromagnetic static discharge (ESD) characteristics

Table 13. ESD ratings[1,2]

Symbol		Parameter	Conditions	Value	Unit
—	SR	ESD for Human Body Model (HBM)	—	2000	V
R1	SR	HBM circuit description	—	1500	Ω
C	SR		—	100	pF
—	SR	ESD for field induced charge Model (FCDM)	All pins	500	V
			Corner pins	750	
—	SR	Number of pulses per pin	Positive pulses (HBM)	1	—
			Negative pulses (HBM)	1	—
—	SR	Number of pulses	—	1	—

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.”

4.6 Power Management Control (PMC) and Power On Reset (POR) electrical specifications

Table 14. PMC Operating conditions and external regulators supply voltage

ID	Name		C	Parameter	Min	Typ	Max	Unit
1	Jtemp	SR	—	Junction temperature	–40	27	150	°C
2	Vddreg	SR	—	PMC 5 V supply voltage VDDREG	4.75[1]	5	5.25	V
3	Vdd	SR	—	Core supply voltage 1.2 V VDD when external regulator is used without disabling the internal regulator (PMC unit turned on, LVI monitor active)[2]	1.26[3]	1.3	1.32	V
3a	—	SR	—	Core supply voltage 1.2 V VDD when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	1.14	1.2	1.32	V
4	Ivdd	SR	—	Voltage regulator core supply maximum DC output current[4]	400	—	—	mA
5	Vdd33	SR	—	Regulated 3.3 V supply voltage when external regulator is used without disabling the internal regulator (PMC unit turned-on, internal 3.3 V regulator enabled, LVI monitor active)[5]	3.3	3.45	3.6	V
5a	—	SR	—	Regulated 3.3 V supply voltage when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	3	3.3	3.6	V
6	—	SR	—	Voltage regulator 3.3 V supply maximum required DC output current	80	—	—	mA

1 During start up operation the minimum required voltage to come out of reset state is 4.6 V.

2 An internal regulator controller can be used to regulate core supply.

3 The minimum supply required for the part to exit reset and enter in normal run mode is 1.28 V.

4 The onchip regulator can support a minimum of 400 mA although the worst case core current is 180 mA.

5 An internal regulator can be used to regulate 3.3 V supply.

Table 15. PMC electrical characteristics

ID	Name		C	Parameter	Min	Typ	Max	Unit	Notes
1	Vbg	CC	C	Nominal bandgap voltage reference	—	1.219	—	V	
1a	—	CC	P	Untrimmed bandgap reference voltage	Vbg–7%	Vbg	Vbg+6%	V	
1b	—	CC	P	Trimmed bandgap reference voltage (5 V, 27 °C)[1]	Vbg–10mV	Vbg	Vbg+10mV	V	
1c	—	CC	C	Bandgap reference temperature variation	—	100	—	ppm /°C	

Table 15. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Min	Typ	Max	Unit	Notes
1d	—	CC	C	Bandgap reference supply voltage variation	—	3000	—	ppm /V	
2	Vdd	CC	C	Nominal VDD core supply internal regulator target DC output voltage[2]	—	1.28	—	V	
2a	—	CC	P	Nominal VDD core supply internal regulator target DC output voltage variation at power-on reset	Vdd – 6%	Vdd	Vdd + 10%	V	
2b	—	CC	P	Nominal VDD core supply internal regulator target DC output voltage variation after power-on reset	Vdd – 10[3]	Vdd	Vdd + 3%	V	
2c	—	CC	C	Trimming step Vdd	—	20	—	mV	
2d	Ivrcctl	CC	C	Voltage regulator controller for core supply maximum DC output current	20	—	—	mA	
3	Lvi1p2	CC	C	Nominal LVI for rising core supply[4,5]	—	1.160	—	V	
3a	—	CC	C	Variation of LVI for rising core supply at power-on reset[5,6]	1.120	1.200	1.280	V	
3b	—	CC	C	Variation of LVI for rising core supply after power-on reset[5,6]	Lvi1p2–3%	Lvi1p2	Lvi1p2+3%	V	
3c	—	CC	C	Trimming step LVI core supply[5]	—	20	—	mV	
3d	Lvi1p2_h	CC	C	LVI core supply hysteresis[5]	—	40	—	mV	
4	Por1.2V_r	CC	C	POR 1.2 V rising	—	0.709	—	V	
4a	—	CC	C	POR 1.2 V rising variation	Por1.2V_r– 35%	Por1.2V_r	Por1.2V_r+ 35%	V	
4b	Por1.2V_f	CC	C	POR 1.2 V falling	—	0.638	—	V	
4c	—	CC	C	POR 1.2 V falling variation	Por1.2V_f– 35%	Por1.2V_f	Por1.2V_f+ 35%	V	
5	Vdd33	CC	C	Nominal 3.3 V supply internal regulator DC output voltage	—	3.39	—	V	
5a	—	CC	P	Nominal 3.3 V supply internal regulator DC output voltage variation at power-on reset[6]	Vdd33 – 8.5%	Vdd33	Vdd3 + 7%	V	

Table 15. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Min	Typ	Max	Unit	Notes
5b	—	CC	P	Nominal 3.3 V supply internal regulator DC output voltage variation after power-on reset	Vdd33 – 7.5%	Vdd33	Vdd33 + 7%	V	With internal load up to Idd3p3
5c	—	CC	D	Voltage regulator 3.3 V output impedance at maximum DC load	—	—	2	Ω	
5d	Idd3p3	CC	P	Voltage regulator 3.3 V maximum DC output current	80	—	—	mA	
5e	Vdd33 ILim[6]	CC	C	Voltage regulator 3.3 V DC current limit	—	130	—	mA	
6	Lvi3p3	CC	C	Nominal LVI for rising 3.3 V supply[5]	—	3.090	—	V	The Lvi3p3 specs are also valid for the Vddeh LVI
6a	—	CC	C	Variation of LVI for rising 3.3 V supply at power-on reset[5]	Lvi3p3–6%	Lvi3p3	Lvi3p3+6%	V	See note [7]
6b	—	CC	C	Variation of LVI for rising 3.3 V supply after power-on reset[5]	Lvi3p3–3%	Lvi3p3	Lvi3p3+3%	V	See note 7
6c	—	CC	C	Trimming step LVI 3.3 V[5]	—	20	—	mV	
6d	Lvi3p3_h	CC	C	LVI 3.3 V hysteresis[5]	—	60	—	mV	
7	Por3.3V_r	CC	C	Nominal POR for rising 3.3 V supply	—	2.07	—	V	The 3.3 V POR specs are also valid for the Vddeh POR
7a	—	CC	C	Variation of POR for rising 3.3 V supply	Por3.3V_r–35%	Por3.3V_r	Por3.3V_r+35%	V	
7b	Por3.3V_f	CC	C	Nominal POR for falling 3.3 V supply	—	1.95	—	V	
7c	—	CC	C	Variation of POR for falling 3.3 V supply	Por3.3V_f–35%	Por3.3V_f	Por3.3V_f+35%	V	
8	Lvi5p0	CC	C	Nominal LVI for rising 5 V VDDREG supply[5]	—	4.290	—	V	
8a	—	CC	C	Variation of LVI for rising 5 V VDDREG supply at power-on reset[5]	Lvi5p0–6%	Lvi5p0	Lvi5p0+6%	V	
8b	—	CC	C	Variation of LVI for rising 5 V VDDREG supply power-on reset[5]	Lvi5p0–3%	Lvi5p0	Lvi5p0+3%	V	
8c	—	CC	C	Trimming step LVI 5 V[5]	—	20	—	mV	

Table 15. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Min	Typ	Max	Unit	Notes
8d	Lvi5p0_h	CC	C	LVI 5 V hysteresis[5]	—	60	—	mV	
9	Por5V_r	CC	C	Nominal POR for rising 5 V VDDREG supply	—	2.67	—	V	
9a	—	CC	C	Variation of POR for rising 5 V VDDREG supply	Por5V_r – 35%	Por5V_r	Por5V_r + 50%	V	
9b	Por5V_f	CC	C	Nominal POR for falling 5 V VDDREG supply	—	2.47	—	V	
9c	—	CC	C	Variation of POR for falling 5 V VDDREG supply	Por5V_f – 35%	Por5V_f	Por5V_f + 50%	V	

1 The limits will be reviewed after data collection from 3 different lots in a full production environment.

2 Using external ballast transistor.

3 Min range is extended to 10% since Lvi1p2 is reprogrammed from 1.2 V to 1.16 V after power-on reset.

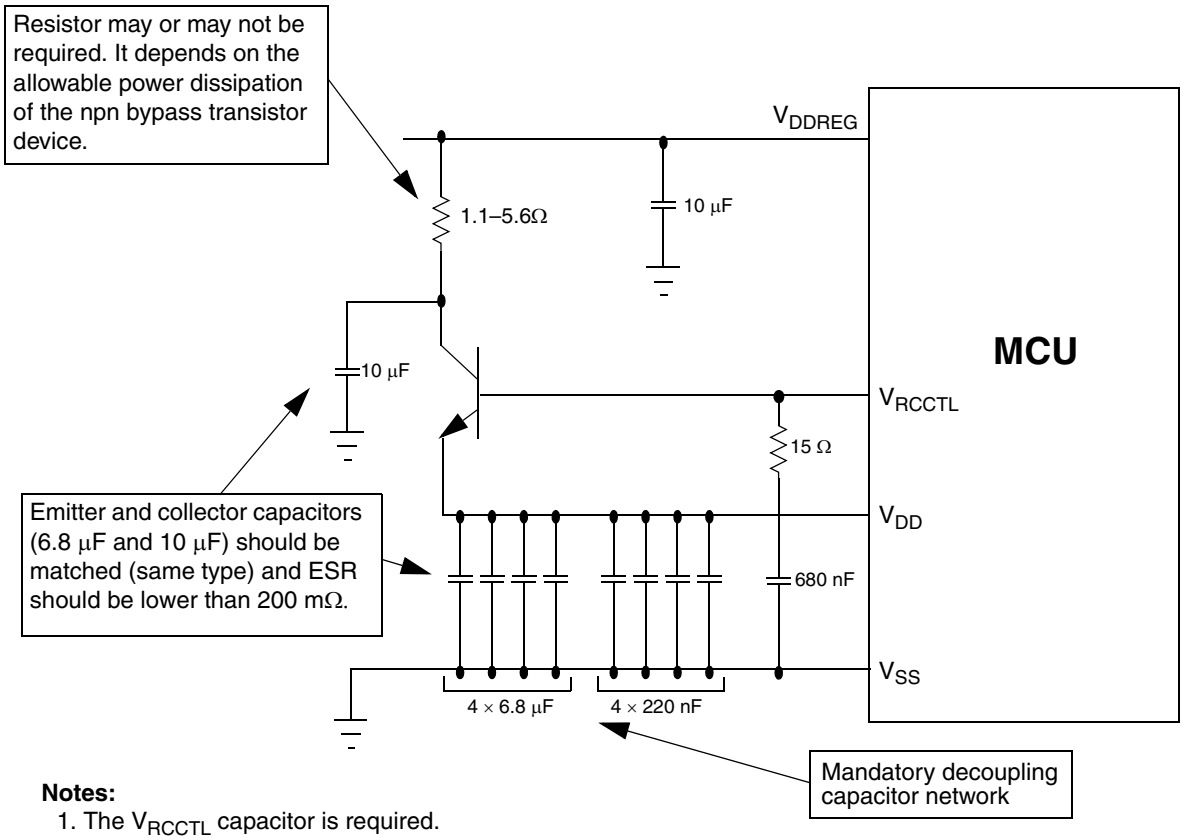
4 LVI for falling supply is calculated as LVI rising - LVI hysteresis.

5 The internal voltage regulator can be disabled by tying the VDDREG pin to ground. When the internal voltage regulator is disabled, the LVI specifications are not applicable because all LVI monitors are disabled. POR specifications remain valid when the internal voltage regulator is disabled as long as VDDEH and VDD33 supplies are within the required ranges.

6 This parameter is the “inrush” current of the internal 3.3 V regulator when it is turned on. This spec. is the current at which the regulator will go into current limit mode.

7 Lvi3p3 tracks DC target variation of internal Vdd33 regulator. Minimum and maximum Lvi3p3 correspond to minimum and maximum Vdd33 DC target respectively.

4.6.1 Regulator example



Notes:
1. The V_{RCCTL} capacitor is required.
2. The bypass transistor MUST be operated out of its saturation region.

Figure 7. Core voltage regulator controller external components preferred configuration

4.6.2 Recommended power transistors

The following NPN transistors are recommended for use with the on-chip voltage regulator controller: ON Semiconductor™ BCP68T1 or NJD2873 as well as Philips Semiconductor™ BCP68. The collector of the external transistor is preferably connected to the same voltage supply source as the output stage of the regulator.

Table 16. Recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE} (β)	DC current gain (Beta)	60 – 550	—
P_D	Absolute minimum power dissipation	>1.0 (1.5 preferred)	W
I_{CMaxDC}	Minimum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage	200–600[1]	mV
V_{BE}	Base-to-emitter voltage	0.4–1.0	V

[1] Adjust resistor at bipolar transistor collector for 3.3 V/5.0 V to avoid VCE < VCE_{SAT}

4.7 Power up/down sequencing

There is no power sequencing required among power sources during power up and power down, in order to operate within specification but use of the following sequence is strongly recommended when the internal regulator is bypassed:

5 V → 3.3 V and 1.2 V

This is also the normal sequence when the internal regulator is enabled.

Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies according to table Table 17 for all pins with fast pads and Table 18 for all pins with medium, slow and multi-voltage pads.[1]

Table 17. Power sequence pin states for fast pads

V_{DDE}	V_{RC33}	V_{DD}	Fast (pad_fc)
LOW	X	X	LOW
V_{DDE}	LOW	X	HIGH
V_{DDE}	V_{RC33}	LOW	HIGH IMPEDANCE
V_{DDE}	V_{RC33}	V_{DD}	FUNCTIONAL

Table 18. Power sequence pin states for medium, slow and multi-voltage pads

V_{DDEH}	V_{DD}	Medium (pad_msr_hv) Slow (pad_ssr_hv) Multi-voltage (pad_multv_hv)
LOW	X	LOW
V_{DDEH}	LOW	HIGH IMPEDANCE
V_{DDEH}	V_{DD}	FUNCTIONAL

1.If an external 3.3 V external regulator is used to supply current to the 1.2 V pass transistor and this supply also supplies current for the other 3.3 V supplies, then the 5V supply must always be greater than or equal to the external 3.3 V supply.

4.8 DC electrical specifications

Table 19. DC electrical specifications[1]

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
V_{DD}	SR	—	Core supply voltage	—	1.14	—	1.32	V
V_{DDE}	SR	—	I/O supply voltage	—	1.62	—	3.6[3]	V
V_{DDEH}	SR	—	I/O supply voltage	—	3.0	—	5.25	V
V_{RC33}	SR	—	3.3 V external voltage[4]	—	3.0	—	3.6	V
V_{DDA}	SR	—	Analog supply voltage	—	4.75[5]	—	5.25	V
V_{INDC}	SR	—	Analog input voltage[6]	—	V_{SSA} – 0.3	—	V_{DDA}+0.3	V
$V_{SS} – V_{SSA}$	SR	—	V_{SS} differential voltage	—	–100	—	100	mV
V_{RL}	SR	—	Analog reference low voltage	—	V_{SSA}	—	V_{SSA}+0.1	V
$V_{RL} – V_{SSA}$	SR	—	V_{RL} differential voltage	—	–100	—	100	mV
V_{RH}	SR	—	Analog reference high voltage	—	V_{DDA} – 0.1	—	V_{DDA}	V
$V_{RH} – V_{RL}$	SR	—	V_{REF} differential voltage	—	4.75	—	5.25	V
V_{DDF}	SR	—	Flash operating voltage [7]	—	1.14	—	1.32	V
V_{FLASH}[8]	SR	—	Flash read voltage	—	3.0	—	3.6	V
V_{STBY}	SR	—	SRAM standby voltage	Unregulated mode	0.95	—	1.2	V
				Regulated mode	2.0	—	5.5	
V_{DDREG}	SR	—	Voltage regulator supply voltage[9]	—	4.75	—	5.25	V
V_{DDPLL}	SR	—	Clock synthesizer operating voltage	—	1.14	—	1.32	V
$V_{SSPLL} – V_{SS}$	SR	—	V_{SSPLL} to V_{SS} differential voltage	—	–100	—	100	mV
V_{IL_S}	CC	C	Slow/medium pad I/O input low voltage	Hysteresis enabled	V_{SS}–0.3	—	0.35*V_{DDEH}	V
		P		hysteresis disabled	V_{SS}–0.3	—	0.40*V_{DDEH}	
V_{IL_F}	CC	C	Fast pad I/O input low voltage	Hysteresis enabled	V_{SS}–0.3	—	0.35*V_{DDE}	V
		P		hysteresis disabled	V_{SS}–0.3	—	0.40*V_{DDE}	

Table 19. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
V_{IL_LS}	CC	C	Multi-voltage pad I/O input low voltage in low-swing mode[10,11,12,13]	Hysteresis enabled	V_{SS}–0.3	—	0.8	V
		P		Hysteresis disabled	V_{SS}–0.3	—	1.1	
V_{IL_HS}	CC	C	Multi-voltage pad I/O input low voltage in high-swing mode	Hysteresis enabled	V_{SS}–0.3	—	0.35 V_{DDEH}	V
		P		Hysteresis disabled	V_{SS}–0.3	—	0.4 V_{DDEH}	
V_{IH_S}	CC	C	Slow/medium pad I/O input high voltage	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH}+0.3	V
		P		hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH}+0.3	
V_{IH_F}	CC	C	Fast pad I/O input high voltage	Hysteresis enabled	0.65 V_{DDE}	—	V_{DDE}+0.3	V
		P		hysteresis disabled	0.55 V_{DDE}	—	V_{DDE}+0.3	
V_{IH_LS}	CC	C	Multi-voltage pad I/O input high voltage in low-swing mode[10,11,12,13,14]	Hysteresis enabled	2.5	—	V_{DDEH}+0.3	V
		P		Hysteresis disabled	2.2	—	V_{DDEH}+0.3	
V_{IH_HS}	CC	C	Multi-voltage pad I/O input high voltage in high-swing mode[15]	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH}+0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH}+0.3	
V_{OL_S}	CC	P	Slow/medium multi-voltage pad I/O output low voltage[18,16]	—	—	—	0.2*V_{DDEH}	V
V_{OL_F}	CC	P	Fast pad I/O output low voltage[17,18]	—	—	—	0.2*V_{DDE}	V
V_{OL_LS}	CC	P	Multi-voltage pad I/O output low voltage in low-swing mode[10,11,12,13,17]	I_{OL} = 2 mA	—	—	0.6	V
V_{OL_HS}	CC	P	Multi-voltage pad I/O output low voltage in high-swing mode[17]	—	—	—	0.2 V_{DDEH}	V
V_{OH_S}	CC	P	Slow/medium pad I/O output high voltage[18,16]	—	0.8 V_{DDEH}	—	—	V
V_{OH_F}	CC	P	Fast pad I/O output high voltage[17,18]	—	0.8 V_{DDE}	—	—	V

Table 19. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode[10,11,12,13,17]	I_{OH_LS} = 0.5 mA Min V_{DDEH} = 4.75 V	2.1	—	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode[17]	—	0.8 V_{DDEH}	—	—	V
V_{HYS_S}	CC	C	Slow/medium/multi-voltage I/O input hysteresis	—	0.1 * V_{DDEH}	—	—	V
V_{HYS_F}	CC	C	Fast I/O input hysteresis	—	0.1 * V_{DDE}	—	—	V
V_{HYS_LS}	CC	C	Low-Swing-Mode Multi-Voltage I/O Input Hysteresis	hysteresis enabled	0.25	—	—	V
I_{DD}+I_{DDPLL}[19]	CC	P	Operating current 1.2 V supplies	V_{DD} = 1.32 V, 80 MHz	—	—	195	mA
	CC	P		V_{DD} = 1.32 V, 60 MHz	—	—	135	
	CC	P		V_{DD} = 1.32 V, 40 MHz	—	—	98	
I_{DDSTBY}	CC	T	Operating current 1 V supplies	T_J = 25 °C	—	—	80	µA
	CC	T		T_J = 55 °C	—	—	100	µA
$I_{DDSTBY150}$	CC	P	Operating current	T_J=150 °C	—	—	700	µA
I_{DDSLOW} I_{DDSTOP}	CC	P	V_{DD} low-power mode operating current @ 1.32 V	Slow mode[20]	—	—	50	mA
		C		Stop mode[21]	—	—	50	
I_{DD33}	CC	T	Operating current 3.3 V supplies @ 80 MHz	V_{RC33}[4,22]	—	—	70	mA
I_{DDA} I_{REF} I_{DDREG}	CC	P	Operating current 5.0 V supplies @ 80 MHz	V_{DDA}	—	—	30	mA
		P		Analog reference supply current	—	—	1.0	
		C		V_{DDREG}	—	—	70	

Table 19. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
I_{DDH1} I_{DDH6} I_{DDH7} I_{DD7} I_{DDH9} I_{DD12}	CC	D	Operating current V_{DDE}[23] supplies @ 80 MHz	V_{DDEH1}	—	—	See note [23]	mA
		D		V_{DDEH6}	—	—		
		D		V_{DDEH7}	—	—		
		D		V_{DDE7}	—	—		
		D		V_{DDEH9}	—	—		
		D		V_{DDE12}	—	—		
I_{ACT_S}	CC	C	Slow/medium I/O weak pull up/down current[24]	3.0 V – 3.6 V	15	—	95	µA
		P		4.75 V – 5.25 V	35	—	200	
I_{ACT_F}	CC	D	Fast I/O weak pull up/down current[24]	1.62 V – 1.98 V	36	—	120	µA
		D		2.25 V – 2.75 V	34	—	139	
		D		3.0 V – 3.6 V	42	—	158	
$I_{ACT_MV_PU}$	CC	C	Multi-voltage pad weak pullup current	V_{DDEH}= 3.0–3.6 V[10], pad_multv_hv, all process corners, high swing mode only	10	—	75	µA
		P		4.75 V – 5.25 V	25	—	200	
$I_{ACT_MV_PD}$	CC	C	Multivoltage pad weak pulldown current	V_{DDEH}= 3.0–3.6 V[10], pad_multv_hv, all process corners, high swing mode only	10	—	60	µA
		P		4.75 V – 5.25 V	25	—	200	
I_{INACT_D}	CC	P	I/O input leakage current[25]	—	–2.5	—	2.5	µA
I_{IC}	CC	T	DC injection current (per pin)	—	–1.0	—	1.0	mA
I_{INACT_A}	CC	P	Analog input current, channel off, AN[0:7], AN38, AN39[26]	—	–250	—	250	nA
		P	Analog input current, channel off, all other analog pins (ANx)[26]	—	–150	—	150	

Table 19. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
C_L	CC	D	Load capacitance (fast I/O)[27]	DSC(PCR[8:9]) = 0b00	—	—	10	pF
		D		DSC(PCR[8:9]) = 0b01	—	—	20	
		D		DSC(PCR[8:9]) = 0b10	—	—	30	
		D		DSC(PCR[8:9]) = 0b11	—	—	50	
C_{IN}	CC	D	Input capacitance (digital pins)	—	—	—	7	pF
C_{IN_A}	CC	D	Input capacitance (analog pins)	—	—	—	10	pF
C_{IN_M}	CC	D	Input capacitance (digital and analog pins[28])	—	—	—	12	pF
$R_{PUPD200K}$	CC	P	Weak Pull-Up/Down Resistance[29,30] 200 kΩ Option	—	130	—	280	kΩ
$R_{PUPDMATCH}$	CC	C	200KΩ Option		–2.5		2.5	%
$R_{PUPD100K}$	CC	P	Weak Pull-Up/Down Resistance[29,30] 100 kΩ Option	—	65	—	140	kΩ
$R_{PUPDMATCH}$	CC	C	100KΩ Option		–2.5		2.5	%
R_{PUPD5K}	CC	D	Weak Pull-Up/Down Resistance[29] 5 kΩ Option	5 V ± 5% supply	1.4	—	7.5	kΩ
T_A (T_L to T_H)	SR	—	Operating temperature range - ambient (packaged)	—	–40.0	—	125.0	°C
—	SR	—	Slew rate on power supply pins	—	—	—	50	V/ms

1 These specifications are design targets and subject to change per device characterization.

2 TBD: To Be Defined.

3 V_{DDE} must be lower than V_{RC33}, otherwise there is additional leakage on pins supplied by V_{DDE}.

4 These specifications apply when V_{RC33} is supplied externally, after disabling the internal regulator (V_{DDREG} = 0).

5 ADC is functional with 4 V ≤ V_{DDA} ≤ 4.75 V but with derated accuracy. This means the ADC will continue to function at full speed with no bad behavior, but the accuracy will be degraded.

6 Internal structures hold the input voltage less than V_{DDA} + 1.0 V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.

7 The V_{DDF} supply is connected to V_{DD} in the package substrate. This specification applies to calibration package devices only.

[8] V_{FLASH} is only available in the calibration package.

[9] Regulator is functional, with derated performance, with supply voltage down to 4.0 V.

[10] Multi-voltage pads (type pad_multv_hv) must be supplied with a power supply between 4.75 V and 5.25 V.

[11] The slew rate (SRC) setting must be 0b11 when in low-swing mode.

[12] While in low-swing mode there are no restrictions in transitioning to high-swing mode.

[13] Pin in low-swing mode can accept a 5 V input.

[14] Values are pending characterization.

[15] Pin in low-swing mode can accept a 5 V input.

[16] Characterization based capability:

IOH_S = {6, 11.6} mA and IOL_S = {9.2, 17.7} mA for {slow, medium} I/O with VDDEH=4.5 V;
IOH_S = {2.8, 5.4} mA and IOL_S = {4.2, 8.1} mA for {slow, medium} I/O with VDDEH=3.0 V

[17] Characterization based capability:

IOH_F = {12, 20, 30, 40} mA and IOL_F = {24, 40, 50, 65} mA for {00, 01,10, 11} drive mode with VDDE=3.0 V;
IOH_F = {7, 13, 18, 25} mA and IOL_F = {18, 30, 35, 50} mA for {00, 01, 10, 11} drive mode with VDDE=2.25 V;
IOH_F = {3, 7, 10, 15} mA and IOL_F = {12, 20, 27, 35} mA for {00, 01, 10, 11} drive mode with VDDE=1.62 V

[18] All VOL/VOH values 100% tested with ± 2 mA load.

[19] Run mode as follows:

System clock = 40/60/80 MHz + FM 2%
Code executed from flash memory
ADC0 at 16 MHz with DMA enabled
ADC1 at 8 MHz
eMIOS pads toggle in PWM mode with a rate between 100 kHz and 500 kHz
eTPU pads toggle in PWM mode with a rate between 10 kHz and 500 kHz
CAN configured for a bit rate of 500 kHz
DSPI configured in master mode with a bit rate of 2 MHz
eSCI transmission configured with a bit rate of 100 kHz

[20] Bypass mode, system clock at 1 MHz (using system clock divider), PLL shut down, CPU running simple executive code, 4 x ADC conversion every 10 ms, 2 × PWM channels at 1 kHz, all other modules stopped.

[21] Bypass mode, system clock at 1 MHz (using system clock divider), CPU stopped, PIT running, all other modules stopped.

[22] When using the internal regulator only, a bypass capacitor should be connected to this pin. External circuits should not be powered by the internal regulator. The internal regulator can be used as a reference for an external debugger.

[23] Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See Table 20 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

[24] Absolute value of current, measured at V_{IL} and V_{IH}.

[25] Weak pull up/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to pad types: fast (pad_fc).

[26] Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types: pad_a and pad_ae.

[27] Applies to CLKOUT, external bus pins, and Nexus pins.

[28] Applies to the FCK, SDI, SDO, and $\overline{SDS}$ pins.

[29] This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics.

[30] When the pull-up and pull-down of the same nominal 200 KΩ or 100 KΩ value are both enabled, assuming no interference from external devices, the resulting pad voltage will be 0.5*V_{DDE} ± 2.5%

4.9 I/O Pad current specifications

NOTE

MPC5634M devices use two sets of I/O pads (5 V and 3.3 V). See Table 3 and Table 4 in Section 3.6, "Signal summary, for the pad type associated with each signal.

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 20 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 20.

Table 20. I/O pad average I_{DDE} specifications[1]

Pad Type	Symbol		C	Period (ns)	Load[2] (pF)	V_{DDE} (V)	Drive/Slew Rate Select	I_{DDE} Avg (mA)[3]	I_{DDE} RMS (mA)
Slow	$I_{DRV_SSR_HV}$	CC	D	37	50	5.25	11	9	—
		CC	D	130	50	5.25	01	2.5	—
		CC	D	650	50	5.25	00	0.5	—
		CC	D	840	200	5.25	00	1.5	—
Medium	$I_{DRV_MSR_HV}$	CC	D	24	50	5.25	11	14	—
		CC	D	62	50	5.25	01	5.3	—
		CC	D	317	50	5.25	00	1.1	—
		CC	D	425	200	5.25	00	3	—
Fast	I_{DRV_FC}	CC	D	10	50	3.6	11	22.7	68.3
		CC	D	10	30	3.6	10	12.1	41.1
		CC	D	10	20	3.6	01	8.3	27.7
		CC	D	10	10	3.6	00	4.44	14.3
		CC	D	10	50	1.98	11	12.5	31
		CC	D	10	30	1.98	10	7.3	18.6
		CC	D	10	20	1.98	01	5.42	12.6
		CC	D	10	10	1.98	00	2.84	6.4
MultiV (High Swing Mode)	$I_{DRV_MULTV_HV}$	CC	D	15	50	5.25	11	21.2[4]	—
		CC	D	30	50	5.25	10	—[5]	—
		CC	D	50	50	5.25	01	6.2[4]	—
		CC	D	300	50	5.25	00	1.1[4]	—
		CC	D	300	200	5.25	00	4.0[4]	—
MultiV (Low Swing Mode)	$I_{DRV_MULTV_HV}$	CC	D	15	30	5.25	11	20.2[6]	—
		CC	D	30	30	5.25	11	NA	—

1 Numbers from simulations at best case process, 150 °C.

2 All loads are lumped.

3 Average current is for pad configured as output only.

[4] Ratio from 5.5 V pad spec to 5.25 V data sheet.
[5] Not specified.
[6] Low swing mode is not a strong function of V_{DDE}.

4.9.1 I/O pad VRC33 current specifications

The power consumption of the VRC33 supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all output pin V_{RC33} currents for all I/O segments. The output pin V_{RC33} current can be calculated from Table 21 based on the voltage, frequency, and load on all medium, slow, and multv_hv pins. The output pin VRC33 current can be calculated from Table 22 based on the voltage, frequency, and load on all fast pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 21 and Table 22.

Table 21. I/O pad V_{RC33} average I_{DDE} specifications[1]

Pad Type	Symbol		C	Period (ns)	Load[2] (pF)	Slew Rate Select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Slow	$I_{DRV_SSR_HV}$	CC	D	100	50	11	0.8	235.7
		CC	D	200	50	01	0.04	87.4
		CC	D	800	50	00	0.06	47.4
		CC	D	800	200	00	0.009	47
Medium	$I_{DRV_MSR_HV}$	CC	D	40	50	11	2.75	258
		CC	D	100	50	01	0.11	76.5
		CC	D	500	50	00	0.02	56.2
		CC	D	500	200	00	0.01	56.2
MultiV[3] (High Swing Mode)	$I_{DRV_MULTV_HV}$	CC	D	40	50	11	2.75	258
		CC	D	100	50	01	0.11	76.5
		CC	D	500	50	00	0.02	56.2
		CC	D	500	200	00	0.01	56.2
MultiV[4] (Low Swing Mode)	$I_{DRV_MULTV_HV}$	CC	D	40	30	11	2.75	258
		CC	D	100	30	11	0.11	76.5
		CC	D	500	30	11	0.02	56.2
		CC	D	500	30	11	0.01	56.2

[1] These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.
[2] All loads are lumped.
[3] Average current is for pad configured as output only.
[4] In low swing mode, multi-voltage pads (pad_multv_hv) must operate in highest slew rate setting.

Table 22. V_{RC33} pad average DC current[1]

Pad Type	Symbol		C	Period (ns)	Load[2] (pF)	V_{RC33} (V)	V_{DDE} (V)	Drive Select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Fast	I_{DRV_FC}	CC	D	10	50	3.6	3.6	11	2.35	6.12
		CC	D	10	30	3.6	3.6	10	1.75	4.3
		CC	D	10	20	3.6	3.6	01	1.41	3.43
		CC	D	10	10	3.6	3.6	00	1.06	2.9
		CC	D	10	50	3.6	1.98	11	1.75	4.56
		CC	D	10	30	3.6	1.98	10	1.32	3.44
		CC	D	10	20	3.6	1.98	01	1.14	2.95
		CC	D	10	10	3.6	1.98	00	0.95	2.62

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

2 All loads are lumped.

4.9.2 LVDS pad specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol which is an enhanced feature of the DSPI module. The LVDS pads are compliant with LVDS specifications and support data rates up to 50 MHz.

Table 23. DSPI LVDS pad specification [1, 2]

#	Characteristic	Symbol	C		Condition	Min. Value	Typ. Value	Max. Value	Unit
Data Rate									
4	Data Frequency	$F_{LVDSCLK}$	CC	D			50		MHz
Driver Specs									
5	Differential output voltage	V_{OD}[3]	CC	P	SRC=0b00 or 0b11	150		430	mV
			CC	P	SRC=0b01	90		340	
			CC	P	SRC=0b10	155		480	
6	Common mode voltage (LVDS), V_{OS}	V_{OS}[3]	CC	P		0.8	1.2	1.6	V
7	Rise/Fall time	T_R/T_F	CC	D			2		ns
8	Propagation delay (Low to High)	T_{PLH}	CC	D			4		ns
9	Propagation delay (High to Low)	T_{PHL}	CC	D			4		ns
10	Delay (H/L), sync Mode	t_{PDSYNC}	CC	D			4		ns
11	Delay, Z to Normal (High/Low)	T_{DZ}	CC	D			500		ns

Table 23. DSPI LVDS pad specification [1, 2] (continued)

12	Diff Skew ltphla-tplhbl or ltplhb-tphlal	T_{SKEW}	CC	D				0.5	ns
Termination									
13	Trans. Line (differential Zo)		CC	D		95	100	105	Ω
14	Temperature		CC	D		–40		150	°C

1 These are typical values that are estimated from simulation.

2 These specifications are subject to change per device characterization.

3 Preliminary target values. Actual specifications to be determined.

4.10 Oscillator and PLLMRFM electrical characteristics

Table 24. PLLMRFM electrical specifications[1]

(V_{DDPLL} =1.14 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)

Symbol		C	Parameter		Conditions	Value		Unit
						min	max	
$f_{ref_crystal}$ f_{ref_ext}	CC	D	PLL reference frequency range[2]		Crystal reference	4	20	MHz
		C			External reference	4	80	
f_{pll_in}	CC	P	Phase detector input frequency range (after pre-divider)		—	4	16	MHz
f_{vco}	CC	P	VCO frequency range[3]		—	256	512	MHz
f_{sys}	CC	C	On-chip PLL frequency[2]		—	16	80	MHz
f_{sys}	CC	T	System frequency in bypass mode[4]		Crystal reference	4	20	MHz
		P			External reference	0	80	
t_{CYC}	CC	D	System clock period		—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	CC	D	Loss of reference frequency window[5]		Lower limit	1.6	3.7	MHz
		D			Upper limit	24	56	
f_{SCM}	CC	P	Self-clocked mode frequency [6,7]		—	1.2	75	MHz
C_{JITTER}	CC	T	CLKOUT period jitter[8,9,10,11]	Peak-to-peak (clock edge to clock edge)	f_{SYS} maximum	–5	5	% f_{CLKOUT}
		T		Long-term jitter (avg. over 2 ms interval)		–6	6	ns
t_{cst}	CC	T	Crystal start-up time [12, 13]		—	—	10	ms
V_{IHEXT}	CC	T	EXTAL input high voltage		Crystal Mode[14], 0.8 ≤ Vxtal ≤ 1.5V[15]	Vxtal + 0.4	—	V
		T			External Reference[14, 16]	V_{RC33}/2 + 0.4	V_{RC33}	

Table 24. PLLMRFM electrical specifications[1]

(V_{DDPLL} =1.14 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					min	max	
V_{ILEXT}	CC	T	EXTAL input low voltage	Crystal Mode[14], 0.65≤Vxtal≤1.25V[15]	—	Vxtal – 0.4	V
		T		External Reference[14, 16]	0	V_{RC33}/2 – 0.4	
—	CC	T	XTAL load capacitance[12]	4 MHz	5	30	pF
				8 MHz	5	26	
				12 MHz	5	23	
				16 MHz	5	19	
				20 MHz	5	16	
t_{lpll}	CC	P	PLL lock time [12, 17]	—	—	200	µs
t_{dc}	CC	T	Duty cycle of reference	—	40	60	%
f_{LCK}	CC	T	Frequency LOCK range	—	–6	6	% f_{sys}
f_{UL}	CC	T	Frequency un-LOCK range	—	–18	18	% f_{sys}
f_{CS} f_{DS}	CC	D	Modulation Depth	Center spread	±0.25	±4.0	%f_{sys}
		D		Down Spread	–0.5	–8.0	
f_{MOD}	CC	D	Modulation frequency[18]	—	—	100	kHz

1 All values given are initial design targets and subject to change.

2 Considering operation with PLL not bypassed.

3 f_{VCO} is calculated as follows:

— In Legacy Mode f_{VCO} = ($f_{crystal}$ / (PREDIV + 1)) * (4 * (MFD + 4))
— In Enhanced Mode fvco = ($f_{crystal}$ / (EPREDIV + 1)) * (EMFD + 4)

4 All internal registers retain data at 0 Hz.

5 “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.

6 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.

7 f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.

8 This value is determined by the crystal manufacturer and board design.

9 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.

10 Proper PC board layout procedures must be followed to achieve specifications.

11 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).

12 This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits. For a 20 MHz crystal the maximum load should be 17 pF.

13 Proper PC board layout procedures must be followed to achieve specifications.

14 This parameter is guaranteed by design rather than 100% tested.

[15] Vxtal range is preliminary and subject to change pending characterization data.

[16] V_{IHEXT} cannot exceed V_{RC33} in external reference mode.

[17] This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

[18] Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

4.11 Temperature sensor electrical characteristics

Table 25. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					min	typical	max	
—	CC	C	Temperature monitoring range		–40	—	150	°C
—	CC	C	Sensitivity		—	6.3	—	mV/°C
—	CC	P	Accuracy	T_J = –40 to 150 °C	–10	—	10	°C

4.12 eQADC electrical characteristics

Table 26. eQADC conversion specifications (operating)

Symbol		C	Parameter	Value		Unit
				min	max	
f_{ADCLK}	SR	—	ADC clock (ADCLK) frequency	2	16	MHz
CC	CC	D	Conversion cycles	2 + 13	128 + 14	ADCLK cycles
T_{SR}	CC	C	Stop mode recovery time[1]	—	10	µs
—	CC	D	Resolution[2]	1.25	—	mV
OFFNC	CC	C	Offset error without calibration	0	160	Counts
OFFWC	CC	C	Offset error with calibration	–4	4	Counts
GAINNC	CC	C	Full scale gain error without calibration	–160	0	Counts
GAINWC	CC	C	Full scale gain error with calibration	–4	4	Counts
I_{INJ}	CC	T	Disruptive input injection current [3, 4, 5, 6]	–3	3	mA
E_{INJ}	CC	T	Incremental error due to injection current[6,7,8]	–4	4	Counts
TUE8	CC	C	Total unadjusted error (TUE) at 8 MHz	–4	4	Counts
TUE16	CC	C	Total unadjusted error at 16 MHz	–8	8	Counts

Table 26. eQADC conversion specifications (operating) (continued)

Symbol		C	Parameter		Value		Unit
					min	max	
GAINVGA1	CC	–	Variable gain amplifier accuracy (gain=1)[9]				
	CC	C	INL	8 MHz ADC	–4	4	Counts[10]
	CC	C		16 MHz ADC	–8	8	Counts
	CC	C	DNL	8 MHz ADC	–3[11]	3[11]	Counts
	CC	C		16 MHz ADC	–3[11]	3[11]	Counts
GAINVGA2	CC	–	Variable gain amplifier accuracy (gain=2)[9]				
	CC	D	INL	8 MHz ADC	–5	5	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–3	3	Counts
	CC	D		16 MHz ADC	–3	3	Counts
GAINVGA4	CC	–	Variable gain amplifier accuracy (gain=4)[9]				
	CC	D	INL	8 MHz ADC	–7	7	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–4	4	Counts
	CC	D		16 MHz ADC	–4	4	Counts
$DIFF_{max}$	CC	C	Maximum differential voltage (DANx+ - DANx-) or (DANx- - DANx+)	PREGAIN set to 1X setting	–	(VRH - VRL)/2	V
$DIFF_{max2}$	CC	C		PREGAIN set to 2X setting	–	(VRH - VRL)/4	V
$DIFF_{max4}$	CC	C		PREGAIN set to 4X setting	–	(VRH - VRL)/8	V
$DIFF_{cmv}$	CC	C	Differential input Common mode voltage (DANx- + DANx+)/2[12]		(VRH - VRL)/2 - 5%	(VRH - VRL)/2 + 5%	V

1 Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions. Delay from power up to full accuracy = 8 ms.

2 At $V_{RH} - V_{RL}$ = 5.12 V, one count = 1.25 mV. Without using pregain.

3 Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater then V_{RH} and 0x0 for values less then V_{RL}. Other channels are not affected by non-disruptive conditions.

4 Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

5 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5$ V and $V_{NEGCLAMP} = -0.3$ V, then use the larger of the calculated values.

6 Condition applies to two adjacent pins at injection limits.

7 Performance expected with production silicon.

8 All channels have same 10 kΩ < Rs < 100 kΩ; Channel under test has Rs=10 kΩ; I_{INJ}=I_{INJMAX},I_{INJMIN}

9 Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.

[10] At $V_{RH} - V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

[11] Guaranteed 10-bit monotonicity.

[12] Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

4.13 Platform flash controller electrical characteristics

Table 27. APC, RWSC, WWSC settings vs. frequency of operation[1]

Target Max Frequency (MHz)	APC[2]	RWSC[2]	WWSC
21[3]	000	000	01
41[3]	001	001	01
62[3]	010	010	01
82[3]	011	011	01
All	111	111	111

1 Illegal combinations exist, all entries must be taken from the same row

2 APC must be equal to RWSC

3 Maximum Frequency includes FM modulation

4.14 Flash memory electrical characteristics

Table 28. Program and erase specifications

Symbol		Parameter	Min Value	Typical Value[1]	Initial Max[2]	Max[3]	Unit
$T_{dwprogram}$	P	Double Word (64 bits) Program Time[4]	—	22	50	500	µs
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time	—	300	500	5000	ms
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	—	400	600	5000	ms
$T_{64kpperase}$	P	64 KB Block Pre-program and Erase Time	—	600	900	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	—	800	1300	7500	ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program & erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

Table 29. Flash module life

Symbol		Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 Kbyte blocks over the operating temperature range (T_J)	—	100,000	—	cycles
P/E	C	Number of program/erase cycles per block for 32 and 64 Kbyte blocks over operating temperature range (T_J)	—	10,000	100,000	cycles
P/E	C	Number of program/erase cycles per block for 128 Kbyte blocks over the operating temperature range (T_J)	—	1,000	100,000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0 – 1,000 P/E cycles	20	—	years
			Blocks with 10,000 P/E cycles	10	—	years
			Blocks with 100,000 P/E cycles	5	—	years

[1] Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

4.15 AC specifications

4.15.1 Pad AC specifications

Table 30. Pad AC specifications (5.0 V)[1,2]

Name		C	Output Delay (ns)[3,4] Low-to-High / High-to-Low		Rise/Fall Edge (ns)[4,5]		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium[6,7,8]	CC	D	4.6/3.7	12/12	2.2/2.2	7/7	50	11[9]
	CC	D	13/10	32/32	9/9	22/22	200	
	N/A							10[10]
	CC	D	12/13	28/34	5.6/6	15/15	50	01
	CC	D	23/23	52/59	11/14	31/31	200	
	CC	D	69/71	152/165	34/35	74/74	50	00
	CC	D	95/90	205/220	44/51	96/96	200	
Slow[8,11]	CC	D	7.3/5.7	19/18	4.4/4.3	14/14	50	11[9]
	CC	D	24/19	58/58	17/15	42/42	200	
	N/A							10[10]
	CC	D	26/27	61/69	13/13	34/34	50	01
	CC	D	49/45	115/115	27/23	61/61	200	
	CC	D	137/142	320/330	72/74	164/164	50	00
	CC	D	182/172	420/420	90/85	200/200	200	
MultiV[12] (High Swing Mode)	CC	D	4.1/3.6	10.3/8.9	3.28/2.98	8/8	50	11[9]
	CC	D	10.4/10.2	24.2/23.6	12.7/11.54	29/29	200	
	N/A							10[10]
	CC	D	8.38/6.11	16/12.9	5.48/4.81	11/11	50	01
	CC	D	15.9/13.6	31/28.5	14.6/13.1	31/31	200	
	CC	D	61.7/10.4	92.2/24.3	42.0/12.2	63/63	50	00
	CC	D	85.5/37.3	132.6/ 78.9	57.7/46.4	85/85	200	
MultiV (Low Swing Mode)	CC	D	2.31/2.34	7.62/6.33	1.26/1.67	7/7	30	11[9]
Fast[13]	N/A							
pad_i_hv[14]	CC	D	0.5/0.5	1.9/1.9	0.3/0.3	1.5/1.5	0.5	N/A
pull_hv	CC	D	NA	6000	—	5000/5000	50	N/A

1 These are worst case values that are estimated from simulation and not tested. Values in the table are simulated at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 1.62 V to 1.98 V, V_{DDEH} = 4.5 V to 5.25 V, $T_A = T_L$ to T_H.

2 TBD: To Be Defined.

[3] This parameter is supplied for reference and is not guaranteed by design and not tested.
[4] Delay and rise/fall are measured to 20% or 80% of the respective signal.
[5] This parameter is guaranteed by characterization before qualification rather than 100% tested.
[6] In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads
[7] Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
[8] Output delay is shown in Figure 8. Add a maximum of one system clock to the output delay for delay with respect to system clock.
[9] Can be used on the tester.
[10] This drive select value is not supported. If selected, it will be approximately equal to 11.
[11] Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
[12] Selectable high/low swing IO pad with selectable slew in high swing mode only.
[13] Fast pads are 3.3 V pads.
[14] Stand alone input buffer. Also has weak pull-up/pull-down.

Table 31. Pad AC specifications (3.3 V)[1]

Pad Type		C	Output Delay (ns)[2,3] Low-to-High / High-to-Low		Rise/Fall Edge (ns)[3,4]		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium[5,6,7]	CC	D	5.8/4.4	18/17	2.7/2.1	10/10	50	11[8]
	CC	D	16/13	46/49	11.2/8.6	34/34	200	
	N/A							10[9]
	CC	D	14/16	37/45	6.5/6.7	19/19	50	01
	CC	D	27/27	69/82	15/13	43/43	200	
	CC	D	83/86	200/210	38/38	86/86	50	00
	CC	D	113/109	270/285	53/46	120/120	200	
Slow[7,10]	CC	D	9.2/6.9	27/28	5.5/4.1	20/20	50	11
	CC	D	30/23	81/87	21/16	63/63	200	
	N/A							10[9]
	CC	D	31/31	80/90	15.4/15.4	42/42	50	01
	CC	D	58/52	144/155	32/26	82/85	200	
	CC	D	162/168	415/415	80/82	190/190	50	00
	CC	D	216/205	533/540	106/95	250/250	200	
MultiV[7,11] (High Swing Mode)	CC	D		3.7/3.1		10/10	30	11[8]
	CC	D		46/49		37/37	200	
	N/A							10[9]
	CC	D		32		15/15	50	01
	CC	D		72		46/46	200	
	CC	D		210		100/100	50	00
	CC	D		295		134/134	200	

Table 31. Pad AC specifications (3.3 V)[1] (continued)

Pad Type		C	Output Delay (ns)[2,3] Low-to-High / High-to-Low		Rise/Fall Edge (ns)[3,4]		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Fast	CC	D		2.5/2.5		1.2/1.2	10	00
	CC	D		2.5/2.5		1.2/1.2	20	01
	CC	D		2.5/2.5		1.2/1.2	30	10
	CC	D		2.5/2.5		1.2/1.2	50	11[8]
pad_i_hv[12]	CC	D	0.5/0.5	3/3	0.4/0.4	1.5/1.5	0.5	N/A
pull_hv	CC	D	NA	6000		5000/5000	50	N/A

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 3 V to 3.6 V, V_{DDEH} = 3 V to 3.6 V, $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

5 In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads

6 Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.

7 Output delay is shown in Figure 8. Add a maximum of one system clock to the output delay for delay with respect to system clock.

8 Can be used on the tester

9 This drive select value is not supported. If selected, it will be approximately equal to 11.

10 Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.

11 Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.

12 Stand alone input buffer. Also has weak pull-up/pull-down.

Table 32. Pad AC specifications (1.8 V)

Pad Type		C	Output Delay (ns)[1,2] Low-to-High / High-to-Low		Rise/Fall Edge (ns)[3]		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Fast	CC	D		3.0/3.0	2.0/1.5		10	00
	CC	D		3.0/3.0	2.0/1.5		20	01
	CC	D		3.0/3.0	2.0/1.5		30	10
	CC	D		3.0/3.0	2.0/1.5		50	11[4]

1 This parameter is supplied for reference and is not guaranteed by design and not tested.

2 Delay and rise/fall are measured to 20% or 80% of the respective signal.

3 This parameter is guaranteed by characterization before qualification rather than 100% tested.

4 Can be used on the tester.

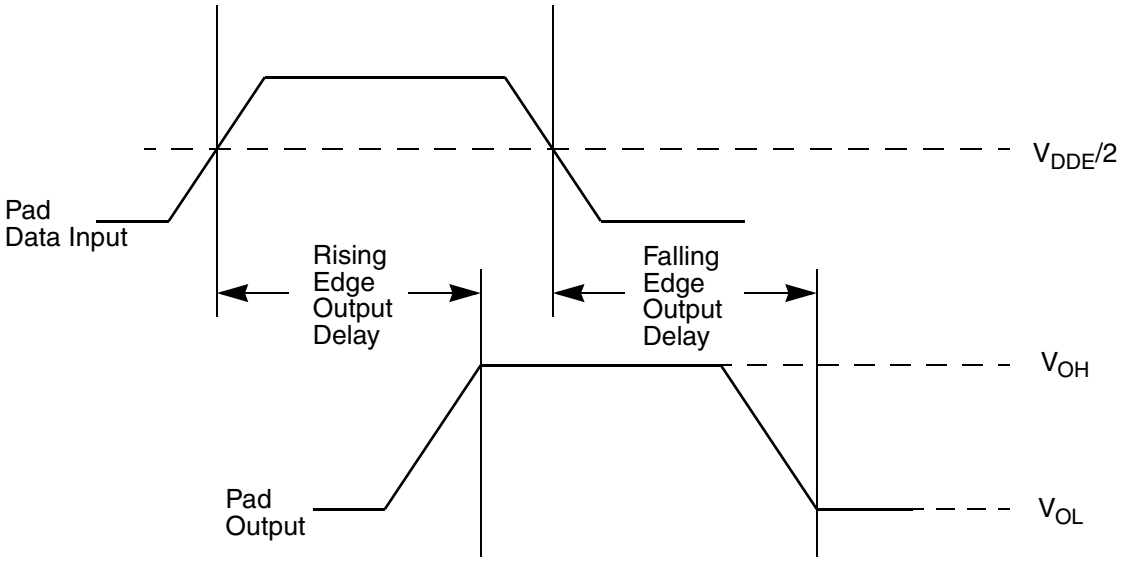


Figure 8. Pad output delay

4.16 AC timing

4.16.1 IEEE 1149.1 interface timing

Table 33. JTAG pin AC electrical characteristics[1]

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
1	t_{JCYC}	CC	D	TCK Cycle Time	100	—	ns
2	t_{JDC}	CC	D	TCK Clock Pulse Width	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times (40% – 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI Data Hold Time	25	—	ns
6	t_{TDOV}	CC	D	TCK Low to TDO Data Valid	—	23	ns
7	t_{TDOI}	CC	D	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK Low to TDO High Impedance	—	20	ns
9	t_{JCMPPW}	CC	D	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	CC	D	TCK Falling Edge to Output Valid	—	50	ns

Table 33. JTAG pin AC electrical characteristics[1] (continued)

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
12	t_{BSDVZ}	CC	D	TCK Falling Edge to Output Valid out of High Impedance	—	50	ns
13	t_{BSDHZ}	CC	D	TCK Falling Edge to Output High Impedance	—	50	ns
14	t_{BSDST}	CC	D	Boundary Scan Input Valid to TCK Rising Edge	50	—	ns
15	t_{BSDHT}	CC	D	TCK Rising Edge to Boundary Scan Input Invalid	50	—	ns

[1] JTAG timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.25 V with multi-voltage pads programmed to Low-Swing mode, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10, SRC = 0b00. These specifications apply to JTAG boundary scan only. See Table 34 for functional specifications.

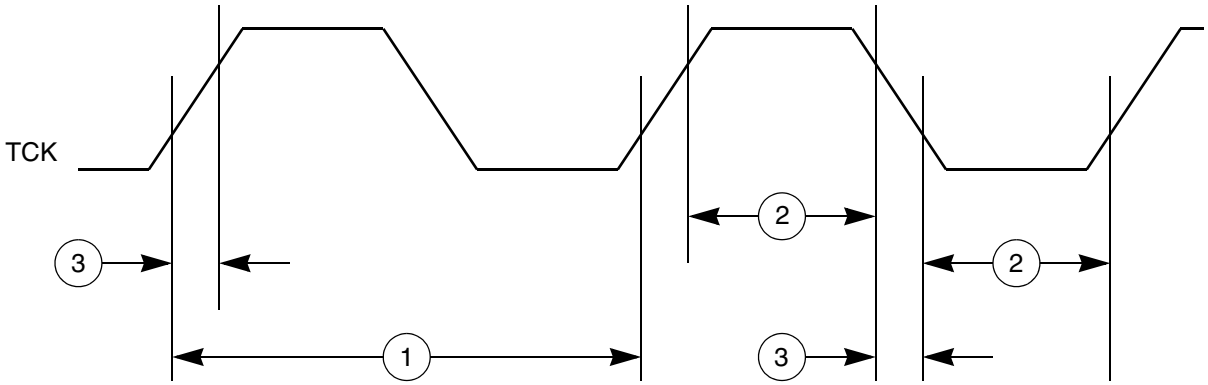


Figure 9. JTAG test clock input timing

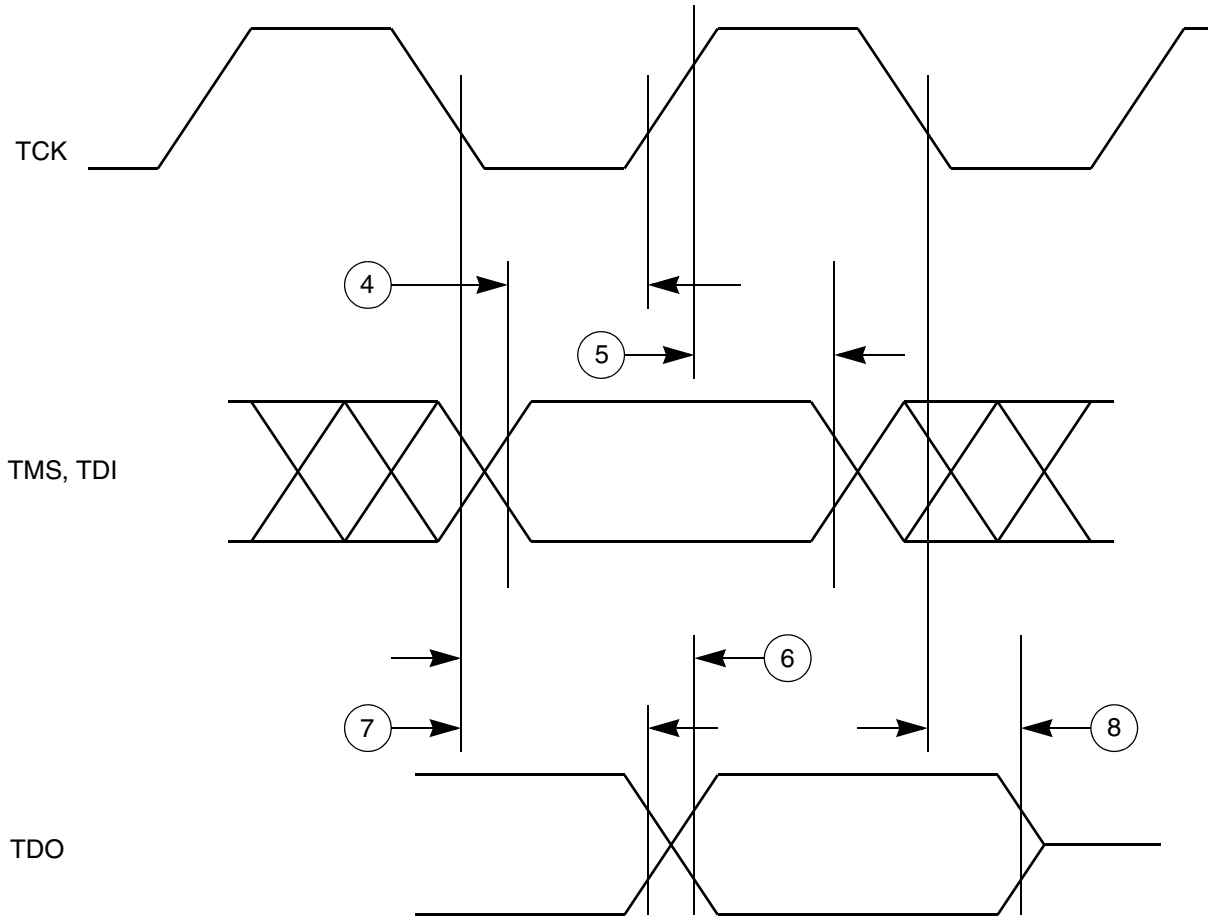


Figure 10. JTAG test access port timing

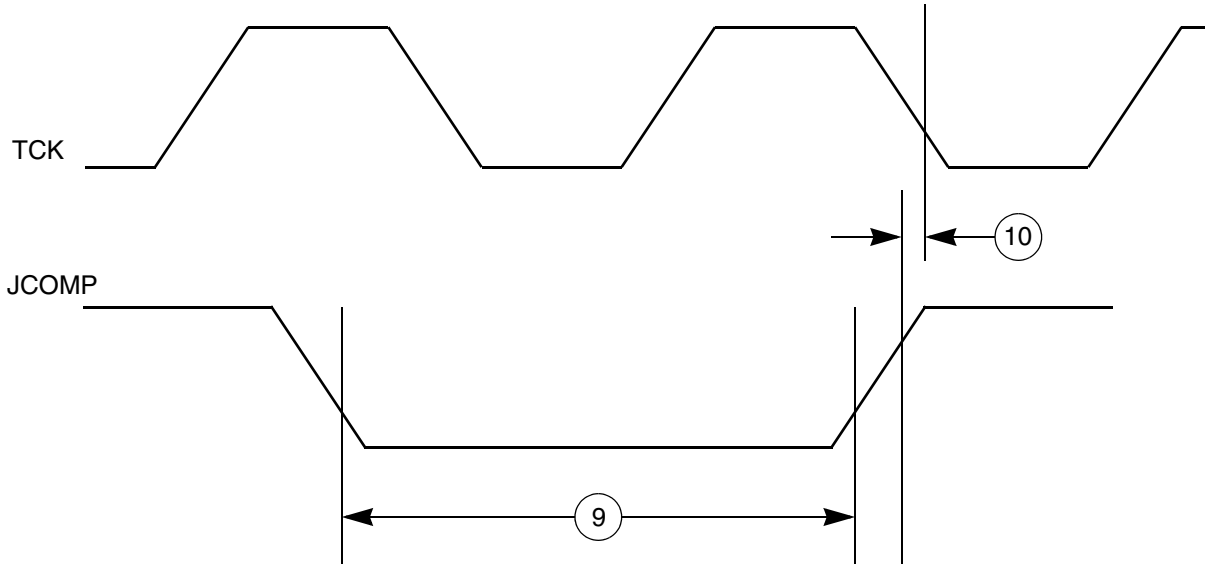


Figure 11. JTAG JCOMP timing

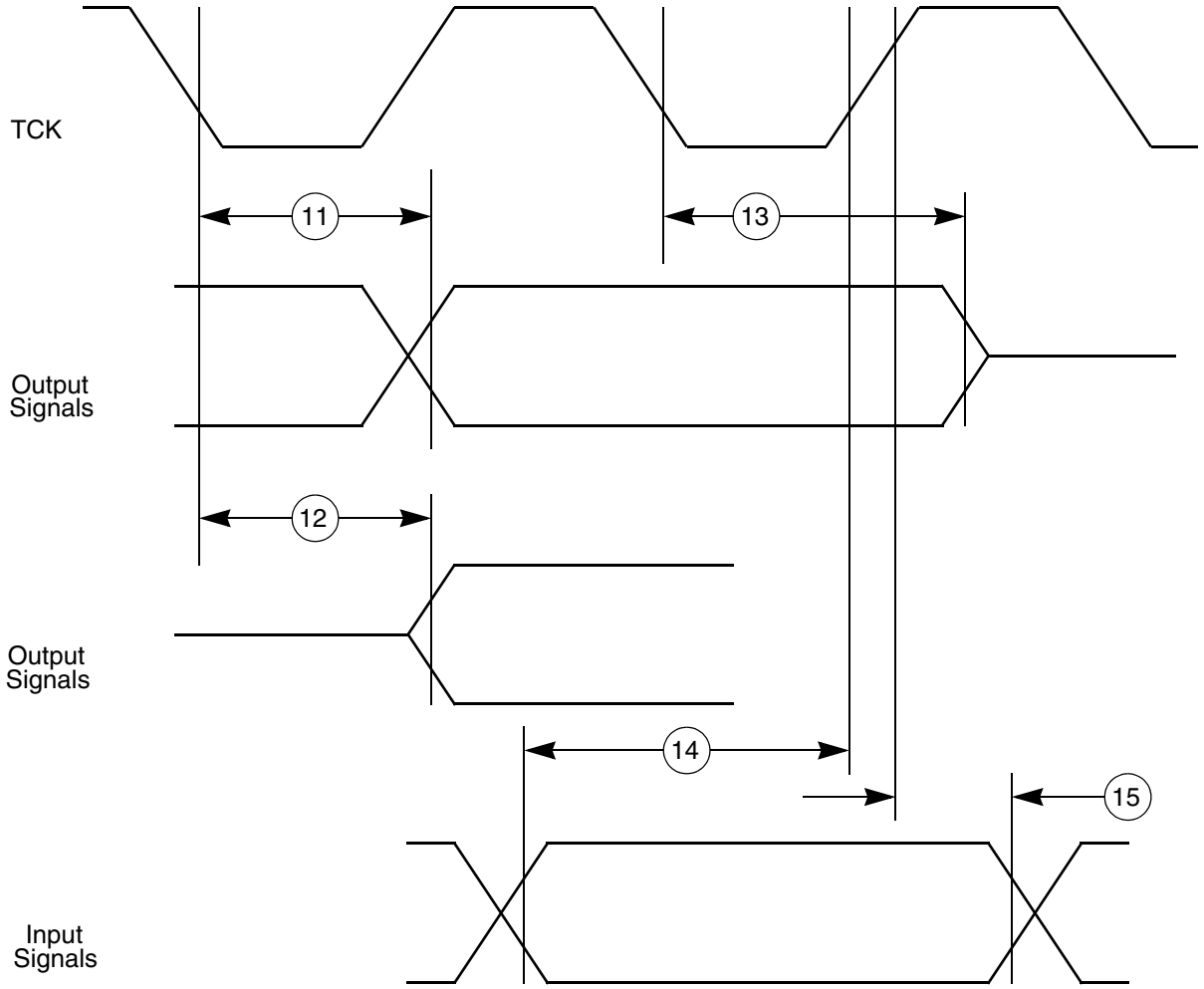


Figure 12. JTAG boundary scan timing

4.16.2 Nexus timing

Table 34. Nexus debug port timing[1]

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
1	t_{MCYC}	CC	D	MCKO Cycle Time	$2^{2,3}$	8	t_{CYC}
1a	t_{MCYC}	CC	D	Absolute Minimum MCKO Cycle Time	100[4]	—	ns
2	t_{MDC}	CC	D	MCKO Duty Cycle	40	60	%
3	t_{MDOV}	CC	D	MCKO Low to MDO Data Valid[5]	– 0.1	0.2	t_{MCYC}
4	t_{MSEOV}	CC	D	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[5]	0.1	0.2	t_{MCYC}
6	t_{EVTOV}	CC	D	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[5]	– 0.1	0.2	t_{MCYC}
7	t_{EVTIPW}	CC	D	$\overline{\text{EVTI}}$ Pulse Width	4.0	—	t_{TCYC}
8	t_{EVTOPW}	CC	D	$\overline{\text{EVTO}}$ Pulse Width	1	—	t_{MCYC}

Table 34. Nexus debug port timing[1] (continued)

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
9	t_{TCYC}	CC	D	TCK Cycle Time	4[6,7]	—	t_{CYC}
9a	t_{TCYC}	CC	D	Absolute Minimum TCK Cycle Time	100[8]	—	ns
10	t_{TDC}	CC	D	TCK Duty Cycle	40	60	%
11	t_{NTDIS}	CC	D	TDI Data Setup Time	5	—	ns
12	t_{NTDIH}	CC	D	TDI Data Hold Time	25	—	ns
13	t_{NTMSS}	CC	D	TMS Data Setup Time	5	—	ns
14	t_{NTMSH}	CC	D	TMS Data Hold Time	25	—	ns
15	t_{JOV}	CC	D	TCK Low to TDO Data Valid	10	20	ns

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.25 V with multi-voltage pads programmed to Low-Swing mode, T_A = TL to TH, and CL = 30 pF with DSC = 0b10.

2 Achieving the absolute minimum MCKO cycle time may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV] depending on the actual system frequency being used.

3 This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum MCKO period specification.

4 This may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV]) depending on the actual system frequency being used.

5 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

6 Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

7 This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.

8 This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

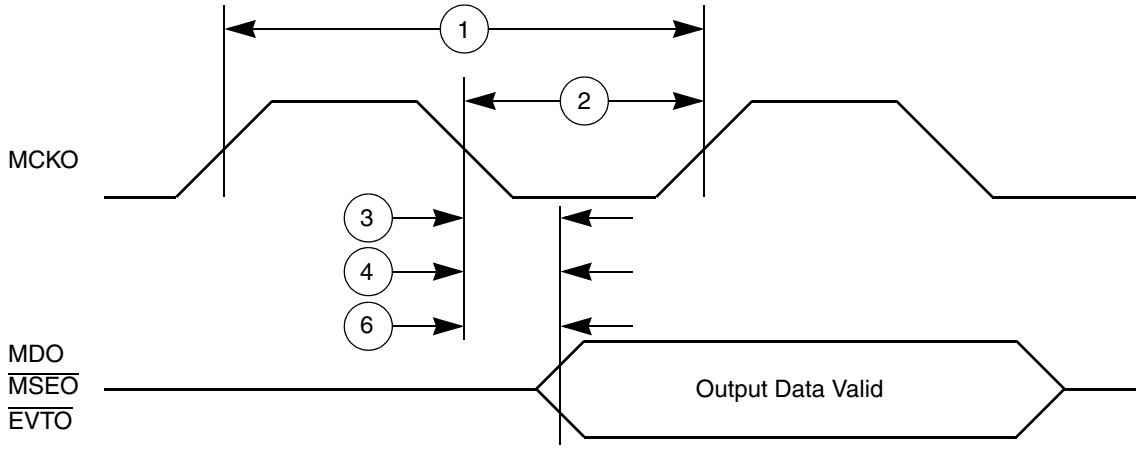


Figure 13. Nexus output timing

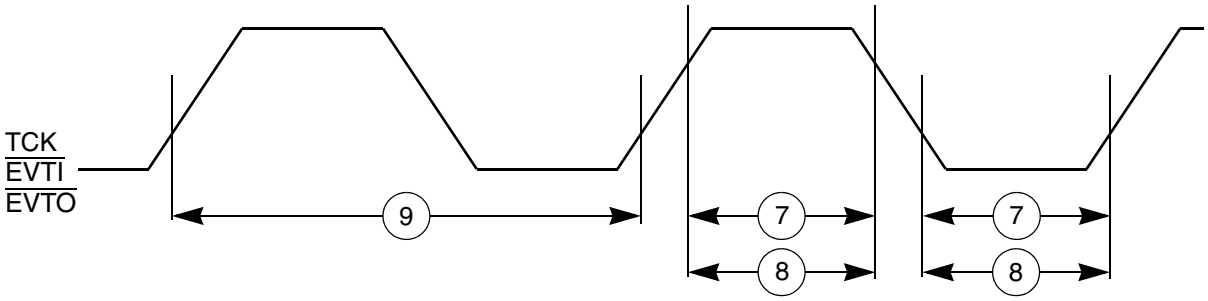


Figure 14. Nexus event trigger and test clock timings

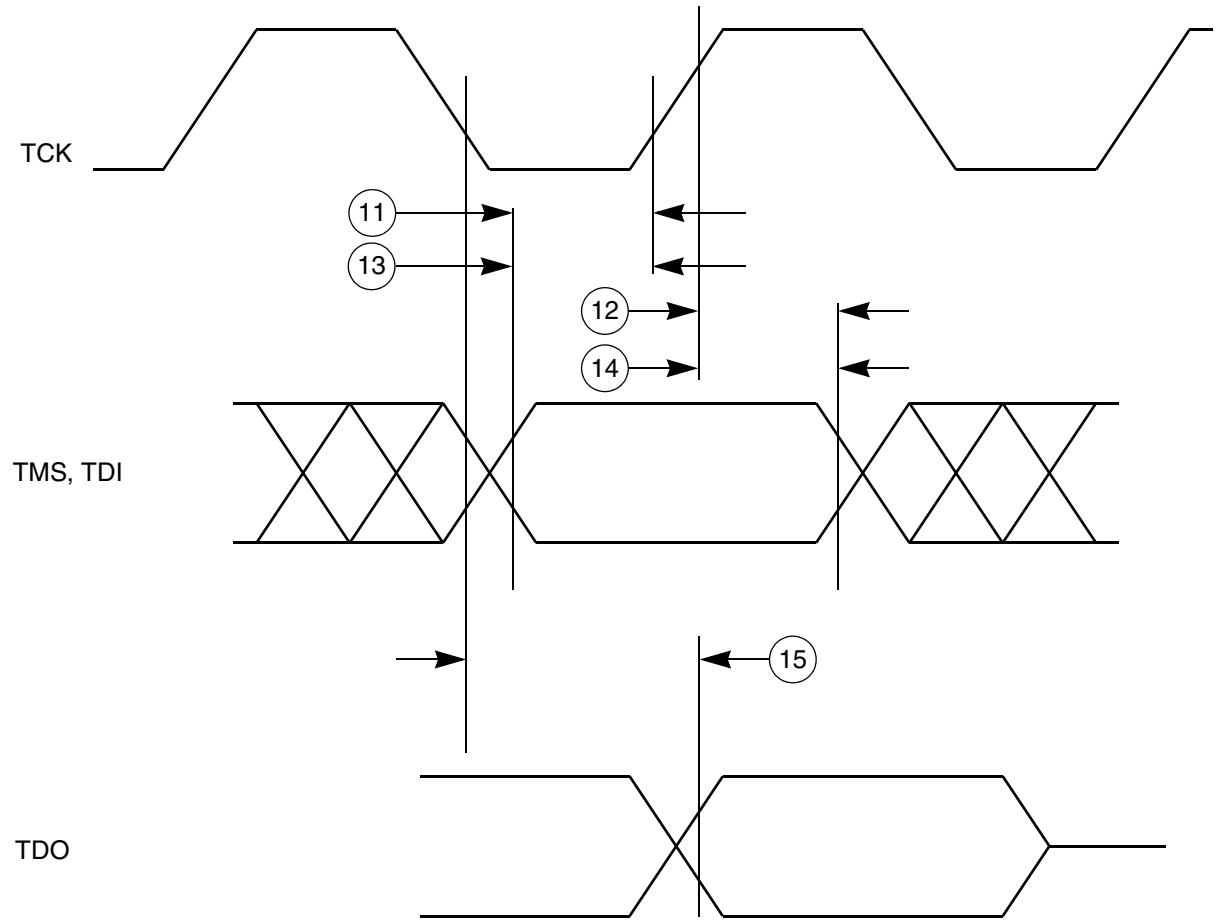


Figure 15. Nexus TDI, TMS, TDO timing

4.16.3 Calibration bus interface timing

Table 35. Calibration bus operation timing [1]

#	Symbol		C	Characteristic	66 MHz (ext. bus)[2]		Unit	Notes
					Min	Max		
1	T_C	CC	P	CLKOUT Period	15.2	—	ns	Signals are measured at 50% V_{DDE}.
2	t_{CDC}	CC	D	CLKOUT duty cycle	45%	55%	T_C	
3	t_{CRT}	CC	D	CLKOUT rise time	—	[3]	ns	
4	t_{CFT}	CC	D	CLKOUT fall time	—	[3]	ns	
5	t_{COH}	CC	D	CLKOUT Posedge to Output Signal Invalid or High Z(Hold Time) ADDR[8:31] CS[0:3] DATA[0:31] OE RD_$\overline{WR}$ TS $\overline{WE}$[0:3]/$\overline{BE}$[0:3]	1.0[4]/1.5	—	ns	Hold time selectable via SIU_ECCR[EBTS] bit: EBTS=0: 1.0ns EBTS=1: 1.5ns
6	t_{COV}	CC	D	CLKOUT Posedge to Output Signal Valid (Output Delay) ADDR[8:31] CS[0:3] DATA[0:31] OE RD_$\overline{WR}$ TS $\overline{WE}$[0:3]/$\overline{BE}$[0:3]	—	6.0[4]/7.0	ns	Output valid time selectable via SIU_ECCR[EBTS] bit: EBTS=0: 5.5ns EBTS=1: 6.5ns
7	t_{CIS}	CC	D	Input Signal Valid to CLKOUT Posedge (Setup Time) DATA[0:31]	5.0	—	ns	
8	t_{CIH}	CC	D	CLKOUT Posedge to Input Signal Invalid (Hold Time) DATA[0:31]	1.0	—	ns	
9	t_{APW}	CC	D	ALE Pulse Width[5]	6.5	—	ns	
10	t_{AAI}	CC	D	ALE Negated to Address Invalid[5]	3	—	ns	

1 Calibration bus timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 1.62 V to 3.6 V (unless stated otherwise), $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.

2 The external bus is limited to half the speed of the internal bus. The maximum external bus frequency is 66 MHz.

3 Refer to Fast Pad timing in Table 31 and Table 32 (different values for 3.3 V vs. 1.8 V).

4 The EBTS=0 timings are only valid/ tested at V_{DDE}=2.25–3.6 V, whereas EBTS=1 timings are valid/tested at 1.6–3.6 V.

5 Measured at 50% of ALE.

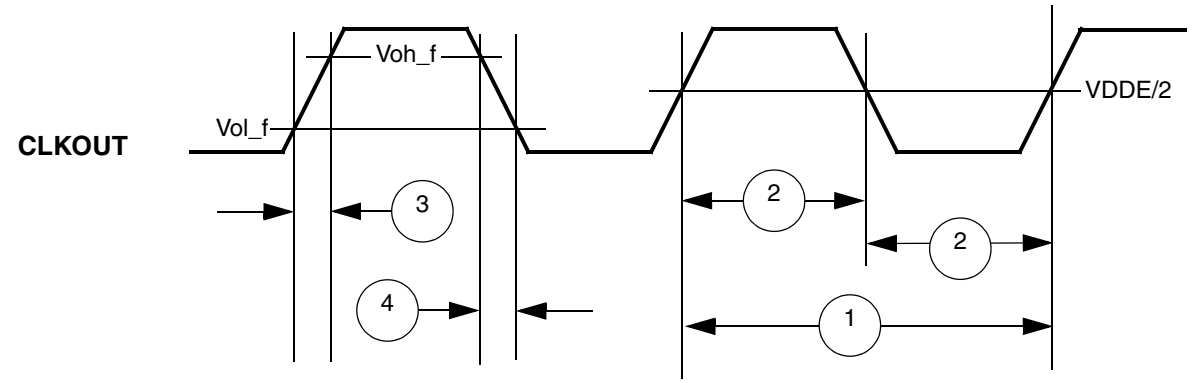


Figure 16. CLKOUT timing

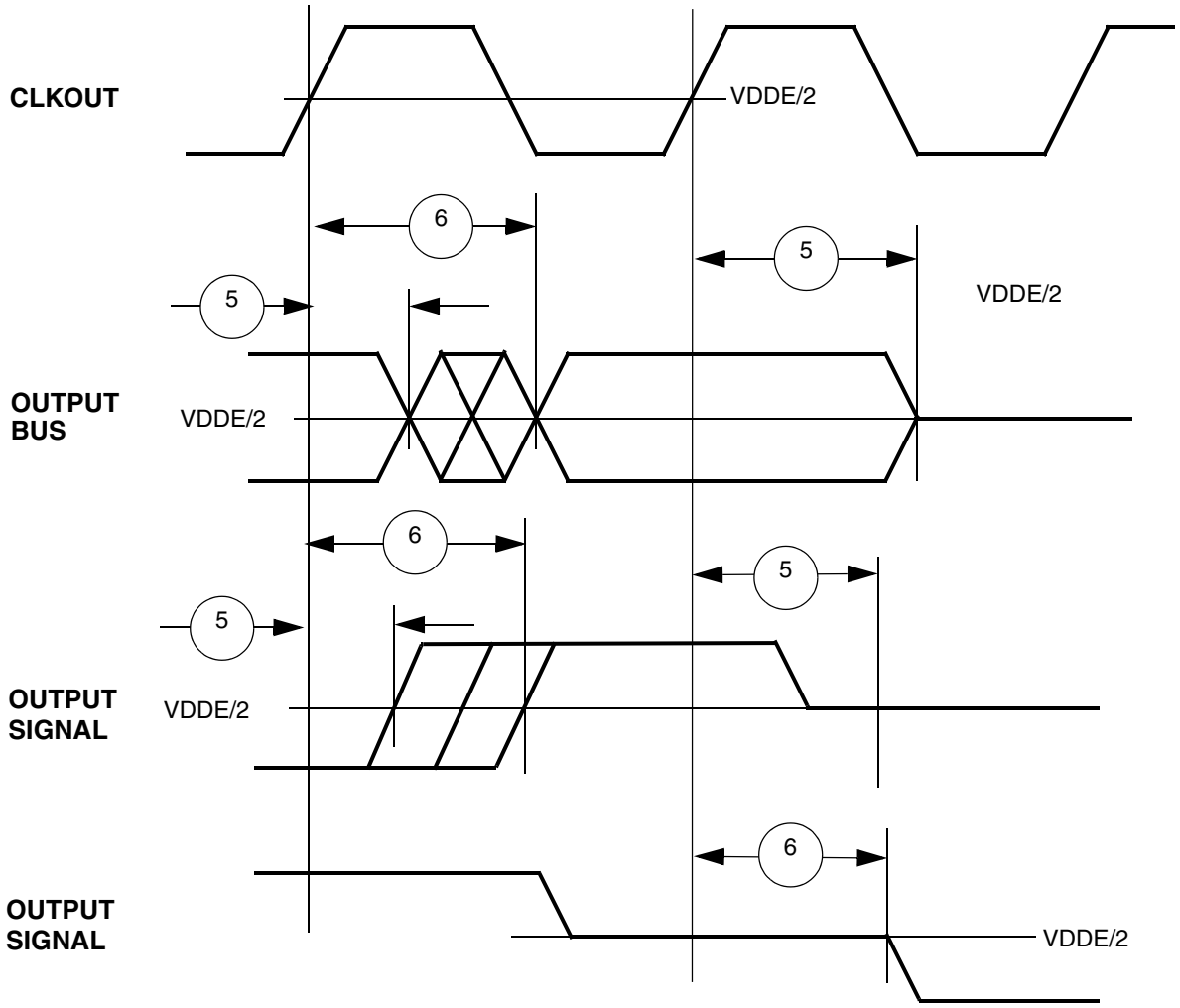


Figure 17. Synchronous output timing

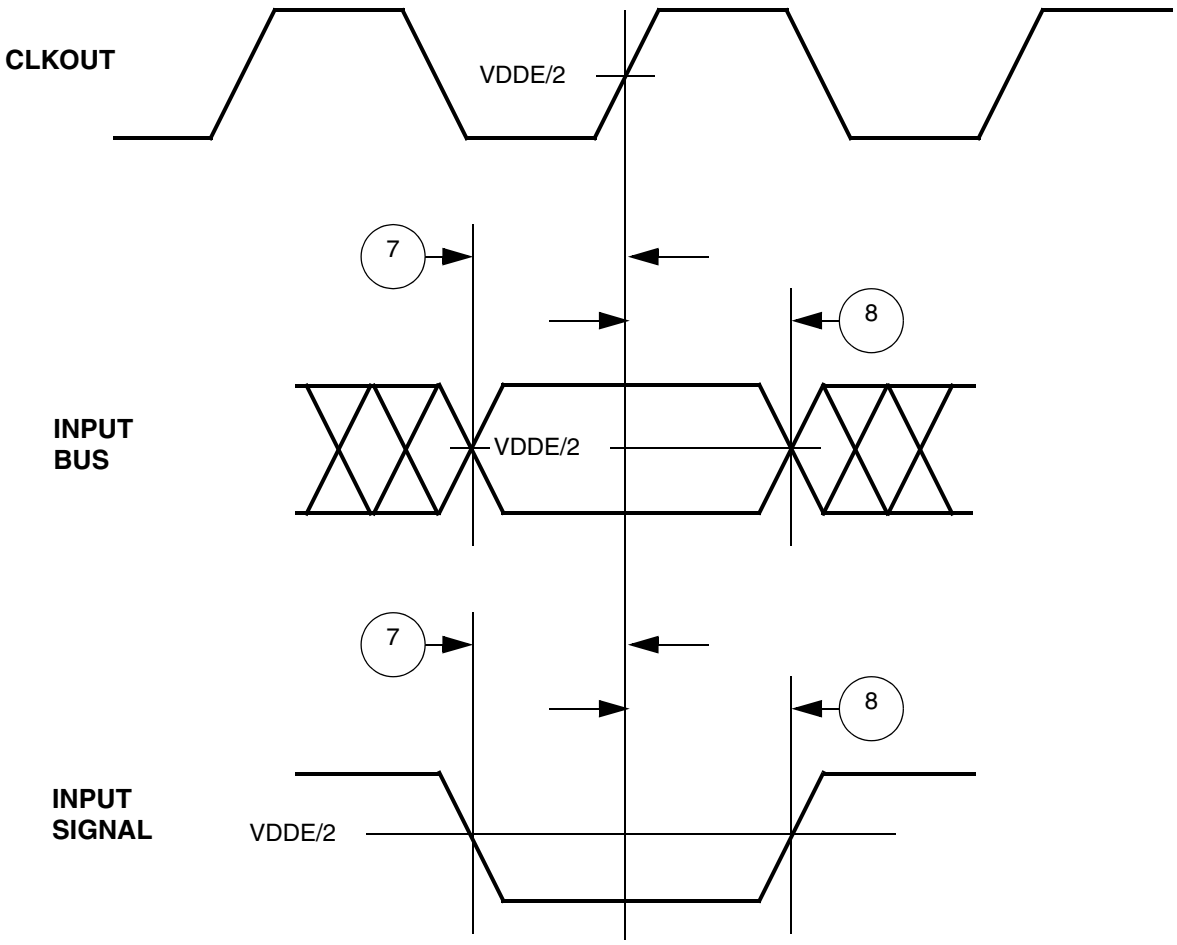


Figure 18. Synchronous input timing

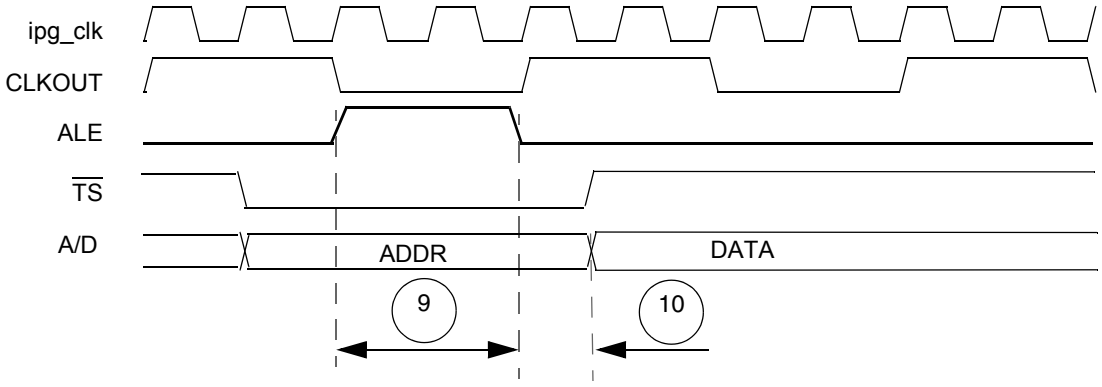


Figure 19. ALE signal timing

4.16.4 eMIOS timing

Table 36. eMIOS timing[1]

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
1	t_{MIPW}	CC	D	eMIOS Input Pulse Width	4	—	t_{CYC}
2	t_{MOPW}	CC	D	eMIOS Output Pulse Width	1	—	t_{CYC}

[1] eMIOS timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.25 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.

4.16.5 DSPI timing

Table 37. DSPI timing[1,2]

#	Symbol		C	Characteristic	40 MHz		60 MHz		80 MHz		Unit
					Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{SCK}	CC	D	SCK Cycle Time[3,4]	48.8 ns	5.8 ms	28.4 ns	3.5 ms	24.4 ns	2.9 ms	—
2	t_{CSC}	CC	D	PCS to SCK Delay[5]	46	—	26	—	22	—	ns
3	t_{ASC}	CC	D	After SCK Delay[6]	45	—	25	—	21	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle	$(½t_{SC}) - 2$	$(½t_{SC}) + 2$	$(½t_{SC}) - 2$	$(½t_{SC}) + 2$	$(½t_{SC}) - 2$	$(½t_{SC}) + 2$	ns
5	t_A	CC	D	Slave Access Time ($\overline{SS}$ active to SOUT driven)	—	25	—	25	—	25	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	—	25	—	25	—	25	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time	4	—	4	—	4	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time	5	—	5	—	5	—	ns
9	t_{SUI}	CC	Data Setup Time for Inputs								
			D	Master (MTFE = 0)	20	—	20	—	20	—	ns
			D	Slave	2	—	2	—	2	—	
			D	Master (MTFE = 1, CPHA = 0)[7]	–4	—	6	—	8	—	
			D	Master (MTFE = 1, CPHA = 1)	20	—	20	—	20	—	

Table 37. DSPI timing[1,2] (continued)

#	Symbol		C	Characteristic	40 MHz		60 MHz		80 MHz		Unit
					Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{HI}	CC	Data Hold Time for Inputs								
			D	Master (MTFE = 0)	–4	—	–4	—	–4	—	ns
			D	Slave	7	—	7	—	7	—	
			D	Master (MTFE = 1, CPHA = 0)[7]	45	—	25	—	21	—	
			D	Master (MTFE = 1, CPHA = 1)	–4	—	–4	—	–4	—	
11	t_{SUO}	CC	Data Valid (after SCK edge)								
			D	Master (MTFE = 0)	—	6	—	6	—	6	ns
			D	Slave	—	25	—	25	—	25	
			D	Master (MTFE = 1, CPHA=0)	—	45	—	25	—	21	
			D	Master (MTFE = 1, CPHA=1)	—	6	—	6	—	6	
12	t_{HO}	CC	Data Hold Time for Outputs								
			D	Master (MTFE = 0)	–5	—	–5	—	–5	—	ns
			D	Slave	5.5	—	5.5	—	5.5	—	
			D	Master (MTFE = 1, CPHA = 0)	8	—	4	—	3	—	
			D	Master (MTFE = 1, CPHA = 1)	–5	—	–5	—	–5	—	

1 All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type M or MH. DSPI signals using pad types of S or SH have an additional delay based on the slew rate. DSPI timing is specified at VDDEH = 3.0–5.25 V, TA = TL to TH, and CL = 50 pF with SRC = 0b11.

2 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 42 MHz parts allow for 40 MHz system clock + 2% FM; 62 MHz parts allow for a 60 MHz system clock + 2% FM, and 82 MHz parts allow for 80 MHz system clock + 2% FM.

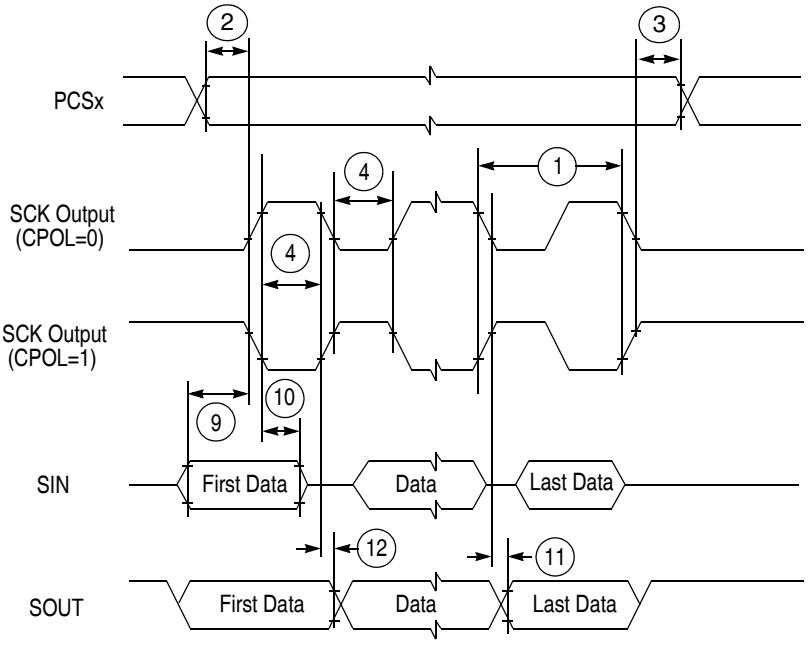
3 The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two MPC5634M devices communicating over a DSPI link.

4 The actual minimum SCK cycle time is limited by pad performance.

5 The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].

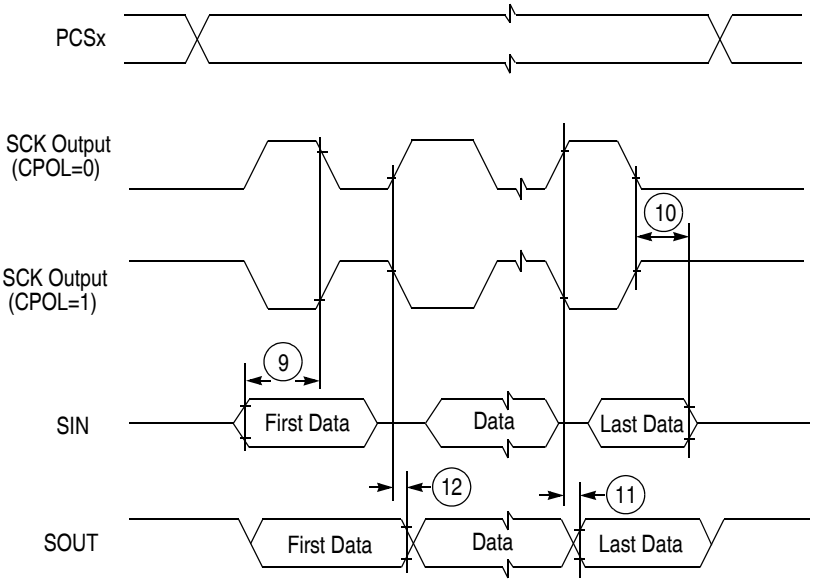
6 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].

7 This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.



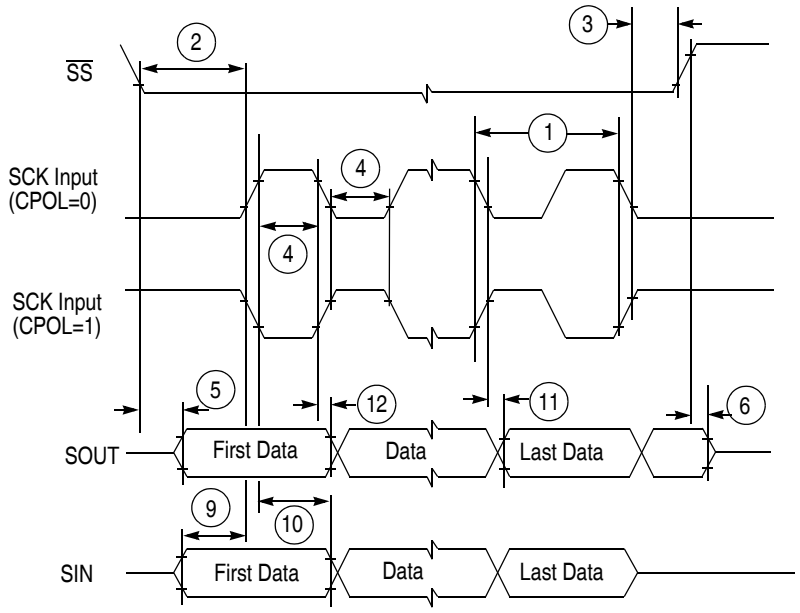
These numbers reference Table 37.

Figure 20. DSPI classic SPI timing – master, CPHA = 0



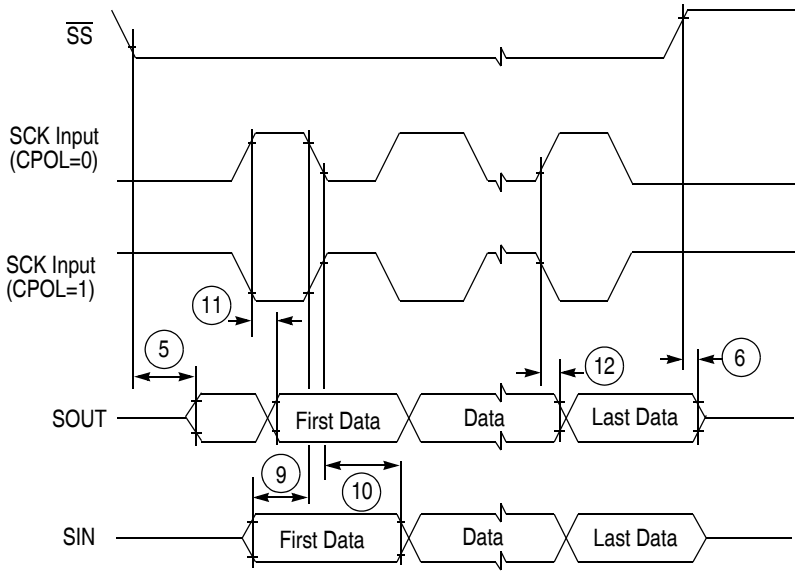
These numbers reference Table 37.

Figure 21. DSPI classic SPI timing – master, CPHA = 1



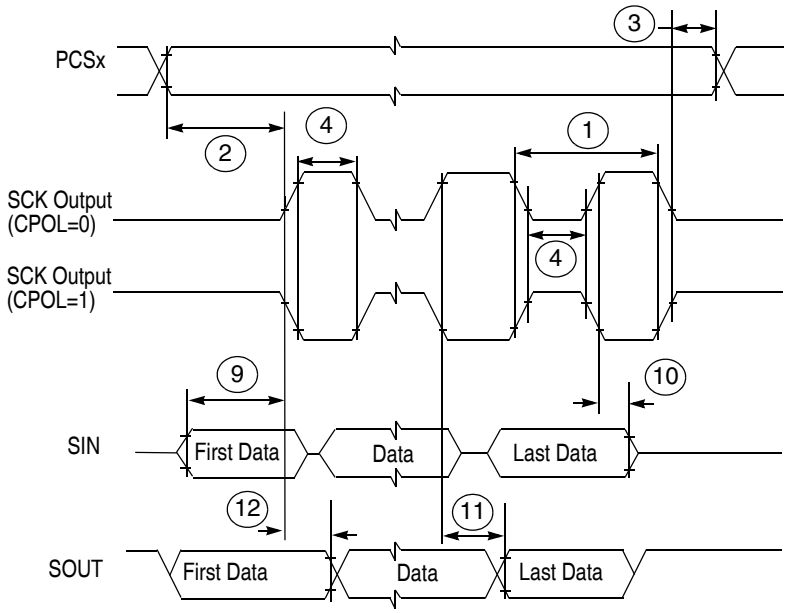
These numbers reference Table 37.

Figure 22. DSPI classic SPI timing – slave, CPHA = 0



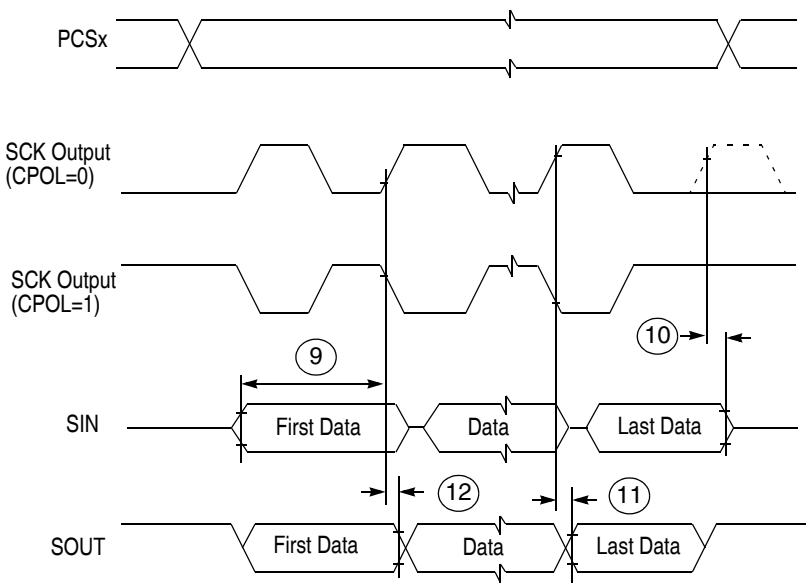
These numbers reference Table 37.

Figure 23. DSPI classic SPI timing – slave, CPHA = 1



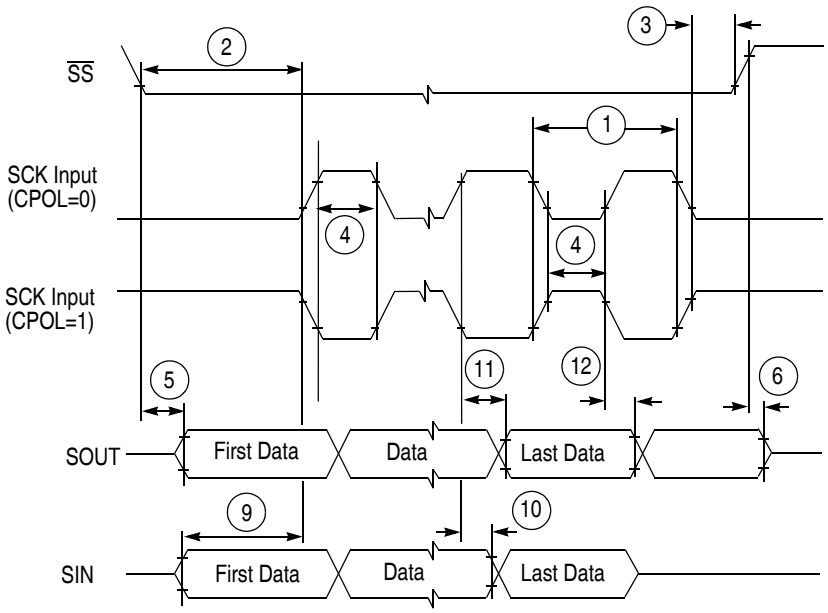
These numbers reference Table 37.

Figure 24. DSPI modified transfer format timing – master, CPHA = 0



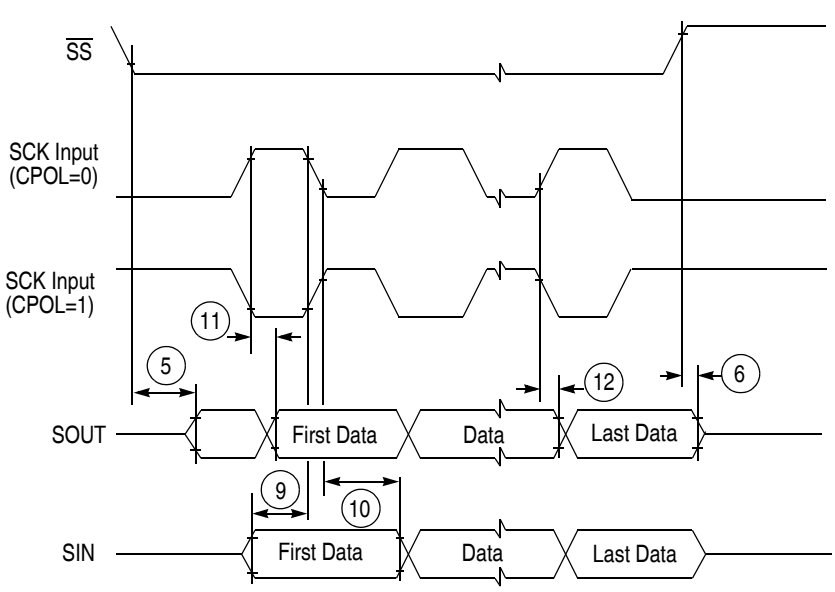
These numbers reference Table 37.

Figure 25. DSPI modified transfer format timing – master, CPHA = 1



These numbers reference Table 37.

Figure 26. DSPI modified transfer format timing – slave, CPHA =0



These numbers reference Table 37.

Figure 27. DSPI modified transfer format timing – slave, CPHA =1

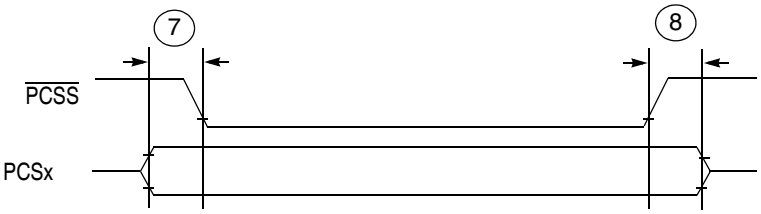


Figure 28. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

4.16.6 eQADC SSI timing

Table 38. eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)[1]

CLOAD = 25pF on all outputs. Pad drive strength set to maximum.								
#	Symbol		C	Rating	Min	Typ	Max	Unit
1	f_{FCK}	CC	D	FCK Frequency [2, 3]	1/17 f_{SYS_CLK}		1/2 f_{SYS_CLK}	Hertz
1	t_{FCK}	CC	D	FCK Period (t_{FCK} = 1/ f_{FCK})	2 t_{SYS_CLK}		17t_{SYS_CLK}	seconds
2	t_{FCKHT}	CC	D	Clock (FCK) High Time	t_{SYS_CLK} − 6.5		$_{9*}$ t_{SYS_CLK} + 6.5	ns
3	t_{FCKLT}	CC	D	Clock (FCK) Low Time	t_{SYS_CLK} − 6.5		$_{8*}$ t_{SYS_CLK} + 6.5	ns
4	t_{SDS_LL}	CC	D	SDS Lead/Lag Time	–7.5		+7.5	ns
5	t_{SDO_LL}	CC	D	SDO Lead/Lag Time	–7.5		+7.5	ns
6	t_{DVFE}	CC	D	Data Valid from FCK Falling Edge (t_{FCKLT}+t_{SDO_LL})	1			ns
7	t_{EQ_SU}	CC	D	eQADC Data Setup Time (Inputs)	22			ns
8	t_{EQ_HO}	CC	D	eQADC Data Hold Time (Inputs)	1			ns

1 SS timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.25 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.

2 Maximum operating frequency is highly dependent on track delays, master pad delays, and slave pad delays.

3 FCK duty is not 50% when it is generated through the division of the system clock by an odd number.

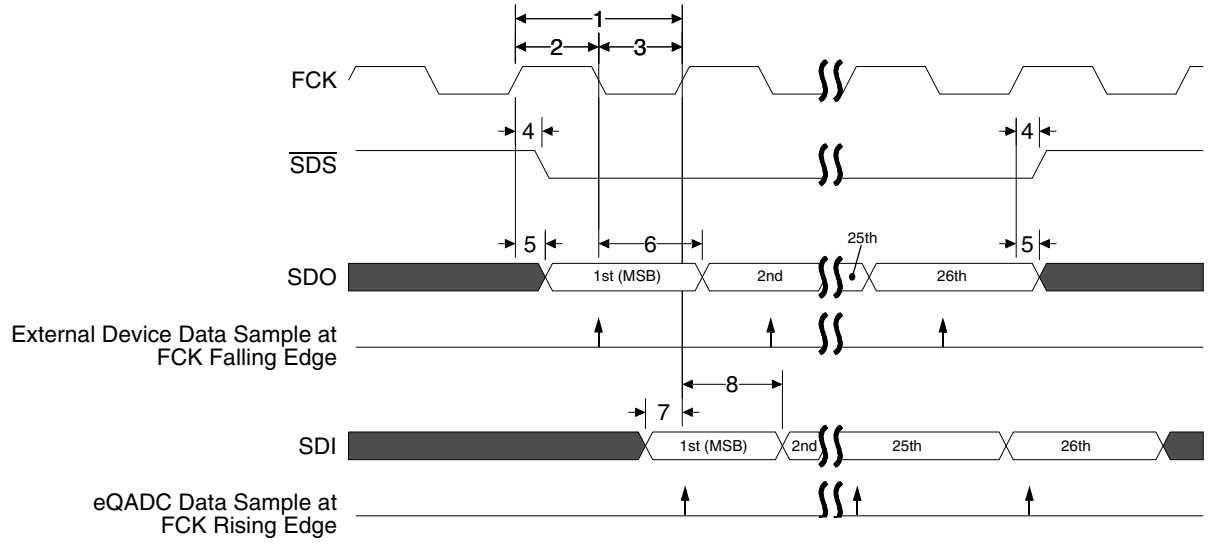


Figure 29. eQADC SSI timing

5 Packages

5.1 Package mechanical data

5.1.1 144 LQFP

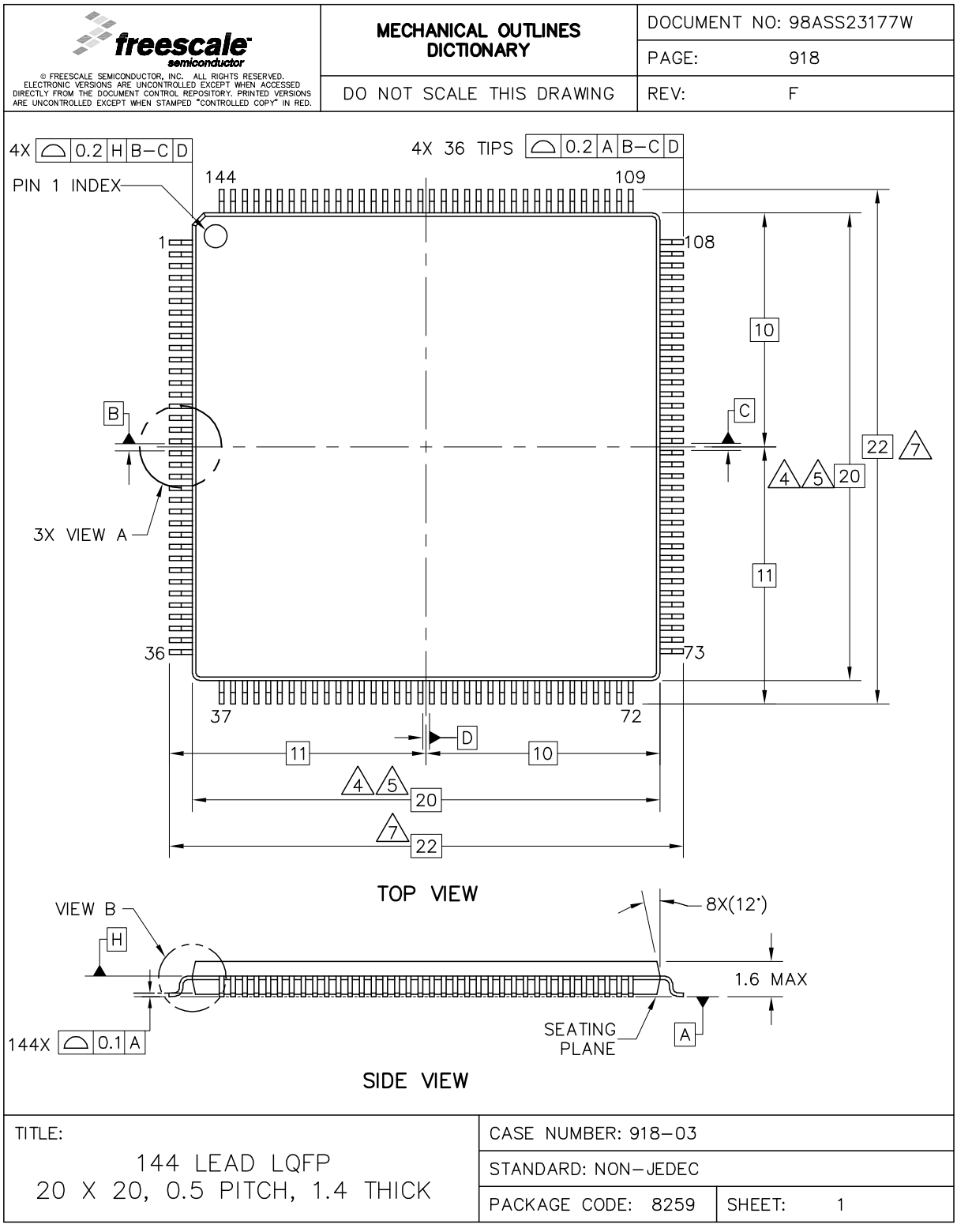


Figure 30. 144 LQFP package mechanical drawing (part 1)

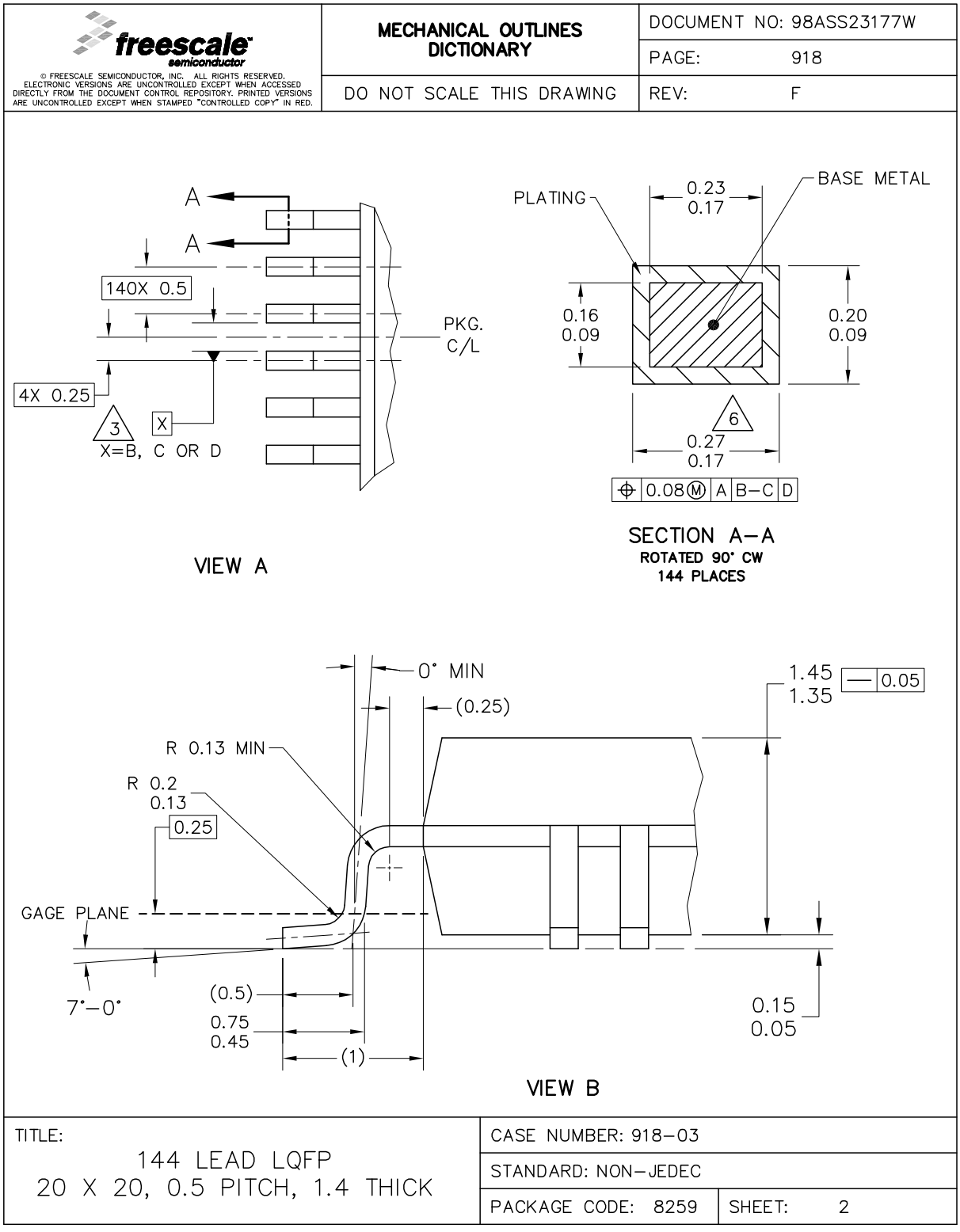


Figure 31. 144 LQFP package mechanical drawing (part 2)

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23177W
		PAGE: 918
	DO NOT SCALE THIS DRAWING	REV: F

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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.
5. THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.
7. THIS DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

TITLE:	CASE NUMBER: 918–03	
144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK	STANDARD: NON–JEDEC	
	PACKAGE CODE: 8259	SHEET: 3

Figure 32. 144 LQFP package mechanical drawing (part 3)

5.1.2 176 LQFP

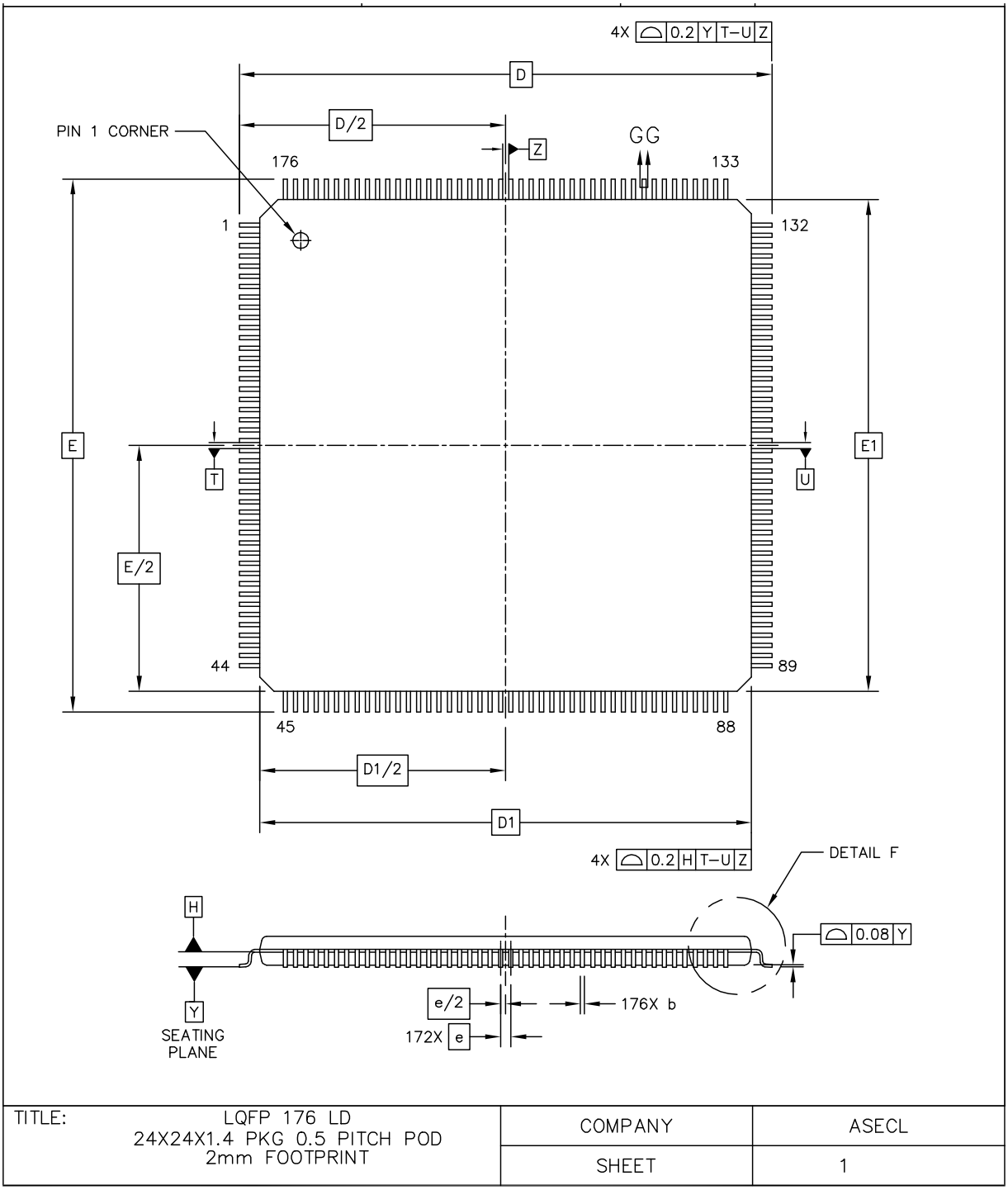

Figure 33. 176 LQFP package mechanical drawing (part 1)

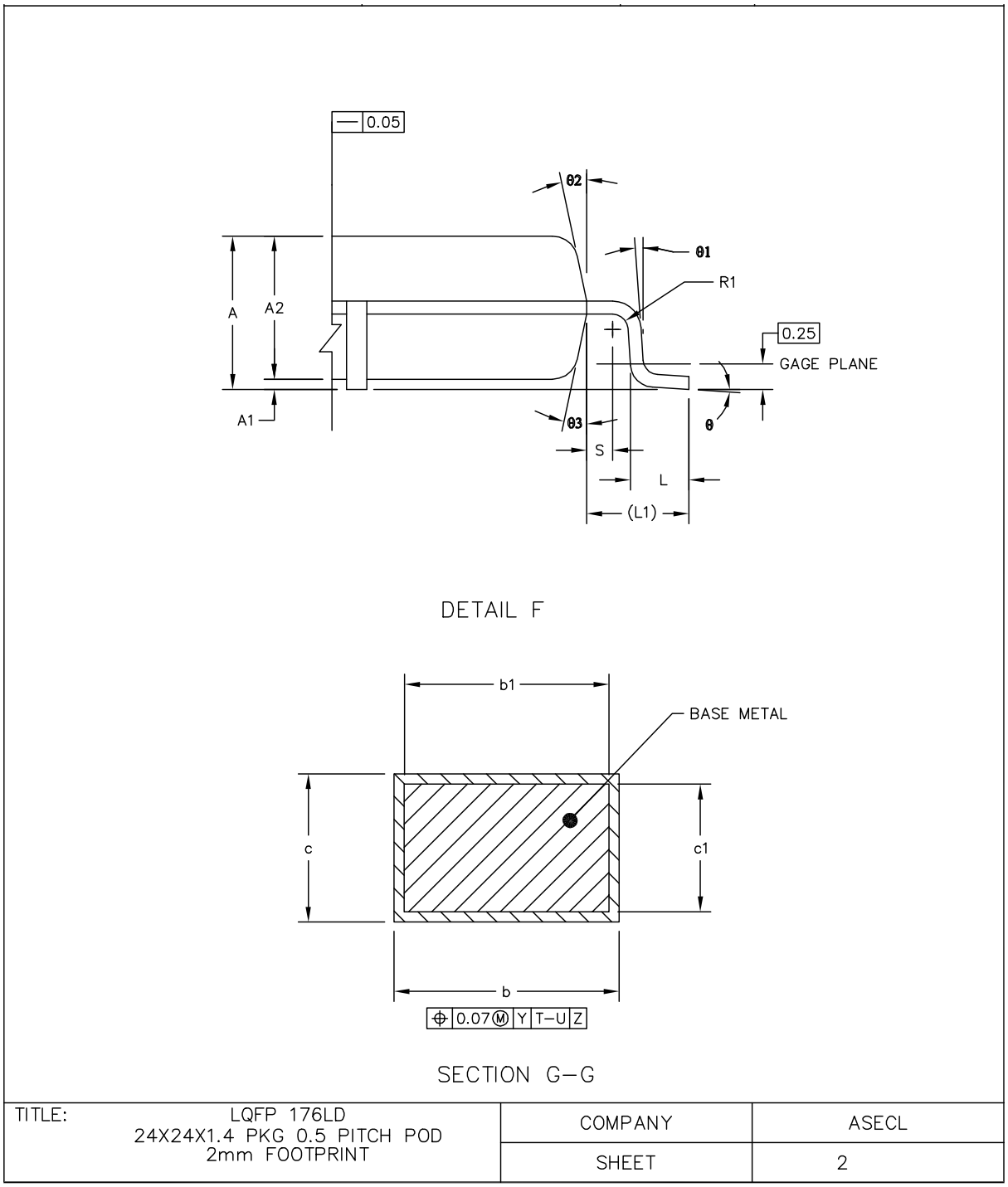

Figure 34. 176 LQFP package mechanical drawing (part 2)

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.

DIM	MIN	NOM	MAX
A	---		1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
b	0.17	0.22	0.27
b1	0.17	0.2	0.23
c	0.09		0.2
c1	0.09		0.16
D		26 BSC	
D1		24 BSC	
e		0.5 BSC	
E		26 BSC	
E1		24 BSC	
L	0.45	0.6	0.75

DIM	MIN	NOM	MAX
L1		1 REF	
R1	0.08		---
R2	0.08		0.2
S		0.2 REF	
θ	0°	3.5°	7°
θ1	0°		---
θ2	11°	12°	13°
θ3	11°	12°	13°

DIM	MIN	NOM	MAX

UNIT	DIMENSION AND TOLERANCES	REFERANCE DOCUMENT
MM	ASME Y14.5M	64-06-280-1392

TITLE:	COMPANY	ASECL
LQFP 176LD 24X24X1.4 PKG 0.5 PITCH POD 2mm FOOTPRINT	SHEET	3

Figure 35. 176 LQFP package mechanical drawing (part 3)

5.1.3 208 MAPBGA

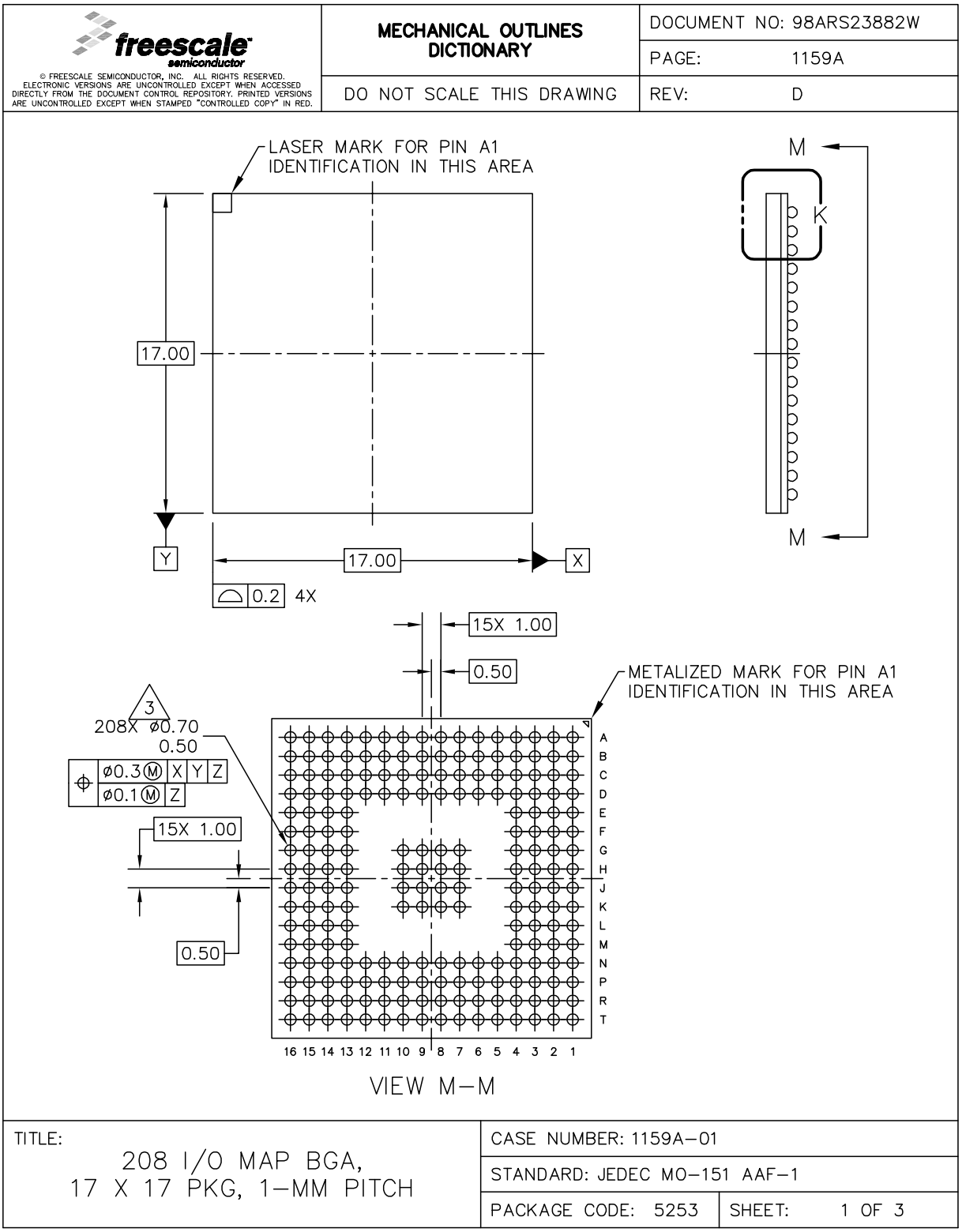

Figure 36. 208 MAPBGA package mechanical drawing (part 1)

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ARS23882W
		PAGE: 1159A
	DO NOT SCALE THIS DRAWING	REV: D

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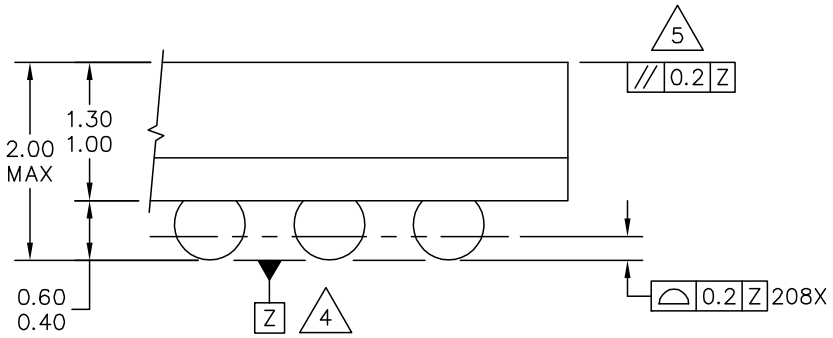

DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	CASE NUMBER: 1159A–01	
	STANDARD: JEDEC MO–151 AAF–1	
	PACKAGE CODE: 5253	SHEET: 2 OF 3

Figure 37. 208 MAPBGA package mechanical drawing (part 2)

6 Ordering information

Table 39 shows the orderable part numbers for the MPC5634M series.

Table 39. Orderable part number summary

Part Number	Flash/SRAM (Kbytes)	Package	Speed (MHz)
SPC5632MF0MLQA6	768 / 48	144 LQFP Pb-free	60
SPC5632MF0MLQA4	768 / 48	144 LQFP Pb-free	40
SPC5633MF0MMGA8	1024 / 64	208 MAPBGA Pb-free	80
SPC5633MF0MLUA8	1024 / 64	176 LQFP Pb-free	80
SPC5633MF0MLQA8	1024 / 64	144 LQFP Pb-free	80
SPC5633MF0MMGA6	1024 / 64	208 MAPBGA Pb-free	60
SPC5633MF0MLUA6	1024 / 64	176 LQFP Pb-free	60
SPC5633MF0MLQA6	1024 / 64	144 LQFP Pb-free	60
SPC5633MF0MLQA4	1024 / 64	144 LQFP Pb-free	40
SPC5634MF0MMGA8	1536 / 94	208 MAPBGA Pb-free	80
SPC5634MF0MLUA8	1536 / 94	176 LQFP Pb-free	80
SPC5634MF0MLQA8	1536 / 94	144 LQFP Pb-free	80
SPC5634MF0MMGA6	1536 / 94	208 MAPBGA Pb-free	60
SPC5634MF0MLUA6	1536 / 94	176 LQFP Pb-free	60
SPC5634MF0MLQA6	1536 / 94	144 LQFP Pb-free	60

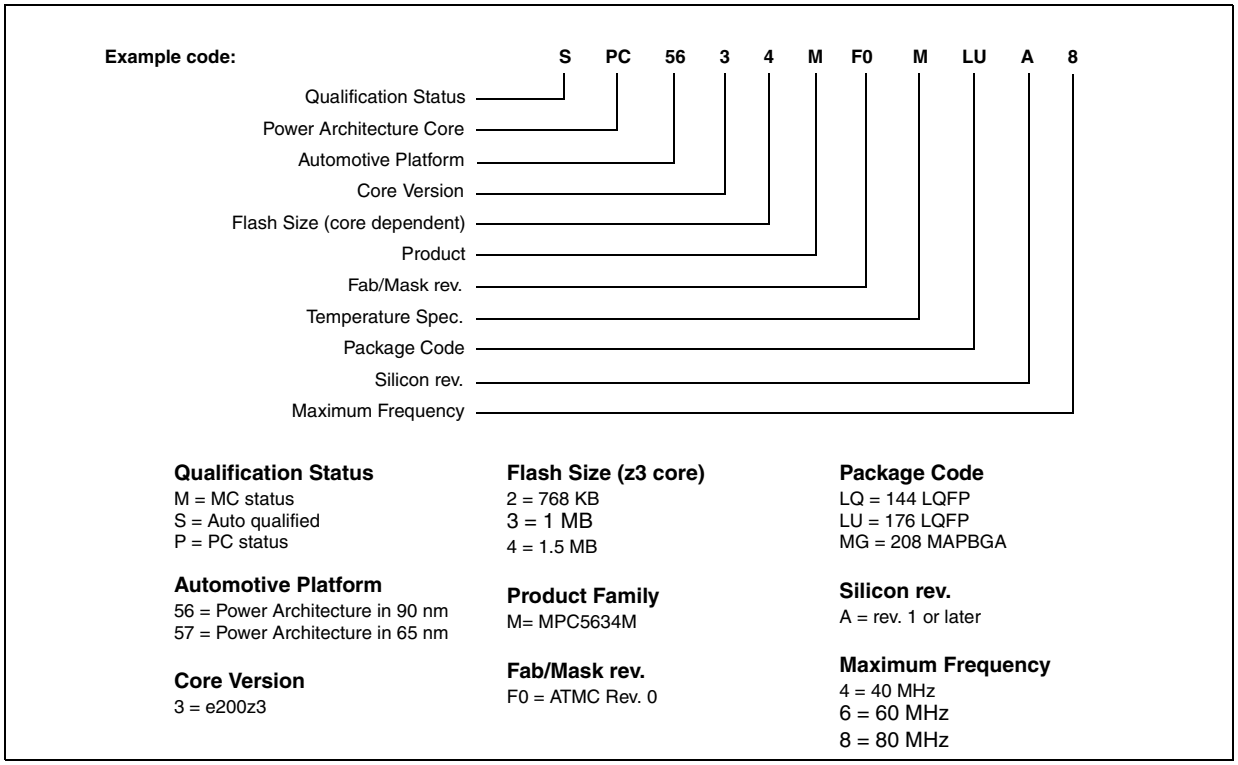

Figure 38. Commercial product code structure

7 Document revision history

Table 40 summarizes revisions to this document.

Table 40. Revision history

Revision	Date	Description of Changes
Rev. 1	4/2008	Initial release
Rev. 2	12/2008	• Maximum amount of flash increased from 1 MB to 1.5 MB. Flash memory type has changed. Rev. 1 and later devices use LC flash instead of FL flash. • Additional packages offered—now includes100 LQFP and 176 LQFP. Please note that the pinouts can vary for the same package depending on the amount of flash memory included in the device. • Device comparison table added. • Feature details section added • Signal summary table expanded. Now includes PCR register numbers and signal selection values and pin numbers for all production packages. • Electrical characteristics updated. • DSPI timing data added for 40 MHz and 60 MHz. • Thermal characteristics data updated. Data added for 100- and 176-pin packages. • DSPI LVDS pad specifications added.
Rev. 3	2/2009	Electrical characteristics updated • Flash memory electrical characteristics updated for LC flash • Power management control (PMC) and Power on Reset (POR) specifications updated • EMI characteristics data added • Maximum ratings updated • I/O pad current specifications updated • I/O Pad VRC33 current specifications added • Temperature sensor electrical characteristics added Pad type added to “Voltage” column of signal summary table Many signal names have changed to make them more understandable • DSPI: PCS_C[n] is now DSPI_C_PCS[n]; SOUT_C is now DSPI_C_SOUT, SIN_C is now DSPI_C_SIN, and SCK_C is now DSPI_C_SCK • CAN: CNTXB is now CAN_B_TX and CNRXB is now CAN_B_RC • SCI: RXDB is now SCI_B_RX and TXDB is now SCI_B_TX • In cases where multiple instances of the same IP block is incorporated into the device, e.g., 2 SCI blocks, the above nomenclature applies to all blocks “No connect” pins on pinouts clarified • Pins labelled “NIC” have no internal connection and should be tied to ground • Pins labelled “NC” are not functional pins but may be connected to internal circuits They are to be left floating Some of the longer multiplexed signal names appearing on pinouts have been moved to the inside of the package body to avoid having to use smaller fonts Orderable parts table updated Part number decoder added

Table 40. Revision history (continued)

Revision	Date	Description of Changes
Rev.4	12/2009	208-pin MAPBGA ballmap for the MPC5633M (1024 KB flash memory) has changed. Power Management Control (PMC) and Power On Reset (POR) electrical specifications updated Temperature sensor data added Specifications now indicate how each controller characteristic parameter is guaranteed. I/O pad current specifications updated I/O Pad VRC33 current specifications updated PAD AC characteristics updated VGA gain specifications added to eQADC electrical characteristics DC electrical specifications updated: • Footnote added to RPUPD100K and RPUPD200K: When the pull-up and pull-down of the same nominal 200 KΩ or 100 KΩ value are both enabled, assuming no interference from other devices, the resulting pad voltage will be 0.5*VDDE ± 2.5% • I_{OL} condition added to V_{OL_LS}. • I_{OH} condition added to V_{OH_LS}. • Minimum V_{OH_LS} is 2.3 V (was 2.7 V). • Separate I_{DDPLL} removed from I_{DD} spec because we can only measure I_{DD} + I_{DDPLL}. I_{DD} increased by 15 mA (to 195 mA) to account for I_{DDPLL}. I_{DD} now documented as I_{DD} + I_{DDPLL}. Footnote added detailing runtime configuration used to measure I_{DD} + I_{DDPLL}. • Specifications for I_{DDSTBY} and $I_{DDSTBY150}$ reformatted to make more clear. • V_{STBY} is now specified by two ranges. The area in between those ranges is indeterminate. LVDS pad specifications updated: • Min value for V_{OD} at SRC=0b01 is 90 mV (was 120); and 160 mV (was 180) at SRC = 0b10 Changes to Signal Properties table: • VDDE7 removed as voltage segment from Calibration bus pins. Calibration bus pins are powered by VDDE12 only. • GPIO[139] and GPIO[87] pins changed to Medium pads • Some signal names have changed on 176-pin QFP package pinout: “CAL_x” signals renamed to “ALT_x”. Changes to Pad Types table: • Column heading changed from “Voltage” to “Supply Voltage” • MultiV pad high swing mode voltage changed to 3.0 V – 5.25 V (was 4.5 V – 5.25 V) • MultiV pad low swing mode voltage changed to 4.5 V – 5.25 V (was 3.0 V – 3.6 V) Signal details table added Power/ground segmentation table added 100-pin package is no longer available

Table 40. Revision history (continued)

Revision	Date	Description of Changes
Rev. 5	04/2010	Updates to features list: • MMU is 16-entry (previously noted as 8-entry) • ECSM features include single-bit error correction reporting • eTPU2 is object code compatible with previous eTPU versions Updates to feature details: • Programming feature: eTPU2 channel flags can be tested Pinout/ballmap changes: 144 pin LQFP package: • Pin 46 is now VDDEH1B (was VDDEH4A) • Pin 61 is now VDDEH6A (was VDDEH4B) 176 pin LQFP package (1.5M devices) • Pin 55 is now VDDEH1B (was VDDEH4A) • Pin 74 is now VDDEH6A (was VDDEH4B) 176 pin LQFP package (1.5M devices) • Pin 55 is now VDDEH1B (was VDDEH4A) • Pin 74 is now VDDEH6A (was VDDEH4B) 208 ball BGA package (all devices) Ball N9 changed to VDDEH1/6 (was VDDEH6). In a future revision of the device this may be changed to NC (no connect). Changes to calibration ball names on devices with 1 MB flash memory: • CAL_MDO0 changed to ALT_MDO0 • CAL_MDO1 changed to ALT_MDO1 • CAL_MDO2 changed to ALT_MDO2 • CAL_MDO3 changed to ALT_MDO3 • CAL_MSEO0 changed to ALT_$\overline{\text{MSEO0}}$ • CAL_MSEO1 changed to ALT_$\overline{\text{MSEO1}}$ • CAL_$\overline{\text{EVTI}}$ changed to ALT_$\overline{\text{EVTI}}$ • CAL_$\overline{\text{EVTO}}$ changed to ALT_$\overline{\text{EVTO}}$ • CAL_MCKO changed to ALT_MCKO Power/ground segment changes: • The following pins are on VDDE7 I/O segment only on the 208-ball BGA package: ALT_MDO[0:3], ALT_MSEO[0:1], ALT_EVTI, ALT_EVTO, ALT_MCKO. • Power segments VDDEH4, VDDEH4A and VDDEH4B have been removed. CLKOUT power segment is VDDE5 (was VDDE12) Thermal characteristics for 176-pin LQFP updated (all parameter values)

Table 40. Revision history (continued)

Revision	Date	Description of Changes
Rev. 5 (cont.)	04/2010	PMC Operating conditions and external regulators supply voltage specifications updated • (2) PMC 5 V supply voltage VDDREG min value is 4.5 V (was 4.75 V) PMC electrical characteristics specifications updated • (1d) Bandgap reference supply voltage variation is 3000 ppm/V (was 1500 ppm/V) • (5a) Nominal 3.3 V supply internal regulator DC output voltage variation at power-on reset min value is Vdd33-8.5% (was unspecified previously) • (5a) Nominal 3.3 V supply internal regulator DC output voltage variation at power-on reset max value is Vdd3+7% (was unspecified previously) • (9a) Variation of POR for rising 5 V VDDREG supply max value is Por5V_r + 50% (was Por5V_r + 35%) • (9c) Variation of POR for falling 5 V VDDREG supply max value is Por5V_f + 50% (was Por5V_f + 35%) • (9c) note added: Minimum loading (<10 mA) for reading trim values from flash, powering internal RC oscillator, and IO consumption during POR. “Core Voltage Regulator Controller External Components Preferred Configuration” circuit diagram updated Changes to DC Electrical Specifications: • Footnote added to V_{DDE}. V_{DDE} must be less than V_{RC33} or there is additional leakage on pins supplied by V_{DDE}. • Low range SRAM standby voltage (V_{STBY}) minimum changed to 0.95 V (was 0.9 V) • Low range SRAM standby voltage (V_{STBY}) maximum changed to 1.2 V (was 1.3 V) • High range SRAM standby voltage (V_{STBY}) minimum changed to 2.0 V (was 2.5 V) • V_{IL_LS} max value (Hysteresis disabled) changed to 0.9 V (was 1.1 V) • V_{OH_LS} min value changed to 2 V (was 2.3 V) • I_{DDSLOW} max value is 50 mA • I_{DDSTOP} max value is 50 mA • I_{DDA} max value is 30 mA (was 15.0 mA) • I_{DD4} and V_{DDEH4} removed—they no longer exist I/O pad average I_{DDE} specifications table updated I/O pad V_{RC33} average I_{DDE} specifications table updated LVDS pad specifications table updated • V_{OS} min value is 0.9 V (was 1.075 V) • V_{OS} max value is 1.6 V (was 1.325 V) Updates to PLLMRFM electrical specifications: • Maximum values for XTAL load capacitance added. The maximum value varies with frequency. • For a 20 MHz crystal the maximum load should be 17 pF. Temperature sensor accuracy is ±10 °C (was ±5 °C) Updates to eQADC conversion specifications (operating): • Offset error without calibration max value is 160 (was 100) • Full scale gain error without calibration min value is –160 (was –120) Changes to Platform flash controller electrical characteristics: • APC, RWSC, WWSC settings vs. frequency of operation table updated

Table 40. Revision history (continued)

Revision	Date	Description of Changes
Rev. 5 (cont.)	04/2010	Changes to flash memory specifications: • T_{BKPRG} 64 KB specification removed (not present in this device) • $T_{64kpperase}$ specification added • Flash module life P/E spec for 32 Kbyte blocks also applies to 64 Kbyte blocks Pad AC specifications (3.3 V) table updated
Rev. 6	04/2010	"Core Voltage Regulator Controller External Components Preferred Configuration" circuit diagram updated. • Clarification added to note: Emitter and collector capacitors (6.8 μF and 10 μF) should be matched (same type) and ESR should be lower than 200 mW. (Added emphasis that only 6.8 μF emitter capacitors need to be matched with collector capacitor. • 220 μF emitter capacitors changed to 220 nF.
Rev. 7	4/2010	No specification or product information changes: • Mechanical outline drawings section renamed to "Packages" and restructured. •
Rev. 8	01/2011	Removed the 208 BGA package from the device-summary table. Revised the "PMC Operating conditions and external regulators supply voltage" table. Revised the "PMC electrical characteristics" table. Revised the pad AC specifications. Revised the "DC electrical specifications" table. Revised the "DSPI LVDS pad specification" table: Revised the "PLLMRFM electrical specifications" table. Change to "Temperature sensor electrical characteristics" table: • Accuracy is guaranteed by production test Revised the "eQADC conversion specifications (operating)" table. Changes to "Calibration bus operation timing" table: • CLKOUT period is guaranteed by production test. All other parameters are guaranteed by design Changes to "Program and erase specifications" table in "Flash memory electrical characteristics" section. • Deleted Bank Program (512KB) (T_{BKPRG}) parameter • TYP P/E values added for 32- and 64 KB blocks and for 128 KB blocks. Changes to Recommended operating characteristics for external power transistor: • VCESAT should be between 200 and 600 mV • VBE should be 0.4V to 1.0V Removed footnote 8 from Vddeh in Maximum ratings. Deleted engineering names for pads in Power UP/DOWN Sequencing Section Changed "sin_c" to DSPI_C_SIN" and "sck_c" to DSPI_C_SCK" on 144 pin LQFP package. Updated the "Electromagnetic Interference Characteristics" table to reflect new parameter levels, test conditions. In the "APC, RWSC, WWSC settings vs. frequency of operation" table, changed 82 MHz entry for WWC from "11" to "01", added an extra row for "All 111 111 11"

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