iC-NT
LIGHT CHAIN PULSE DRIVER

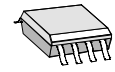
FEATURES

- Adjustable LED pulse operation, set range of 0.4..1A
- Controlled current slew rate enables short light pulses down to 1µs
- LED efficiency degradation compensated by positive current temperature coefficient
- Low standby current; circuit activation by input data
- Low power requirement for external set resistor
- Control logic with 3-step shift register
- Compatible to CMOS levels
- Data output buffer with built-in 120Ω wave impedance adaption
- Single 5V supply
- Thermal shutdown and power-down reset
- ESD protection
- Small outline package SO8
- Suited for high-risk applications according to IEC 1496-1
- ◊ Option: Extended temperature range of -20°C..85°C

APPLICATIONS

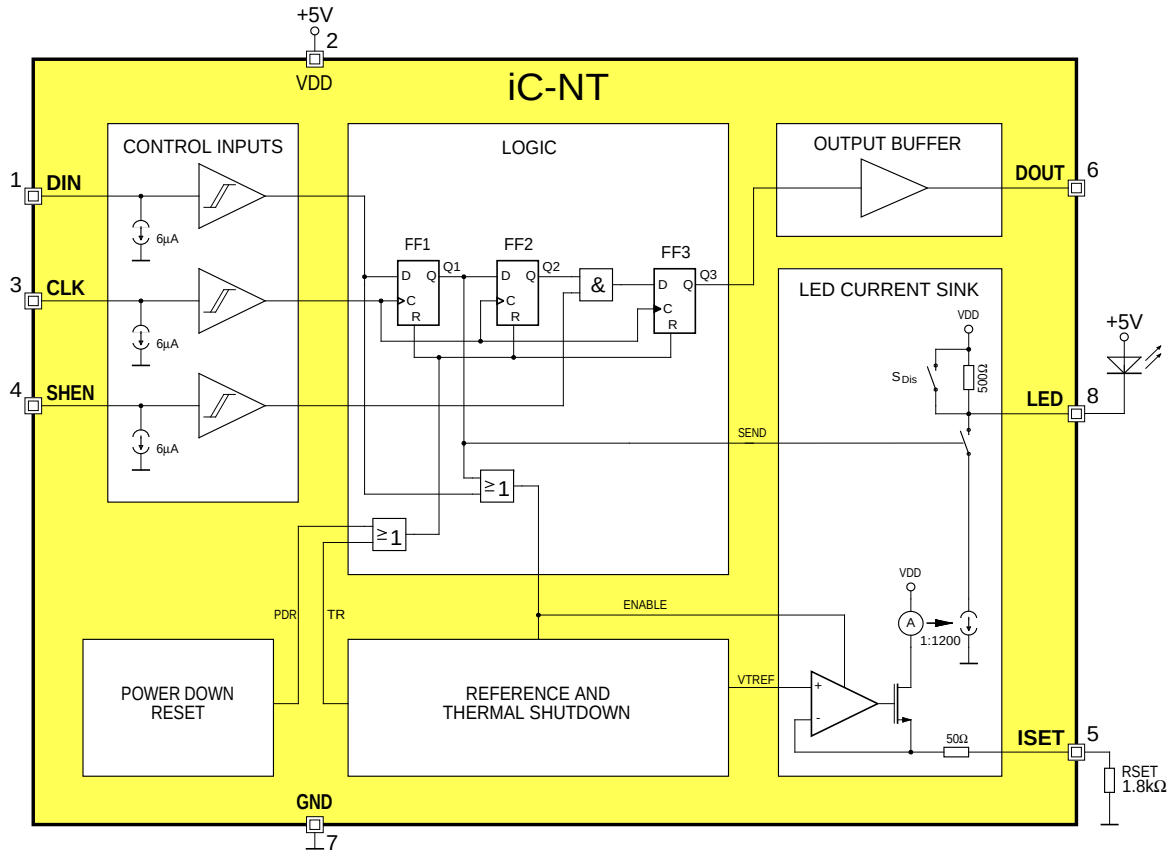
- Electro-sensitive protective equipment (ESPE)
- Light curtain LED driver
- Light barrier LED driver

PACKAGES



SO8

BLOCK DIAGRAM



Rev A0

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DESCRIPTION

The iC-NT device is an LED pulse driver for light barrier applications, especially light chain circuitries.

The device, which is controlled by a shift register logic, features an adjustable LED current sink with a set range of 0.4..1A (at room temperature). For chain circuitries with several transmitters in operation, the internal set of three flipflops enables a secure beam and data shift control, free of race conditions.

The decrease in LED efficiency with a rise in temperature is almost compensated by a positive temperature coefficient of the current sink. In order to generate steep light pulses, the LED switch off is actively supported by the discharge of its junction capacitance. The duration of this LED short-circuiting is controlled by a monoflop. In the event of a quick follow-up light pulse, a monoflop reset is performed automatically to protect against cross currents.

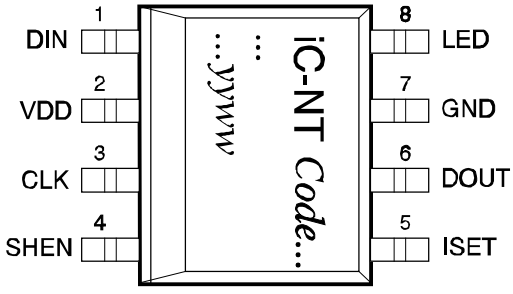
The driver stage for the LED output prepares for a light pulse when DIN reads a high signal; synchronized with the CLK leading edge, the first flipflop transfers the DIN data to Q1 and powers up the LED sink.
Since the chain is loaded with just one single high bit and DIN is given by the output DOUT of the previous device, input DIN now reads low at the falling edge of CLK. The LED current sink stops the power, at the same time as an internal data shift from Q1 to Q2 occurs. The LED pulse is well-defined by the time difference between two leading edges of the clock signal CLK. The second falling edge of CLK triggers the third flipflop and activates the next device in the chain via DOUT if enabled by SHEN.

Since only one device is activated at a time, several iC-NT drivers may share one resistor, RSET, to define the LED current value.

The shift register is reset and the LED current sink is turned off in the event of excessive temperature or undervoltage. Protective diodes to prevent destruction through ESD are also included. The iC-NT device fulfills safety requirements according to IEC 1496-1. An extended temperature range of -20°C..85°C is also available as an option.

PACKAGE SO8 to JEDEC Standard

PIN CONFIGURATION SO8
(top view)



PIN FUNCTIONS

No.	Name	Function
1	DIN	Data Input
2	VDD	Supply Voltage 5V
3	CLK	Clock
4	SHEN	Shift Enable
5	ISET	Current Adjust, attachement RSET
6	DOUT	Data Output
7	GND	Ground
8	LED	Pulse Output, LED Cathode

ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
G001	VDD	Supply Voltage			-0.5	7	V
G002	V()	Voltage at Inputs DIN, CLK, SHEN			-0.5	VDD+0.5	V
G003	V()	Voltage at DOUT, ISET, LED			-0.5	VDD+0.5	V
E001	Vd()	ESD Susceptibility at VDD, ISET and digital inputs/outputs	MIL-STD-883, HBM 100pF discharged through 1.5kΩ			2	kV
E002	Vd(LED)	ESD Susceptibility at LED	with standard circuitry, HBM 100pF discharged through 1.5kΩ	5		2	kV
TG1	Tj	Junction Temperature			-40	150	°C
TG2	Ts	Storage Temperature			-40	150	°C

THERMAL DATA

Operating Conditions: VDD= 4.75..5.5V

Item	Symbol	Parameter	Conditions	Fig.	Min.	Typ.	Max.	Unit
T1	Ta	Operating Ambient Temperature Range (Extended temperature range of -20..85°C on request)			0		70	°C
T2	Rthja	Thermal Resistance Junction to Ambient	surface mounted without special cooling areas				170	K/W

All voltages are referenced to ground unless otherwise noted.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions:
VDD= 4.75..5.5V, RSET= 1.8..4.5kΩ, Tj= -20..125°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Total Device									
001	VDD	Permissible Supply Voltage Range				4.75		5.5	V
002	I(VDD)	Supply Current in VDD (Standby)	Analog section disabled; DIN= lo, CLK,SHEN= hi or lo, logic levels: lo= 0..0.45V, hi= VDD-0.45V..VDD					60	µA
003	I(VDD)	Supply Current in VDD	Analog section disabled; DIN= lo CLK, SHEN hi or lo, logic levels: lo= 22%VDD, hi= 78%VDD					1	mA
004	I(VDD)	Supply Current in VDD	Analog section enabled; RSET≥ 1.8kΩ, LED current sink off	-20 27 85 Toff				7.5 7.5 8.5 1.0	mA mA mA mA
005	I(VDD)	Supply Current in VDD	Analog section enabled; RSET≥ 1.8kΩ, LED current sink on	-20 27 85 Toff				25 25 26 1.0	mA mA mA mA
006	VDDon	Turn-on Threshold VDD (Power-on Release)						4.3	V
007	VDDoff	Undervoltage Threshold at VDD (Power-down Reset)	decreasing voltage VDD			2.7			V
008	VDDhys	Hysteresis	VDDhys= VDDon-VDDoff			100			mV
009	Vc()hi	Clamp Voltage hi at DIN, CLK, SHEN, DOUT, ISET, LED	Vc()hi= V()-VDD, I()= 10mA			0.4		1.25	V
010	Vc()lo	Clamp Voltage lo at DIN, CLK, SHEN, DOUT, ISET, LED	I()= -10mA, VDD= 0V other pins open			-1.25		-0.4	V
011	Toff	Shutdown Temperature				110		150	°C
LED Current Sink									
101	V(ISET)	Reference Voltage at ISET		-20 27 85 Toff			1.27 1.50 1.79 0		V V V V
102	TC(ISET)	Temperature Coefficient of Reference Voltage at ISET		27		0.30	0.33	0.36	%/K
103	CR()	Current Ratio I(LED) / -I(ISET)					1200		
104	I(LED)	LED Pulse Current	duty cycle I(LED)≤ 1%, RSET= 1.8kΩ, V(LED)= 1.0V..VDD	-20 27 85 Toff		0.65 0.82 0.93	0.85 1.00 1.2 0	1.06 1.18 1.48	A A A A
105	I(LED)	LED Pulse Current	duty cycle I(LED)≤ 1%, RSET= 4.5kΩ, V(LED)= 0.85V..VDD	-20 27 85 Toff		0.26 0.33 0.37	0.34 0.40 0.48 0	0.44 0.48 0.61	A A A A
106	tr(LED)	LED Current Rise Time			3			150	ns
107	tf(LED)	LED Current Fall Time			3			150	ns
108	tdis(LED)	LED Discharge Duration	LED shutdown, switch Sdis closed					400	ns

ELECTRICAL CHARACTERISTICS

Operating Conditions:
VDD= 4.75..5.5V, RSET= 1.8..4.5kΩ, Tj= -20..125°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
LED Current Sink (continued)									
109	Ir(LED)	LED Discharge Current	V(VDD/LED)= 1.5V				200		mA
110	Rpu(LED)	Pull-up Resistor at LED				300	500	850	Ω
Control Inputs DIN, SHEN, CLK									
201	Vt()hi	Threshold Voltage hi						78	%VDD
202	Vt()lo	Threshold Voltage lo				22			%VDD
203	Vhys()	Schmitt-Trigger Input Hysteresis				400			mV
204	Ipd()	Pull-Down Current	V()= 5.0V			3	6	12	µA
Output Buffer DOUT									
301	Vs()hi	Saturation Voltage hi	Vs(DOUT)hi= VDD-V(DOUT), I(DOUT)= -4mA					0.4	V
302	Vs()lo	Saturation Voltage lo	I(DOUT)= 4mA					0.4	V
303	Isc()hi	Short-Circuit Current hi	V(DOUT)= 0V			-100	-40	-20	mA
304	Isc()lo	Short-Circuit Current lo	V(DOUT)= VDD			20	40	100	mA
305	Rout()	Output Resistance	VDD= 5.0V, V(DOUT)= 2.5V			80	120	190	Ω
306	tr()	Rise Time	CL(DOUT)≤ 50pF				20	60	ns
307	tf()	Fall Time	CL(DOUT)≤ 50pF				20	60	ns
Switching Characteristics									
401	tphl(CLK-LED)	LED Pulse Turn-on Delay	DIN= hi, CLK lo→hi until I(LED)= 10% set value		4			100	ns
402	tplh(CLK-LED)	LED Pulse Turn-off Delay	DIN= lo, CLK lo→hi until I(LED)= 90% set value		4			80	ns
403	tplh(CLK-DOUT)	DOUT Switch Delay hi	CL(DOUT)≤ 50pF, CLK hi→lo		2		25	60	ns
404	tphl(CLK-DOUT)	DOUT Switch Delay lo	CL(DOUT)≤ 50pF, CLK hi→lo		2		25	60	ns

OPERATING REQUIREMENTS: Logic

Operating Conditions: VDD= 4.75..5.5V, Ta= 0..70°C, CL()= 50pF,
input levels lo= 0..0.45V, hi= VDD-0.45V..VDD, see Fig. 1 for reference levels and waveforms

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
I1	t_{en}	Activation Time (standby to operation): DIN lo→hi before CLK lo→hi		4	5		µs
I2	t_{set1}	Setup time: DIN stable before CLK lo→hi		2	50		ns
I3	t_{hold1}	Hold time: DIN stable after CLK lo→hi		2	50		ns
I4	t_{set2}	Setup time: SHEN stable before CLK hi→lo		2	50		ns
I5	t_{hold2}	Hold time: SHEN stable after CLK hi→lo		2	50		ns
I6	t_w	LED Pulse time: 1st to 2nd CLK lo→hi		4	1.0		µs

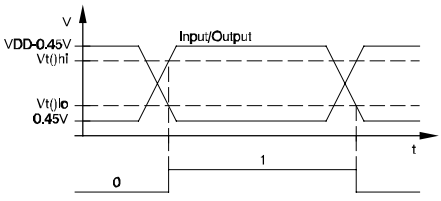


Fig. 1: Reference levels

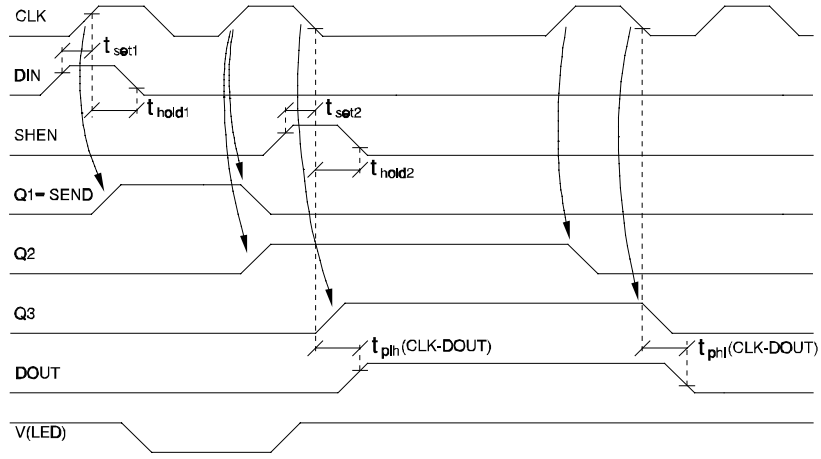


Fig. 2: Timing characteristics

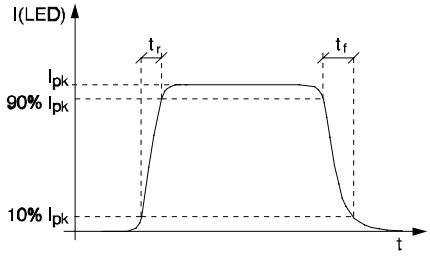


Fig. 3: LED Current Pulse

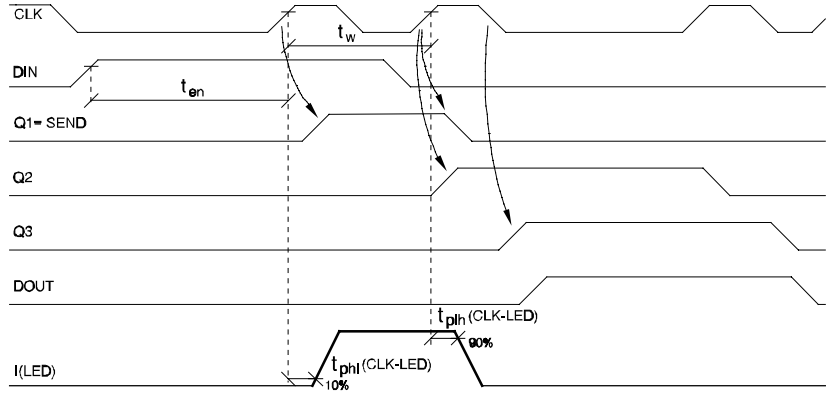


Fig. 4: Chain configuration (SHEN= hi),
LED pulse definition by clock signal

APPLICATIONS INFORMATION

Light curtain

The circuit in Figure 5 shows iC-NT chained to a light curtain where consecutive LEDs emit clock-driven light pulses.

When discussing the function of iC-NT, it is assumed that all flipflops in IC1..ICn have been reset, for example after the operating voltage has been switched on. The signal DIN1= hi activates the IC1 current sink which is switched to LED1 with the CLK rising edge. With DIN1= lo, the next CLK rising edge resets FF1, turns off the LED and deactivates the current sink in IC1. Simultaneously, FF1 sends the stored information to FF2. FF3 also accepts this information via the CLK trailing edge (provided that SHEN= hi) and activates the current sink in the next component, IC2, via the output driver. The pulse diagram in Figure 6 is also valid for the subsequent components in the chain, i.e. the ICs switched as a light curtain make up a clock-driven shift register which passes on the input information.

The typical timing of a CLK signal, shown in Figure 6, is characterized by two successive pulses which determine the length of a light pulse t_W from 1..3µs, followed by a longer activation time of t_{en} ≥5µs. In general, the CLK pulse interval is determined and lengthened by the activation time required by the receiver or by more extensive, system-set default options.

Because of the high LED pulse currents, the PCB layout of the light curtain sender must be designed to avoid large voltage drops on the supply lines. The high, short-term pulse current is provided by back-up capacitors C1..Cn at the pulse driver ICs; these should have a low inductance due to the high current increase rate. The leads to the LED anode and to iC-NT's GND pin should be as short as possible. The capacitors selected should ensure that the voltage drop caused by the light pulse is less than 1V, i.e. that C1..Cn= 1µF for a light pulse of 1A x 1µs, for example. In practice, the voltage at the IC drops much less during a light pulse, as charge from the back-up capacitors of neighboring ICs also flows into the chip. A low-inductance capacitance distribution can be achieved more economically by placing further smaller capacitors in parallel.

Since only one device is activated at a time within one section of a light curtain, several iC-NTs may share the external resistor RSET, needed to set the pulse current. This parallel chain circuit should be limited to ca. 5 ICs due to the increasing capacitive loading at pin ISET.

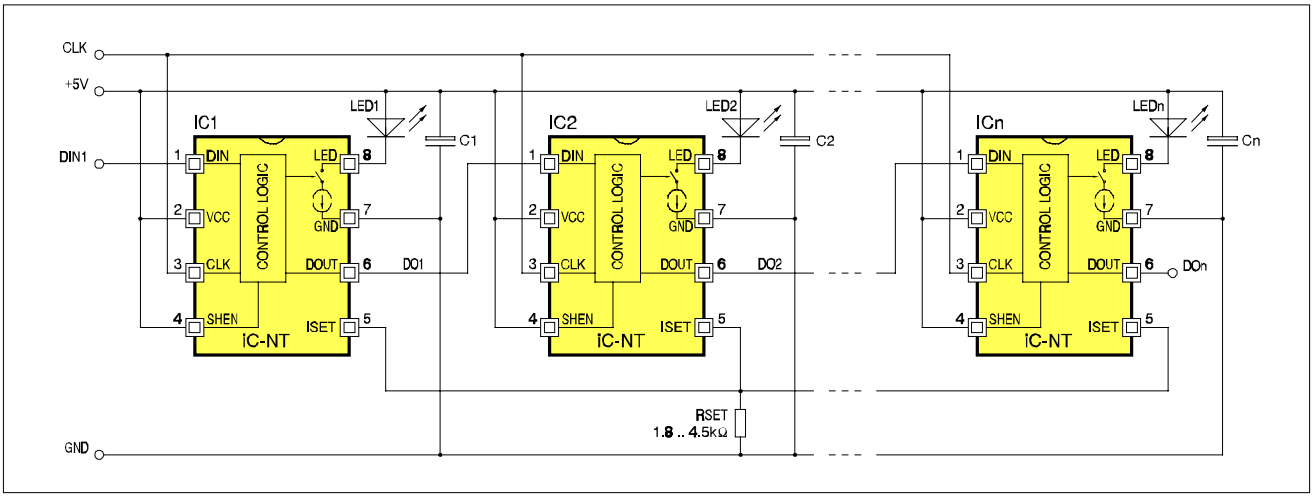


Fig. 5: Schematic of a Chain Configuration

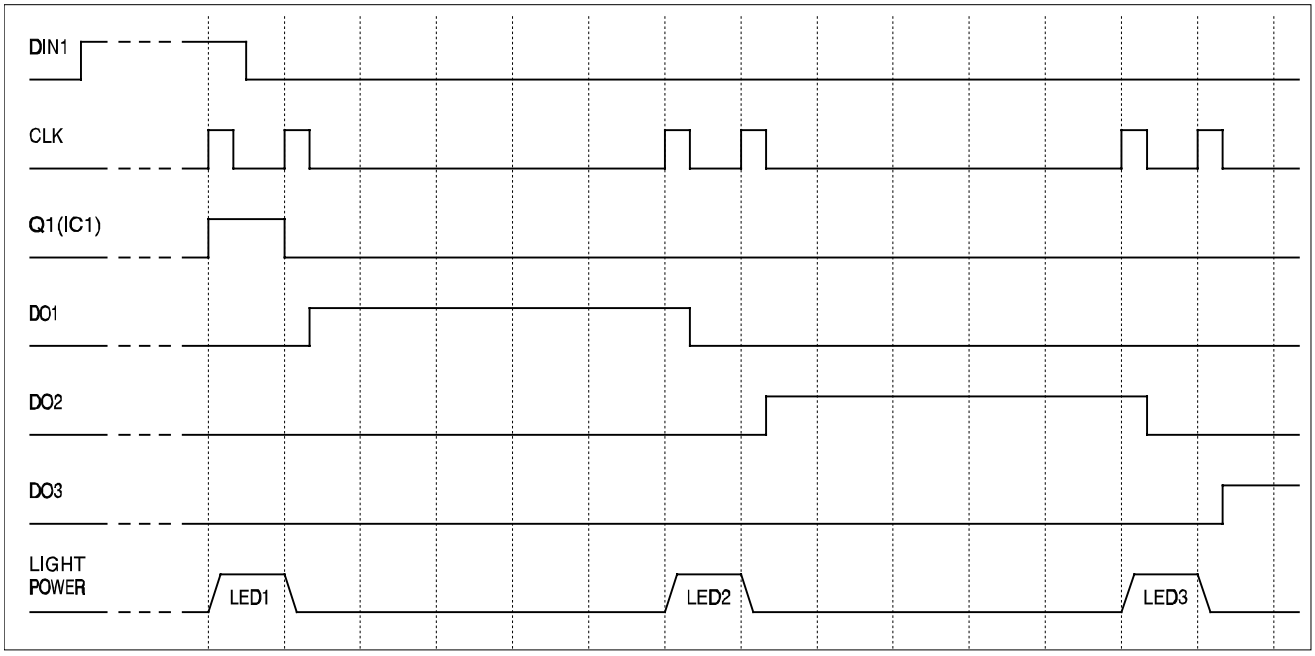


Fig. 6: Signals of the Chain Configuration of Figure 5

ORDERING INFORMATION

Type	Package	Order designation
iC-NT	SO8	iC-NT-SO8

For information about prices, terms of delivery, options for other case types, etc., please contact:

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