



REVISION HISTORY

| <u>Revision</u> | <u>Description</u> | <u>Issue Date</u> |
|-----------------|---|-------------------------------|
| Rev. 1.0 | Initial Issue | Jul.25.2004 |
| Rev. 1.1 | Delete Icc1 Spec. | Sep.21.2004 |
| Rev. 2.0 | Adding -10ns Spec. | Aug.30.2005 |
| Rev. 2.1 | Revised V_{TERM} to V_{T1} and V_{T2} Revised Test Condition of I_{SB1}/I_{DR} Added LL Spec. | Feb.2.2009 |
| Rev.2.2 | Revised Test Condition of I_{CC}/I_{SB} Revised FEATURES & ORDERING INFORMATION <u>Lead free and green package available to Green package available</u> Deleted T_{SOLDER} in <u>ABSOLUTE MAXIMUM RATINGS</u> Added packing type in <u>ORDERING INFORMATION</u> | Feb.2.2009 Apr.17.2009 |



FEATURES

- Fast access time : 10/12/15ns
- Low power consumption:
Operating current : 75/70/65mA (TYP.)
Standby current : 0.6mA (TYP.)
1μA (TYP.) LL -version
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 32-pin 300 mil SOJ
32-pin 8mm x 20mm TSOP-I
32-pin 8mm x 13.4mm STSOP

GENERAL DESCRIPTION

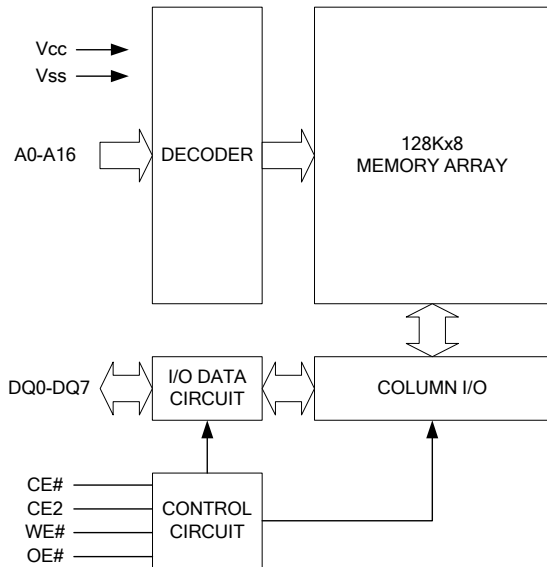
The LY61L1024 is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The LY61L1024 is well designed for very high speed system applications, and particularly well suited for battery back-up nonvolatile memory application.

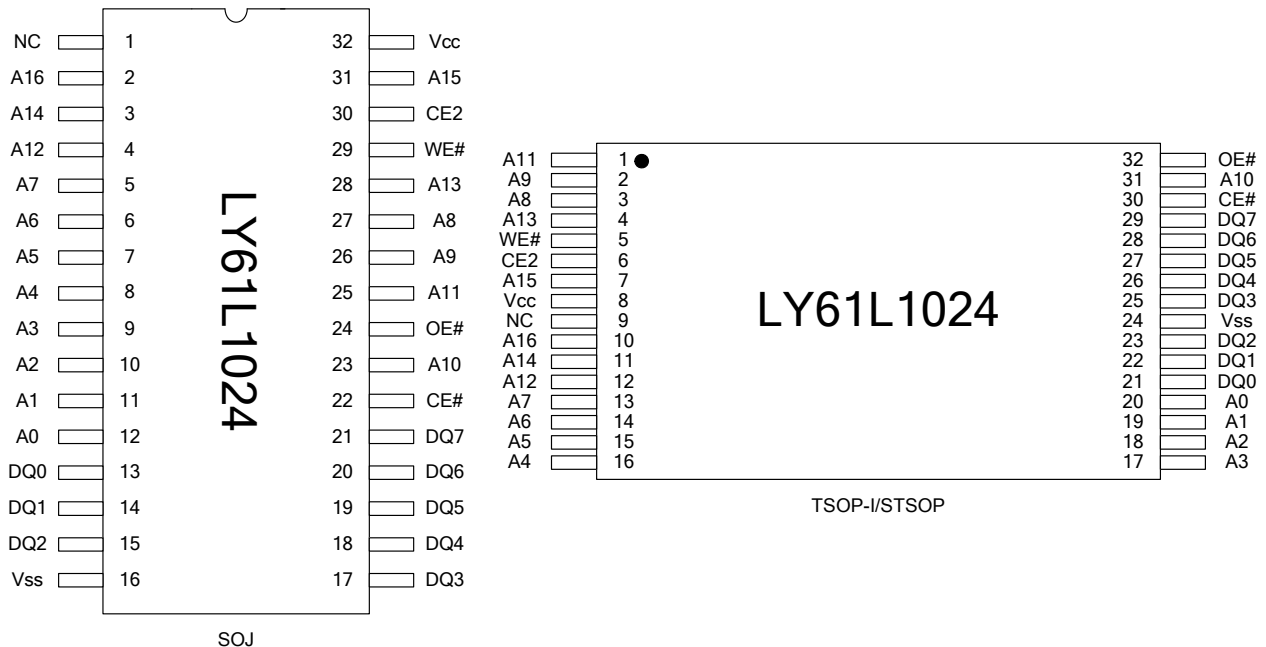
The LY61L1024 operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

| Product Family | Operating Temperature | Vcc Range | Speed | Power Dissipation | |
|----------------|-----------------------|-------------|---------|----------------------------------|-----------------------------------|
| | | | | Standby(I _{SB1} , TYP.) | Operating(I _{CC} , TYP.) |
| LY61L1024 | 0 ~ 70°C | 3.15 ~ 3.6V | 10ns | 0.6mA | 75mA |
| LY61L1024 | 0 ~ 70°C | 3.0 ~ 3.6V | 12/15ns | 0.6mA | 70/65mA |
| LY61L1024(E) | -20 ~ 80°C | 3.15 ~ 3.6V | 10ns | 0.6mA | 75mA |
| LY61L1024(E) | -20 ~ 80°C | 3.0 ~ 3.6V | 12/15ns | 0.6mA | 70/65mA |
| LY61L1024(LL) | 0 ~ 70°C | 3.15 ~ 3.6V | 10ns | 1μA | 75mA |
| LY61L1024(LL) | 0 ~ 70°C | 3.0 ~ 3.6V | 12/15ns | 1μA | 70/65mA |
| LY61L1024(LLE) | -20 ~ 80°C | 3.15 ~ 3.6V | 10ns | 1μA | 75mA |
| LY61L1024(LLE) | -20 ~ 80°C | 3.0 ~ 3.6V | 12/15ns | 1μA | 70/65mA |

FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|-----------|---------------------|
| A0 - A16 | Address Inputs |
| DQ0 - DQ7 | Data Inputs/Outputs |
| CE#, CE2 | Chip Enable Inputs |
| WE# | Write Enable Input |
| OE# | Output Enable Input |
| Vcc | Power Supply |
| Vss | Ground |
| NC | No Connection |

PIN CONFIGURATION




ABSOLUTE MAXIMUM RATINGS*

| PARAMETER | SYMBOL | RATING | UNIT |
|--|------------------|--------------------|------|
| Voltage on Vcc relative to Vss | V _{T1} | -0.5 to 4.6 | V |
| Voltage on any other pin relative to Vss | V _{T2} | -0.5 to Vcc+0.5 | V |
| Operating Temperature | T _A | 0 to 70(C grade) | °C |
| | | -20 to 80(E grade) | °C |
| Storage Temperature | T _{STG} | -65 to 150 | °C |
| Power Dissipation | P _D | 1 | W |
| DC Output Current | I _{OUT} | 50 | mA |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

| MODE | CE# | CE2 | OE# | WE# | I/O OPERATION | SUPPLY CURRENT |
|----------------|-----|-----|-----|-----|------------------|------------------------------------|
| Standby | H | X | X | X | High-Z | I _{SB} , I _{SB1} |
| | X | L | X | X | High-Z | I _{SB} , I _{SB1} |
| Output Disable | L | H | H | H | High-Z | I _{CC} |
| Read | L | H | L | H | D _{OUT} | I _{CC} |
| Write | L | H | X | L | D _{IN} | I _{CC} |

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. ⁴ | MAX. | UNIT | |
|--|------------------------------|--|--------|-------------------|----------------------|------|----|
| Supply Voltage | V _{CC} | | 3.0 | 3.3 | 3.6 | V | |
| Input High Voltage | V _{IH} ¹ | | 2.0 | - | V _{CC} +0.5 | V | |
| Input Low Voltage | V _{IL} ² | | -0.5 | - | 0.6 | V | |
| Input Leakage Current | I _{LI} | V _{CC} ≥ V _{IN} ≥ V _{SS} | -1 | - | 1 | μA | |
| Output Leakage Current | I _{LO} | V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled | -1 | - | 1 | μA | |
| Output High Voltage | V _{OH} | I _{OH} = -4mA | 2.2 | - | - | V | |
| Output Low Voltage | V _{OL} | I _{OL} = 8mA | - | - | 0.4 | V | |
| Average Operating Power supply Current | I _{CC} | Cycle time = Min. CE# = V _{IL} and CE2 = V _{IH} , I _{I/O} = 0mA Others at V _{IL} or V _{IH} | -10 | - | 75 | 120 | mA |
| | | | -12 | - | 70 | 100 | mA |
| | | | -15 | - | 65 | 90 | mA |
| Standby Power Supply Current | I _{SB} | CE# = V _{IH} or CE2 = V _{IL} Others at V _{IL} or V _{IH} | - | 3 | 20 | mA | |
| | I _{SB1} | CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V | Normal | - | 0.6 | 3 | mA |
| | | CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Others at 0.2V or V _{CC} -0.2V | LL | - | 1 | 30 | μA |

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

| PARAMETER | SYMBOL | MIN. | MAX | UNIT |
|--------------------------|------------------|------|-----|------|
| Input Capacitance | C _{IN} | - | 6 | pF |
| Input/Output Capacitance | C _{I/O} | - | 8 | pF |

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

| | |
|--|---|
| Input Pulse Levels | 0.2V to V _{CC} - 0.2V |
| Input Rise and Fall Times | 3ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -4mA/8mA |

AC ELECTRICAL CHARACTERISTICS
(1) READ CYCLE

| PARAMETER | SYM. | LY61L1024-10 | | LY61L1024-12 | | LY61L1024-15 | | UNIT |
|------------------------------------|--------------------|--------------|------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Read Cycle Time | t _{RC} | 10 | - | 12 | - | 15 | - | ns |
| Address Access Time | t _{AA} | - | 10 | - | 12 | - | 15 | ns |
| Chip Enable Access Time | t _{ACE} | - | 10 | - | 12 | - | 15 | ns |
| Output Enable Access Time | t _{OE} | - | 5 | - | 6 | - | 7 | ns |
| Chip Enable to Output in Low-Z | t _{CLZ} * | 2 | - | 3 | - | 4 | - | ns |
| Output Enable to Output in Low-Z | t _{OLZ} * | 0 | - | 0 | - | 0 | - | ns |
| Chip Disable to Output in High-Z | t _{CHZ} * | - | 5 | - | 6 | - | 7 | ns |
| Output Disable to Output in High-Z | t _{OHZ} * | - | 5 | - | 6 | - | 7 | ns |
| Output Hold from Address Change | t _{OH} | 3 | - | 3 | - | 3 | - | ns |

(2) WRITE CYCLE

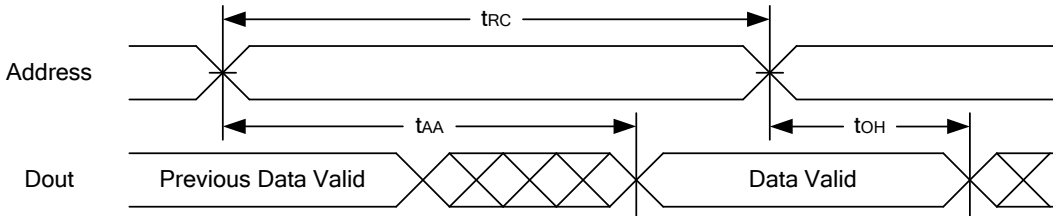
| PARAMETER | SYM. | LY61L1024-10 | | LY61L1024-12 | | LY61L1024-15 | | UNIT |
|----------------------------------|--------------------|--------------|------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Write Cycle Time | t _{WC} | 10 | - | 12 | - | 15 | - | ns |
| Address Valid to End of Write | t _{AW} | 8 | - | 10 | - | 12 | - | ns |
| Chip Enable to End of Write | t _{CW} | 8 | - | 10 | - | 12 | - | ns |
| Address Set-up Time | t _{AS} | 0 | - | 0 | - | 0 | - | ns |
| Write Pulse Width | t _{WP} | 8 | - | 9 | - | 10 | - | ns |
| Write Recovery Time | t _{WR} | 0 | - | 0 | - | 0 | - | ns |
| Data to Write Time Overlap | t _{DW} | 6 | - | 7 | - | 8 | - | ns |
| Data Hold from End of Write Time | t _{DH} | 0 | - | 0 | - | 0 | - | ns |
| Output Active from End of Write | t _{OW} * | 2 | - | 3 | - | 4 | - | ns |
| Write to Output in High-Z | t _{WHZ} * | - | 6 | - | 7 | - | 8 | ns |

*These parameters are guaranteed by device characterization, but not production tested.

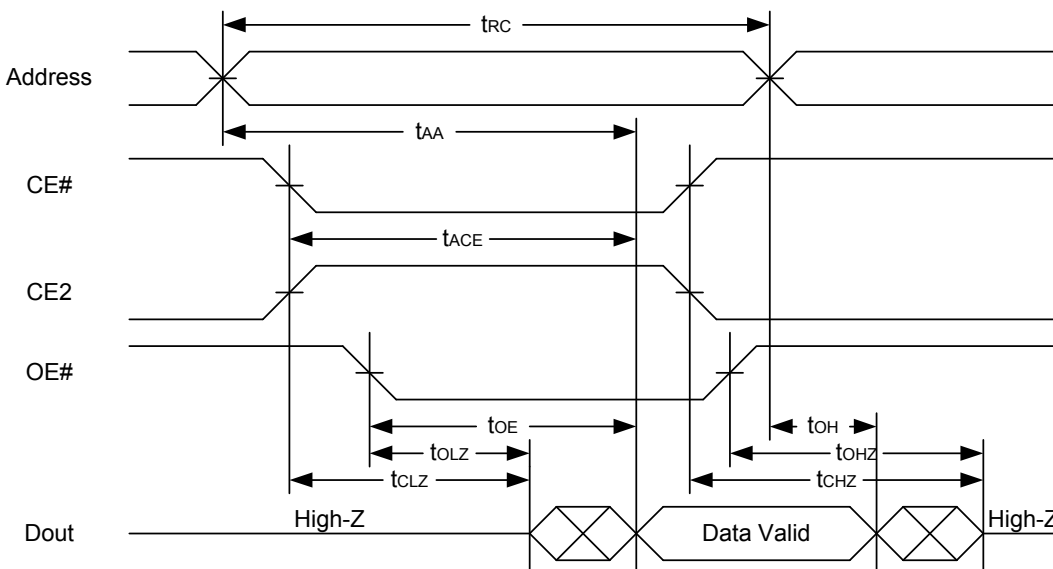


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

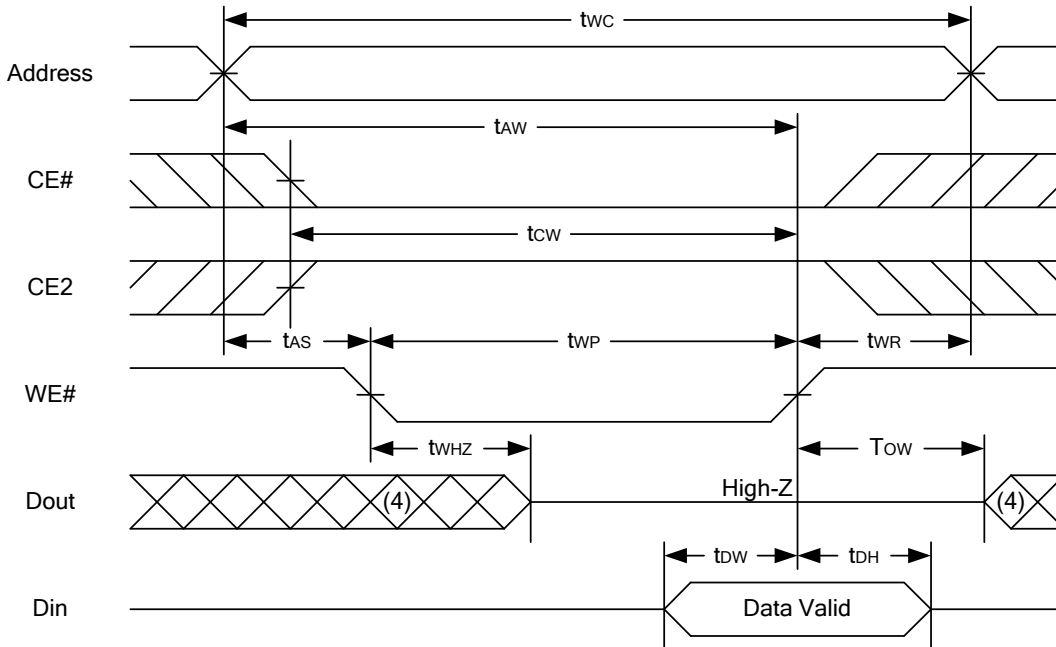
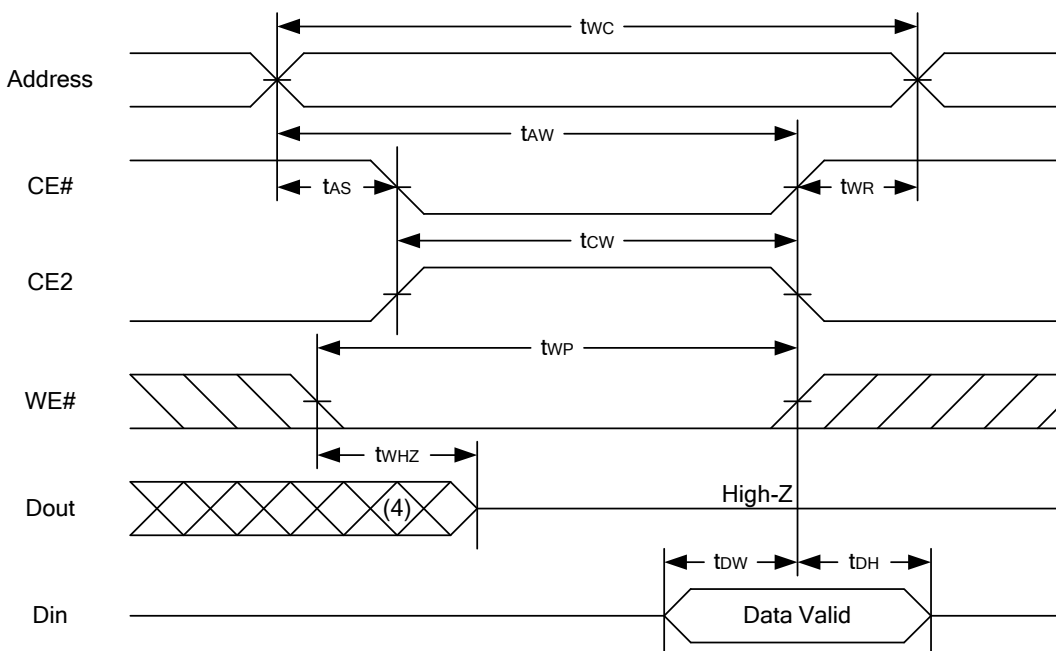


READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise tAA is the limiting parameter.
4. tCLZ, tOLZ, tCHZ and tOHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tOHZ is less than tOLZ.

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)

WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)

Notes :

1. WE#, CE# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#.
3. During a WE#-controlled write cycle with OE# low, t_{wp} must be greater than $t_{whz} + t_{dw}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{ow} and t_{whz} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.



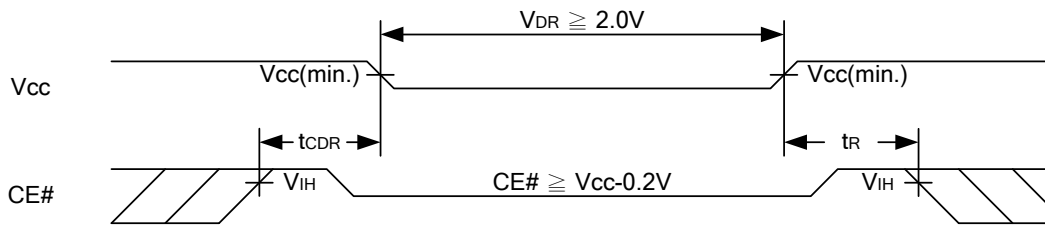
DATA RETENTION CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT | |
|-------------------------------------|------------------|--|------------------|------|-------|------|----|
| Vcc for Data Retention | V _{DR} | CE# ≥ V _{cc} - 0.2V or CE2 ≤ 0.2V | 2.0 | - | 3.6 | V | |
| Data Retention Current | I _{DR} | V _{cc} = 2.0V CE# ≥ V _{cc} - 0.2V or CE2 ≤ 0.2V | Normal | - | 0.006 | 2 | mA |
| | | V _{cc} = 2.0V CE# ≥ V _{cc} - 0.2V or CE2 ≤ 0.2V others at 0.2V or V _{cc} -0.2V | LL | - | 0.5 | 30 | μA |
| Chip Disable to Data Retention Time | t _{CDR} | See Data Retention Waveforms (below) | 0 | - | - | ns | |
| Recovery Time | t _R | | t _{RC*} | - | - | ns | |

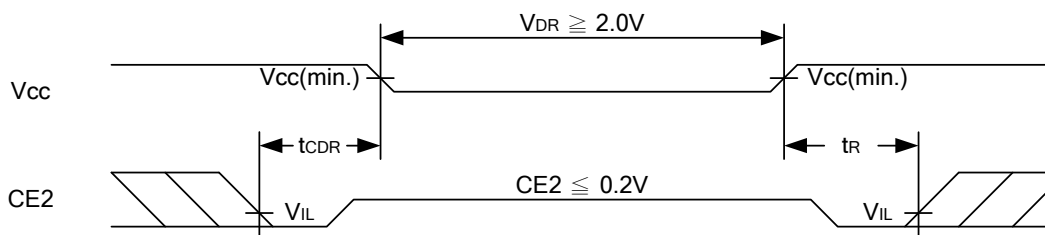
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) (CE# controlled)



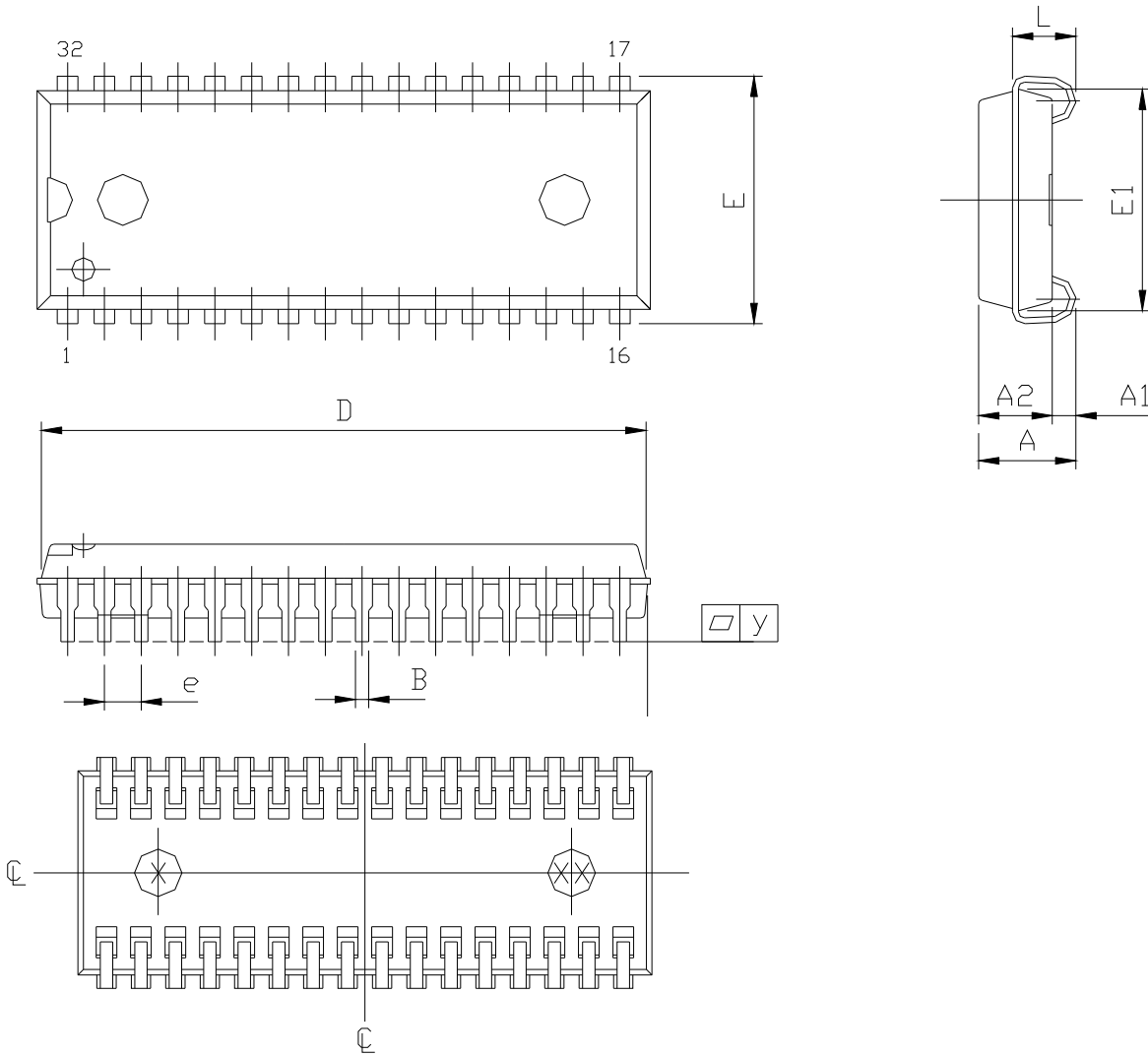
Low Vcc Data Retention Waveform (2) (CE2 controlled)



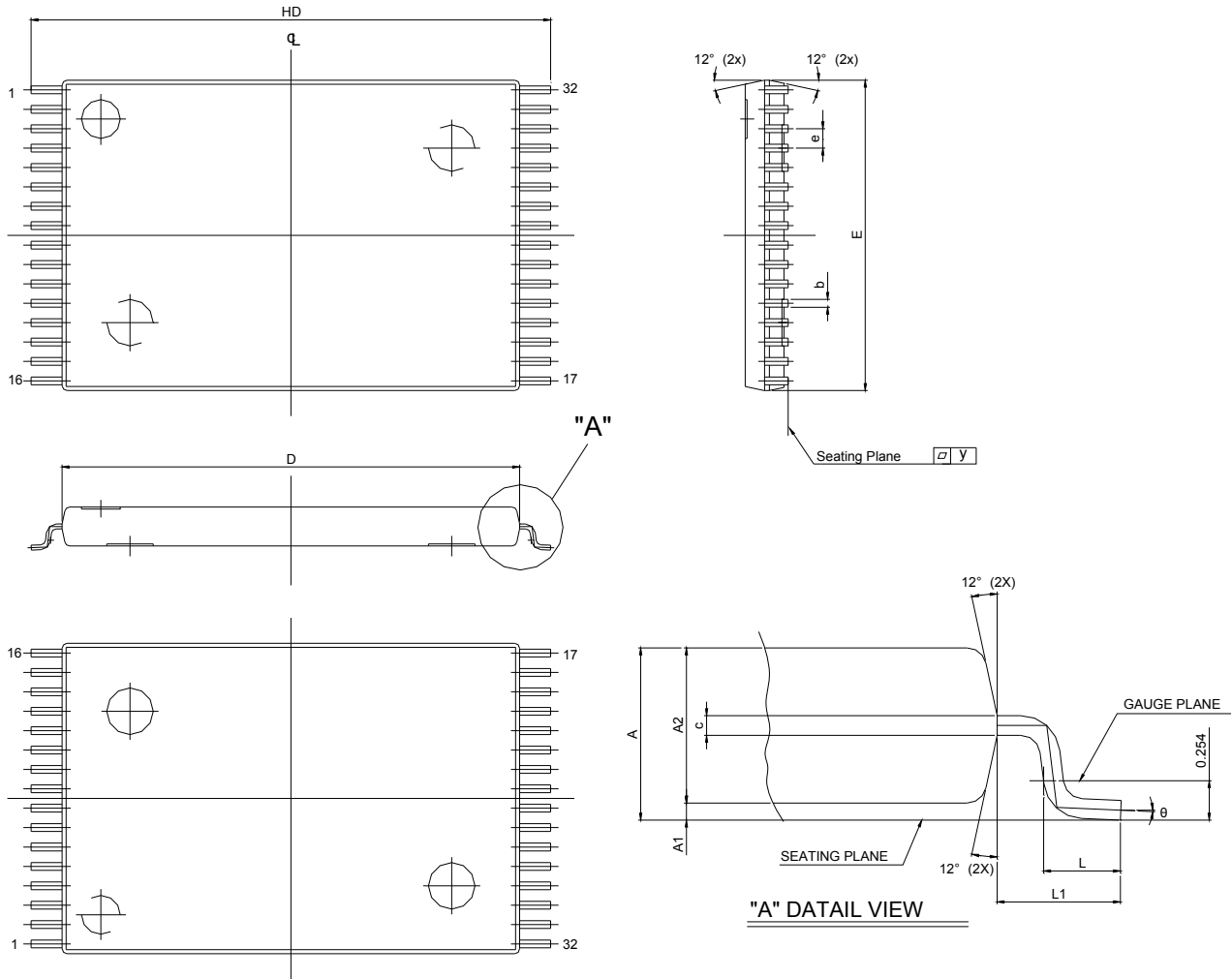


PACKAGE OUTLINE DIMENSION

32 pin 300mil SOJ Package Outline Dimension



| SYMBOL | UNIT | INCH(BASE) | MM(REF) |
|--------|------|--------------|--------------|
| A | | 0.148 (MAX) | 3.759 (MAX) |
| A1 | | 0.026 (MIN) | 0.660 (MIN) |
| A2 | | 0.100 ±0.005 | 2.540 ±0.127 |
| B | | 0.018 (TYP) | 0.457 (TYP) |
| D | | 0.830 (MAX) | 21.082 (MAX) |
| E | | 0.335 (TYP) | 8.509 (TYP) |
| E1 | | 0.300 ±0.005 | 7.620 ±0.127 |
| e | | 0.050 (TYP) | 1.270 (TYP) |
| L | | 0.086 ±0.010 | 2.184 ±0.254 |
| y | | 0.003 (MAX) | 0.076 (MAX) |

32 pin 8mm x 13.4mm STSOP Package Outline Dimension


| SYM. | UNIT | INCH(BASE) | MM(REF) |
|------|------|---------------|--------------|
| A | | 0.049 (MAX) | 1.25 (MAX) |
| A1 | | 0.005 ±0.002 | 0.130 ±0.05 |
| A2 | | 0.039 ±0.002 | 1.00 ±0.05 |
| b | | 0.008 ±0.01 | 0.20±0.025 |
| c | | 0.005 (TYP) | 0.127 (TYP) |
| D | | 0.465 ±0.004 | 11.80 ±0.10 |
| E | | 0.315 ±0.004 | 8.00 ±0.10 |
| e | | 0.020 (TYP) | 0.50 (TYP) |
| HD | | 0.528±0.008 | 13.40 ±0.20. |
| L | | 0.0197 ±0.004 | 0.50 ±0.10 |
| L1 | | 0.0315 ±0.004 | 0.8 ±0.10 |
| y | | 0.003 (MAX) | 0.076 (MAX) |
| Θ | | 0°~5° | 0°~5° |



ORDERING INFORMATION

LY61L1024 U V - WW XX Y Z

Z : Packing Type
Blank : Tube or Tray
T : Tape Reel

Y : Temperature Range
Blank : (Commercial) 0°C ~ 70°C
E : (Extended) -20°C ~ +80°C
I : (Industrial) -40°C ~ +85°C

XX : Power Type
LL : Ultra Low Power

WW : Access Time(Speed)

V : Lead Information
L : Green Package

U : Package Type
J : 32-pin 300 mil SOJ
L : 32-pin 8 mm x 20 mm TSOP-I
R : 32-pin 8 mm x 13.4 mm STSOP



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