A1 PROs

A*i*5412

Timing Controller for CCD Monochrome Camera

Description

The *Ai5412* is a timing and sync one chip controller IC with auto IRIS function for B/W CCD camera systems, which is fabricated in the Hynix 0.8§ CMOS process.
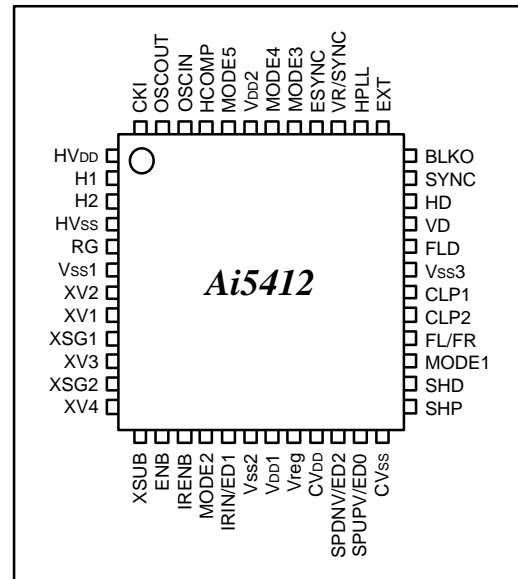
Feature

- EIA / CCIR standards
- Auto IRIS function
- Supports field / frame accumulation mode
- Supports external sync mode
- Supports non-interlacing mode
- Oscillator frequency : 1212fh
  (EIA : 19.0699MHz, CCIR : 18.9375MHz)
- 48 pin TQFP
- Kit with *Ai1001S*, *Ai4402*
- Built-in sync signal generation function

Application

CCD monochrome camera systems.

Pin Configuration

Top pins (left to right): CKI, OSCOUT, OSCIN, HCOMP, MODE5, V$_{DD}$2, MODE4, MODE3, ESYNC, VR/SYNC, HPLL, EXT

Left pins (top to bottom): HV$_{DD}$, H1, H2, HV$_{SS}$, RG, V$_{SS}$1, XV2, XV1, XSG1, XV3, XSG2, XV4

Right pins (top to bottom): BLKO, SYNC, HD, VD, FLD, V$_{SS}$3, CLP1, CLP2, FL/FR, MODE1, SHD, SHP

Bottom pins (left to right): XSUB, ENB, IRENB, MODE2, IRIN/ED1, V$_{SS}$2, V$_{DD}$1, Vreg, CV$_{DD}$, SPDNV/ED2, SPUPV/ED0, CV$_{SS}$

Ai5412

48 PIN TQFP
(Top View)

Absolute Maximum Ratings (Ta = 25¡ÉVss=0V)

Symbol	Parameter	Rating	Unit
V$_{DD}$	Supply Voltage	Vss-0.5 to +7.5	V
V$_I$	Input Voltage	Vss-0.5 to V$_{DD}$+0.5	V
Vo	Output Voltage	Vss-0.5 to V$_{DD}$+0.5	V
T$_{OPR}$	Operating Temperature	-20 ~ +75	¡É
T$_{STG}$	Storage Temperature	-55 ~ +150	¡É

Operating Conditions

Symbol	Parameter	Rating	Unit
V$_{DD}$	Supply Voltage	5.0¡¾0.25	V
T$_{OPR}$	Operating Temperature	-20 ~ +75	¡É

Block Diagram
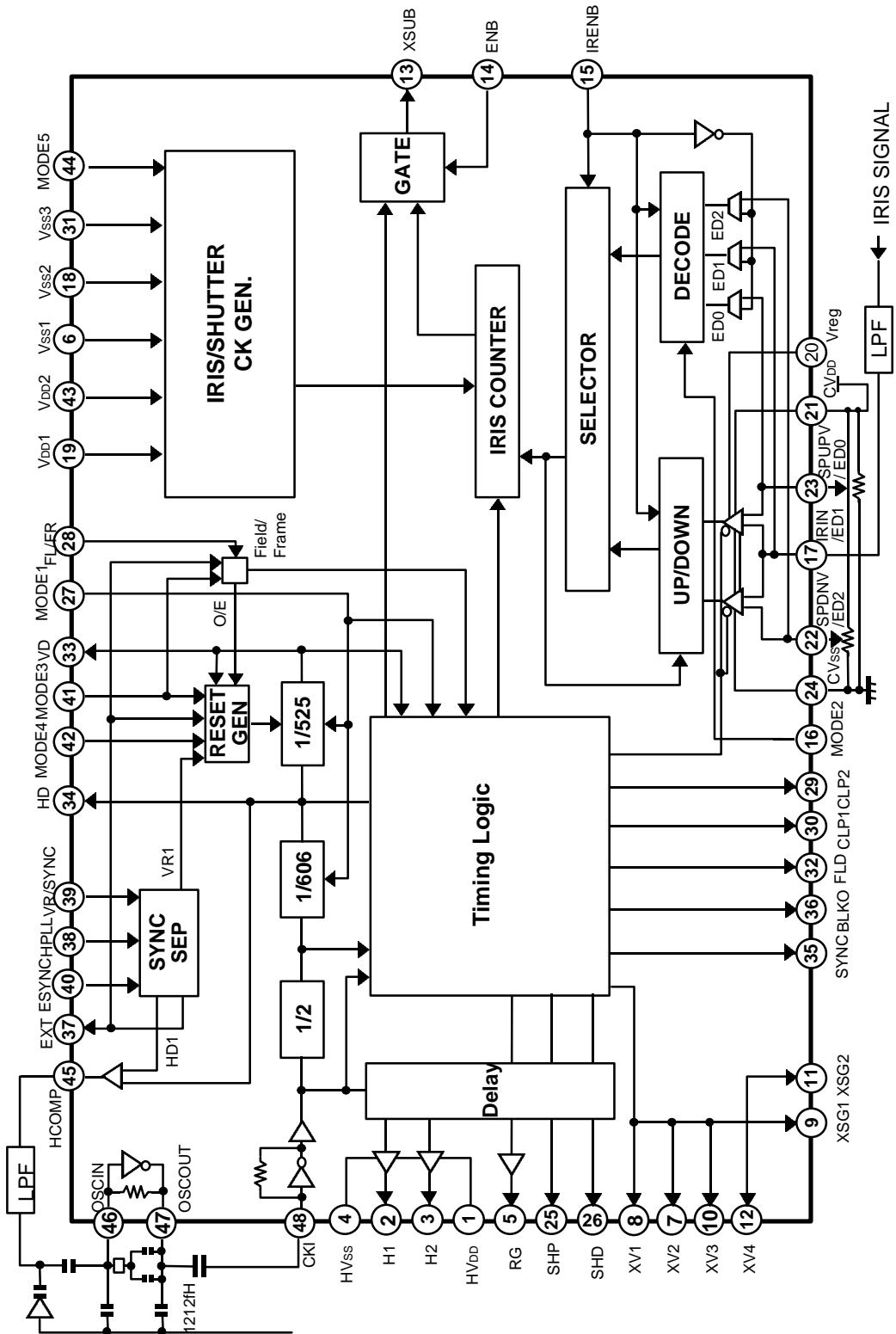
Pin Description

NO.	Symbol	I/O	Description
1	HV_{DD}	-	Power supply (for H1, H2)
2	H1	O	H1 clock output for CCD horizontal register drive
3	H2	O	H2 clock output for CCD horizontal register drive
4	HV_{SS}	-	GND(for H1, H2)
5	RG	-	Reset gate pulse output
6	$V_{SS}1$	-	GND
7	XV2	O	XV2 clock output for CCD vertical register drive
8	XV1	O	XV1 clock output for CCD vertical register drive
9	XSG1	O	CCD sensor charge readout pulse output
10	XV3	O	XV3 clock output for CCD vertical register drive
11	XSG2	O	CCD sensor charge readout pulse output
12	XV4	O	XV4 clock output for CCD vertical register drive
13	XSUB	O	CCD discharge pulse output
14	ENB	I	XSUB pulse output ON/OFF control (with pull-up resistance) Low : XSUB pulse output stop ; High : XSUB pulse output
15	IRENB	I	Low : Electronic shutter mode ; High : Auto iris mode (with pull-up resistance)
16	MODE2	I	Electronic shutter speed input switchover (with pull-up resistance) Low : serial input ; High : parallel input
17	IRIN/ED1	I[*1]	Iris signal input/shutter speed setting ; clock input in serial mode
18	Vss2	-	GND
19	$V_{DD}1$	-	Power supply
20	Vreg	-	Bias current supply for comparator
21	CV_{DD}	-	Power supply (for comparator)
22	SPDNV /ED2	I[*1]	Shutter speed down reference voltage/ Shutter speed setting ; data input in serial mode
23	SPUPV /ED0	I[*1]	Shutter speed up reference voltage / Shutter speed setting ; strobe input in serial mode
24	CV_{SS}	-	GND(for comparator)
25	SHP	O	Pre charge level sample-and-hold pulse
26	SHD	O	Data sample-and-hold pulse
27	MODE1	I	Low : EIA ; High : CCIR (with pull-down resistance)

NO.	Symbol	I/O	Description
28	FL/FR	I	Field accumulation/frame accumulation, odd field/even field switchover (with pull-down resistance)
29	CLP2	O	Pulse output for clamp
30	CLP1	O	Pulse output for clamp
31	$V_{SS}3$	-	GND
32	FLD	O	Field identification signal output (High : odd field ; Low : even field)
33	VD	O	Vertical drive output
34	HD	O	Horizontal drive output
35	SYNC	O	Composite sync output
36	BLKO	O	Composite blanking output
37	EXT	O	External sync/internal sync identification signal High : external sync ; Low : internal sync
38	HPLL	I	Horizontal drive signal input (with pull-up resistance)
39	VR/SYNC	I	Vertical drive signal input/composite sync input (with pull-up resistance)
40	ESYNC	I	Low : SYNC sync or internal sync ; High : VD/HD sync (with pull-down resistance)
41	MODE3	I	Low : interlace mode ; High : non-interlace mode (with pull-down resistance)
42	MODE4	I	Line number selection pin (with pull-down resistance) Low : EIA 262H/CCIR 312H ; High : EIA 263H/CCIR 313H
43	$V_{DD}2$	-	Power supply
44	MODE5	I*2	Low : Normal mode ; High : Test mode (with pull-down resistance)
45	HCOMP	O	Comparator output (H phase comparator)
46	OSCIN	I*3	Oscillation (crystal oscillator) inverter input
47	OSCOUT	O	Oscillation (crystal oscillator) inverter output
48	CKI	I*4	Clock input

I*1 ⟶ Comparator Input

I*2 ⟶ Fixed to low level

I*3 ⟶ OSCILLATOR Cell

I*4 ⟶ Input cell with feedback resistance

Electrical Characteristics

1) DC Characteristics   (VDD = 5V ±0.25V, Topr = -20 to 75 ℃)

Item	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.75	5.0	5.25	V
Input voltage	V_{IH}		$0.7V_{DD}$			V
	V_{IL}				$0.3V_{DD}$	V
Output voltage 1 (All output pins except those below)	V_{OH1}	I_{OH} = -2mA	V_{DD} - 0.8			V
	V_{OL1}	I_{OL} = 4mA			0.4	V
Output voltage 2 (Pins 25, 26)	V_{OH2}	I_{OH} = -4mA	V_{DD} - 0.8			V
	V_{OL2}	I_{OL} = 8mA			0.4	V
Output voltage 3 (Pin 5, 45)	V_{OH3}	I_{OH} = -8mA	V_{DD} - 0.8			V
	V_{OL3}	I_{OL} = 8mA			0.4	V
Output voltage 4 (Pins 2, 3)	V_{OH4}	I_{OH} = -12mA	V_{DD} - 8			
	V_{OL4}	I_{OL} = 12mA			0.4	
Output voltage 5 (Pin 47)	V_{OH5}	I_{OH} = -1mA	V_{DD} / 2			V
	V_{OL5}	I_{OL} = 1mA			0.4	V
Feedback resistance	R_{FB}	V_{IN} = V_{SS} or V_{DD}	250K	1M	2.5M	Ω
Pull-up current	I_{PU}	V_{IL} = 0V	-80		-30	µA
Pull-down current	I_{PD}	V_{IH} = V_{DD}	40		110	µA
Current consumption	I_{DD}	V_{DD} = 5V normal operating state		28		mA

2) AC Characteristics
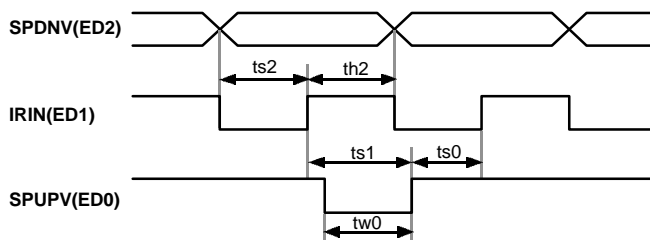
Symbol	Item	Min.	Max.
ts2	SPDNV (ED2) setup time for IRIN (ED1) rise	20ns	-
th2	SPDNV (ED2) hold time for IRIN (ED1) rise	20ns	-
ts1	IRIN (ED1) setup time for SPUPV (ED0) rise	20ns	-
tw0	SPUPV (ED0) pulse width	20ns	50µs
ts0	SPUPV (ED0) setup time for IRIN (ED1) rise	20ns	-

Electronic Shutter/Auto IRIS

By setting the ENB pin (Pin 14) high, the XSUB pulse is output for a specific period to activate the electronic shutter and auto iris.

1) Auto Iris (IRENB=high, MODE2=any level)

Symbol	NO.	Function
IRIN/ED1	17	Iris signal input
SPDNV/ED2	22	Shutter speed down reference voltage
SPUPV/ED0	23	Shutter speed up reference voltage

2) Parallel input electronic shutter (IRENB=low, MODE2=high)

Symbol	NO.	Function							
SPDNV/ED2	22	H	H	H	H	L	L	L	L
IRIN/ED1	17	H	H	L	L	H	H	L	L
SPUPV/ED0	23	H	L	H	L	H	L:	H	L
Shutter speed		EIA: 1/100 CCIR: 1/120	1/250	1/500	1/1000	1/2000	1/5000	1/10000	1/100000

3) Serial input electronic shutter (IRENB=low, MODE2=high)

Serial input data format
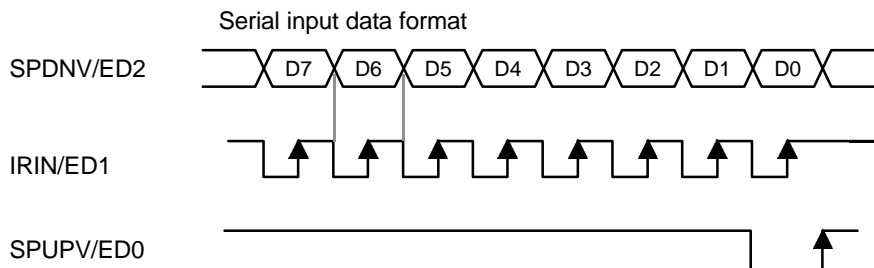
The ED2 data is latched in the register at the ED1 rise, and retrieved internally at the ED0 rise.

Typical shutter speed

EIA		CCIR	
Load value	Shutter speed	Load value	Shutter speed
00h	1/100000	00h	1/80000
4Eh	1/10000	4Ah	1/10000
6Ah	1/5000	65h	1/5000
87h	1/2000	82h	1/2000
9Ch	1/1000	97h	1/1000
ACh	1/500	A7h	1/500
CAh	1/250	C5h	1/250
EDh	1/100	E1h	1/120

External Synchronization

1) External/internal sync selection

External or internal synchronization is selected automatically by a combination of 3 pins (VR/SYNC, HPLL and ESYNC) to which the sync signal is input externally. The table below shows the input pattern combinations.

Input pattern	VR/SYNC pin : SYNC signal HPLL pin : Open ESYNC pin : Open	VR/SYNC pin : VD signal HPLL pin : HD signal ESYNC pin : V_{DD}	VR/SYNC pin : Open HPLL pin : Open ESYNC pin : Open
EXT pin output	High	High	Low
Sync state	External sync	External sync	Internal sync

Note) Operation is possible even if the VD cycle of the VD input in the VD/HD sync mode is longer than normal.

The EXT pin is the external/internal sync identification signal output pin. This output signal can be used as the signal to select LC oscillation for expanding the lock range for external synchronization or the oscillator for improving the oscillation accuracy for internal synchronization.

2) Modes for external synchronization

Mode		Field accumulation	Frame accumulation
SYNC synchronization	Interlace	O	O
	Non-interlace	X (Cannot be accomplished since interlace operation is the prior condition)	X (Cannot be accomplished since interlace operation is the prior condition)
VD/HD synchronization	Interlace	O	O
	Non-interlace	O	X (Not practically applicable since the sensitivity is halved)

3) Reset operation

SYNC synchronization
The VR1 signal component is extracted from the SYNC signal supplied externally and, for EIA,V reset is performed so that the VD pulse falls at the count of 259H (262.5-3.5H) from the fall of the VR1 pulse. For CCIR, it is reset in such a way that the VD pulse falls at the count of 309H(312.5-3.5H).For these reasons, it is a prerequisite that the SYNC signal input comply with the EIA or CCIR standard.

VD/HD synchronization
V reset is performed so that the VD pulse 1H later after detecting the fall of the VD(VDR) pulse supplied externally. Therefore, this enables V reset operation regardless of the field line number. The phase difference between the VDRpulse and HD pulse which is locked horizontally at PLL circuit identifies whether the field is odd or even.
 (VDR must have a pulse width of 2H or more.)

Mode Control

Symbol	NO.	I/O	Low	High	Remarks
ENB	14	I	XSUB stop	XSUB output	
IRENB	15	I	Electronic shutter	Auto iris	Valid only when ENB is high.
MODE2	16	I	Serial input	Parallel input	Valid only when ENB is high and IRENB is low
IRIN/ED1	17	I	Auto iris control signal input pin (IRENB = high) Shutter speed setting pin (IRENB = low)		Valid only when ENB is high.
SPDNV/ED2	22	I			
SPUPV/ED0	23	I			
MODE1	27	I	EIA	CCIR	
FL/FR	28	I	Odd field	Even field	Valid only when MODE3 is high and EXT is low.
			Field accumulation	Frame accumulation	Valid in all other modes.
HPLL	38	I	Internal sync : HPLL (open) VR/SYNC (open) SYNC sync : HPLL (open) VR/SYNC (SYNC input) VD/HD sync : HPLL (HD input) VR/SYNC (VD input)		
VR/SYNC	39	I			
ESYNC	40	I	SYNC sync Internal sync	VD/HD sync	
MODE3	41	I	Interlace	Non-interlace	Valid only when EXT is low.
MODE4	42	I	EIA : 262H CCIR : 312H	EIA : 263H CCIR : 313H	Valid only when EXT is low and MODE 3 is high.
EXT	37	O	Internal sync	External sync	Switchover between internal and external sync is automatically identified by input state at Pins 38, 39 and 40.

Mode Tables

1) Internal sync mode

HPLL pin (Pin 38)   : Open
VR/SYNC pin (Pin 39) : Open
ESYNC pin (Pin 40)   : Open

	Interlace		Non-interlace			
			Odd field *2		Even field *2	
	Field readout	Frame readout	Field readout	Frame readout	Field readout	Frame readout
XSUB pulse OFF*1	O	O	O	X	O	X
Electronic shutter ON	O	O	O	X	O	X
Auto iris ON	O	O	O	X	O	X

*1 EIA for 1/60 s accumulation ; CCIR for 1/50 s accumulation
*2 Line number is 262H or 263H for EIA and 312H or 313H for CCIR.

O : Can be used.
X : Cannot be used.

2) SYNC sync (external sync) mode

HPLL pin (Pin 38)   : Open
VR/SYNC pin (Pin 39) : SYNC input
ESYNC pin (Pin 40)   : Open

	Interlace		Non-interlace			
			Odd field *2		Even field *2	
	Field readout	Frame readout	Field readout	Frame readout	Field readout	Frame readout
XSUB pulse OFF*1	O	O	X	X	X	X
Electronic shutter ON	O	O	X	X	X	X
Auto iris ON	O	O	X	X	X	X

*1 EIA for 1/60 s accumulation ; CCIR for 1/50 s accumulation
*2 Line number is 262H or 263H for EIA and 312H or 313H for CCIR.

O : Can be used.
X : Cannot be used.

3) VD/HD sync (external sync) mode

HPLL pin (Pin 38)   : HD input
VR/SYNC pin (Pin 39) : VD input
ESYNC pin (Pin 40)   : VDD (power supply)

	VD input with normal cycle						VD input with longer cycle than normal Interlace	
	Interlace		Non-interlace					
			Odd field *2		Even field *2			
	Field readout	Frame readout	Field readout	Frame readout	Field readout	Frame readout	Field readout	Frame readout
XSUB pulse OFF*1	O	O	O	X	O	X	O	X
Serial input electronic shutter ON	O	O	O	X	O	X	X	X
Parallel input electronic shutter ON	O	O	¡â	X	¡â	X	X	X
Auto iris ON	O	O	O	X	O	X	X	X

*1 EIA for 1/60 s accumulation ; CCIR for 1/50 s accumulation
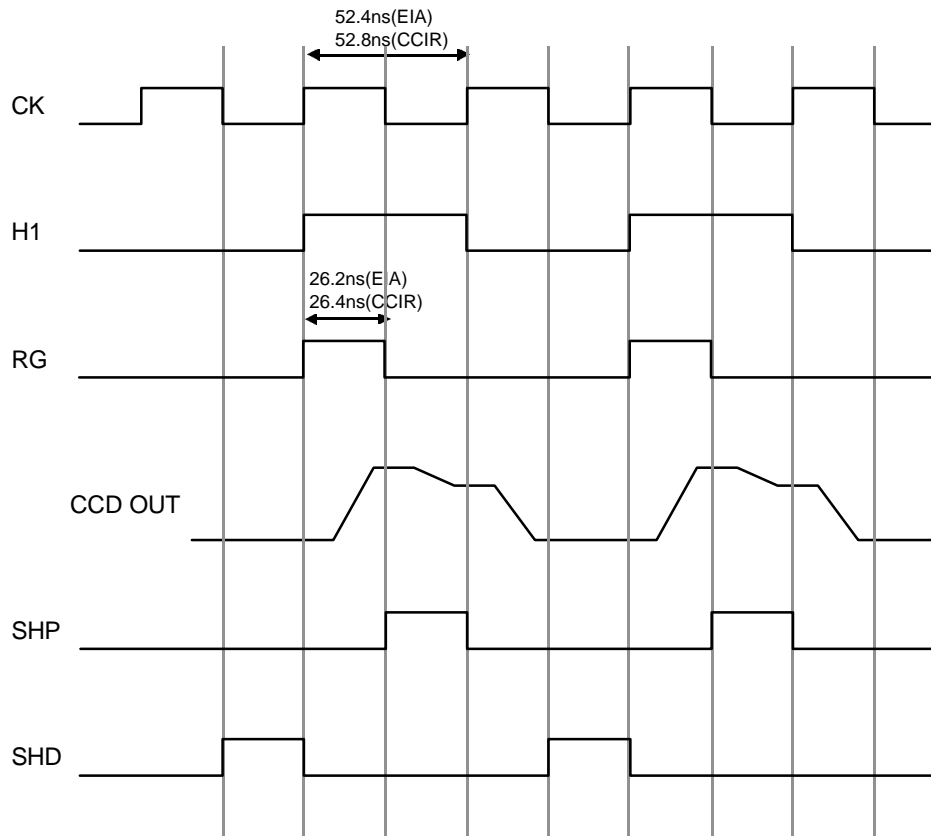*2 Line number is 262H or 263H for EIA and 312H or 313H for CCIR.

O : Can be used.
¡â The shutter speed may change from its value in the interlace mode.
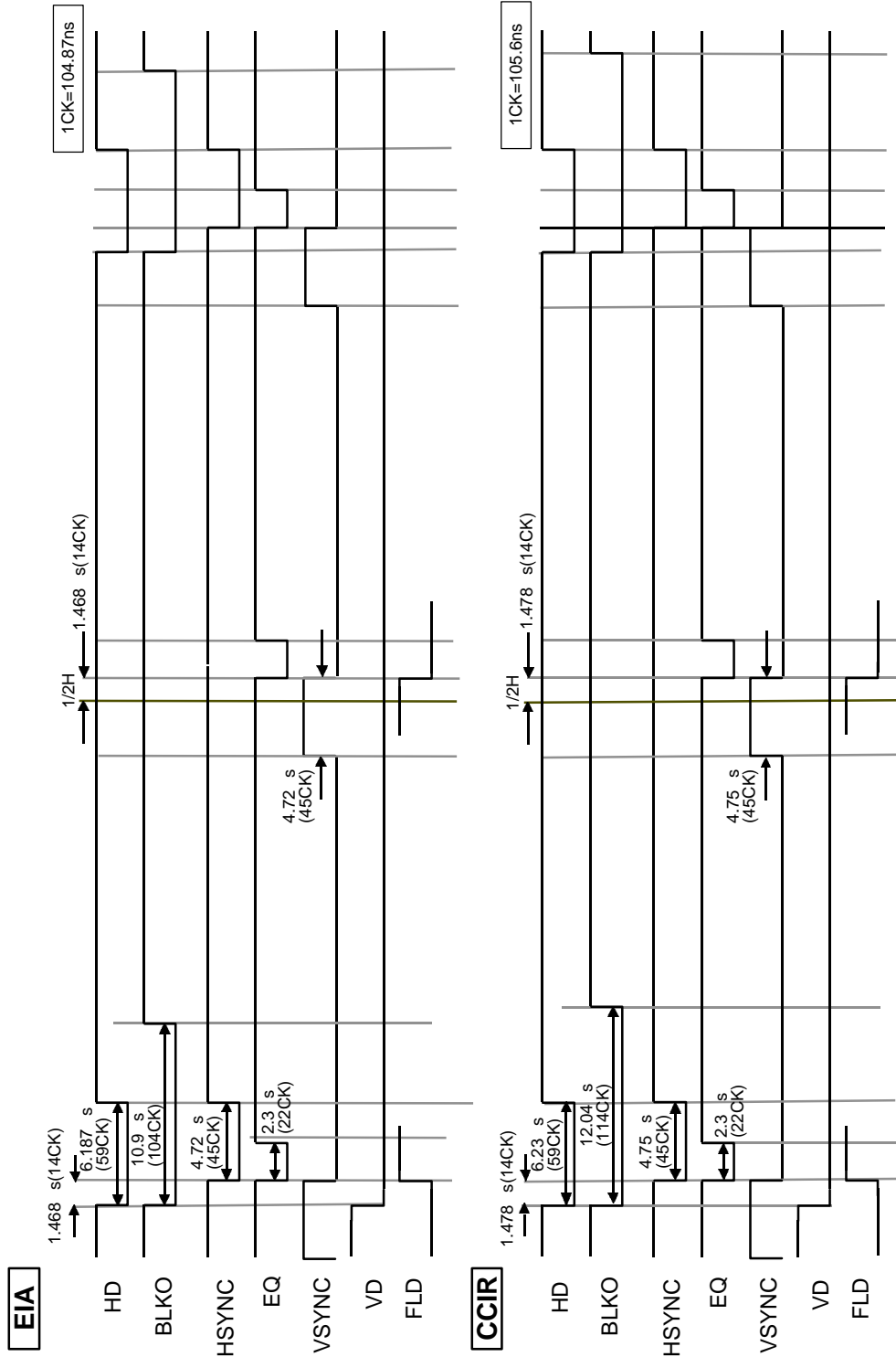X : Cannot be used.

Note) Only in the VD/HD sync mode, the external synchronization is possible during which VD pulses with longer cycle than normal are input to the VR/SYNC pin.

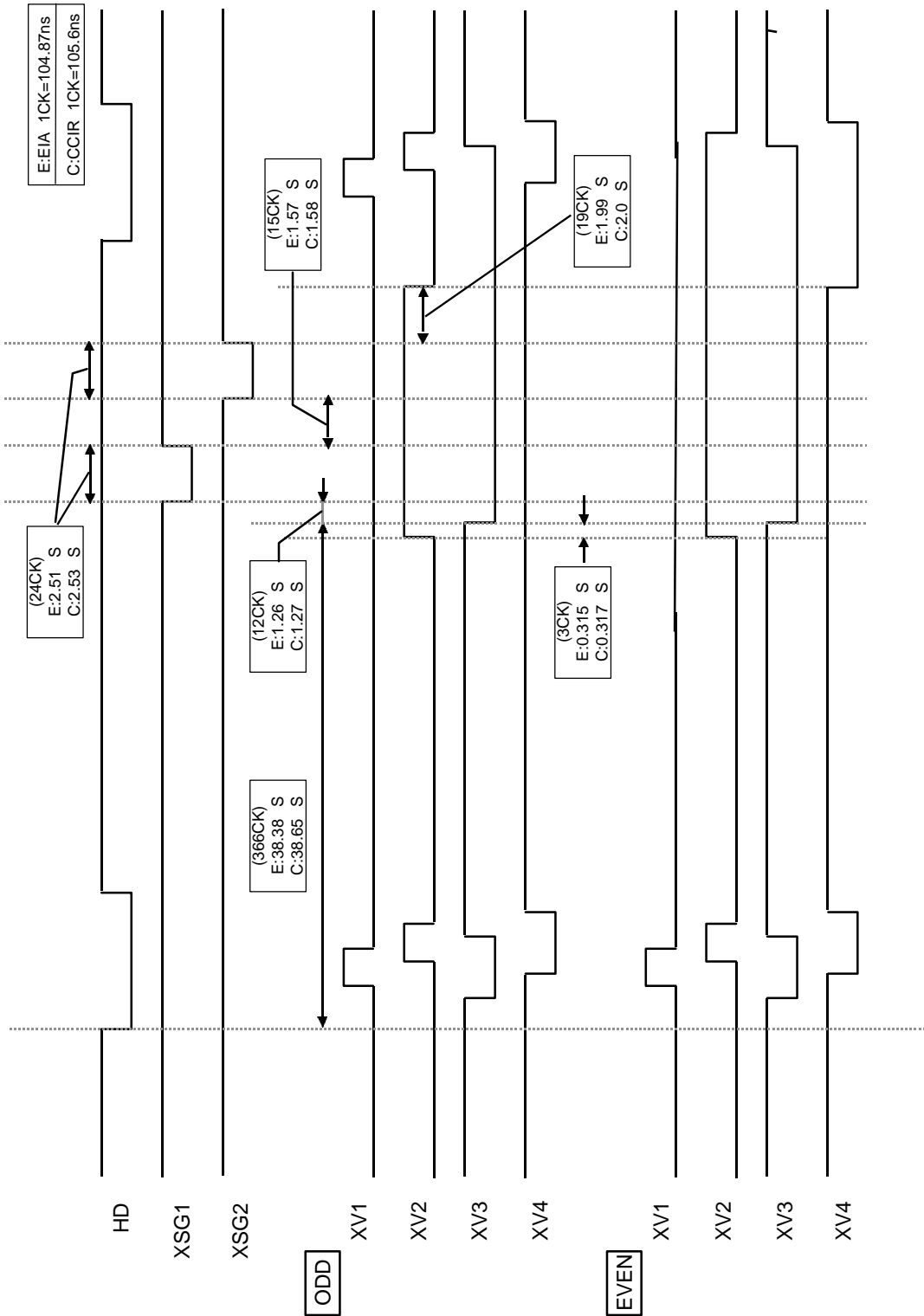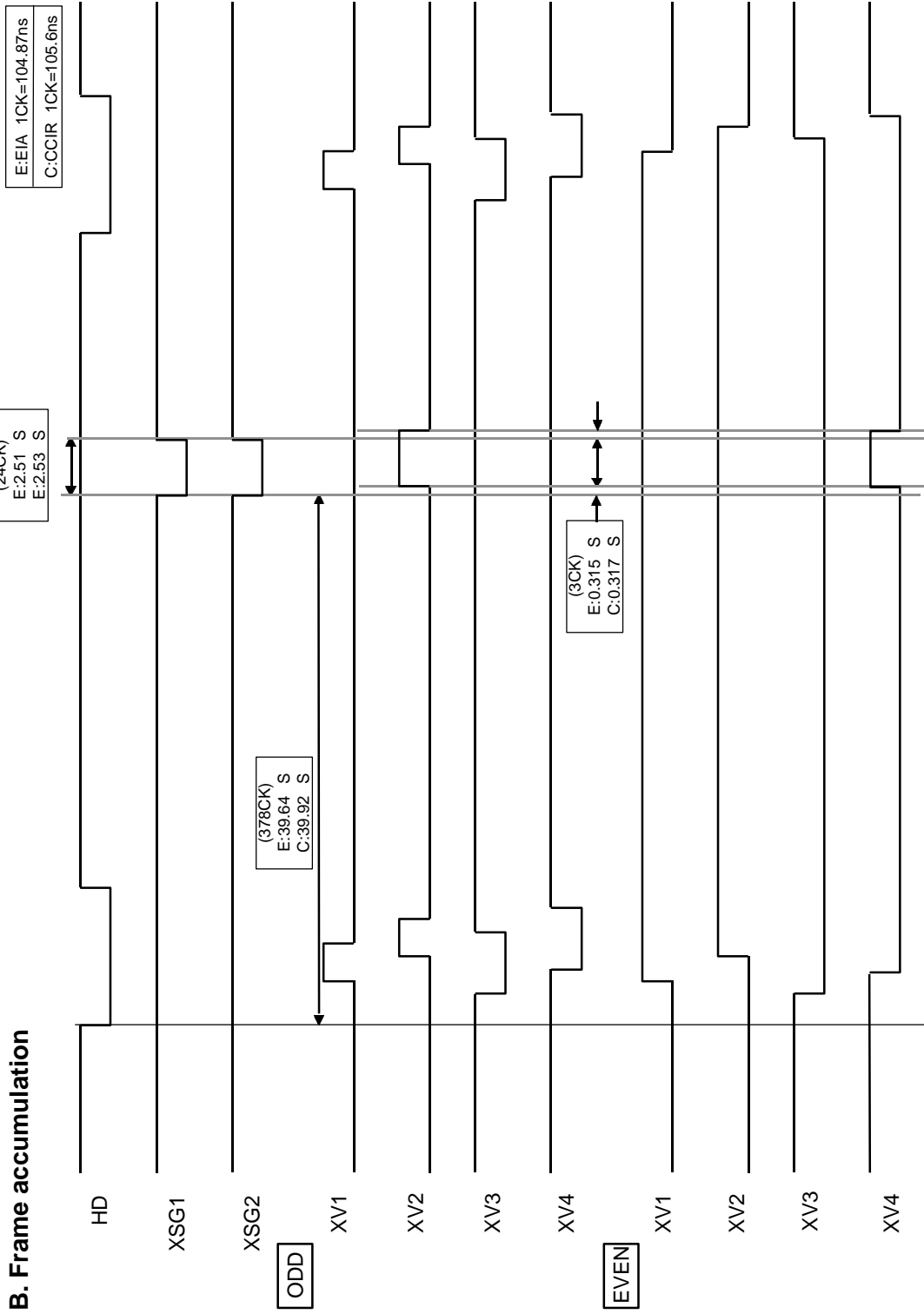## (Timing Chart 1)　High-Speed phase

EIA/CCIR

(Timing Chart 2) Horizontal effective period

1CK=104.87ns

1CK=105.6ns

1.468 s(14CK)

1/2H

4.72 s
(45CK)

1.468 s(14CK)

6.187 s
(59CK)

10.9 s
(104CK)

4.72 s
(45CK)

2.3 s
(22CK)

EIA

HD

BLKO

HSYNC

EQ

VSYNC

VD

FLD

1.478 s(14CK)

1/2H

4.75 s
(45CK)

1.478 s(14CK)

6.23 s
(59CK)

12.04 s
(114CK)

4.75 s
(45CK)

2.3 s
(22CK)

CCIR

HD

BLKO

HSYNC

EQ

VSYNC

VD

FLD

(Timing Chart 3) Charge Readout Timing

A. Field accumulation

| E:EIA 1CK=104.87ns |
| C:CCIR 1CK=105.6ns |

(24CK)
E:2.51 S
C:2.53 S

(15CK)
E:1.57 S
C:1.58 S

(19CK)
E:1.99 S
C:2.0 S

(12CK)
E:1.26 S
C:1.27 S

(3CK)
E:0.315 S
C:0.317 S

(366CK)
E:38.38 S
C:38.65 S

HD

XSG1

XSG2

ODD   XV1

XV2

XV3

XV4

EVEN XV1

XV2

XV3

XV4

B. Frame accumulation

Ai5412

(Timing Chart 4)

A. H direction, EIA

(MCK=CKI/2)

Signal	
HD	
MCK	
H1	
H2	
RG	
SHP	
SHD	
CLP1	
CLP2	
XV1	
XV2	
XV3	
XV4	
XSUB	
HSYNC	
EQ	
VSYNC	
FLD	
VD	

14

B. H direction, CCIR

(MCK=CKI/2)

Signals: HD, MCK, H1, H2, RG, SHP, SHD, CLP1, CLP2, XV1, XV2, XV3, XV4, XSUB, HSYNC, EQ, VSYNC, FLD, VD

Timing markers:
- HD: 59, 114
- CLP1: 7, 23
- CLP2: 84, 98, 107
- XV1: 37, 55
- XV2: 49, 67
- XV3: 31, 61, 73
- XV4: 43, 77
- XSUB: 60
- HSYNC: 14, 59
- EQ: 14, 36
- VSYNC: 14
- FLD: 14

Scale markers: 10, 20, 30, 40, 50, 60, 70, 80, 90, 100
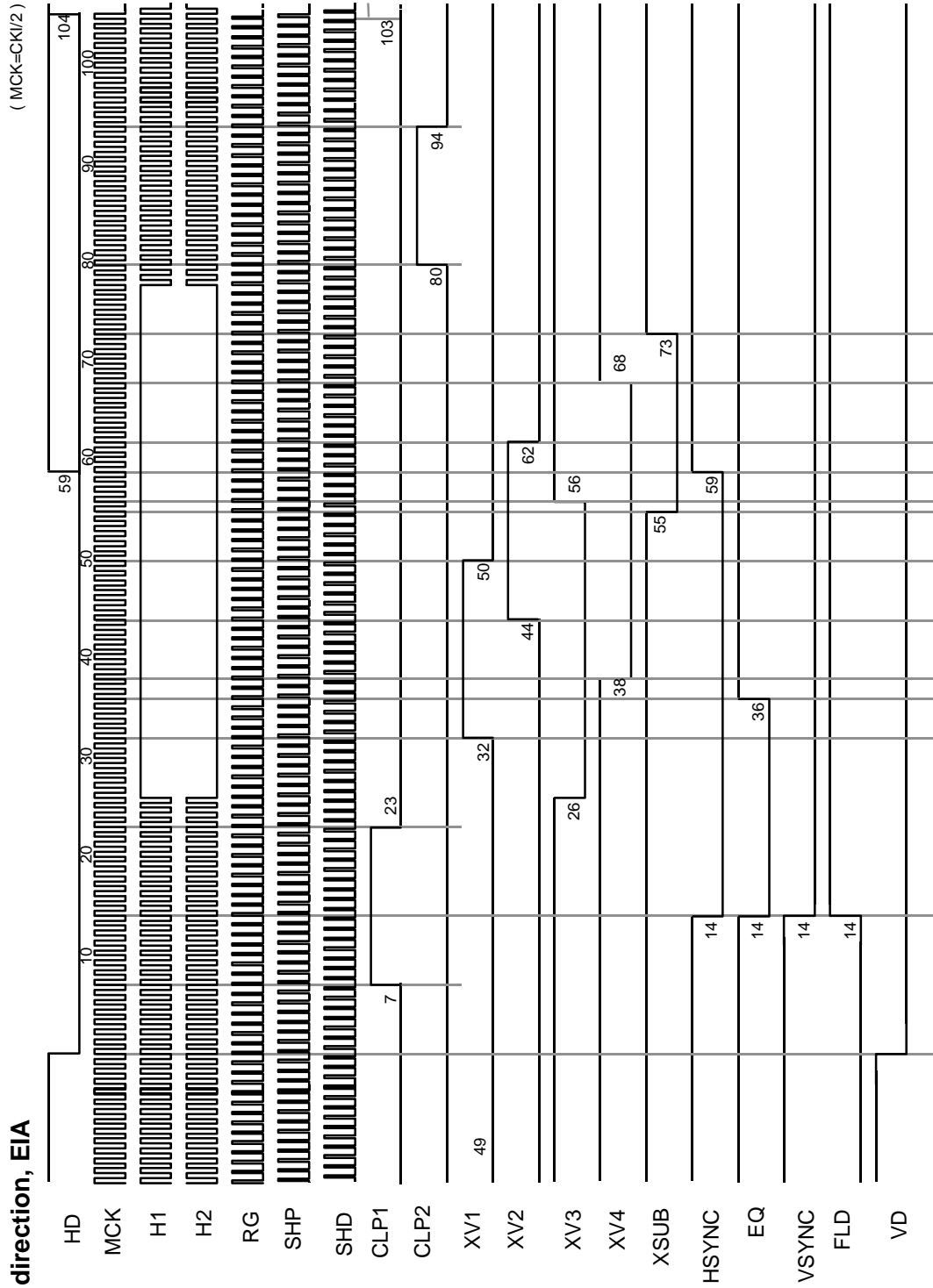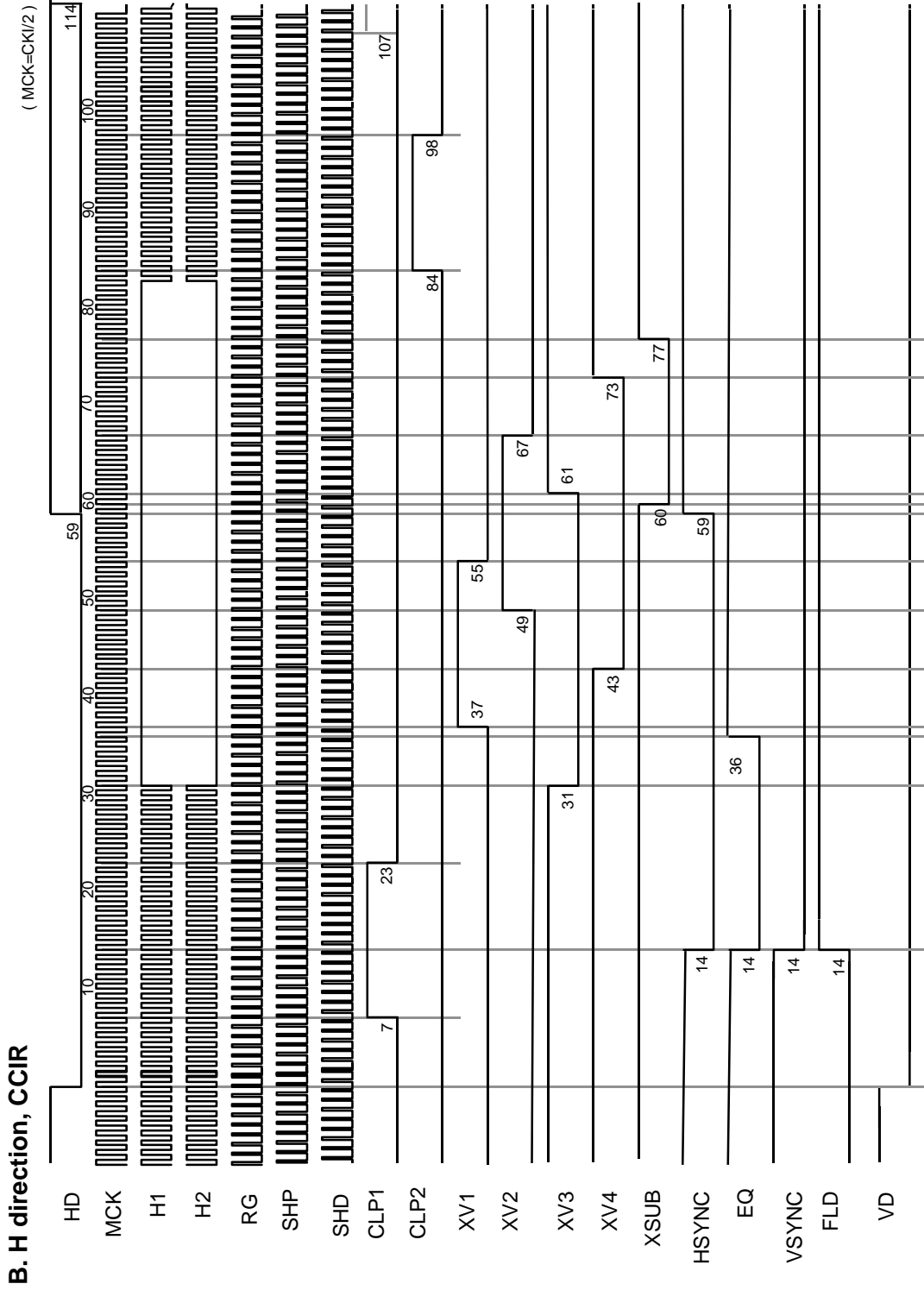
(Timing Chart 5) Low - Speed Phase
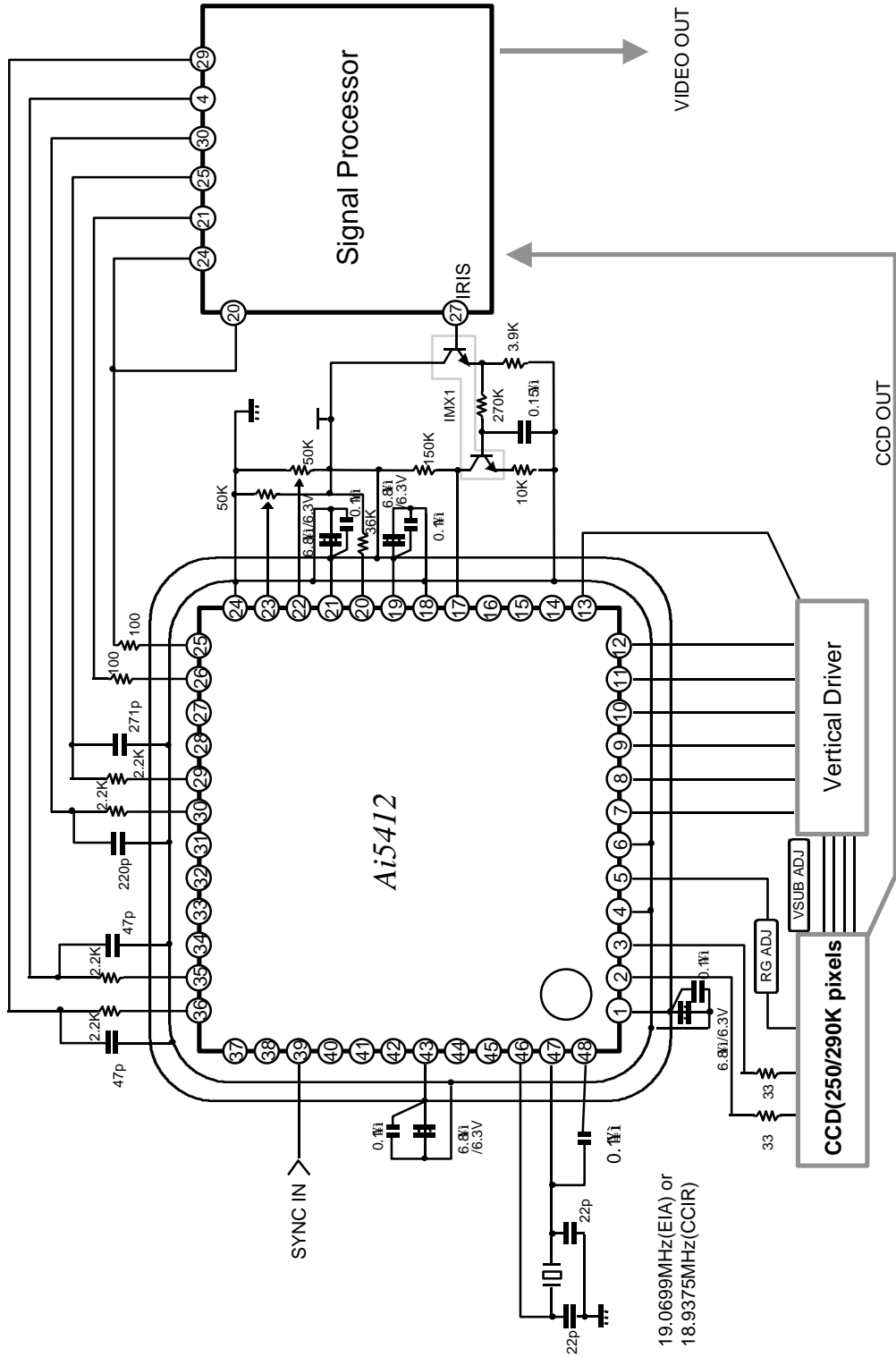
A. V direction, EIA
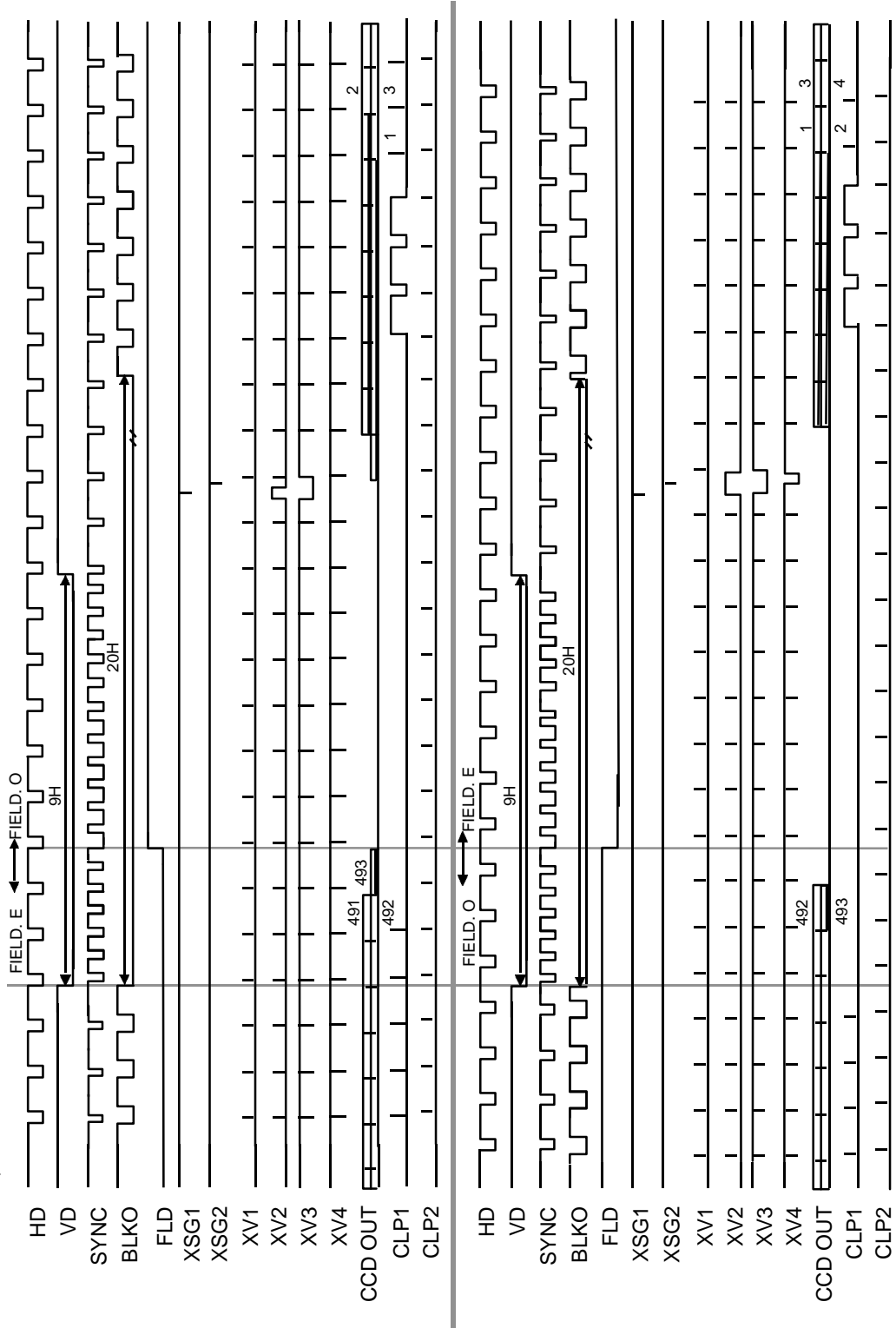
B. V direction, CCIR
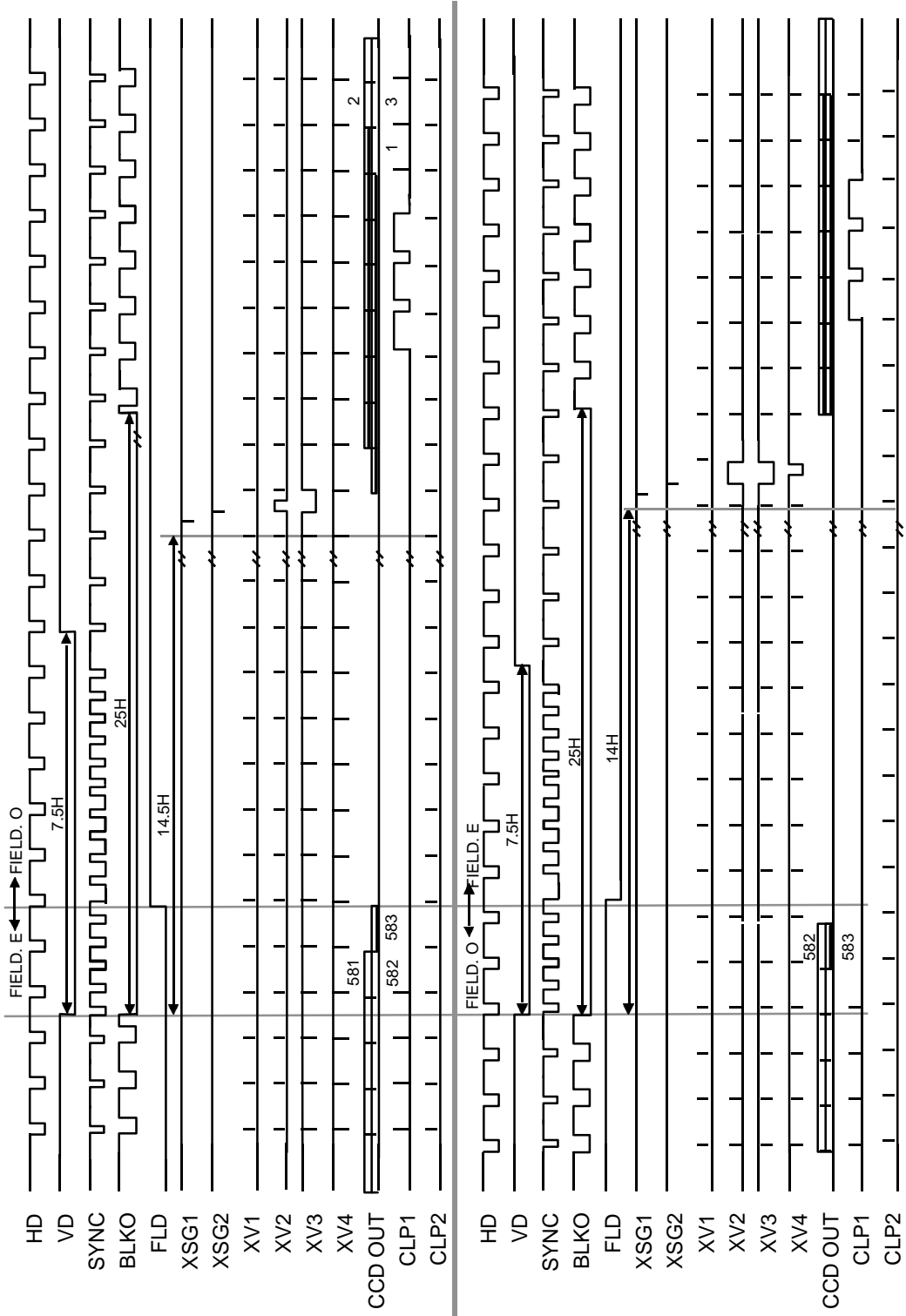
(Timing Chart 6)

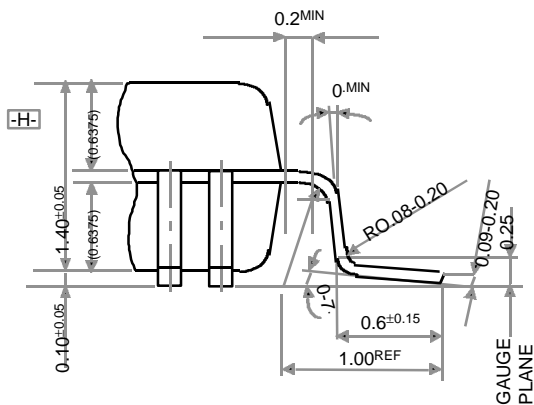### External Synchronization reset Operation

EIA

FIELD. E ←→ FIELD. O

9H

FIELD. O ←→ FIELD. E

9H

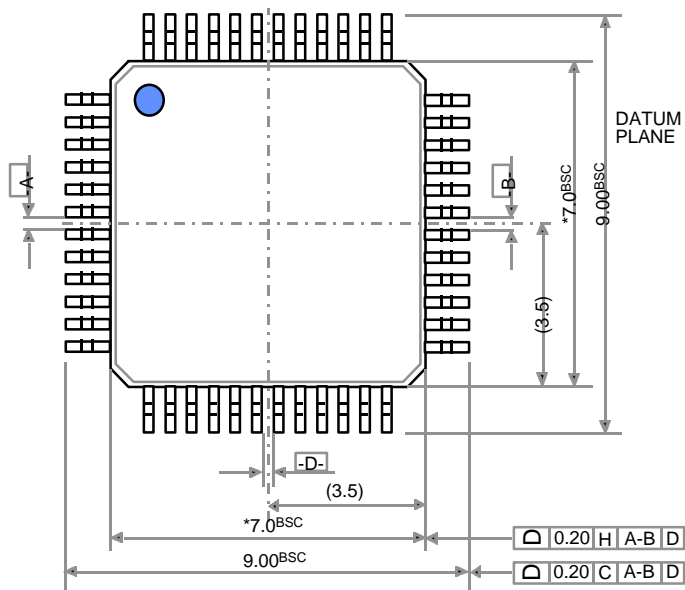CCIR

FIELD. E ←→ FIELD. O

7.5H

FIELD. O ←→ FIELD. E

7.5H

HD
VD
SYNC
HD1
VR1
VDR
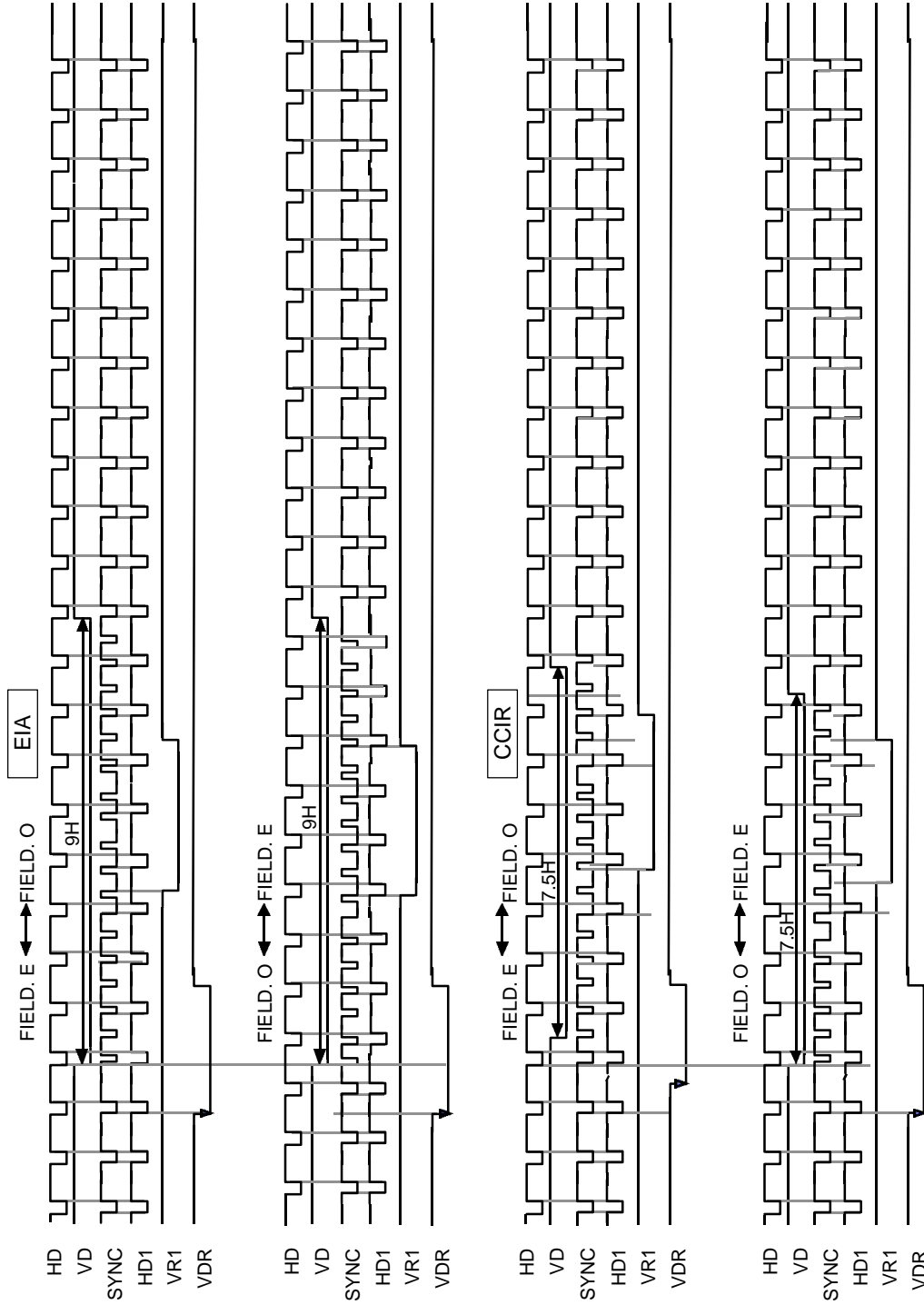
Application Circuit

Package Outline

UNIT : mm

48pin TQFP(PLASTIC)

DATUM
PLANE

*7.0 BSC
9.00 BSC

(3.5)

-D-
(3.5)
*7.0 BSC
9.00 BSC

| ⌀ | 0.20 | H | A-B | D |

| ⌀ | 0.20 | C | A-B | D |

1.50 MAX

8-12±1

0.5 BSC

0.22±0.05

| ⌀ | 0.20 | C | A-B | D |

0.2 MIN
0.MIN
-H-
(0.6375)
1.40±0.05
(0.6375)
0.10±0.05
R0.08-0.20
0.09-0.20
0.25
0.6±0.15
1.00 REF
GAUGE
PLANE
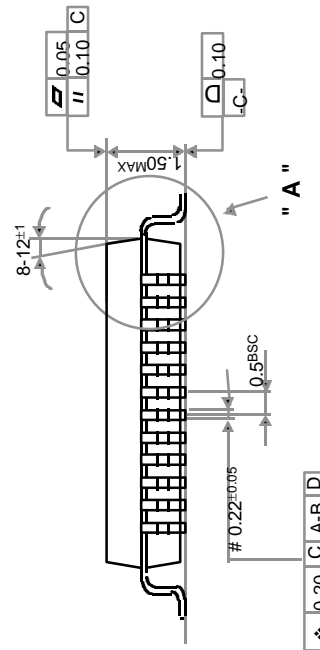
DETAILS of " A "

Note)

1. DIMENSION * MARK DOES NOT INCLUDE MOLD FLASH

2. DIMENSION # MARK DOES NOT INCLUDE DAMBAR PROTRUSION

3.UNSPECIFIED IS ACCORDING TO JEDEC MO-136, VARIATION "BE"