

28C256

型 名	社 名	温度範囲 (°C)	スイッチング特性					電 源		入 力			出力/測定電流			備 考 [*typ]
			TAAC max (ns)	TCAC max (ns)	TOH max (ns)	TOE max (ns)	TOD max (ns)	VDD (V)	I DD/STANDBY (mA)	VIL max (V)	VIH min (V)	Ci max (pF)	VOL/I VOL max (V/mA)	VOH/I VOH min (V/mA)	Co max (pF)	
AT28HC256L-90	ATMEL	0~70	90	90	0	40	40	4.5~5.5	80/5	0.8	2	4*	0.45/8	2.4/4	8*	
HN58C256FP-20	HITACHI	0~70	200	200	0	90	70	4.5~5.5	30/1	0.8	2.2	6	0.4/2.1	2.4/0.4	12	
HN58C256P-20	HITACHI	0~70	200	200	0	90	70	4.5~5.5	30/1	0.8	2.2	6	0.4/2.1	2.4/0.4	12	
HN58C256P/FP-20	HITACHI	0~70	200	200	0	90	70	4.5~5.5	33/0.2	0.8	2.2	6	0.4/2.1	2.4/0.4	12	
KM28C256-15	SAM	0~70	150	150	0	80	50	4.5~5.5	60/1	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
KM28C256-20	SAM	0~70	200	200	0	100	50	4.5~5.5	60/1	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
KM28C256-25	SAM	0~70	250	250	0	120	50	4.5~5.5	60/1	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
MEM832V/J-120	MOSAIC	0~70	120	120	0	50	50	4.5~5.5	3/0.3	0.8	2.0	4*	0.45/2.1	2.4/0.4	8*	
MEM832V/J-150	MOSAIC	0~70	150	150	0	60	60	4.5~5.5	3/0.3	0.8	2.0	4*	0.45/2.1	2.4/0.4	8*	
MEM832V/J-90	MOSAIC	0~70	90	90	0	40	40	4.5~5.5	3/0.3	0.8	2.0	4*	0.45/2.1	2.4/0.4	8*	
X28C256	XICOR	0~70	300	300	0	100	50	4.5~5.5	60/2	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
X28C256-20	XICOR	0~70	200	200	0	80	50	4.5~5.5	60/2	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
X28C256-25	XICOR	0~70	250	250	0	100	50	4.5~5.5	60/2	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
X28C256-35	XICOR	0~70	350	350	0	100	50	4.5~5.5	60/2	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
X28C256B-15	XICOR	0~70	150	150	0	50	50	4.5~5.5	60/2	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
X28C256B-18	XICOR	0~70	180	180	0	50	50	4.5~5.5	60/2	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
X28C256B1-15	XICOR	-40~85	150	150	0	50	50	4.5~5.5	60/2	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
X28C256B1-18	XICOR	-40~85	180	180	0	50	50	4.5~5.5	60/2	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
X28C256I	XICOR	-40~85	300	300	0	100	50	4.5~5.5	60/2	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
X28C256I-20	XICOR	-40~85	200	200	0	80	50	4.5~5.5	60/2	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
X28C256I-25	XICOR	-40~85	250	250	0	100	50	4.5~5.5	60/2	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
X28C256I-35	XICOR	-40~85	350	350	0	100	50	4.5~5.5	60/2	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
X28256	XICOR	0~70	300	300	0	100	80	4.75~5.25	120/60	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
X28256-25	XICOR	0~70	250	250	0	100	80	4.75~5.25	120/60	0.8	2.0	6	0.4/2.1	2.4/0.4	10	
uPD28C256CD-20	NEC	0~70	200	200	0	75	60	4.5~5.5	50/1	0.8	2.0	12	0.45/2.1	2.4/0.4	10	
uPD28C256CD-25	NEC	0~70	250	250	0	100	80	4.5~5.5	50/1	0.8	2.0	12	0.45/2.1	2.4/0.4	10	

- 入出力はすべて TTL コンパチブル。
- データ出力 DO は 3 ステート。
- チップセレクトは 1 本で出力イネーブルあり。
- スタンバイモードあり。
- 28C256 (Seeq)。

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graph TD
    A0A14[A0~A14] --> D1[デコーダ]
    A0A14 --> D2[デコーダ]
    D1 --> ROM["(262144) ROMセル"]
    D2 --> SEL[セレクトタ]
    ROM --> SEL
    SEL --> BUF[バッファ]
    BUF --> IO["8  
I/O0~I/O7"]
    CS[CS] --> ROM
    OE[OE] --> BUF
  
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V_{DD} : +5V Pin 28
V_{SS} (GND) Pin 14

入 力			I/O	動 作
CE	OE	WE		
H	X	X	High-Z	Stand-by
L	L	H	DO	Read
L	H	L	DI	Write
X	X	H	High-Z	Write Inhibit
X	L	X	High-Z	Write Inhibit

The timing diagram illustrates the relationship between various signals during a memory access cycle. The signals shown are:

- Address ($A_0 - A_{14}$):** A bus signal that changes at the start of the cycle.
- $\overline{CE}$ (Chip Enable):** An active-low signal that goes low to initiate the cycle.
- $\overline{OE}$ (Output Enable):** An active-low signal that goes low to enable the data bus.
- $\overline{WE}$ (Write Enable):** An active-low signal that goes low to indicate a write operation.
- DO (Data Bus):** The data being transferred, shown as a sequence of hexagonal data bytes.

Key timing parameters are indicated:

- T_{CAC} (Access Time):** The time from the falling edge of $\overline{CE}$ to the first valid data on the DO bus.
- T_{OH} (Output Hold Time):** The time from the rising edge of $\overline{OE}$ to the last valid data on the DO bus.
- T_{AAC} (Access After Write Time):** The time from the rising edge of $\overline{WE}$ to the last valid data on the DO bus.
- T_{DC} (Data Hold Time):** The time from the rising edge of $\overline{OE}$ to the last valid data on the DO bus.