

IRF7751

HEXFET® Power MOSFET

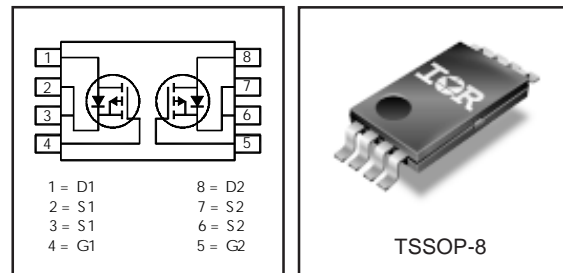
- Ultra Low On-Resistance
- Dual P-Channel MOSFET
- Very Small SOIC Package
- Low Profile (< 1.2mm)
- Available in Tape & Reel

V_{DSS}	$R_{DS(on)}$ max	I_D
-30V	$35m\Omega @ V_{GS} = -10V$	-4.5A
	$55m\Omega @ V_{GS} = -4.5V$	-3.8A

Description

HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the ruggedized device design, that International Rectifier is well known for, provides the designer with an extremely efficient and reliable device for use in battery and load management.

The TSSOP-8 package has 45% less footprint area than the standard SO-8. This makes the TSSOP-8 an ideal device for applications where printed circuit board space is at a premium. The low profile (<1.2mm) allows it to fit easily into extremely thin environments such as portable electronics and PCMCIA cards.



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-Source Voltage	-30	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-4.5	A
$I_D @ T_C = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-3.6	
I_{DM}	Pulsed Drain Current ①	-18	
$P_D @ T_C = 25^\circ C$	Power Dissipation ③	1.0	W
$P_D @ T_C = 70^\circ C$	Power Dissipation ③	0.64	
	Linear Derating Factor	0.008	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +150	°C

Thermal Resistance

	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ③	125	°C/W

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10/04/2000

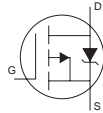
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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-30	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.020	—	V/°C	Reference to 25°C , $I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	35	m Ω	$V_{GS} = -10V, I_D = -4.5A$ ②
		—	—	55		$V_{GS} = -4.5V, I_D = -3.8A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	-2.5	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	6.8	—	—	S	$V_{DS} = -10V, I_D = -4.5A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	-15	μA	$V_{DS} = -24V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -24V, V_{GS} = 0V, T_J = 70^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
Q_g	Total Gate Charge	—	29	44	nC	$I_D = -4.5A$
Q_{gs}	Gate-to-Source Charge	—	5.5	—		$V_{DS} = -15V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	5.0	—		$V_{GS} = -10V$
$t_{d(on)}$	Turn-On Delay Time	—	13	20	ns	$V_{DD} = -15V$
t_r	Rise Time	—	16	24		$I_D = -1.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	155	233		$R_G = 6.0\Omega$
t_f	Fall Time	—	80	120		$V_{GS} = -10V$ ②
C_{iss}	Input Capacitance	—	1464	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	227	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	146	—		$f = 1.0\text{MHz}$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-1.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-18		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -1.0A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	23	35	ns	$T_J = 25^\circ\text{C}, I_F = -1.0A$
Q_{rr}	Reverse Recovery Charge	—	19	28	nC	$di/dt = 100A/\mu s$ ②

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

③ When mounted on 1 inch square copper board, $t < 10$ sec.

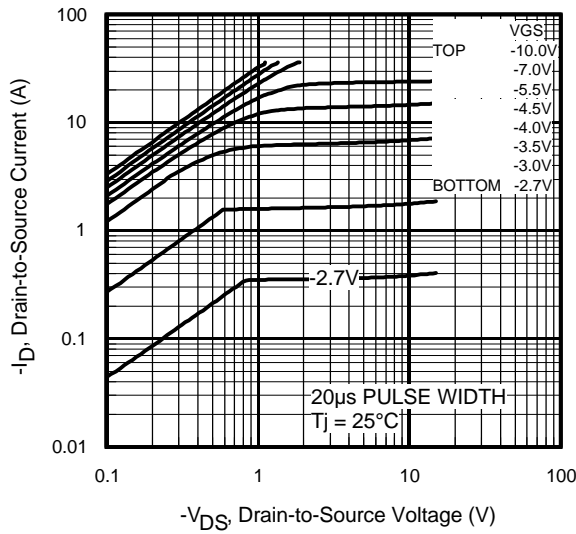


Fig 1. Typical Output Characteristics

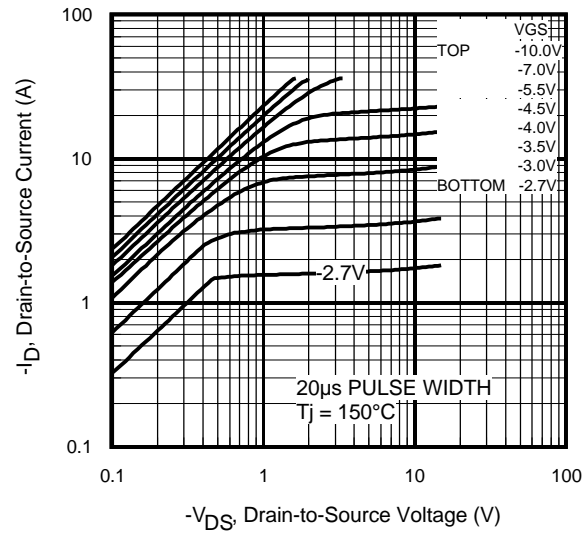


Fig 2. Typical Output Characteristics

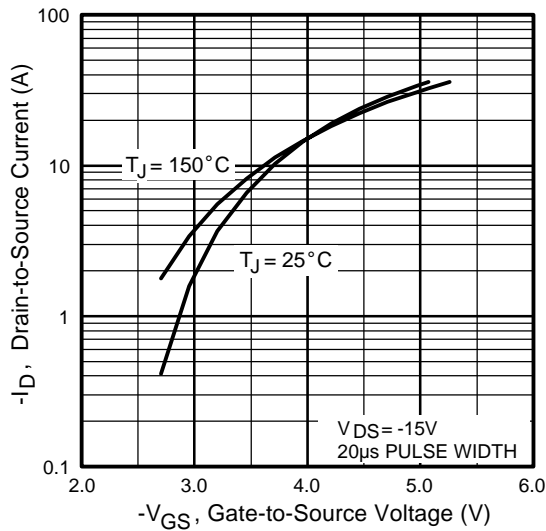


Fig 3. Typical Transfer Characteristics

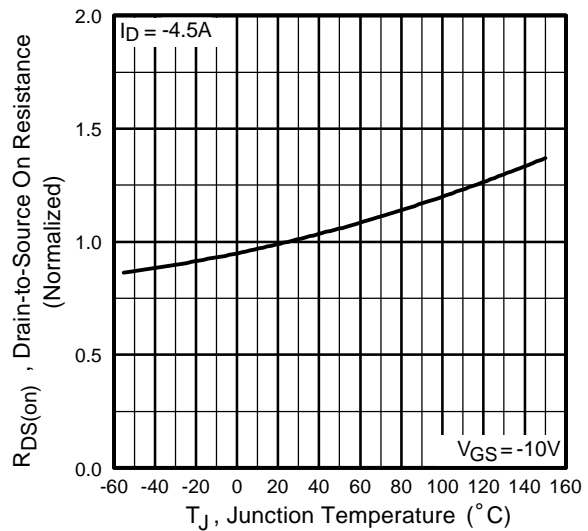


Fig 4. Normalized On-Resistance Vs. Temperature

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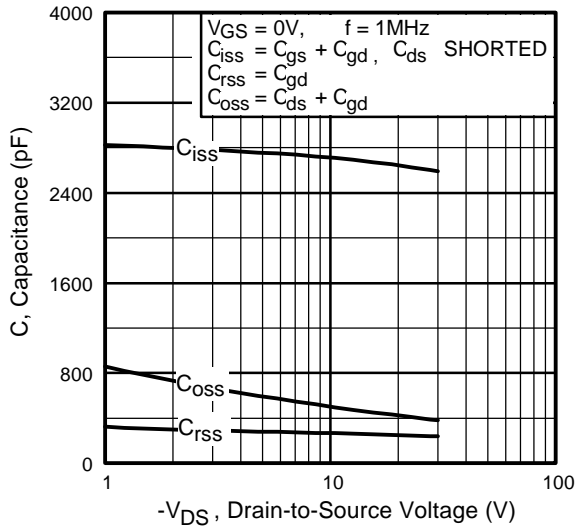


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

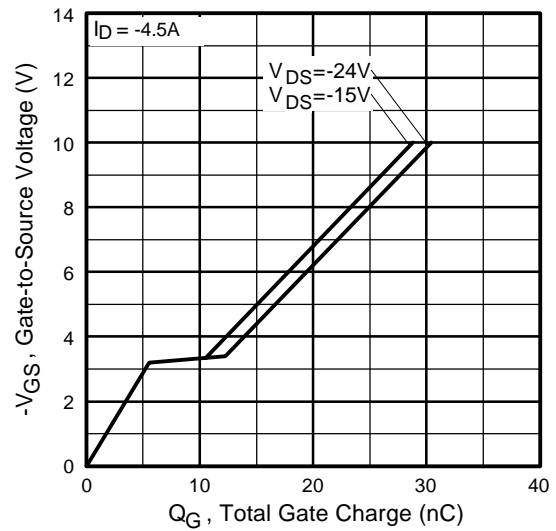


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

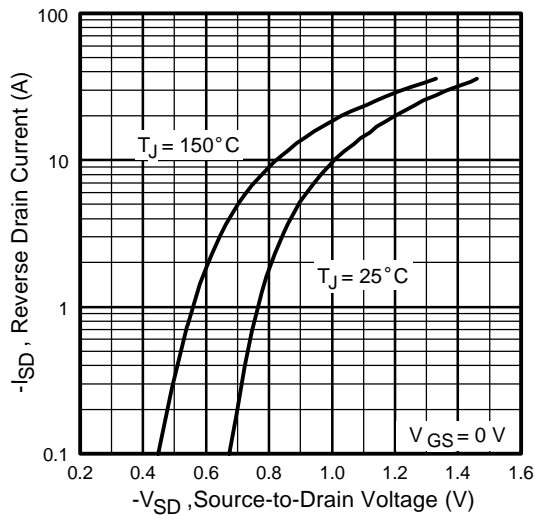


Fig 7. Typical Source-Drain Diode Forward Voltage

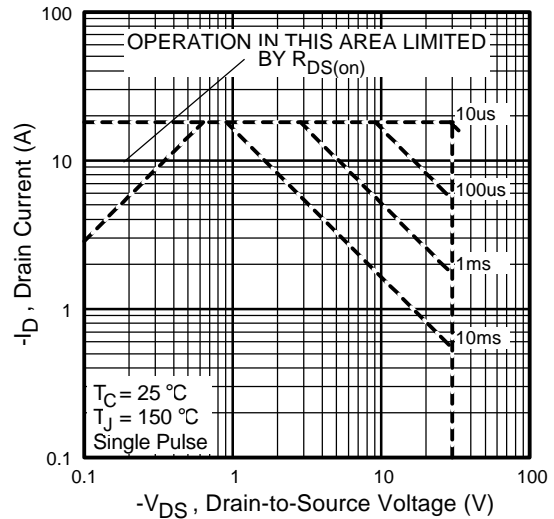


Fig 8. Maximum Safe Operating Area

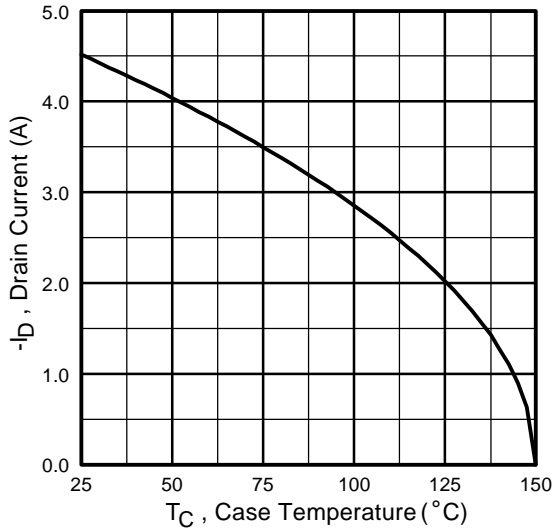


Fig 9. Maximum Drain Current Vs. Case Temperature

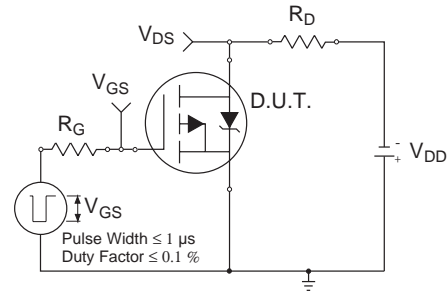


Fig 10a. Switching Time Test Circuit

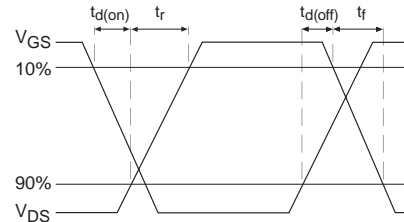


Fig 10b. Switching Time Waveforms

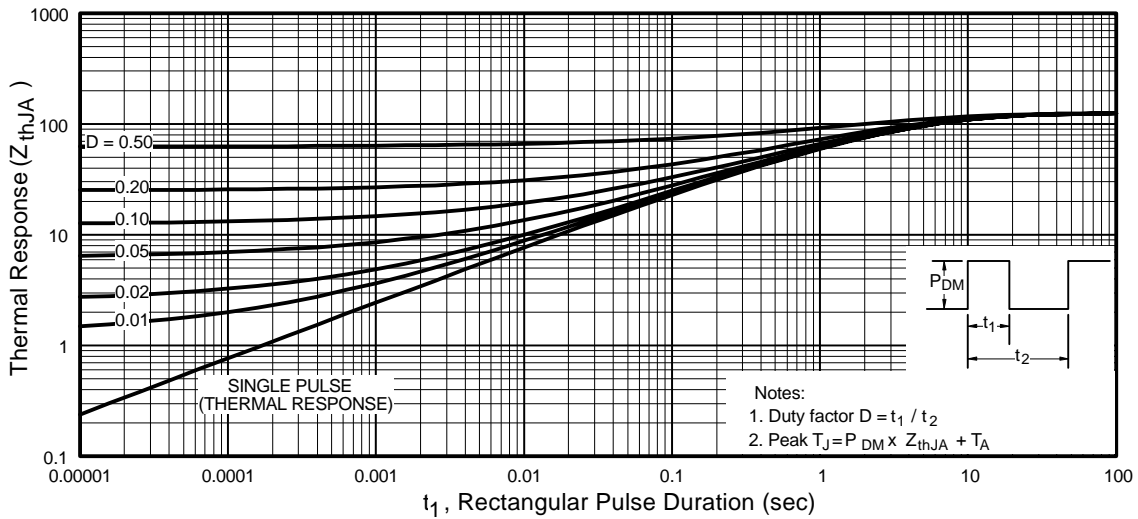


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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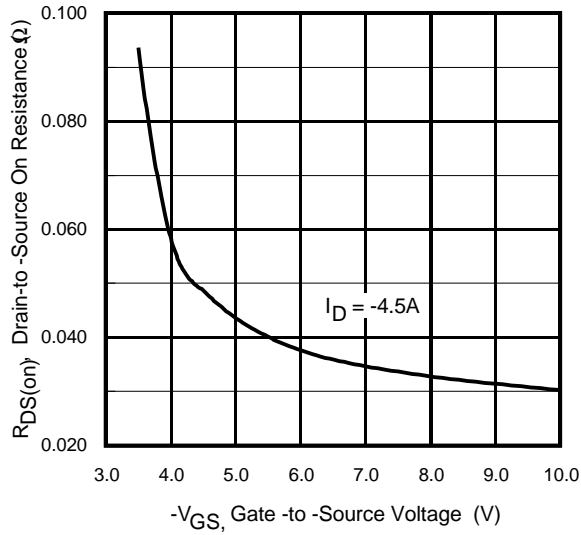


Fig 12. Typical On-Resistance Vs. Gate Voltage

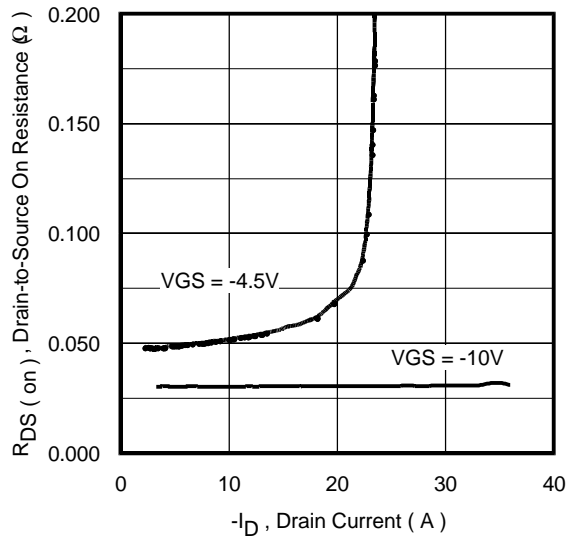


Fig 13. Typical On-Resistance Vs. Drain Current

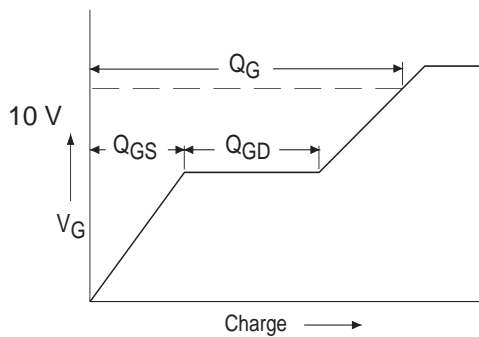


Fig 14a. Basic Gate Charge Waveform

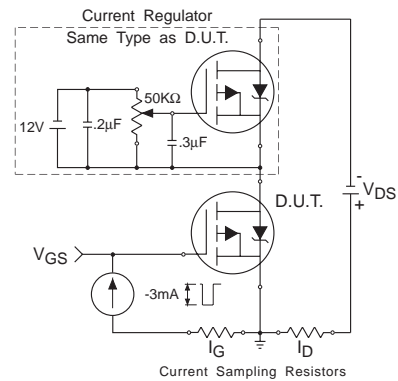
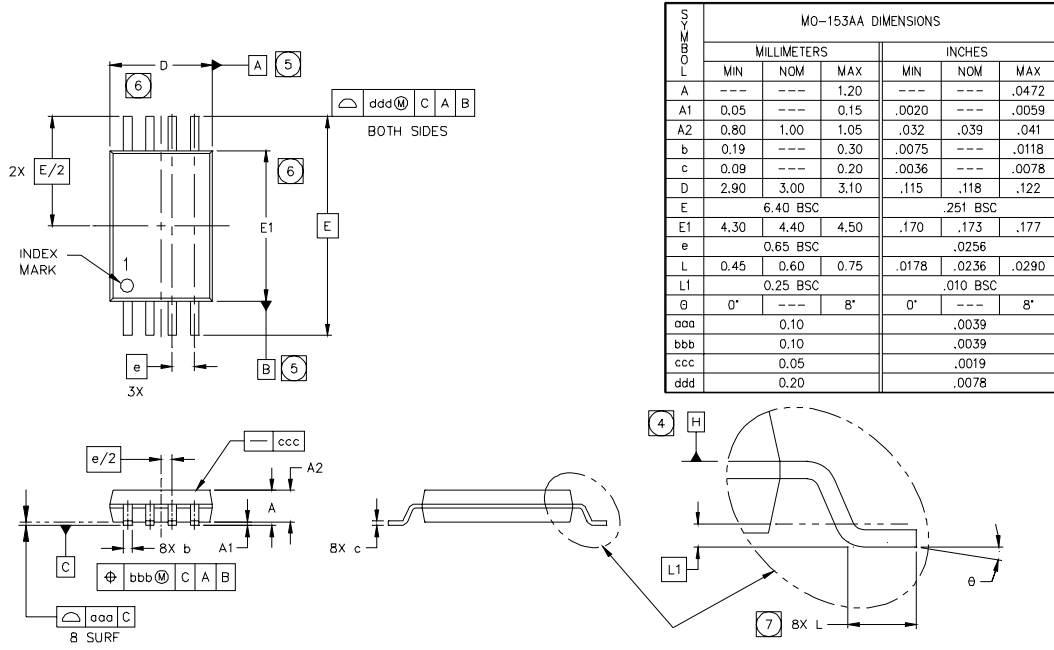


Fig 14b. Gate Charge Test Circuit

TSSOP-8 Package Outline



LEAD ASSIGNMENTS



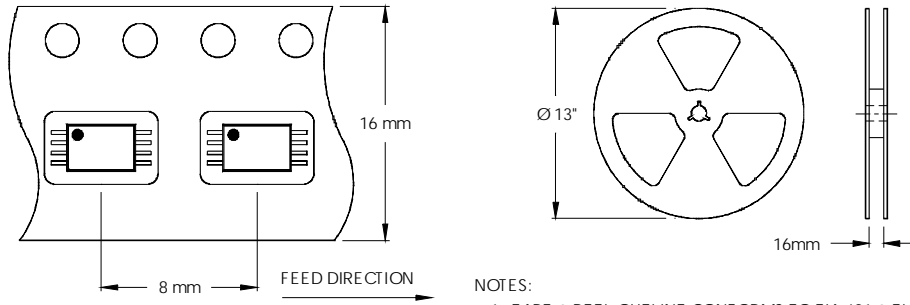
NOTES

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
- CONTROLLING DIMENSION: MILLIMETER.
- DATUM PLANE H IS LOCATED AS SHOWN.
- DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
- DIMENSIONS D AND E1 ARE MEASURED AT DATUM PLANE H.
- DIMENSION L IS THE LEAD LENGTH FOR SOLDERING TO A SUBSTRATE.
- OUTLINE CONFORMS TO JEDEC OUTLINE MO-153AA.

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TSSOP-8 Tape and Reel Information

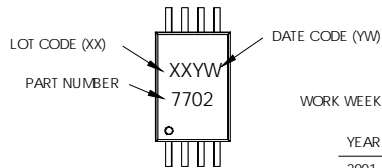
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NOTES:
1. TAPE & REEL OUTLINE CONFORMS TO EIA-481 & EIA-541.

TSSOP-8 Part Marking

EXAMPLE: THIS IS AN IRF7702



DATE CODE EXAMPLES:

9503 = 5C
9532 = EF

TABLE 1

WORK WEEK 1-26, NUMERIC YEAR CODE (1,2,...ETC.)

YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
1994	4	04	D
1995	5		
1996	6		
1997	7		
1998	8		
1999	9		
2000	0	24	X
		25	Y
		26	Z

TABLE 2

WORK WEEK 27-52, ALPHANUMERIC YEAR CODE (AB,...ETC.)

YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
1994	D	30	D
1995	E		
1996	F		
1997	G		
1998	H		
1999	J		
2000	K	50	X
		51	Y
		52	Z

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN: 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

Data and specifications subject to change without notice. 10/00