iT3042D

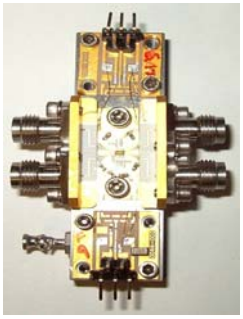
40 Gb/s High-Sensitivity Limiting Amplifier

Description

The iT3042D is a MMIC limiter amplifier for use in 40-Gb/s optical communications systems. Signals at levels as low as +/-25 mVpp differential can be amplified up to 1.0 Vpp differentially. The design allows an offset correction function, output voltage control, and output power monitoring. The inputs are AC and DC coupled and the output is DC coupled.

Features

- Small-signal differential gain: 28 dB
- Differential output voltage: 1000 mVpp
- Input sensitivity: +/-25 mVpp at Vout = 500 mVpp
- Single bias supply: -3.3 VDC
- Power consumption: 400 mW
- DC offset control
- Output voltage control
- Power monitoring
- Jitter degradation (rms): 0.6 ps



iT3042D in evaluation fixture

Absolute Maximum Ratings

Symbol	Parameters/conditions	Min.	Max.	Units
Vee	Power supply voltage	-4	0	V
Vd	Applied voltage at data input (differential)		3	V
Vm	Applied voltage at data input (single ended)		1.5	V
Vof	Offset control voltage	-3	0	V
Vofb	Offset control voltage	-3	0	V
Vctrl	Amplitude control voltage	-7	0	V
Tstg	Storage temperature	-65	150	°C

Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
VEE	Power supply voltage	-3.4	-3.3	-3.2	V
IEE	Total bias supply current	95	120	140	mA
Vof	Offset control voltage	-1.5	0	1.5	V
Vofb	Offset control voltage	-1.5	0	1.5	V
Vctrl	Amplitude voltage control	-2		-1.2	V
IAC	Voltage control current	0	4	5	mA
Vd	Applied peak-to-peak voltage at data input (diff.)	25		500	mVpp
Vm	Applied peak-to-peak voltage at data input (SE)	50		1000	mVpp
Vom	Output DC monitor (+)	-0.1	-0.25	-0.4	V
Vomb	Output DC monitor (-)	-0.1	-0.25	-0.4	V
	Input interface	AC/DC coupled			
	Output interface	DC coupled			

Electrical Characteristics

At 25 °C
50-ohm system VEE
= -3.3 VDC

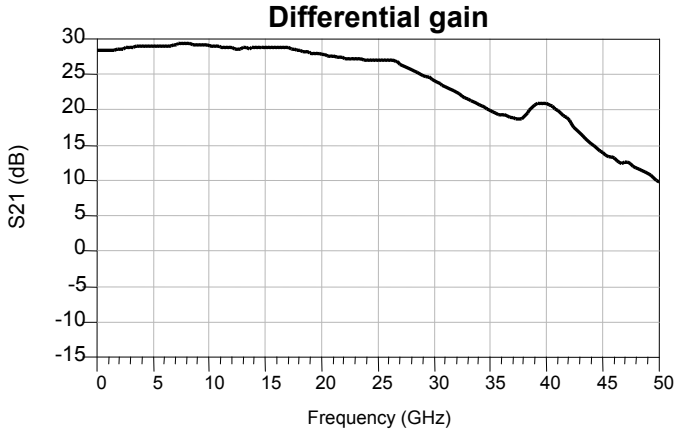
Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
P	Power consumption (500 mVpp single-ended output)	300	400	460	mW
G	Differential small-signal gain at 2 GHz Pin = -30 dBm	26	28		dB
B3dB	3 dB bandwidth Pin = -30 dBm		28		GHz
Rlin	Input return loss up to 50 GHz	12			dB
Rlout	Output return loss up to 50 GHz	5			dB
Vin	Input signal	+/-25		+/-500	mVpp
Voutdc	Average DC output voltage	-0.15	-0.25	-0.35	V
Vout	Output peak-to-peak voltage (either Q or \Q) (Vin from +/-25 mVpp to +/-500 mVpp)	500			mVpp
T_r	Rise time (20% to 80%), single-ended output		11.5	12.5	ps
T_f	Fall time (20% to 80%), single-ended output		9.5	10.5	ps
JRMS	Jitter rms (1)		0.6	1	ps

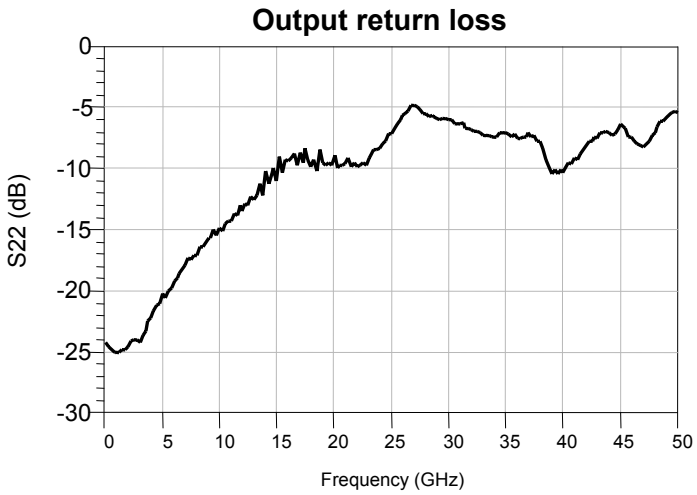
(1) **Jitter RMS measured as** $(Jitter_{RMS\_output}^2 - Jitter_{RMS\_input}^2)^{1/2}$

S-Parameter Data

VEE = -3.3 VDC
Vctrl = -1.6 VDC

Pin = -30 dBm (linear)
Wafer probe tested

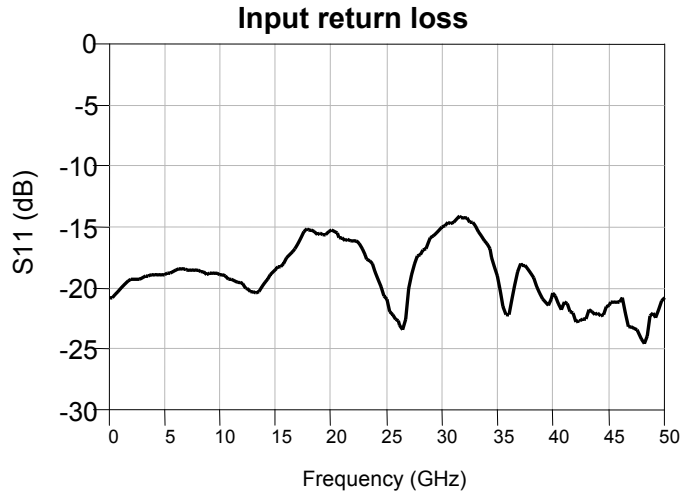




S-Parameter Data (cont.)

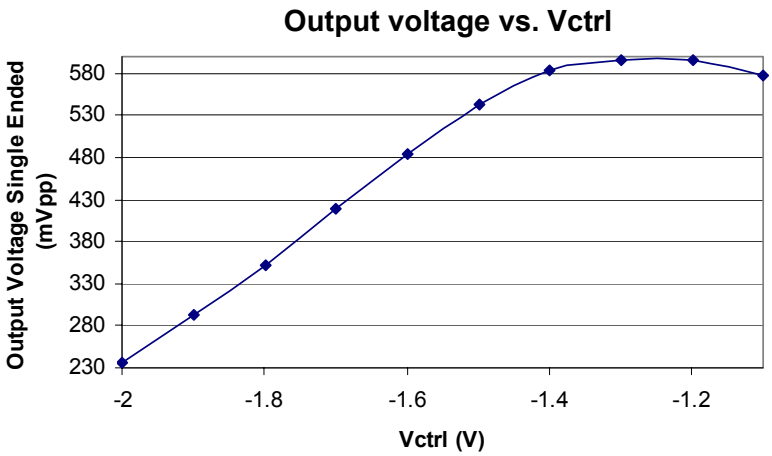
VEE = -3.3 VDC
Vctrl = -1.6 VDC

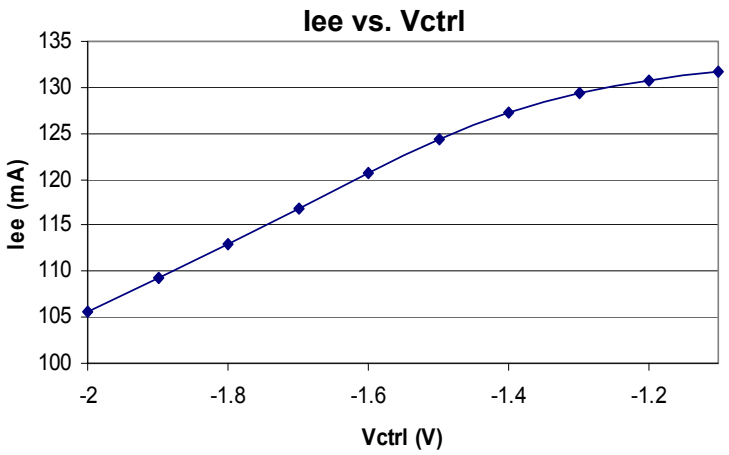
Pin = -30 dBm (linear)
Wafer probe tested



Output Voltage Control

At ambient temperature and 40-Gb/s



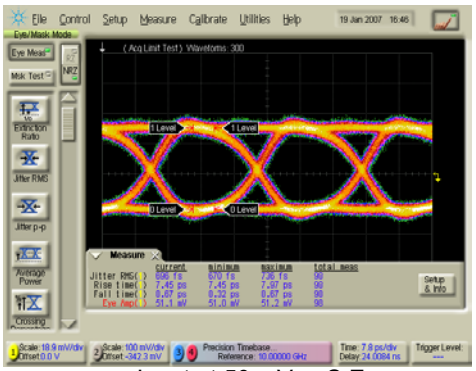


Eye Diagram Performance

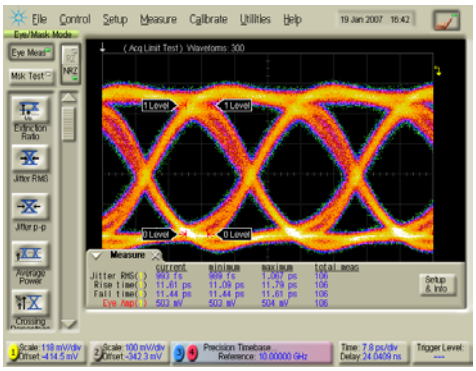
At ambient temperature

All outputs shown are single-ended.

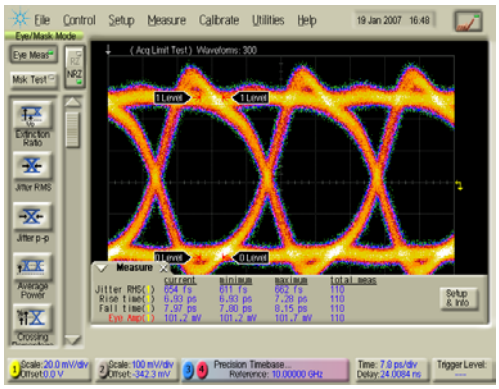
Tested on a fixture



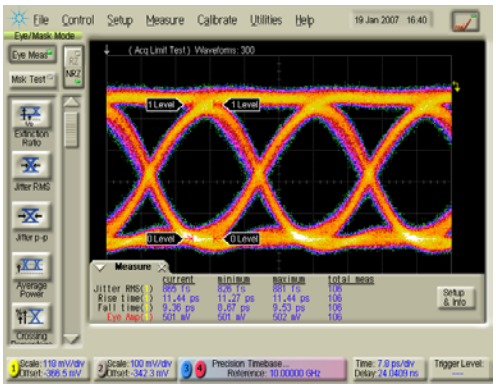
Input at 50 mVpp S.E.
Bit rate: 40 Gb/s
Jitter $_{RMS}$= 0.74 ps



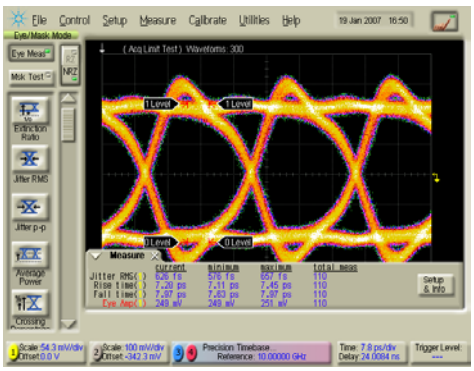
Input = 50 mVpp SE., Output = 503 mV SE
Bit rate: 40 Gb/s
Jitter $_{RMS}$ degradation = 0.75 ps, Vctrl = -1.4 V



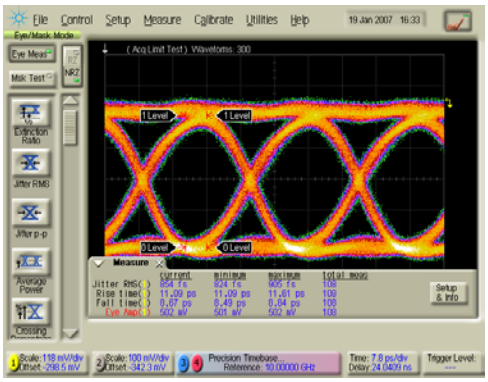
Input at 100 mVpp SE
Bit rate: 40 Gb/s
Jitter $_{RMS}$ = 0.66 ps



Input = 100 mVpp SE., Output = 502 mV SE
Bit rate: 40 Gb/s
Jitter $_{RMS}$ degradation = 0.58 ps, Vctrl = -1.58 V

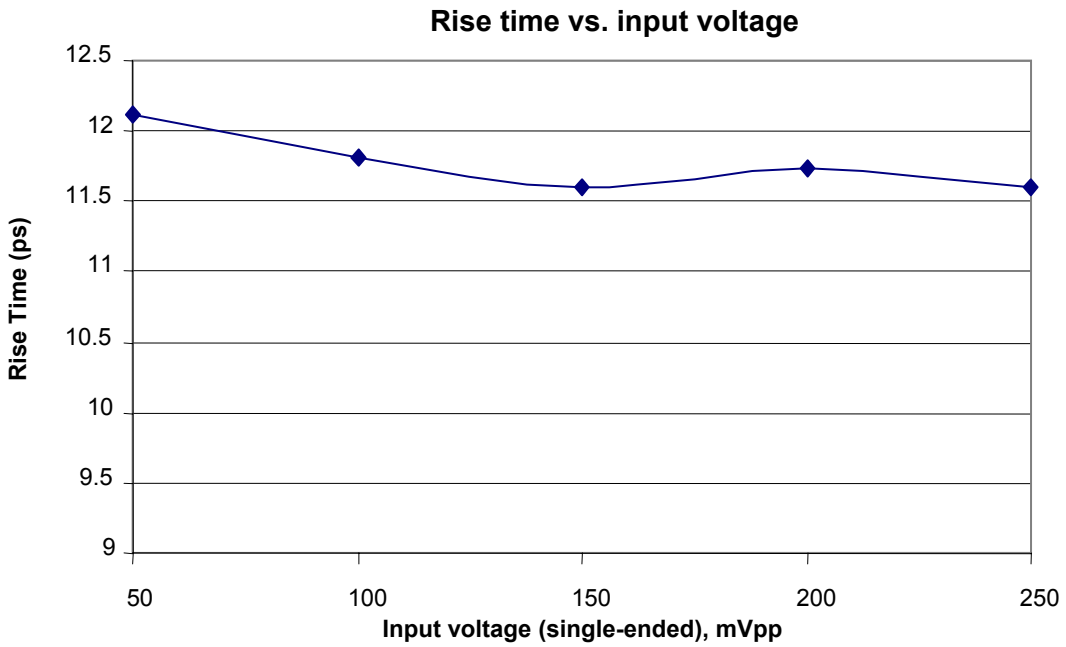


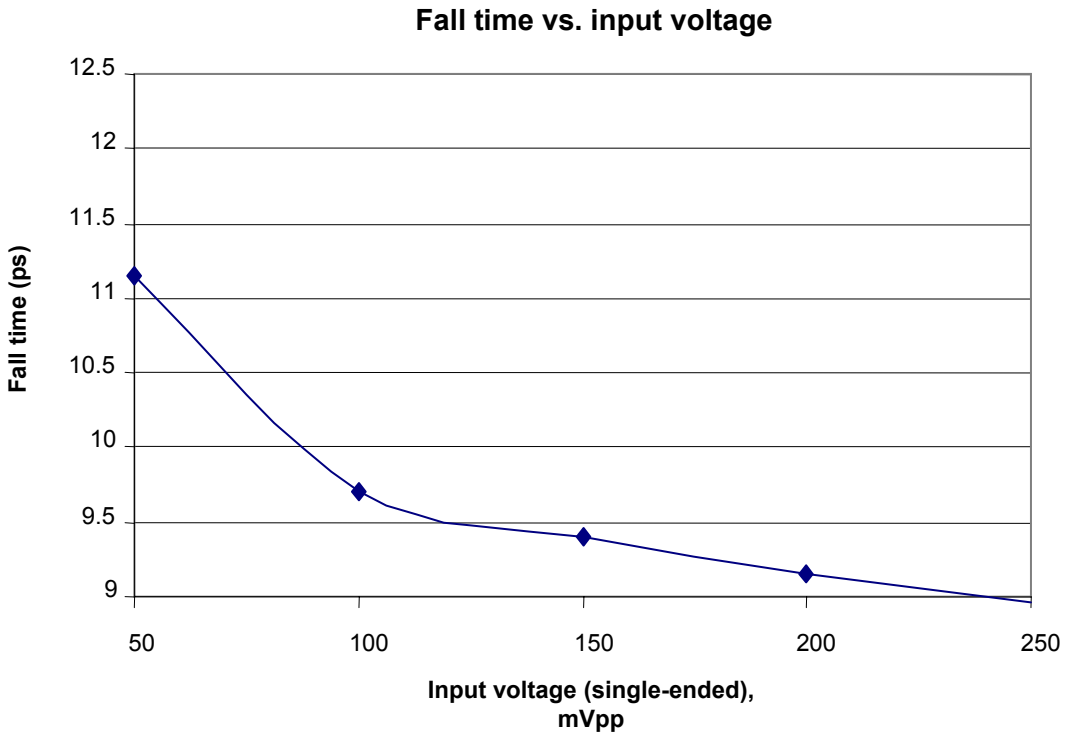
Input at 250 mVpp SE
Bit rate: 40 Gb/s
Jitter $_{RMS}$= 0.66 ps



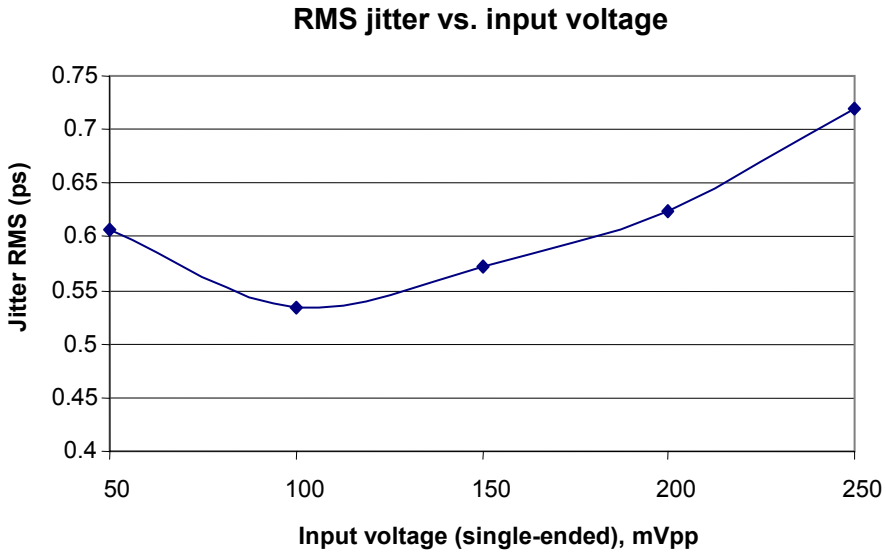
Input = 250 mVpp SE, Output = 502 mV SE
Bit rate: 40 Gb/s
Jitter $_{RMS}$ degradation = 0.62 ps, Vctrl = -1.59 V

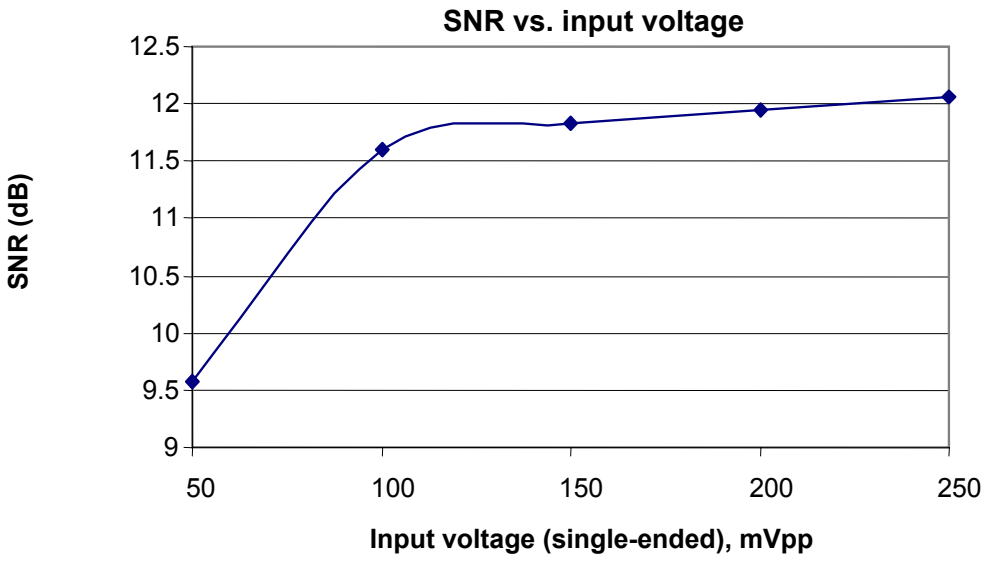
Performance As Function of Input Voltage





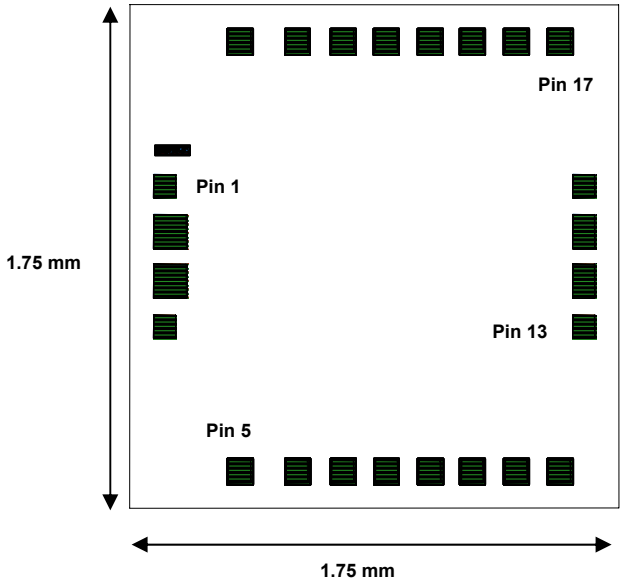
Performance As Function of Input Voltage (cont.)





Chip Layout, Front View and Bond Pad Locations

Back of chip is connected to RF and DC ground.



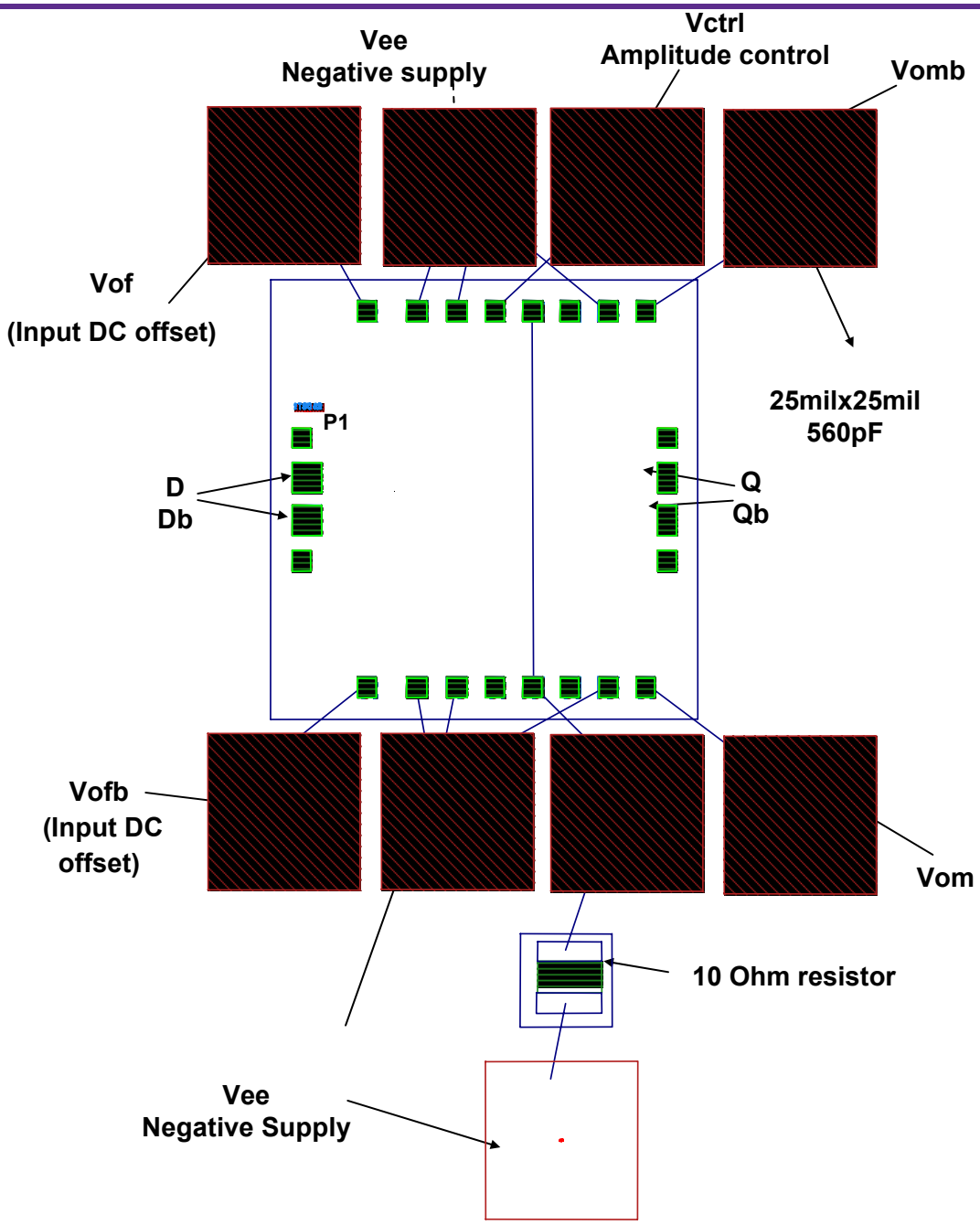
Pinouts

Pin	Designation	Description
P1	GND	Ground
P2	D	Data Input +
P3	Db	Data Input -
P4	GND	Ground
P5	Vofb	DC offset on Input -
P6	Ve1l	Power Supply, -3.3 V
P7	Ve2l	Power Supply, -3.3 V
P8	NC	No connection
P9	Vee1l(1)	Power Supply –3.0V
P10	NC	No connection
P11	Ve3l	Power Supply, -3.3 V
P12	Vom	DC monitor on output +

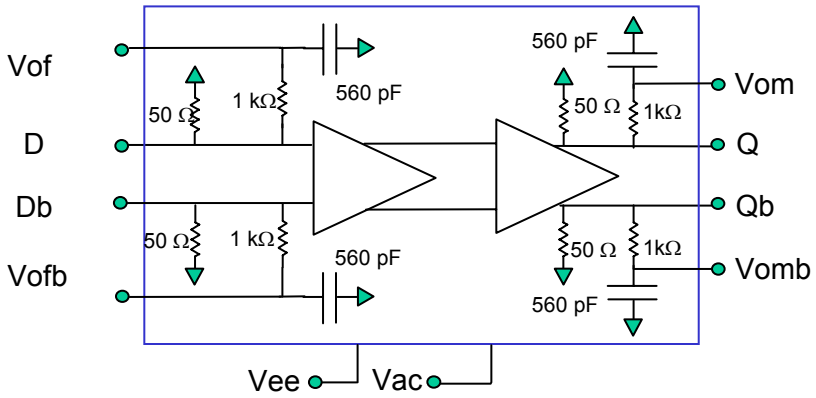
Pin	Designation	Description
P13	GND	Ground
P14	Qb	Data Output -
P15	Q	Data Output +
P16	GND	Ground
P17	Vomb	DC monitor on output -
P18	Ve3u	Power Supply, -3.3 V
P19	NC	No Connection
P20	Vee1u(1)	Power Supply, -3.0 V
P21	Vctrl	Amplitude Control
P22	Ve2u	Power Supply, -3.3 V
P23	Ve1u	Power Supply, -3.3 V
P24	Vof	DC offset on Input +

1. The -3.0 VDC supply can be achieved on Pin P9 and P20 by connecting a 10 ohm resistance in series with the -3.3 VDC supply and the two die pads.

Recommended Assembly Diagram



Device Diagram



Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

Chip carrier material should be selected to have InP compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325° C for 15 min.

Die attachment for power devices should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for HBT devices. Note that the backside of the chip is gold plated and it is connected to RF and DC ground.

These InP devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. The devices should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding: for signal input/output connections, use either 3 mil wide and 0.5 mil thick gold ribbon or a pair of 1mil diameter wires with lengths as short as practical allowing for appropriate stress relief (typically 400 +/- 100 µm long). For all other connections, a single 1 mil dia wire of appropriate minimum length may be used.