KRYPTON K²940G/ K²940GU DAA CHIPSET

HIGH PERFORMANCE, LOW COST, ALL SILICON DAA (DATA ACCESS ARRANGEMENT)

FEATURES:

- High performance for modems up to V.34, 33.6Kbps, and 56Kbps **(Flat frequency response down to 10Hz)**
- 1.5 KVDC/1KVAC isolation and 2.5KVDC/1.5KVAC isolation for UL safety approval
- *KRYPTON Patented Technology* isolation techniques eliminate transformer or linear opto-coupler
- Low cost complete DAA function connects directly to phone line Tip and Ring
- Low profile surface mount for PCMCIA and daughter-card applications
- FCC Part 68, DOC CS-03 and UL 1459 protection circuitry
- OFFHOOK switch implemented with low cost SMD transistors
- Caller ID capability built in
- Powered from +5V and telephone line; 20 mW from +5V active, only 0.1 mW in stand-by mode
- 2/4 Wire hybrid converter built in
- Differential input and output, local analog loop back
- Easy interface to all modem/AFE chipsets

APPLICATIONS:

- Modems
- Fax Machines
- PDAs (Personal Digital Assistants)
- Answering Machines
- Key Telephone
- Devices attached to customer premises side of phone line (e.g. TV set-top boxes)

DESCRIPTIONS:

The *KRYPTON* K²940G DAA (Data Access Arrangement) chipset consists of K²941C, K²942C and K²934-2. The *KRYPTON* K²940GU DAA chipset consists of K²941C, K²942C and K²944-2, which is a UL-recognized component (file #E176027). The silicon chipsets, with their associated external components, provide all the necessary line monitoring, filtering, isolation, protection and signal conversion functions for the connection of high speed analog modem devices (V.32bis, V.34, 33.6Kbps, 56 Kbps) to the public switched telephone network using only +5V power supply (20mW active, 0.1mW standby) for modem applications. The chip set is designed for isolation from 1 KVrms for FCC/DOC and 1.5KVrms for UL safety requirements.

The *KRYPTON* K²940G/K²940GU is an SSOP (0.150 inch) packaged chipset.

FUNCTIONAL DESCRIPTION:

K²941C:

The K²941C is a 16-pin integrated circuit which interfaces to a modem chipset or other complex electronic system. It contains

- **differential Transmit input buffer**
- **differential Receive output buffer**
- **voltage reference input circuit**
- **power down circuit**
- **OFFHOOK and CALLER ID control input circuit**
- **local analog loop-back**
- **on-chip 350 KHz oscillator**
- **input/output interface circuit**

The K²941C is in a 16-pin SSOP (0.150 inch) package.

The **differential Transmit input buffer** receives the input signals from the modem chipset's Transmit output pins. The K²941C differential Transmit input pins have an internal DC bias at approximately 2.5V and 200 KOhm input impedance. The input mode can be differential, or single ended if one of the TXA+ or TXA- (Pin 1 or Pin 2) pins is AC grounded.

The **differential Receive output buffers** output signals to the modem chipset's Receive pins. With the DC bias at approximately 2.5V, the buffers can have a maximum load (lowest resistance) of 10KΩ at RCV+ or RCV- pins (Pin 4 or Pin 5) to an AC ground.

The **voltage reference input circuit** senses the external modem chipset's DC common mode voltage (VCM) reference level. The K²941 will then bias the transmit input buffer with this voltage level, if the VFIN (Pin 7) has been connected to the external VCM. This results in saving AC coupling capacitors from modem chips to the K²941 pin1 (TXA+) and pin2 (TXA-). If the VFIN (Pin 7) is grounded, the K²941 will self-bias at approximately 2.5V; then AC coupling capacitors may be required to prevent undesired DC current flow.

The **OFFHOOK and CALLER ID control input circuit** senses the control levels from the input pins OFFHK\ and CLID\ (active low). This circuit then transfers these control signals through the K²934-2 or K²944-2 to the K²942C, which controls the external transistors that constitute the OFFHOOK and the CALLER ID switches. (See Functional Diagram, Figure 1.)

The K²941 also provides a **local analog loop-back** feature when the OFFHK\ and CLID\ signals are not active (both inputs high). The differential TXA+/- pins are connected internally to the RXA+/- pins for this local analog loop-back modem test feature.

The **power down circuit** is controlled by the OFFHK\ and CLID\ control input pins (Pins 14 and 11). When the OFFHOOK and CALLER ID both are not active (both inputs high), the K²941 is in a power-down mode with only 0.1mW power consumption. When either control input is active (input low), the K²941 exits the **power-down mode** and requires 20mW power to operate. The circuit will not operate properly if both OFFHOOK and CALLER ID are active simultaneously (both inputs low).

The K²941C has an **on-chip 350 KHz oscillator**. The RSET pin (Pin 8) requires a 150 kΩ/1% resistor (see Functional Diagram, Figure 1). This resistor sets the operating frequency of this oscillator, as well as internal current biasing levels within

the integrated circuit.

An **input/output interface circuit** transfers all signals through the isolation barrier constituted by the custom capacitive arrays, K²934-2 or K²944-2, using ***KRYPTON Patented Technology.***

K²942C:

The K²942C is powered from the telephone line. It receives the OFFHOOK or CALLER ID control signals from the K²941C, which then enables the K²942C to activate the external transistors which allow it to receive power from the line (different amount of power for CALLER ID than for OFFHOOK). The K²942C then transfers all necessary analog signals from/to the telephone line (TIP and RING) through the custom capacitive isolation arrays (K²934-2 or K²944-2) to/from the K²941C. It contains

- **DC voltage termination and line power reference block**
- **2 to 4 wire converter hybrid**
- **Transmit and receive drivers**
- **Transmit and trans-hybrid loss gain control**
- **OFFHOOK and Caller ID control output circuit**
- **Caller ID Receive buffer**
- **Input/output interface circuit**

The K²942C is in a 28-pin SSOP (0.150 inch) package.

The **DC voltage termination and line power reference block** regulates telephone line current to supply the K²942C reference voltage. The circuit is designed to provide a termination over a loop current range from 15mA to 120 mA during the OFFHOOK mode. The voltage termination falls within the worst case current requirements of FCC Part 68 and DOC CS-03. By changing the 51Ω resistor value or setting a different DC level at SET pin (Pin 19), the K²942 DC V/I termination will change. The line power reference block will regulate 3 mA (maximum) line current from LINE pin (Pin 21) and generate 3.2VDC at VDR pin (PIN 16). The 80.6 kΩ external resistor sets the internal current and must be 1% tolerance. The TER1 pin and TER2 pin control the external NPN transistor Q3 to meet the line DC V/I termination requirements. (See Functional Diagram, Figure 1)

The **2 to 4 wire converter hybrid** has a trans-hybrid loss of typically 30dBm when connected as shown in Functional Diagram Figure 1, when the telephone line has a 600Ω AC termination. For minimum echo on the line, Pin LINE (Pin 21) connects to an AC termination network RT1(1K) and RT2 (1.5K), whose parallel equivalent value is equal to 600Ω. The use of external components allows the termination (or return loss) to be adjustable in a manner that is in accordance with the requirements of the different regulatory agencies. Because of the linear characteristics of the K²942, the degree of return loss is totally dependent on the impedance values matching between the external AC termination network and the phone line AC impedance.
(See Functional Diagram, Figure 1).

The **transmit and receive drivers** interface to a 2 to 4 wire converter and hybrid circuit for optimizing the impedance match. When the K²941C OFFHK\ input is low (active), the transmit driver outputs a signal to the phone line. The receive driver receives a 2 to 4 wire converted signal from the phone line. When the K²941C PIN CLID\ inputs are low (active), only the receive driver acquires Caller ID signal from the phone line.

The **Transmit Gain** and **Trans-Hybrid Loss** are both set by an external resistor, nominally 84.5Ω. The value of 84.5Ω is set at maximum trans-hybrid loss for a 600Ω AC line termination. Changing the value will change both the trans-hybrid loss and the transmit gain. (See Functional Diagram, Figure 1).

The **OFFHOOK and Caller ID control circuits** receive the control signals from the K²941C via the custom capacitive isolation arrays K²934-2 or K²944-2, convert and output the appropriate control signals to external OFFHOOK and Caller ID circuits. The **KRYPTON** K²940G/K940GU chipset has been designed in such a way that by using K²934-2 or K²944-2 as the isolation barriers for all signals, the external OFFHOOK switch circuit and Caller ID circuit can be built using low cost surface mount (SOT-23) 300V transistors. (See Functional Diagram, Figure 1.)

The Caller ID Receive buffer circuit will be active when the K²941C CLID\ pin (Pin 11) input is low. This circuit will draw less than 1 mA of current from the telephone line and pass the Caller ID signal to the Receive driver, transferring the signal through the K²934-2 or K²944-2 to the K²941C. The Caller ID signal then is presented at the RCV+/RCV- output pins (Pin 4 and Pin 5) of the K²941C.

The **Input/output interface circuit** connects to the custom capacitive isolation arrays K²934-2 or K²944-2 to transfer the signals through the isolation barrier using ***KRYPTON Patented Technology.***

K²934-2 and K²944-2

The K²940G chipset includes three K²934-2 **custom capacitive isolation arrays.** This isolation barrier withstands the minimum 1000VAC/1500VDC required by FCC Part 68 and DOC CS-03 standards. The K²940GU chipset includes three K²944-2 **custom capacitive isolation arrays**. The K²944-2 has received UL component recognition (file #: E176027) to UL1950, and can withstand 1500VAC/2500VDC. The K²934-2 or K²944-2 arrays connect between the K²941C and K²942C input/output interface circuits to transfer signals across the isolation barrier using ***KRYPTON Patented Technology.*** The K²934-2 and K²944-2 are packaged in surface mount 4-pad low profile packages.

ABSOLUTE MAXIMUM RATINGS (At 25°C, unless otherwise specified)

K²941C

Power Supply Voltage, -- Pin 3	----------	7V
Input Voltage, -- Pin 1,2,7,11,14	----------	-0.3V to 7V
Storage Temperature	----------	-25°C to +150°C
Package Lead Temperature		
Soldering (10 sec.)	----------	260°C
Vapor Phase (60 sec.)	----------	215°C
Infrared (15 sec.)	----------	220°C
Operating Temperature	----------	0°C to +70°C

K²942C

Line Supply Voltage, -- Pin 21	----------	18V
Storage Temperature	----------	-25°C to +150°C
Package Lead Temperature		
Soldering (10 sec.)	----------	260°C
Vapor Phase (60 sec.)	----------	215°C
Infrared (15 sec.)	----------	220°C
Operating Temperature	----------	0°C to +70°C

ELECTRICAL SPECIFICATIONS (at 25° C):

Minimum and Maximum values are testing requirements. Typical values are characteristics of the devices and are the results of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements. All of the specifications in the tables below assume the recommended components are in place.

Table 1. DC and AC Termination Characteristics

Parameter	*Symbol*	*Test Condition*	*Min*	*Typ*	*Max*	*Unit*
DC Termination Voltage	Vter	See Figure 2. Is=20mA Vs=0 Is=120mA Vs=0		 7.0 16.5		 V V
AC Line Impedance	Zter	See Figure 2. Is=30mA Zter=Rref(Vter÷(Vs-Vter)) Vs=-3dBm/100Hz-4KHz	580		650	Ohm

Table 2. Receive Path Characteristics

Parameter	*Symbol*	*Test Condition*	*Min*	*Typ*	*Max*	*Unit*
Receive Gain	Gr(ac)	See Figure 3. Is=30mA Vs=-3dBm/1004Hz, Vg=0 Gr(ac)=(Vr+) or (Vr-)÷Vt	-6.7	-6.0	-5.3	dB
Receive Frequency Response	Gr(f)	See Figure 3. Is=30mA, Vg=0 Gr(f)=Vr(f)÷Vr(1004Hz)				dB
		Vs=-3dBm/100Hz-3400Hz	-0.10		+0.10	
		Vs=-3dBm/20Hz-100Hz	0.00		+0.50	
		Vs=-3dBm/10Hz-20Hz	0.00		+1.00	
Receive 2nd/3th/4th Harmonic Distortion	Vr+(dis) Vr-(dis)	See Figure 3. Is=30mA Vg=0 Vs=-3dBm/150Hz		-82		dBm
		Vs=-3dBm/1004Hz		-85		dBm
Resistive Load	Rload	K²941C Rcv+ (Pin4) and Rcv-(Pin5) to AC ground	10			KOhm
Trans-hybrid Loss	THL	See Figure 3. Is=30mA Vg(f)=200-3400Hz, Vg=-3dBm THL=Vg(f)÷(Vr+) or (Vr-), Vs=0	30	35		dB
Receive noise floor	Vr+(noi) Vr-(noi)	See Figure 3. Is=30mA, Vs=Vg=0 f=200-3400Hz , 100Hz BW		-95		dBm

Table 3. Transmit Path Characteristics

Parameter	*Symbol*	*Test Condition*	*Min*	*Typ*	*Max*	*Unit*
Transmit gain	Gt(ac)	See Figure 3. Is=30mA Vg=-9dBm/1004Hz , Vs=0 Gt(ac)=Vt÷Vg	-0.7	0.0	+0.7	dB
Transmit Frequency Response	Gt(f)	See Figure 3. Is=30mA Vs=0 Gt(f)=Vt(f)÷Vt(1004Hz) Vg=-9dBm/150Hz-4000Hz	-0.20		+0.20	dB
Transmit 2nd/3rd/4th Harmonic Distortion	Vt(dis)	See Figure 3. Is=30mA Vg=-3dBm/1004Hz, Vs=0		-85		dBm
Transmit Input Impedance	Zin(ac)	K²941C TXA+(Pin1) and TXA-(Pin 2) to AC Ground		200		KOhm
Max. Line Drive Voltage	Vt(max)	See Figure 3. Is=30mA		3.0		V pk-pk
Transmit Noise Floor	Vt(noi)	See Figure 3. Vg=0, Vs=0, Is=30mA f=200-3400Hz, 100Hz BW		-89		dBm

Table 4. Power and DC Logic Input Characteristics

Parameter	*symbol*	*Test Condition*	*Min*	*Typ*	*Max*	*Unit*
DC current Supply	Icc	Input to K²941C VCC (Pin 3)	3.0	4.0	5.0	mA
DC Voltage Supply	Vcc	K²941C VCC (Pin 3) to GND (Pin 6)	4.50		5.5	V
Tip/Ring DC Loop Current	Il	K²942C LINE (Pin 21) + Ic (Q3) DC Loop Current Input See Figure 1.	15		120	mA
Offhook Logic Input	Voh	K²941C OFFHK\ (Pin 14) to GND (Pin 6) Active (Off-hook) Inactive (On-hook)	 Vcc-0.5		0.8	 V V
Caller ID Logic Input	Vid	K²941C CLID\ (Pin 11) to GND (Pin 6) Active (Call ID On) Inactive (Call ID Off)	 Vcc-0.5		0.8	 V V
Ref. Voltage Input range	Vrefin	Input to K²941C VFIN (Pin 7) to GND (Pin 6)	2.3	2.5	2.7	V

Table 5. Caller ID Receive Path Characteristics

Parameter	*Symbol*	*Test Condition*	*Min*	*Typ*	*Max*	*Unit*
Caller ID Receive Gain	Gid(ac)	See Figure 4. Es=48V Vs=-15dBm/1004Hz Gid(ac)=(Vr+) or (Vr-)÷Vs	-7.0	-6.0	-5.0	dB
Caller ID DC Current	Iid(dc)	See Figure 4. Es=48V Vs=0			1.0	mA

Table 6. Common Mode Noise Rejection Ratio Characteristics

Parameter	*Symbol*	*Test Condition*	*Min*	*Typ*	*Max*	*Unit*
Transmit Path CMRR	Tcmrr	See Figure 5. Tcmrr=Vcm÷Vt Vcm=100Vrms/60Hz Vcm=2Vrms/4KHz		 100 80		 dB dB
Receive Path CMRR	Rcmrr	See Figure 5. Rcmrr=Vcm÷(Vr+) or (Vr-) Vcm=100Vrms/60Hz Vcm=2Vrms/4KHz		 100 80		 dB dB

Table 7. FCC Part 68 Requirement Characteristics

Parameter	*Symbol*	*Test Condition*	*Min*	*Typ*	*Max*	*Unit*
Dielectric Voltage Rating	Vbrk	See Figure 7. And for using K²934-2	1000 1500			Vac Vdc
		See Figure 7. And for using K²944-2 *(UL recognized)*	1500 2500			Vac Vdc
Longitudinal Balance	LBC	FCC Part 68.310 On-hook and Offhook mode 200 to 1000Hz 1000 to 4000Hz	 60 40			 dB dB
On-hook DC Resistance	Ronhk	FCC Part 68.312 1VDC to 200VDC	10			MOhm

This data sheet or catalog has been carefully checked and believed to be reliable; however, no responsibility is assumed for possible omissions or inaccuracies. Specifications and drawings are subject to change without notice.

ORDERING INFORMATION

Chipsets	*Device*	*Qty*	*Package*	*Marking*
K²940G (SSOP Package)	K²941C	1	16-Pin SSOP (3.9mm/150mil)	K²941C-Date Code - Rev
	K²942C	1	28-Pin SSOP (3.9mm/150mil)	K²942C-Date Code - Rev
	K²934-2AR	3	4-Pad Array (3.4mm/134mil)	None
K²940GU (SSOP Package) UL-recognized	K²941C	1	16-Pin SSOP (3.9mm/150mil)	K²941C-Date Code - Rev
	K²942C	1	28-Pin SSOP (3.9mm/150mil)	K²942C-Date Code - Rev
	K²944-2AR	3	4-Pad Array (3.85mm/151mil)	None

note: Ask for K²940GT or K²940GUT for extended temperature (-25°C to +85°C) rating

PIN DEFINITIONS:

K²941C PIN DEFINITIONS

PIN	NAME	DESCRIPTION
1	TXA+	Differential Transmit Input
2	TXA-	Differential Transmit Input
3	VCC	+5V Power Supply
4	RXA+	Differential Receive Output
5	RXA-	Differential Receive Output
6	GND	Analog Ground Reference
7	VFIN	External Reference Voltage Input
8	RSET	Oscillator Frequency Reference
9	D6	Isolation Signal Output
10	D5	Isolation Signal Output
11	CLID\	Caller ID Control Input, Active Low
12	D4	Isolation Signal Input
13	D3	Isolation Signal Input
14	OFFHK\	Off-Hook Control Input, Active Low
15	D2	Isolation Signal Output
16	D1	Isolation Signal Output

K²934-2 or K²944-2 PIN DEFINITIONS

PIN	NAME	DESCRIPTION
1 - 4	P1 - P4	Isolation Signal Inputs & Outputs

K²942C PIN DEFINITIONS

PIN	NAME	DESCRIPTION
1	D1	Isolation Signal Input
2	D2	Isolation Signal Input
3	LCOM	Line Side Common Ground Reference
4	D3	Isolation Signal Output
5	D4	Isolation Signal Output
6	D7	NC. Test point, do not connect
7	D5	Isolation Signal Input
8	D6	Isolation Signal Input
9	LIM3	Test point, connect to pin LCOM
10	LIM2	NC. Test point, do not connect
11	LIM1	NC. Test point, do not connect
12	IDC	Caller ID Control Output 1
13	COM	Offhook & Caller ID Control Output 2
14	OHC	Offhook Control Output 1
15	IREF	Current Reference Setting
16	VDR	Internal 3.2V Reference
17	TER2	Current Regulator Control Feedback
18	TER1	Current Regulator Control Output
19	SET	DC Termination Voltage Setting
20	LINEV	Line DC Voltage Input
21	LINE	Line AC Signal Output
22	IDG	Caller ID Voltage Reference Input
23	IDI	Caller ID Signal Input
24	LINI	Line AC Signal Input
25	GAIN	Transmit Gain/Trans-Hybrid Loss Set
26	LCOM	Line Side Common Ground Reference
27	AIN	Analog Signal Input
28	AOUT	Analog Signal Output

BILL OF MATERIALS FOR TOTAL DAA

using K²940G/K²940GU chipset

Qty	Description	Package	Reference
1	K²941C	SSOP-16	U1
1	K²942C	SSOP-28	U2
3	K²934-2AR/K²944-2	Array	U3,4,5
1	Opto Coupler	SMD-4	U6
1	Sidactor	SMD	V1
3	18V Zener Diode	SOT-23	D1,2,3
2	Diode, Dual, 300V	SOT-23	D5,6
3	Switch Diode	SOT-23	D4
1	NPN Transistor, 300V	SOT-23	Q2
1	NPN Transistor, 300V	SOT-89	Q3
1	PNP Transistor, 300V	SOT-23	Q1
1	Cap Cer 0.47uF 250V Z5U +/-20%	SMD1812	C9
2	Cap Cer 1000pF 1000VAC, X7R +/-10%	SMD1808	C7,8
1	Cap Cer 2200pF 50V X7R +/-10%	SMD 0805	C5
1	Cap Tan 10uF 10V +/-20%	SMD-A	C1
2	Cap Tan 1uF 16V +/-20%	SMD-A	C12,2
1	Cap Tan 15uF 16V +/-20%	SMD-C	C3
1	Cap Tan 4.7uF 10V +/-20%	SMD-A	C6
1	Res 150K 1% 1/10W or 1/16W	SMD0805 or 0603	R1
1	Res 80.6K 1% 1/10W or 1/16W	SMD0805 or 0603	R5
1	Res 84.5Ω 1% 1/10W or 1/16W	SMD0805 or 0603	R6
3	Res 1K 1% 1/10W or 1/16W	SMD0805 or 0603	R4,14,15
1	Res 1.5K 1% 1/10W or 1/16W	SMD0805 or 0603	R3
1	Res 51.1K 1% 1/10W or 1/16W	SMD0805 or 0603	R16
1	Res 20K 5% 1/10W or 1/16W	SMD0805 or 0603	R2
1	Res 47K 5% 1/10W or 1/16W	SMD0805 or 0603	R9
1	Res 10 Ω 5% 1/4W	SMD1210	R10
1	Res 7.5K 5% 1/4W	SMD1210	R8
1	Res 51Ω 5% 1W	SMD2512	R7

(Above BOM is based on Figure 7)

Additional components for CALLER ID function: (See figure 9)

1	NPN Transistor, 300V	SOT-23	Q4
1	PNP Transistor, 300V	SOT-23	Q5
2	Res 47K 5% 1/10W or 1/16W	SMD0805 or 0603	R12,13
1	Cap Cer 1000pF 50V X7R +/-10%	SMD0805	C10

Additional components for pulse dialing function: (See figure 8)

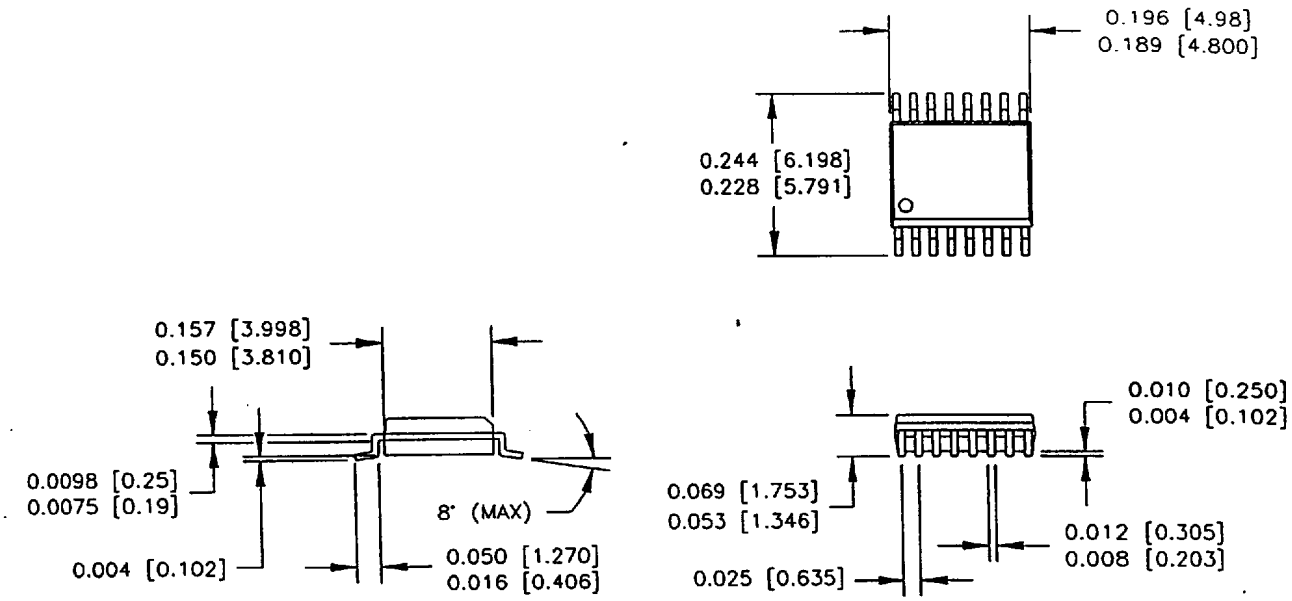
1	NPN Transistor, 300V	SOT-23	Q6

SUGGESTIONS FOR MANUFACTURERS OF EXTERNAL COMPONENTS

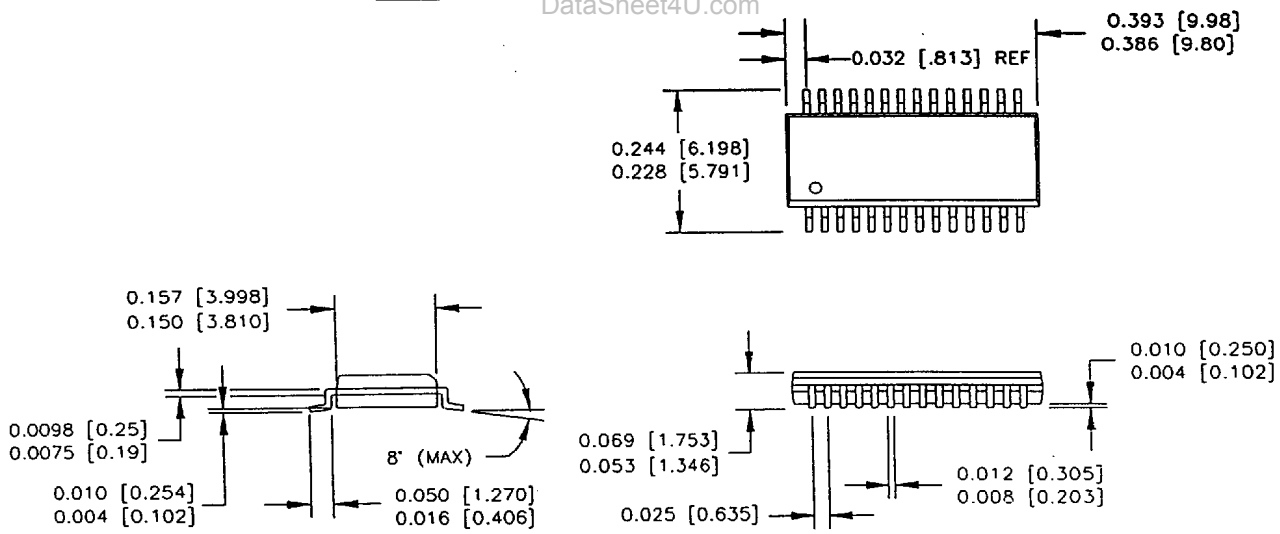
Ref. #	Description	Manufacturer	Part Number	Package	Qty
U6	Opto Coupler	NEC	PS2701-1	SOP-4	1
		Sharp	PC317	SOP-4	
		Any	4N35	DIP-6	
V1	Sidactor	Teccor Electronics	P2600SB	SMD	1
			P2600BA70	TO-92	
Q2,4	NPN Transistor 300V, 300mW	Motorola	MPSA42	TO-92	2
			MMBTA42L	SOT-23	
		Zetex	FMMTA42	SOT-23	
		Siemens	BFN26	SOT-23	
		Central Semiconductor	CMPTA42	SOT-23	
Q1,5	PNP Transistor β>50 300V, 300mW	Zetex	FMMT597	SOT-23	2
		Zetex	ZTX557	TO-92	
Q3,6	NPN Transistor 300V, 1W	Motorola	MPSA92	TO-92	2
		Zetex	SXTA42	SOT-89	
		Simens	SXTA42	SOT-89	
		Central Semiconductor	CXTA42	SOT-89	
D5,6	Diode, 300V	Any	1N4004	Through hole	4
		Rohm	1SS367TE-17	SMD	
			RLS245	SMD	
		Central Semiconductor	CMPD2004S	SOT-23	2
C9	Cap 0.47uF 250V	Novacap	1812Z474M251NXT	SMD-1812	1
C7,8	Cap 1000pF 1000VAC	Novacap	AC1808B102K102NT	SMD-1808	2
		MuRata	GHM2243B102MAC250	SMD-1808	

Package Dimensions:

K²941C PACKAGE DIMENSIONS

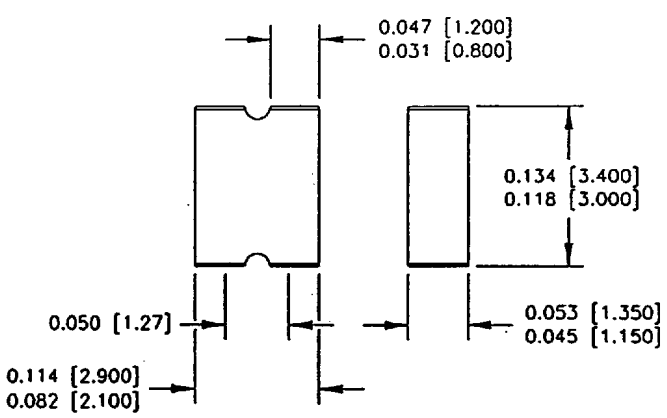


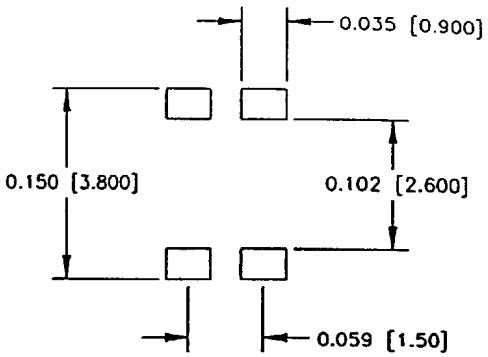
K²942C PACKAGE DIMENSIONS



Dimensions are in inches and (millimeters).

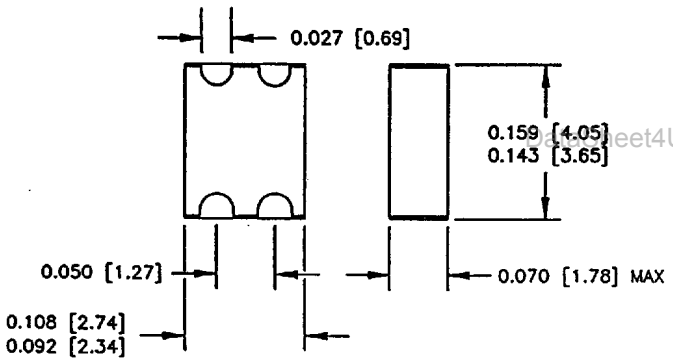
K²934-2 PACKAGE DIMENSIONS

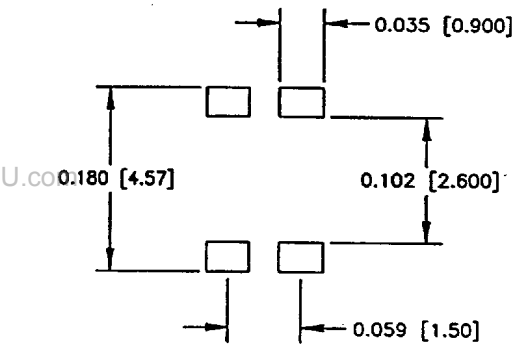




RECOMMENDED LAND PATTERN:

K²944-2 PACKAGE DIMENSIONS





RECOMMENDED LAND PATTERN:

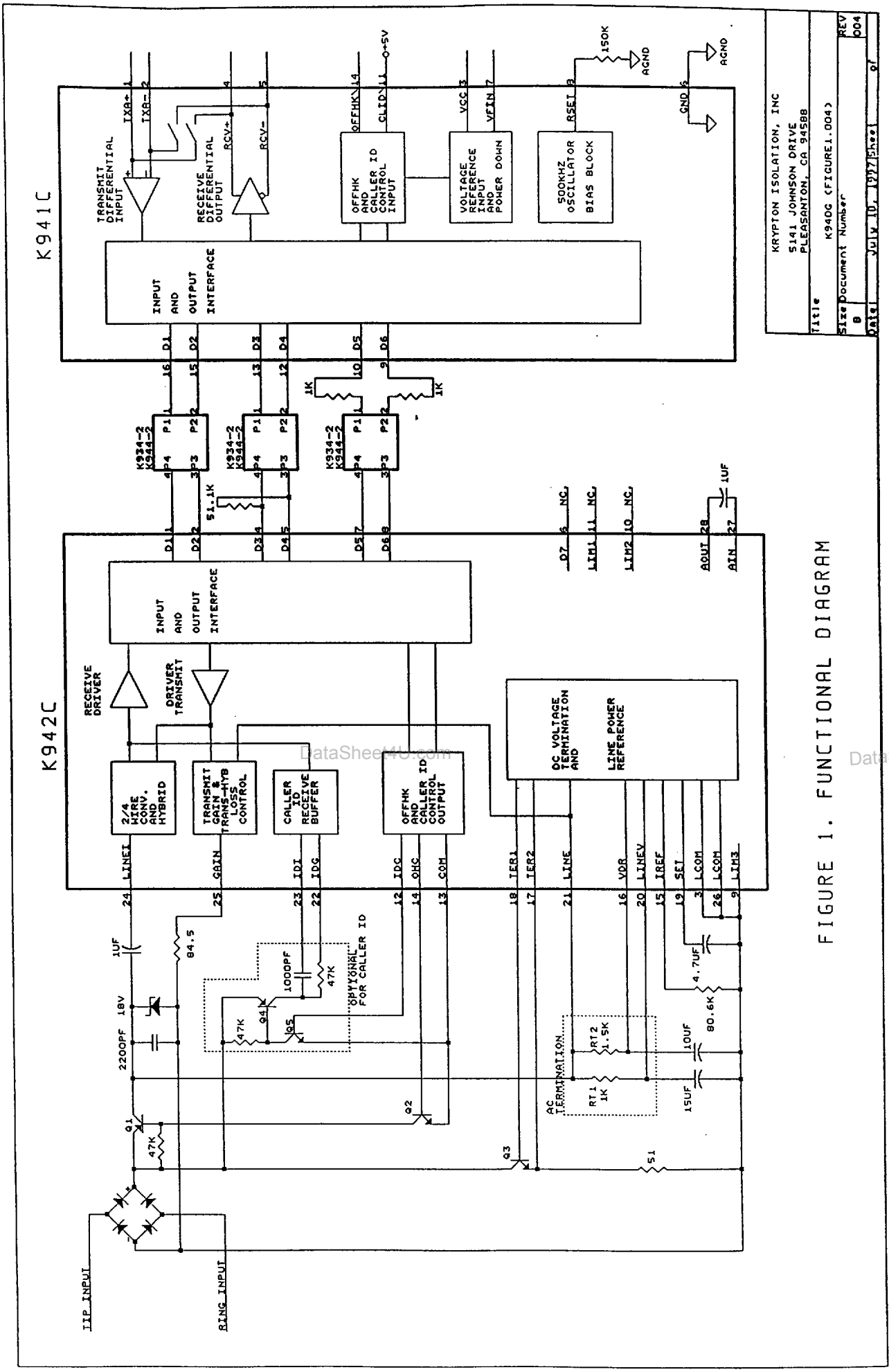


FIGURE 1. FUNCTIONAL DIAGRAM

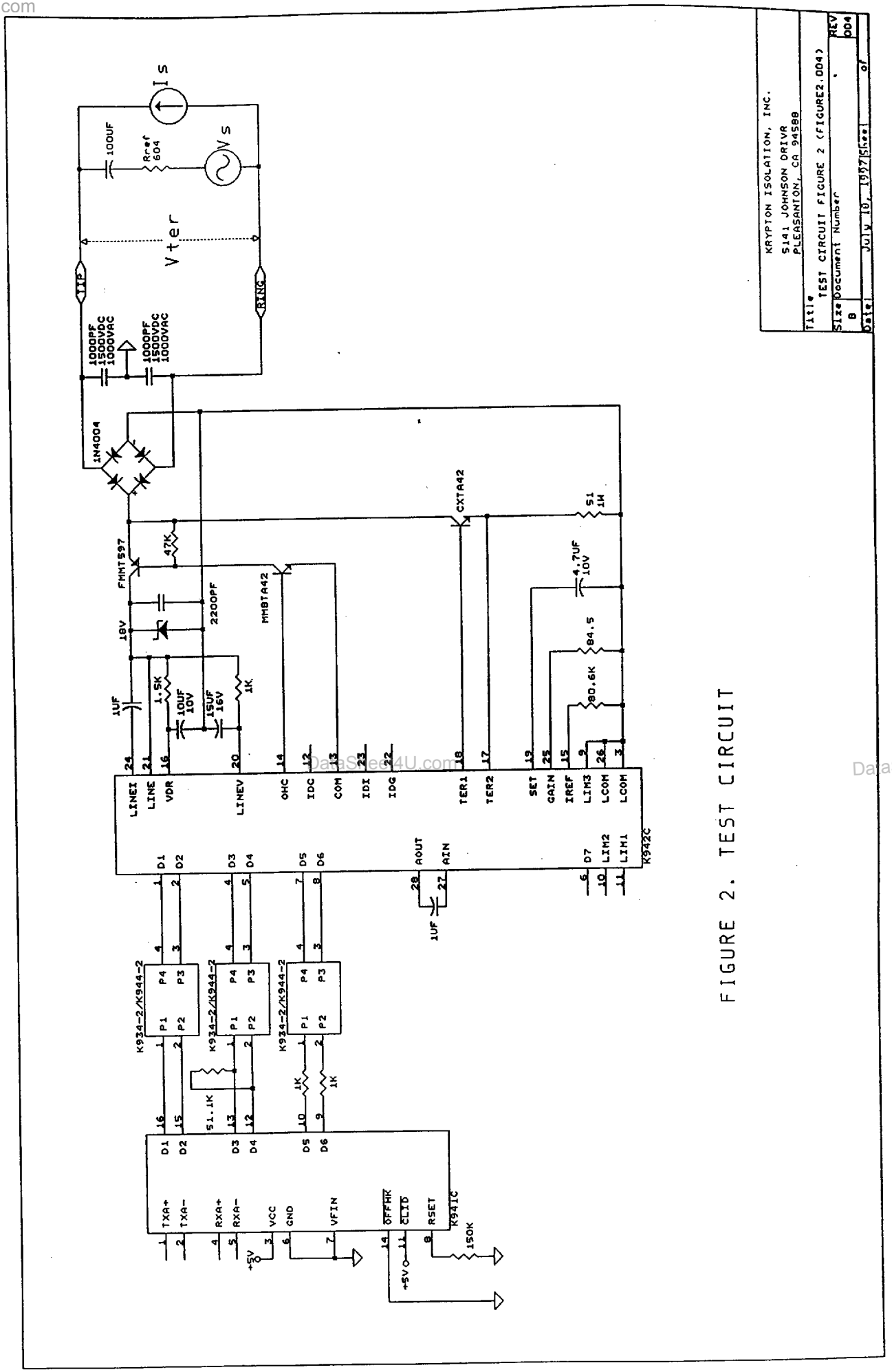


FIGURE 2. TEST CIRCUIT

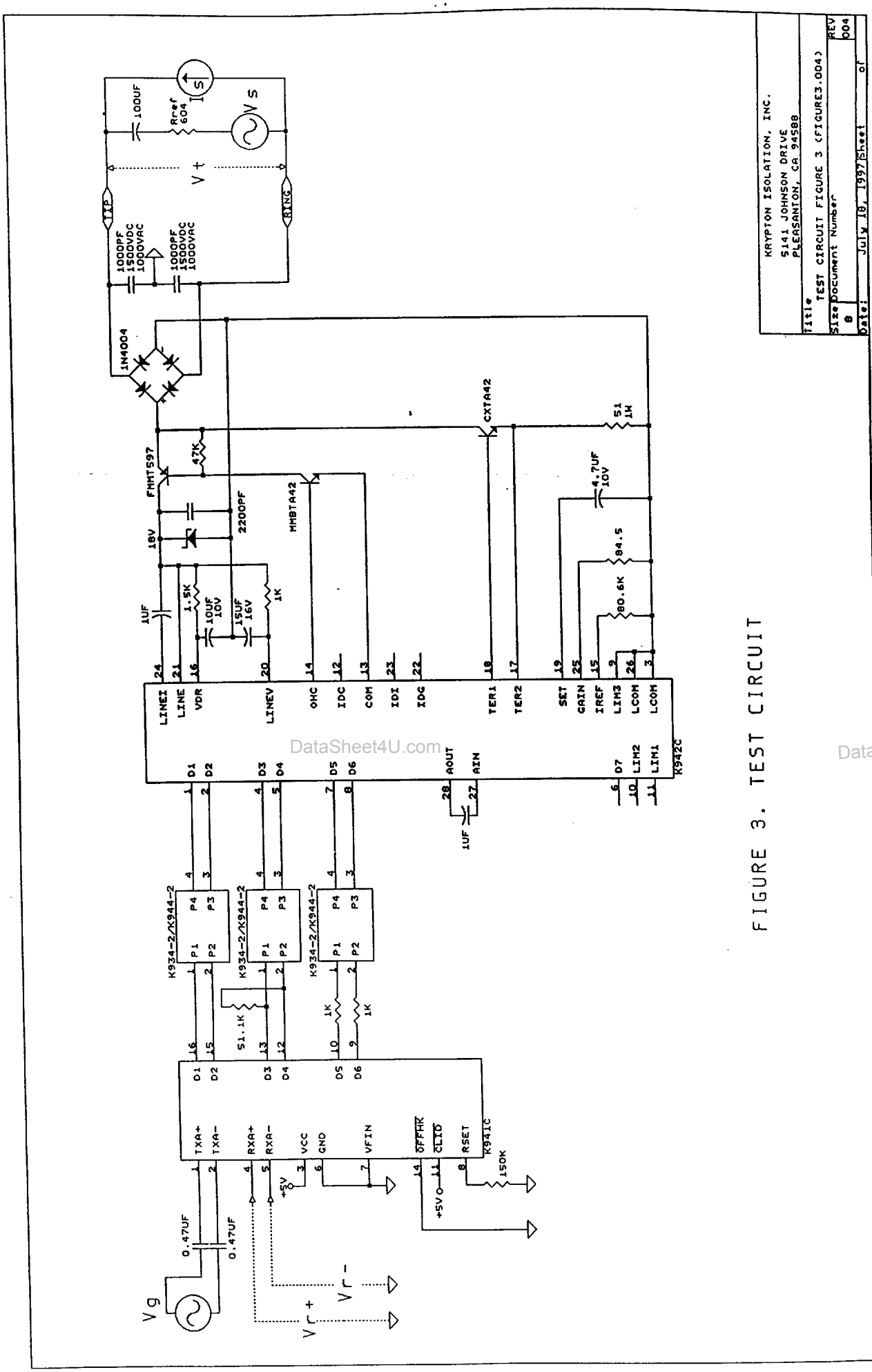


FIGURE 3. TEST CIRCUIT

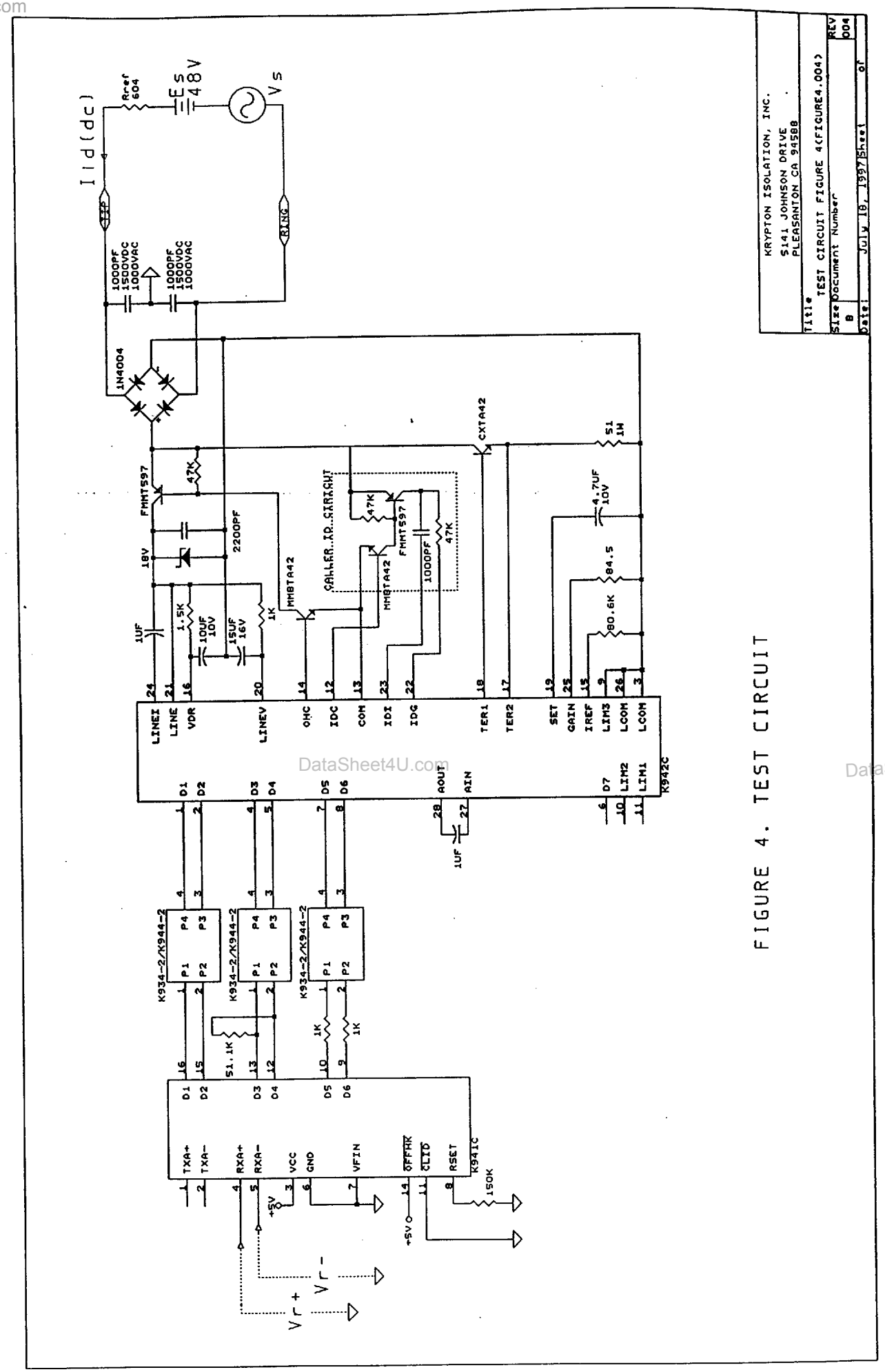
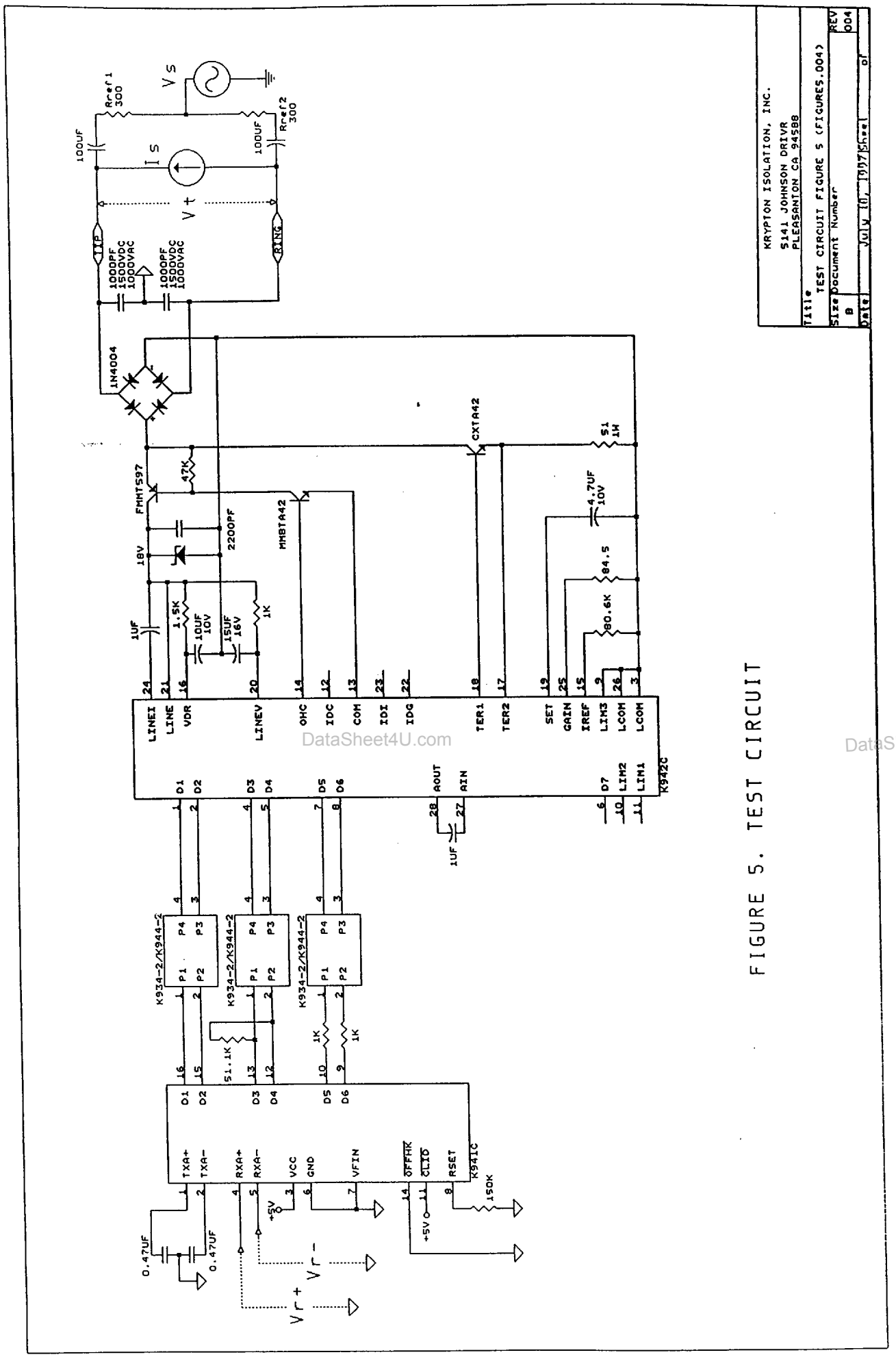


FIGURE 4. TEST CIRCUIT



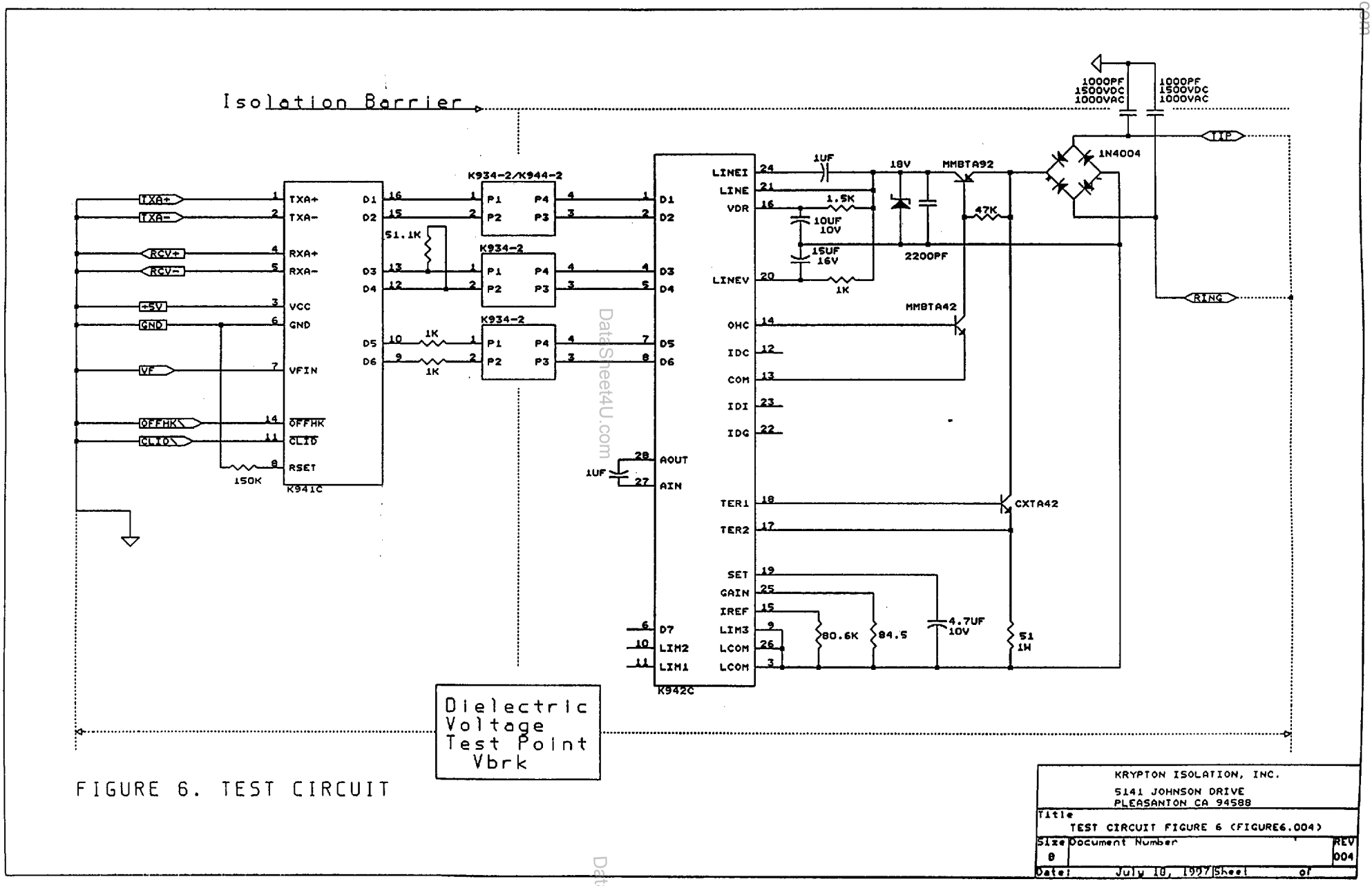


FIGURE 6. TEST CIRCUIT

KRYPTON ISOLATION, INC. 5141 JOHNSON DRIVE PLEASANTON CA 94588		
Title: TEST CIRCUIT FIGURE 6 (FIGURE6.004)		
Size: B	Document Number:	REV: 004
Date: July 10, 1997	Sheet: of	

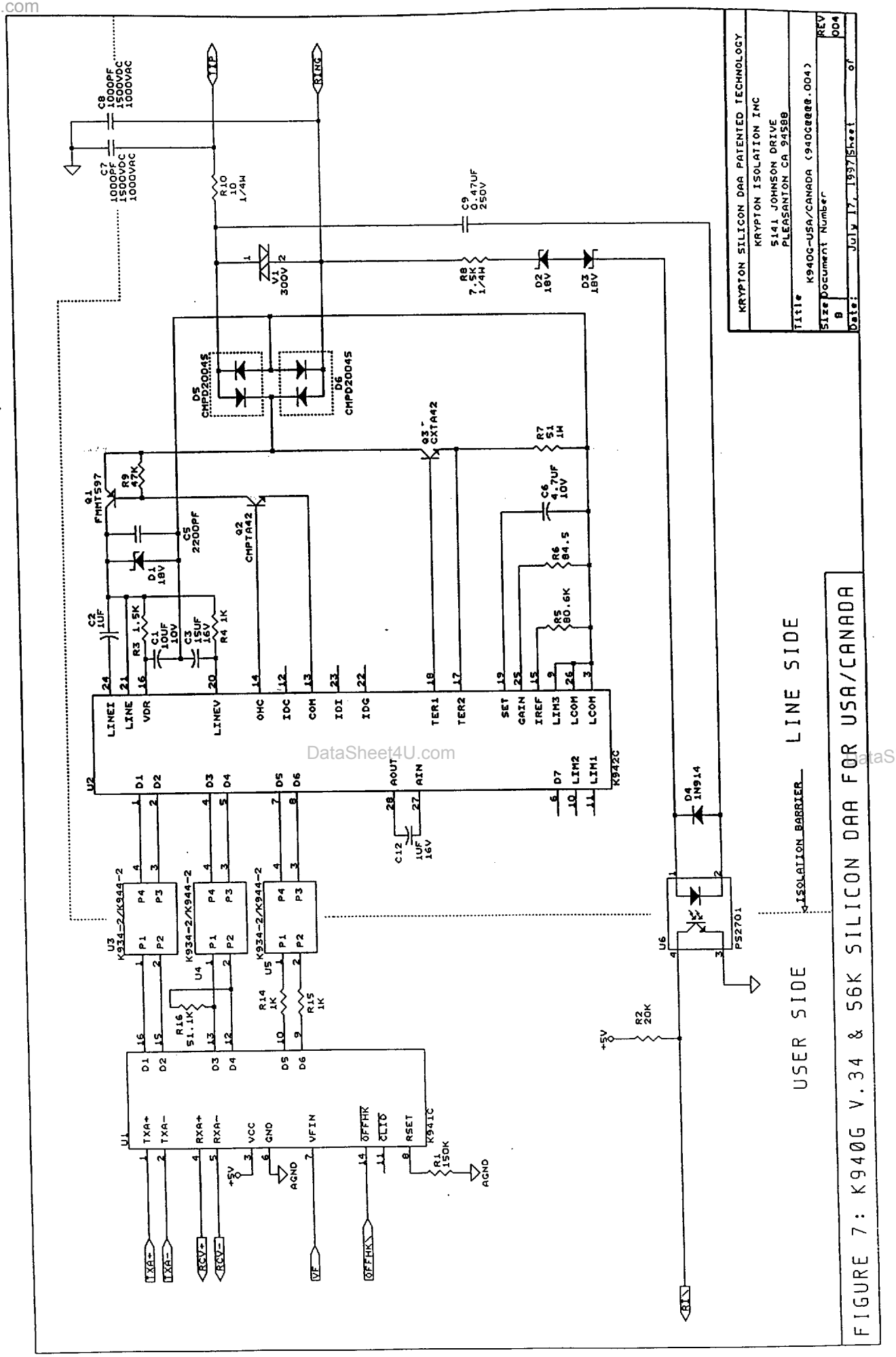


FIGURE 7: K940G V.34 & S6K SILICON DAA FOR USA/CANADA

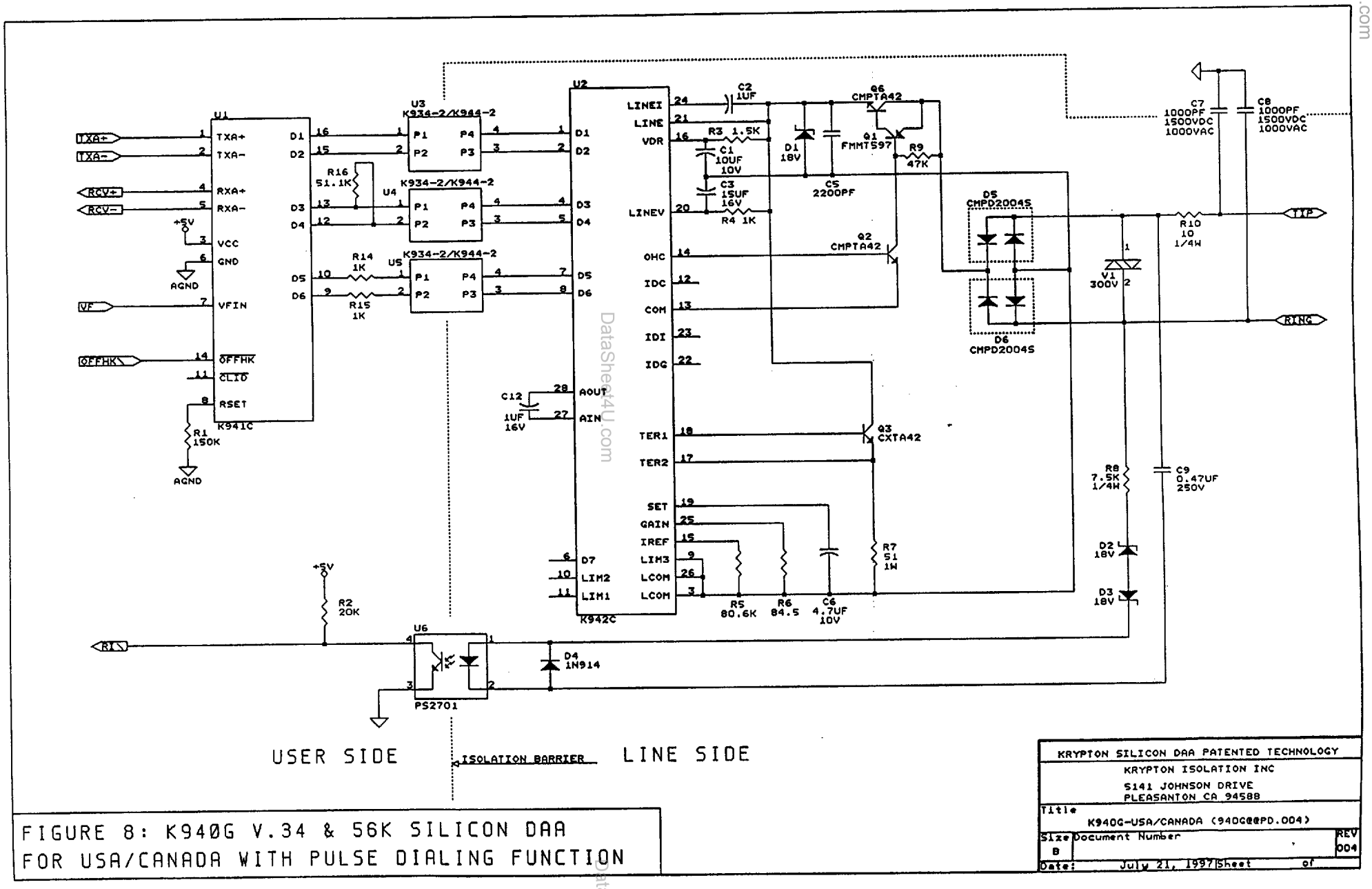


FIGURE 8: K940G V.34 & 56K SILICON DAA
FOR USA/CANADA WITH PULSE DIALING FUNCTION

KRYPTON SILICON DAA PATENTED TECHNOLOGY
KRYPTON ISOLATION INC
5141 JOHNSON DRIVE
PLEASANTON CA 94588

Title: K940G-USA/CANADA (940G@@PD.004)
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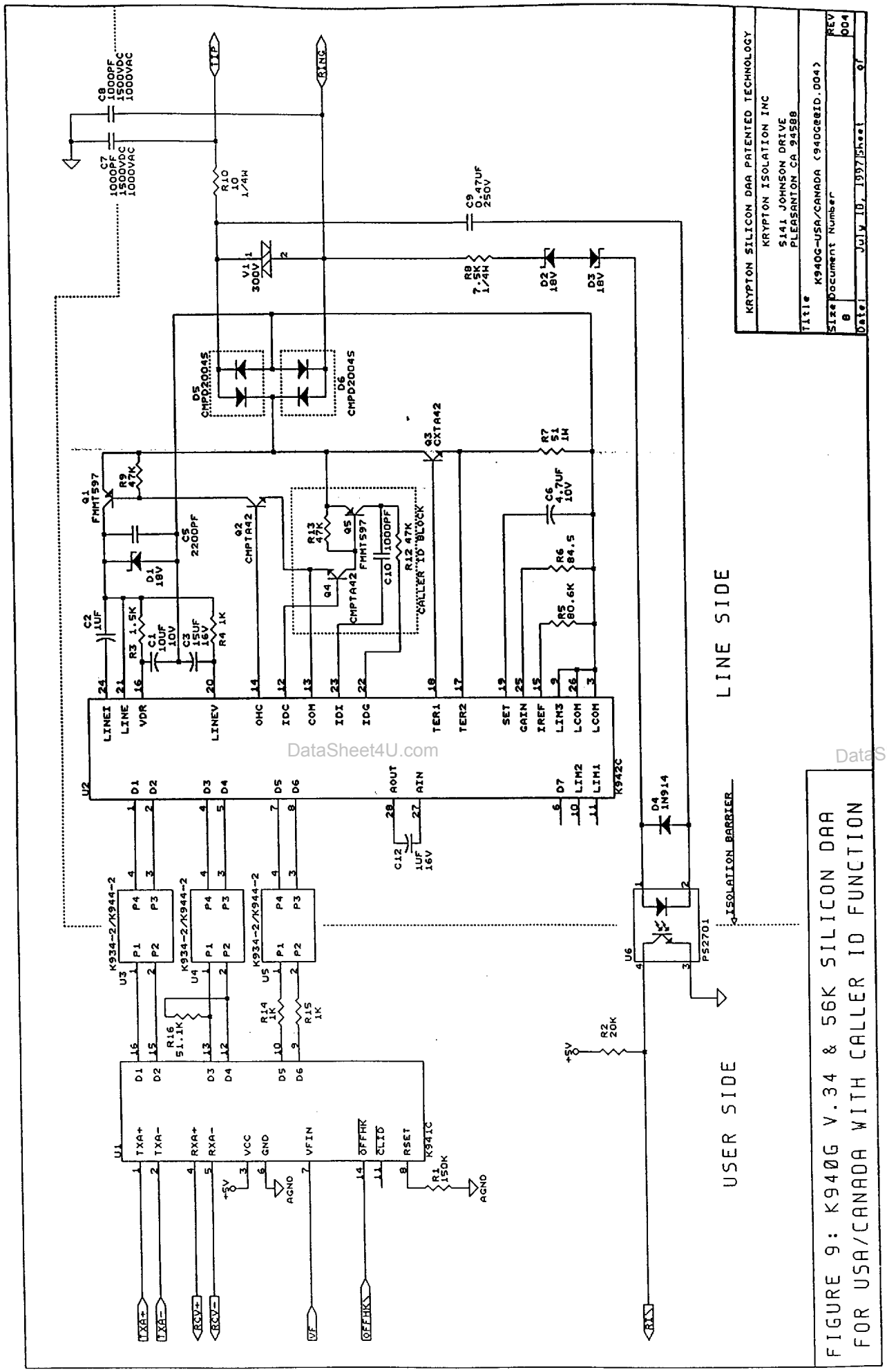

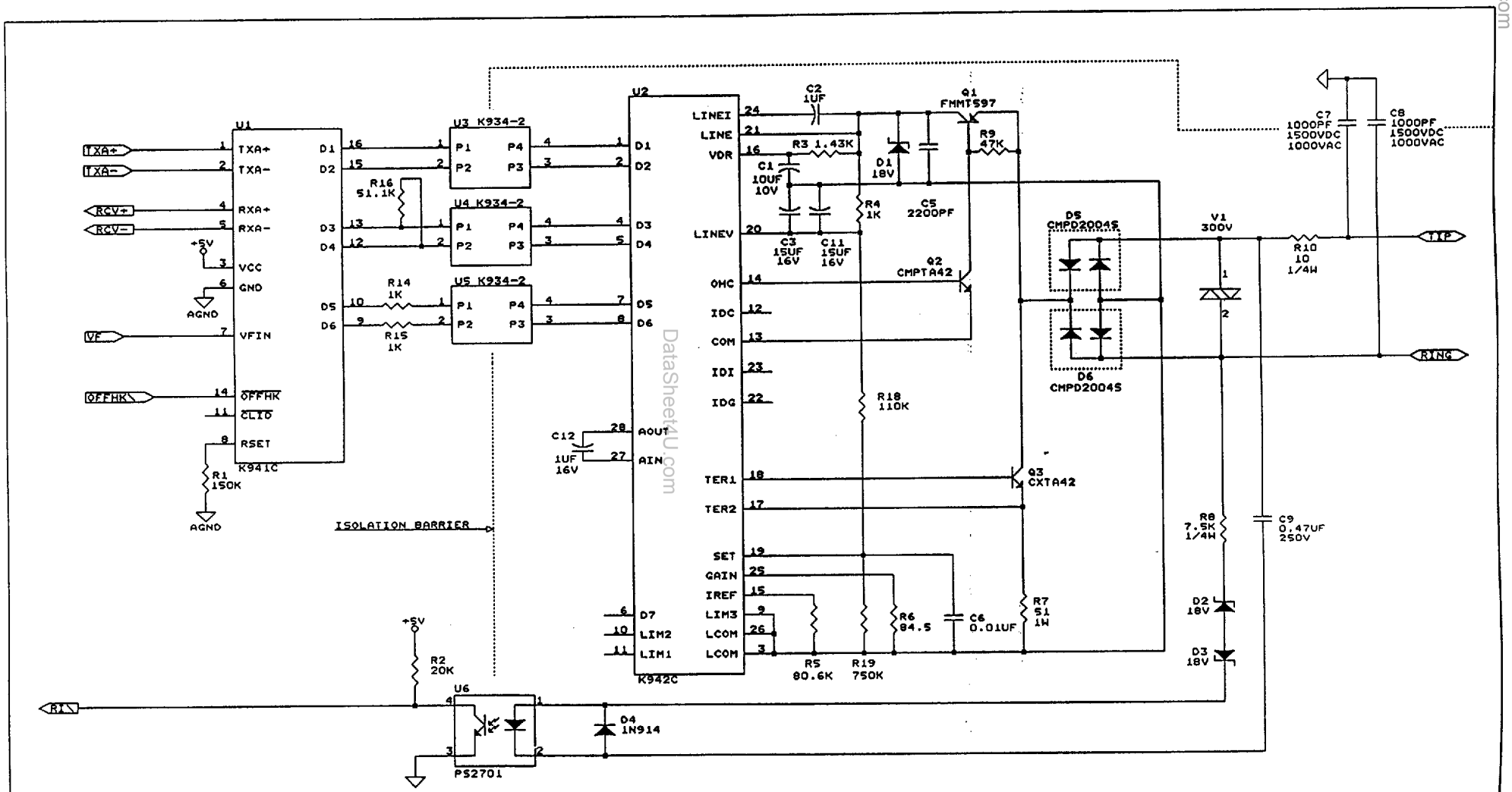

1: FOR SPECIFIC MODEM CHIPSET INTERFACE, SEE FIG. 11 THROUGH 19

2: ADJUST RTX VALUE FOR -15dbm MAX TRANSMIT LEVEL AT TIP/RING

3: SET AT COMMAND S6=10 FOR LONGER DIALTONE WAITING

FIGURE 10: K940G V.34 & 56K SILICON DAA FOR JAPAN

KRYPTON SILICON DAA PATENTED TECHNOLOGY

KRYPTON ISOLATION INC

5141 JOHNSON DRIVE

PLEASANTON CA 94588

Title: K940G-JAPAN (940GJ###.004)

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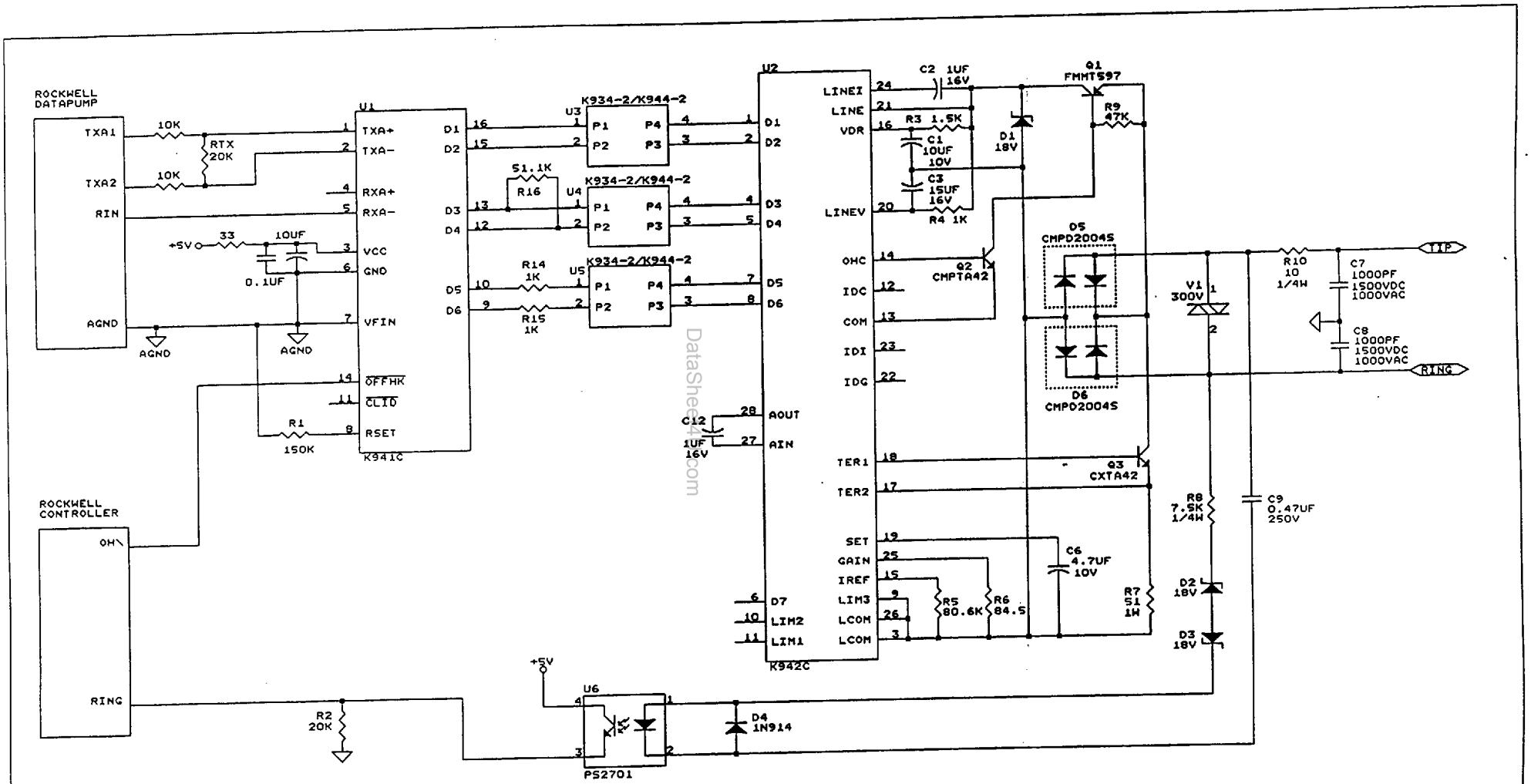


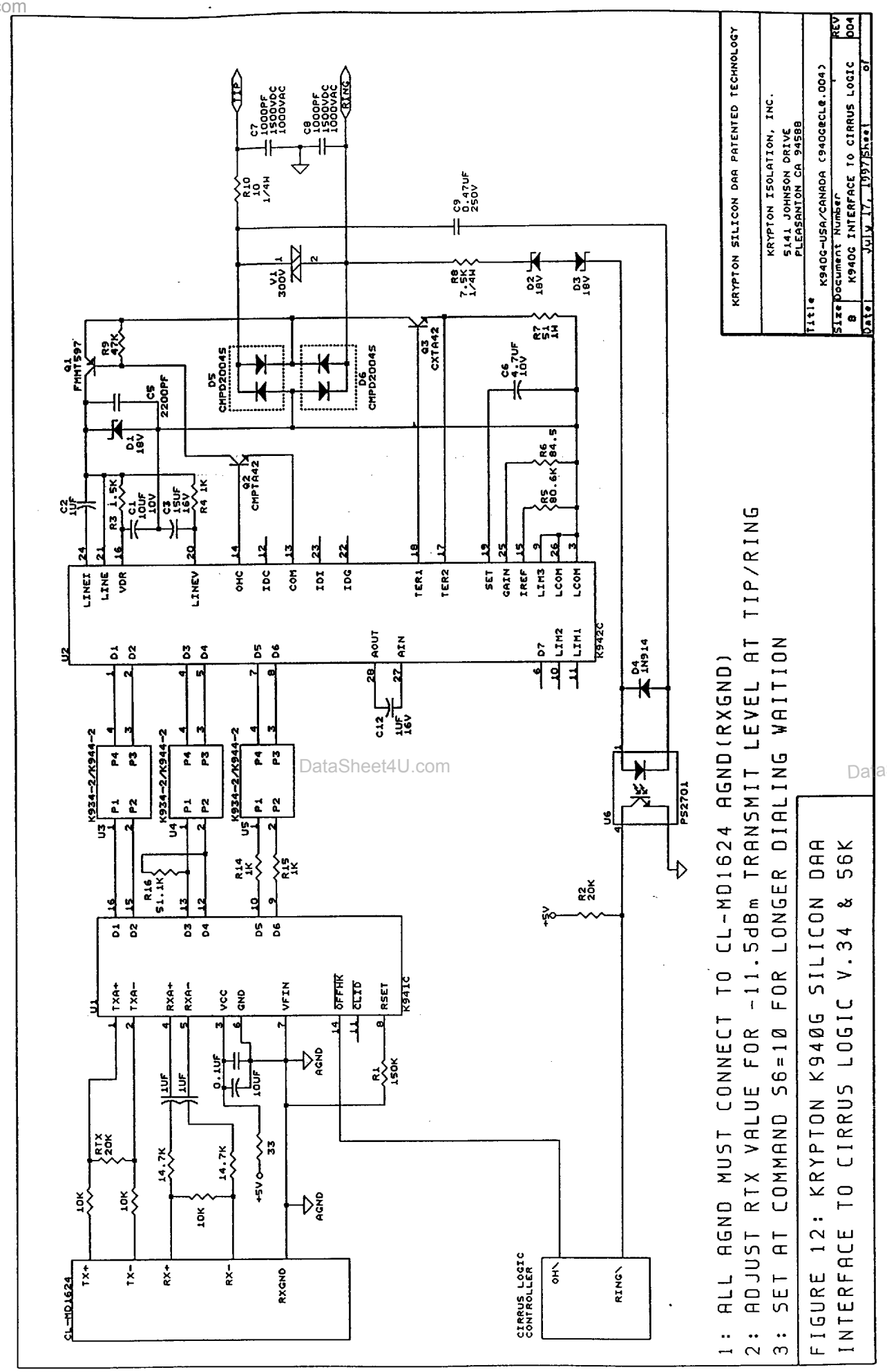
1: ALL AGND MUST CONNECT TO ROCKWELL DATAPUMP AGND
2: ADJUST RTX VALUE FOR -11.5dBm TRANSMIT LEVEL AT TIP/RING
3: SET AT COMMAND S6=10 FOR LONGER DIALTONE WAITING

FIGURE 11: KRYPTON K940G SILICON DAA INTERFACE TO ROCKWELL V.34 & 56K

KRYPTON SILICON DAA PATENTED TECHNOLOGY

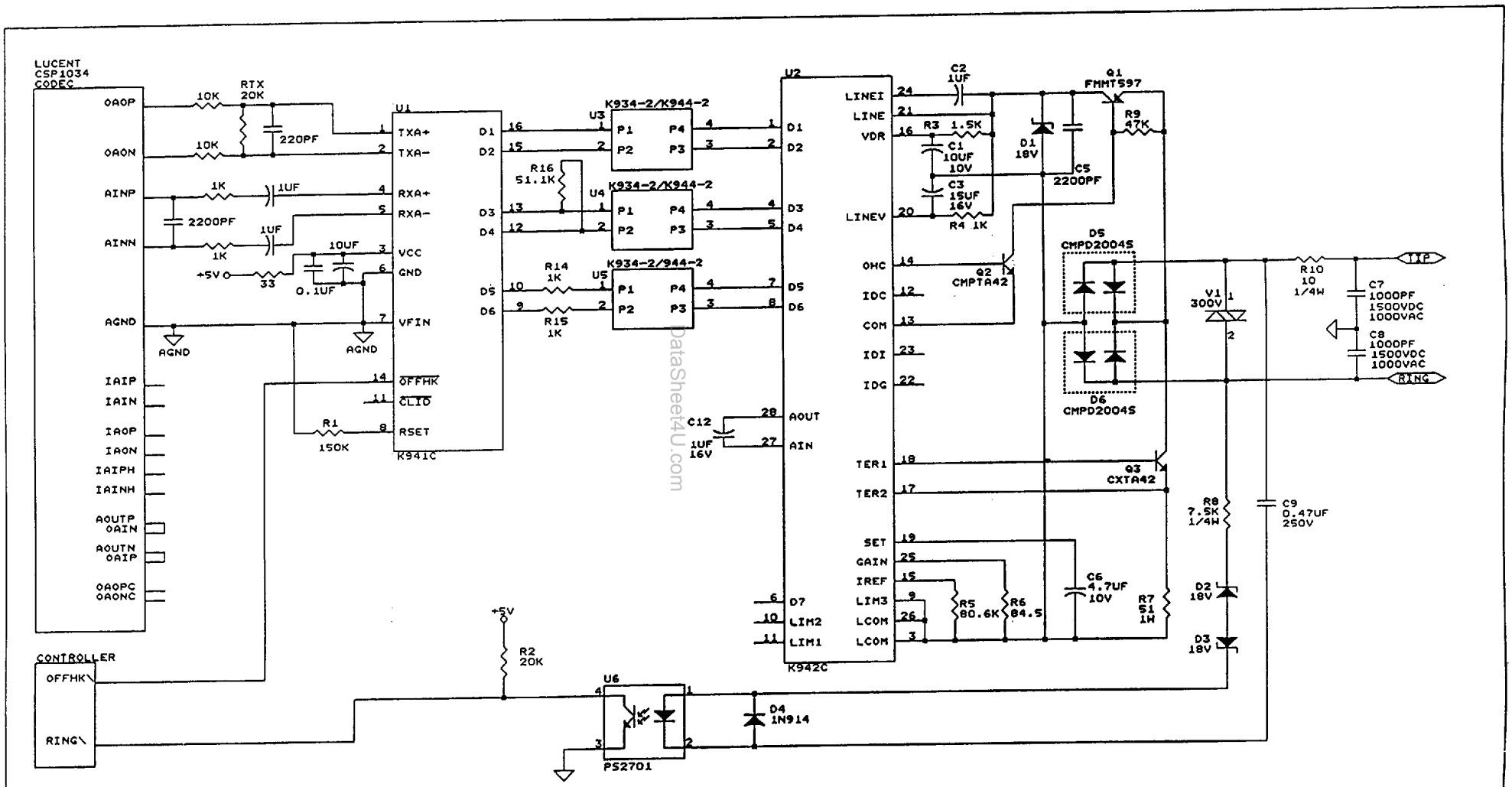
KRYPTON ISOLATION, INC.
5141 JOHNSON DRIVE
PLEASANTON CA 94588

Title: K940G-USA/CANADA (940GRW@.004)
Size: B | Document Number: K940G INTERFACE TO ROCKWELL | REV: 004
Date: July 17, 1997 | Sheet of



1: ALL AGND MUST CONNECT TO CL-MD1624 AGND(RXGND)
2: ADJUST RTX VALUE FOR -11.5dBm TRANSMIT LEVEL AT TIP/RING
3: SET AT COMMAND S6=10 FOR LONGER DIALING WAITION

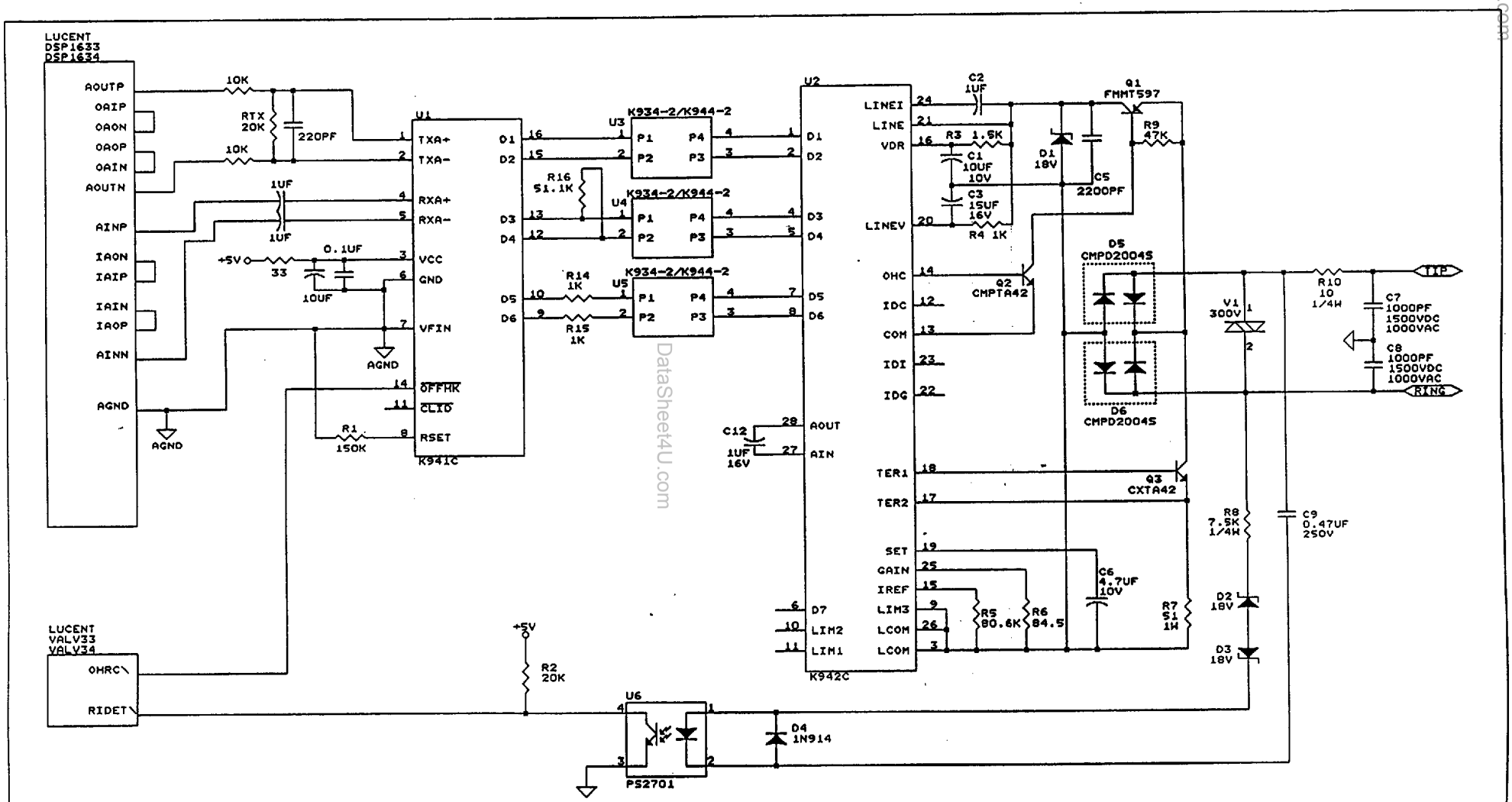
FIGURE 12: KRYPTON K940G SILICON DAA
INTERFACE TO CIRRUS LOGIC V.34 & 56K



1. ALL AGND MUST CONNECT TO CODEC AGND
2. ADJUST RTX VALUE FOR -11.5dBm TRANSMIT LEVEL AT TIP/RING
3. SET AT COMMAND S6=10 FOR LONGER DIALTONE WAITING

FIGURE 13: KRYPTON K940G SILICON DAA INTERFACE TO LUCENT CSP1034 V.34 & 56K

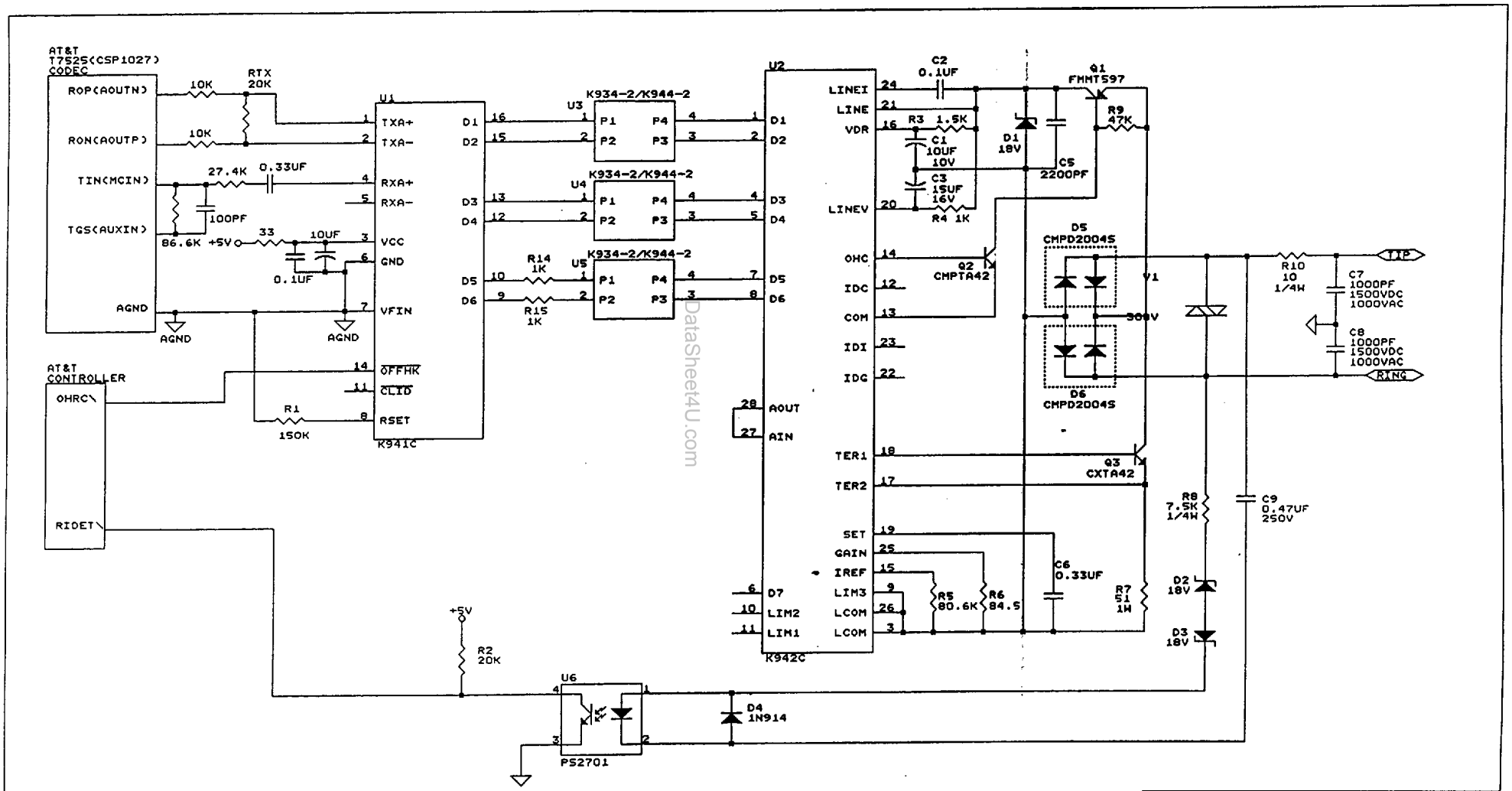
KRYPTON SILICON DAA PATENTED TECHNOLOGY	
KRYPTON ISOLATION, INC. 5141 JOHNSON DRIVE PLEASANTON CA 94588	
Title: K940G-USA/CANADA (940G@AT3.004)	
Size: B	Document Number: K940G INTERFACE TO LUCENT CSP1034
Date: July 17, 1997	Sheet of
	REV: 004



1. ALL AGND MUST CONNECT TO DSP1633/34 AGND
2. ADJUST RTX VALUE FOR -11.5dBm TRANSMIT LEVEL AT TIP/RING
3. SET AT COMMAND S6=10 FOR LONGER DIALTONE WAITING

FIGURE 14: K940G SILICON DAA
INTERFACE TO LUCENT DSP1633/34 V.34 & 56K

KRYPTON SILICON DAA PATENTED TECHNOLOGY	
KRYPTON ISOLATION, INC. 5141 JOHNSON DRIVE PLEASANTON CA 94588	
Title	K940G-USA/CANADA (940G@AT2.004)
Size: B	Document Number: K940G INTERFACE TO LUCENT DSP1633/34
REV	004
Date: July 17, 1997	Sheet of



1. ALL AGND MUST CONNECT TO CODEC AGND
2. ADJUST RTX VALUE FOR -10.5dBm TRANSMIT LEVEL AT TIP/RING
3. SET AT COMMAND S6=10 FOR LONGER DIALTONE WAITING

FIGURE 15: KRYPTON K940G SILICON DAA INTERFACE TO LUCENT T7525 V.32bis

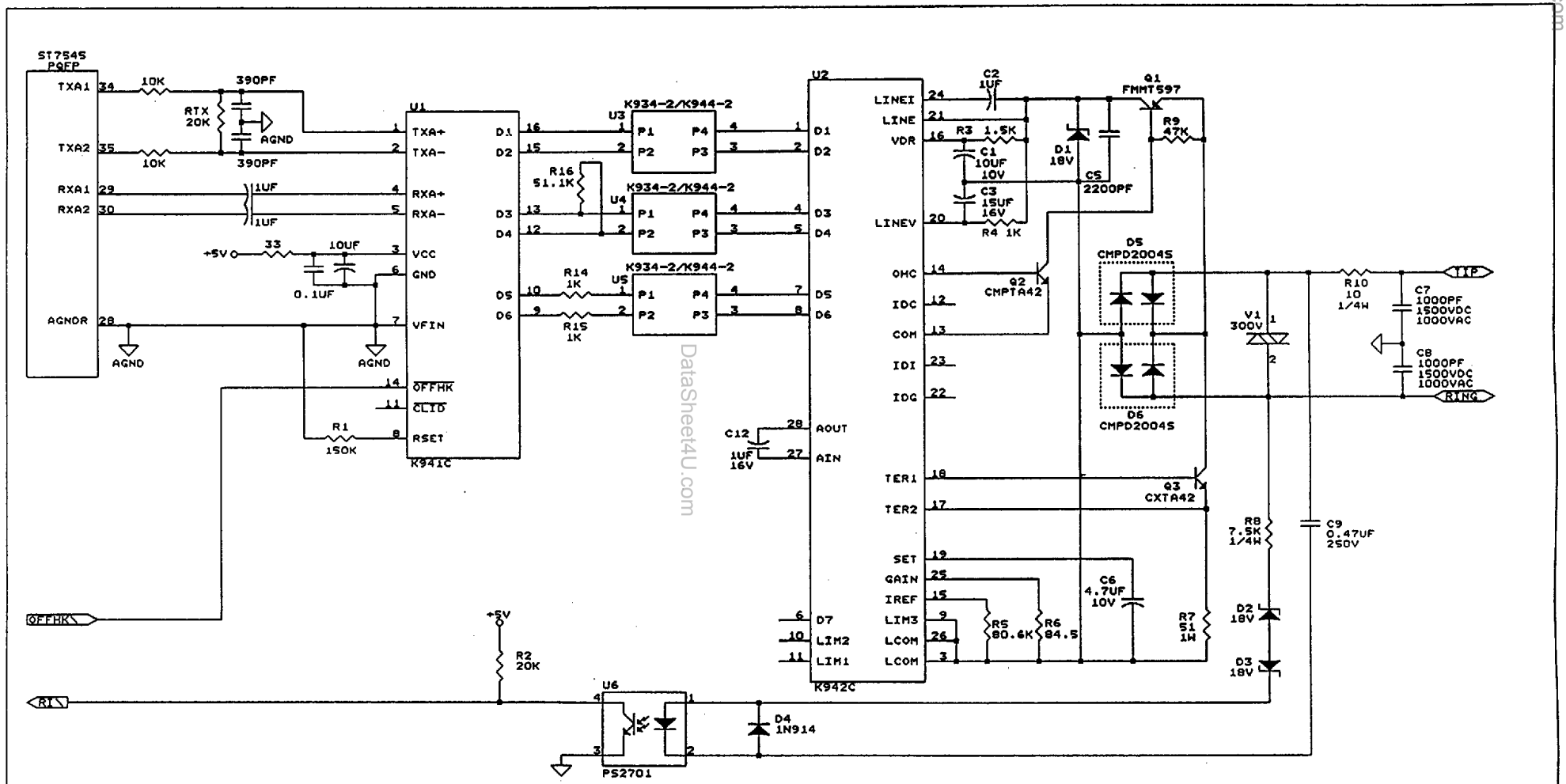
KRYPTON SILICON DAA PATENTED TECHNOLOGY

KRYPTON ISOLATION, INC.
5141 JOHNSON DRIVE
PLEASANTON CA 94588

Title: K940G-USA/CANADA (940G@AT1.004)

Size: B | Document Number: K940G INTERFACE TO LUCENT T7525 V.32 | REV: 004

Date: July 22, 1997 | Sheet: of



1: ALL AGND MUST CONNECT TO ST75XX AGND(AGNDR)

2: ADJUST RTX VALUE FOR -11.5dBm TRANSMIT LEVEL AT TIP/RING

3: SET AT COMMAND S6=10 FOR LONGER DIALTONE WAITING

FIGURE 16: K940G SILICON DAA INTERFACE
TO SGS-THOMSON ST75XX AFE FOR V.34 & 56K

KRYPTON SILICON DAA PATENTED TECHNOLOGY

KRYPTON ISOLATION, INC.
5141 JOHNSON DRIVE
PLEASANTON CA 94588

Title: K940G-SGS-7545 CODEC (940G@SG1.004)

Size: B | Document Number: | REV: 004

Date: July 17, 1997 | Sheet of

The update list from K²940G/K²40GU Rev.003 to K²940G/K²940GU Rev.004:

(7-21-1997)

1. Add figure 8 for pulse dialing application to rev.004.
2. Add figure 19 for Rockwell V.22bis/2400bps application to rev.004.
3. Add note 3 from figure 10 to figure 18 on rev.004.
4. Delete C4/0.1uF & C11/10uF from figure 1 to figure 17 from rev.003.
5. Delete R17/56.2K from figure 1 to figure 16 from rev.003.
6. Change value R16 from 56.2K of rev.003 to 51.1K of rev.004.
7. Change value C6 from 10uF of rev.003 to 4.7uF of rev.004.
8. Change value C2 from 0.33uF of rev.003 to 1uF of rev.004.
9. Change Q1(on all figures) part number from CMPTA92 of rev.003 to FMMT597 of rev.004.
10. Update value from rev.003 figure 9 (Japan application) to rev.004 figure 10.
11. Update value from rev.003 figure 17 (ESS 2818/2819 codec) to rev.004 figure 17.
12. Update interface from rev.003 figure 12 (Lucent CSP1034 codec) to rev.004 figure 13
13. Update value from rev.003 figure 14 (Lucent T7525 codec) to rev.004 figure 15
14. Update 'Bill of materials for total DAA' from rev.003 to rev.004 on page 11.
15. Update 'Suggestions for manufacturers of external components' from rev.003 to rev.004 on page 12 for Q1 changing to FMT597 from CMPTA92.
16. Update Figure numbers for application schematics:
    a. from Figure 8 to Figure 9;
    b. from Figure 9 to Figure 10;
    c. from Figure 10 to Figure 11;
    d. from Figure 11 to Figure 12;
    e. from Figure 12 to Figure 13;
    f. from Figure 13 to Figure 14;
    g. from Figure 14 to Figure 15;
    h. from Figure 15 to Figure 16;
    i. from Figure 16 to Figure 18