FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27235-2E

*ASSP For Power Supply Applications*
*(General Purpose DC/DC Converter)*

# 2-Channel DC/DC Converter IC

## with Overcurrent Protection Symmetrical-Phase Type

# MB39A106

## ■ DESCRIPTION

The MB39A106 is a symmetrical-phase type of two-channel, DC/DC converter IC using pulse width modulation (PWM) , incorporating an overcurrent protection circuit (requiring no current sense resistor) and an overvoltage protection circuit. Providing high output driving capabilities, the MB39A106 is suitable for down-conversion.

The MB39A106 adopts both synchronous rectification to provide high efficiency and symmetrical phasing (two anti-phase triangular waves) which contributes to making the input capacitor small.

The MB39A106 contains a Bootstrap diode resulting in a reduced number of components used. It also contains a variety of protection features which output the protection status upon detection of an overvoltage or overcurrent while reducing the number of external protective devices required.

The result is an ideal built-in power supply for driving products with high speed CPU's such as home TV game devices and notebook PC's.

## ■ FEATURES

- Built-in bootstrap diode
- Built-in timer-latch overcurrent protection circuit (requiring no current sense resistor)
- Built-in timer-latch overvoltage protection circuit
- Synchronous rectification system providing high efficiency
- Power supply voltage range: 6.5 V to 18 V
- PWRGOOD terminals (open-drain) to output the protection status
- Symmetrical-phase system reducing the input capacitor loss
- Built-in channel control function
- One type of package (TSSOP-30pin : 1 type)
- Reference voltage: 3.5 V ± 1 %
- Error amplifier threshold voltage: 1.23 V ± 1 % (Ta = 0 °C to + 85 °C)
- Support for frequency setting using an external resistor (Frequency setting capacitor integrated)
- Oscillation frequency range: 100 kHz to 500 kHz
- Standby current : 0 µA (Typ)
- Built-in circuit for load-independent soft-start and discharge control
- Built-in totem-pole output for N-ch MOS FET
- One type of package (TSSOP-30 pin : 1 type)

## ■ APPLICATION

- Home Video Game
- IP phone
- Printer etc.



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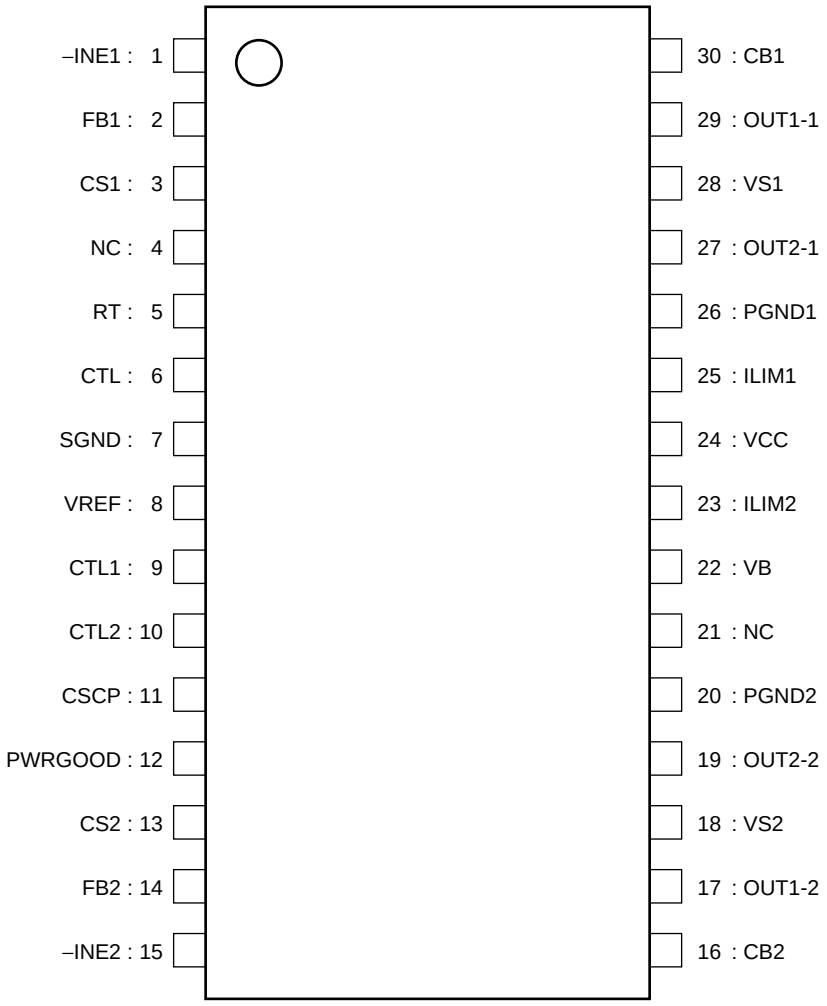
## ■ PIN ASSIGNMENT

(TOP VIEW)

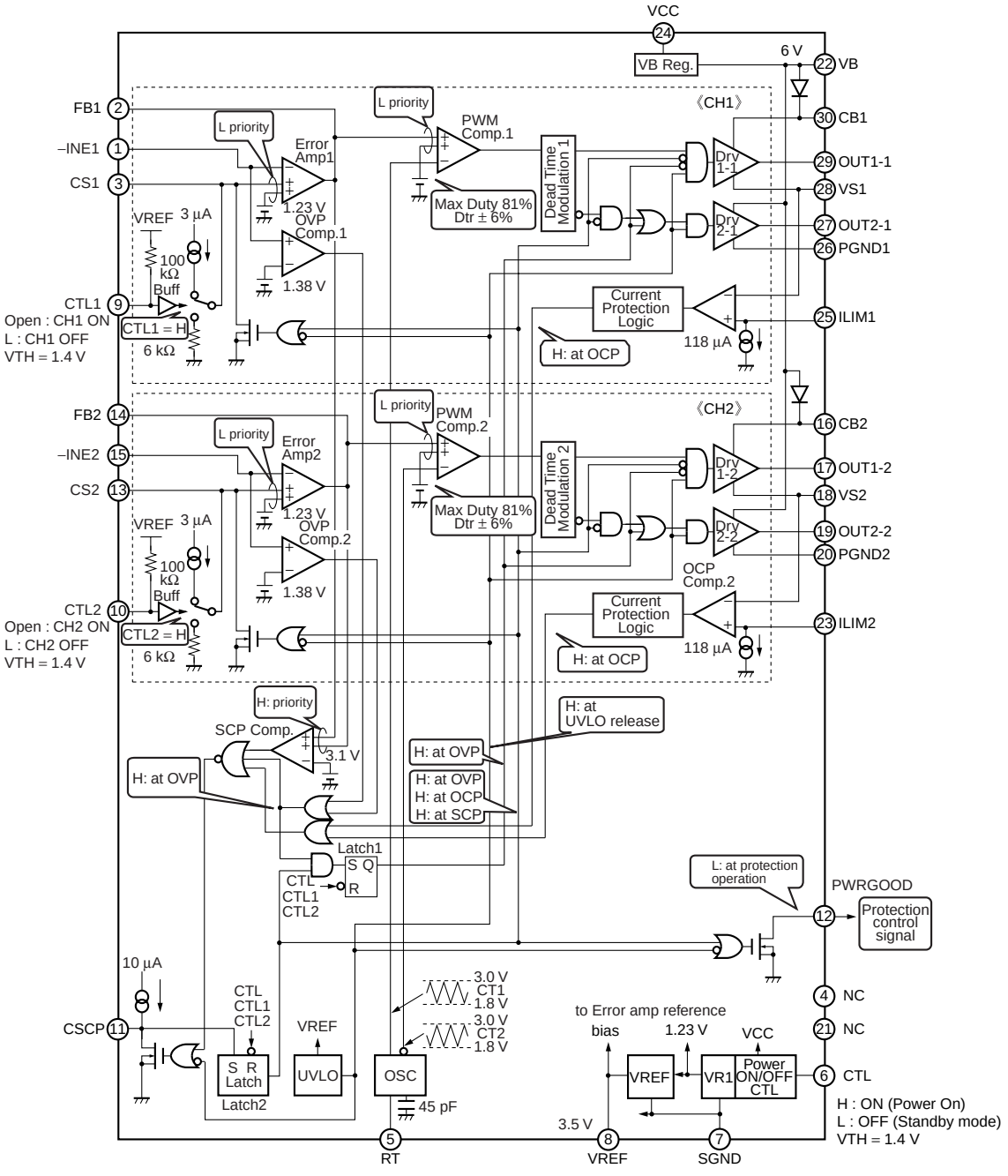



(FPT-30P-M04)

## ■ PIN DESCRIPTION

| Pin No. | Symbol | I/O | Descriptions |
|---|---|---|---|
| 1 | –INE1 | I | CH1 error amp inverted input terminal |
| 2 | FB1 | O | CH1 error amp output terminal |
| 3 | CS1 | — | CH1 soft-start capacitor connection terminal |
| 4 | NC | — | No connection |
| 5 | RT | — | Triangular waveform oscillation frequency setting resistor connection terminal |
| 6 | CTL | I | Power supply control terminal<br>“H” level : IC operating mode<br>“L” level : IC Standby mode |
| 7 | SGND | — | Ground terminal |
| 8 | VREF | O | Reference voltage output terminal |
| 9 | CTL1 | I | CH1 control terminal<br>“H” level : CH1 ON state<br>“L” level : CH1 OFF state and protection status reset |
| 10 | CTL2 | I | CH2 control terminal<br>“H” level : CH2 ON state<br>“L” level : CH2 OFF state and protection status reset |
| 11 | CSCP | — | Timer-latch short-circuit protection capacitor connection terminal |
| 12 | PWRGOOD | O | CH1, CH2 protection status output terminal |
| 13 | CS2 | — | CH2 soft-start capacitor connection terminal |
| 14 | FB2 | O | CH2 error amp output terminal |
| 15 | –INE2 | I | CH2 error amp inverted input terminal |
| 16 | CB2 | — | CH2 boot capacitor connection terminal<br>Connect a capacitor between the CB2 and VS2 terminals. |
| 17 | OUT1-2 | O | CH2 totem-pole output terminal (External main-side FET gate drive) |
| 18 | VS2 | — | CH2 external main-side FET source connection terminal |
| 19 | OUT2-2 | O | CH2 totem-pole output terminal (External synchronous-rectification-side FET gate drive) |
| 20 | PGND2 | — | Ground terminal |
| 21 | NC | — | No connection |
| 22 | VB | O | Output circuit bias output terminal |
| 23 | ILIM2 | I | CH2 overcurrent detection resistor connection terminal |
| 24 | VCC | — | Reference voltage, control circuit power supply terminal |
| 25 | ILIM1 | I | CH1 overcurrent detection resistor connection terminal |
| 26 | PGND1 | — | Ground terminal |
| 27 | OUT2-1 | O | CH1 totem-pole output terminal (External synchronous-rectification-side FET gate drive) |
| 28 | VS1 | — | CH1 external main-side FET source connection terminal |
| 29 | OUT1-1 | O | CH1 totem-pole output terminal (External main-side FET gate drive) |
| 30 | CB1 | — | CH1 boot capacitor connection terminal<br>Connect a capacitor between the CB1 and VS1 terminals. |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Power-supply voltage | $V_{CC}$ | — | — | 20 | V |
| Boot voltage | $V_{CB}$ | CB terminal | — | 25 | V |
| Output current | $I_O$ | — | — | 120 | mA |
| Peak output current | $I_{OP}$ | Duty ≤ 5% ($t = 1 / f_{OSC} \times$ Duty) | — | 800 | mA |
| Power dissipation | $P_D$ | Ta ≤ +25 °C | — | 1390* | mW |
| Storage temperature | $T_{STG}$ | — | −55 | +125 | °C |

* : The packages are mounted on the dual-sided epoxy board (10 cm × 10 cm) .

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Power-supply voltage | $V_{CC}$ | — | 6.5 | 12 | 18 | V |
| Boot voltage | $V_{CB}$ | CB terminal | — | — | 24 | V |
| Reference voltage output current | $I_{OR}$ | VREF terminal | − 1 | — | 0 | mA |
| Bias output current | $I_{OB}$ | VB terminal | − 1 | — | 0 | mA |
| Input voltage | $V_{IN}$ | –INE terminal | 0 | — | $V_{CC}$ − 1.8 | V |
| | $V_{CTL}$ | CTL1, CTL2 terminal | 0 | — | $V_{REF}$ | V |
| | | CTL terminal | 0 | — | $V_{CC}$ | V |
| Output voltage | $V_{PG}$ | PWRGOOD terminal | 0 | — | 15 | V |
| Output current | $I_O$ | — | − 100 | — | +100 | mA |
| Peak output current | $I_{OP}$ | Duty ≤ 5% ($t = 1 / f_{OSC} \times$ Duty) | − 700 | — | +700 | mA |
| Oscillation frequency | $f_{OSC}$ | — | 100 | 300 | 500 | kHz |
| Timing resistor | $R_T$ | — | 30 | 47 | 130 | kΩ |
| Boot capacitor | $C_B$ | — | — | 0.1 | 1.0 | µF |
| Reference voltage output capacitor | $C_{REF}$ | VREF terminal | — | 0.1 | 1.0 | µF |
| Bias output capacitor | $C_{VB}$ | VB terminal | 1.0 | 4.7 | 10 | µF |
| Soft-start capacitor | $C_S$ | — | — | 0.1 | 1 | µF |
| Short-circuit detection capacitor | $C_{SCP}$ | — | — | 0.01 | 1 | µF |
| Overcurrent detection setting resistor | $R_{LIM}$ | — | 0.1 | 1 | 10 | kΩ |
| Operating ambient temperature | Ta | — | − 30 | + 25 | + 85 | °C |

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

(VCC = 12 V, VB = 0 mA, VREF = 0 mA, Ta = +25 °C)

| Parameter | | Symbol | Pin No. | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| Reference Voltage Block [REF] | Output voltage | $V_{REF}$ | 8 | Ta = + 25 °C | 3.465 | 3.500 | 3.535 | V |
| | | $\Delta V_{REF}/V_{REF}$ | 8 | Ta = 0 °C to + 85 °C | — | 0.5* | — | % |
| | Input stability | Line | 8 | VCC = 6.5 V to 18 V | — | 1 | 10 | mV |
| | Load stability | Load | 8 | VREF = 0 mA to – 1 mA | — | 3 | 10 | mV |
| | Short-circuit output current | $I_{OS}$ | 8 | VREF = 0 V | – 40 | – 20 | – 10 | mA |
| Bias Voltage Block [VB] | Output voltage | $V_B$ | 22 | — | 5.88 | 6.00 | 6.12 | V |
| Triangular Waveform Oscillator Block [OSC] | Oscillation frequency | $f_{OSC}$ | 17, 29 | $R_T$ = 47 kΩ | 270 | 300 | 330 | kHz |
| | Frequency/ temperature variation | $\Delta f_{OSC}/f_{OSC}$ | 17, 29 | Ta = 0 °C to + 85 °C | — | 1* | — | % |
| Undervoltage (VCC) Lockout Circuit Block [UVLO] | Threshold voltage | $V_{TH}$ | 8 | VREF = ↗ | 2.6 | 2.8 | 3.0 | V |
| | Hysteresis width | $V_H$ | 8 | — | — | 0.2* | — | V |
| | Reset voltage | $V_{RST}$ | 8 | VREF = ↘ | 1.7 | 2.1 | 2.5 | V |
| Short-circuit Protection Circuit Block [SCP] | Threshold voltage | $V_{TH}$ | 11 | — | 0.65 | 0.70 | 0.75 | V |
| | Input source current | $I_{CSCP}$ | 11 | — | – 14 | – 10 | – 6 | µA |
| Overcurrent Protection Circuit Block [OCP] | ILIM terminal input current | $I_{LIM}$ | 23, 25 | $R_T$ = 47 kΩ | 106 | 118 | 130 | µA |
| | Offset voltage | $V_{IO}$ | 23, 25 | — | — | 1* | — | mV |
| Overvoltage Protection Circuit Block [OVP] | Threshold voltage | $V_{TH}$ | 1, 15 | –INE = ↗ | 1.35 | 1.38 | 1.41 | V |
| | Input bias current | $I_B$ | 1, 15 | –INE = 0 V | –730 | –110 | — | nA |
| Protection Status Output Circuit Block [PWRGOOD] | Output leakage current | $I_{LEAK}$ | 12 | PWRGOOD = 5 V | — | — | 40 | µA |
| | Output "L" level voltage | $V_{OL}$ | 12 | PWRGOOD = 1 mA | — | 0.1 | 0.4 | V |
| Soft-start Circuit Block [CS] | Charge current | $I_{CS}$ | 3, 13 | — | – 4.2 | – 3.0 | – 1.8 | µA |

*(Continued)*

(VCC = 12 V, VB = 0 mA, VREF = 0 mA, Ta = +25 °C)

| Parameter | | Symbol | Pin No. | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| Error Amp Block [Error Amp] | Threshold voltage | $V_{TH1}$ | 1, 15 | FB = 2.4 V, Ta = + 25 °C | 1.221 | 1.230 | 1.239 | V |
| | | $V_{TH2}$ | 1, 15 | FB = 2.4 V, Ta = 0 °C to + 85 °C | 1.218 | 1.230 | 1.242 | V |
| | Input bias current | $I_B$ | 1, 15 | –INE = 0 V | – 730 | – 110 | — | nA |
| | Voltage gain | $A_V$ | 2, 14 | DC | 60 | 100 | — | dB |
| | Frequency bandwidth | BW | 2, 14 | $A_V$ = 0 dB | — | 1.5* | — | MHz |
| | Output voltage | $V_{FBH}$ | 2, 14 | — | 3.2 | 3.4 | — | V |
| | | $V_{FBL}$ | 2, 14 | — | — | 40 | 200 | mV |
| | Output source current | $I_{SOURCE}$ | 2, 14 | FB = 2.4 V | — | – 2 | – 1 | mA |
| | Output sink current | $I_{SINK}$ | 2, 14 | FB = 2.4 V | 150 | 250 | — | µA |
| PWM Comparator Block [PWM Comp.] | Threshold voltage | $V_{TL}$ | 2, 14 | Duty cycle = 0 % | 1.7 | 1.8 | — | V |
| | | $V_{TH}$ | 2, 14 | Duty cycle = Dtr | — | 2.86 | 3.00 | V |
| Dead Time Control Block [DTC] | Maximum duty cycle | Dtr | 17, 29 | $R_T$ = 47 kΩ | 75 | 81 | 87 | % |
| Output Block [Drive] | Output current (main side) | $I_{SOURCE1}$ | 17, 29 | OUT1 = 12 V, CB = 17 V, VS = 12 V, Duty ≤ 5 % (t = 1/ $f_{OSC}$ × Duty) | — | – 700* | — | mA |
| | | $I_{SINK1}$ | 17, 29 | OUT1 = 17 V, CB = 17 V, VS = 12 V, Duty ≤ 5 % (t = 1/ $f_{OSC}$ × Duty) | — | 900* | — | mA |
| | Output voltage (main side) | $V_{OH1}$ | 17, 29 | OUT1 = – 100 mA, CB = 17 V, VS = 12 V | $V_{CB}$ – 2.5 | $V_{CB}$ – 0.9 | — | V |
| | | $V_{OL1}$ | 17, 29 | OUT1 = 100 mA, CB = 17 V, VS = 12 V | — | $V_S$ + 0.9 | $V_S$ + 1.4 | V |
| | Output current (synchronous rectification side) | $I_{SOURCE2}$ | 19, 27 | OUT2 = 0 V, Duty ≤ 5 % (t = 1/ $f_{OSC}$ × Duty) | — | – 750* | — | mA |
| | | $I_{SINK2}$ | 19, 27 | OUT2 = 6 V, Duty ≤ 5 % (t = 1/ $f_{OSC}$ × Duty) | — | 900* | — | mA |

*(Continued)*

*(Continued)*

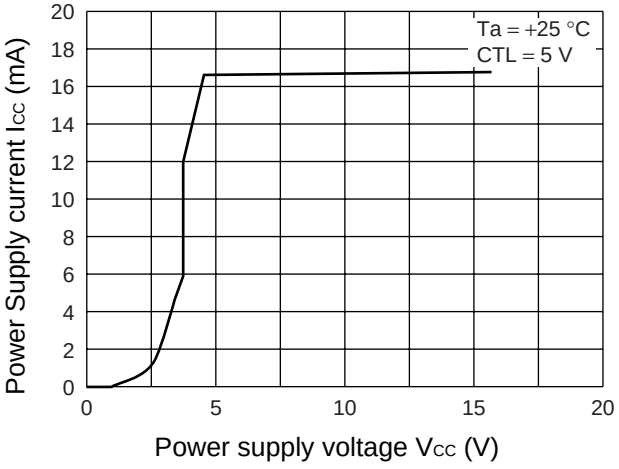
(VCC = 12 V, VB = 0 mA, VREF = 0 mA, Ta = + 25 °C)

| Parameter | | Symbol | Pin No. | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| Output Block [Drive] | Output voltage (synchronous rectification side) | $V_{OH2}$ | 19, 27 | OUT2 = – 100 mA | 3.5 | 5.1 | — | V |
| | | $V_{OL2}$ | 19, 27 | OUT2 = 100 mA | — | 1.0 | 1.4 | V |
| | Diode voltage | $V_D$ | 16, 30 | VB = 10 mA | — | 0.8 | 1.0 | V |
| | Dead time | $t_{D1}$ | 29, 27, 17, 19 | OUT1 = OUT2 = OPEN, VS = 0 V OUT2 : ↓ – OUT1 : ↑ | 40 | 80 | 120 | ns |
| | | $t_{D2}$ | 29, 27, 17, 19 | OUT1 = OUT2 = OPEN, VS = 0 V OUT1 : ↓ – OUT2 : ↑ | 60 | 120 | 180 | ns |
| Control Block [CTL, CTL1, CTL2] | Output ON condition | $V_{ON}$ | 9, 10 | — | 2 | — | $V_{REF}$ | V |
| | Output OFF condition | $V_{OFF}$ | 9, 10 | — | 0 | — | 0.8 | V |
| | Output ON condition | $V_{ON}$ | 6 | — | 2 | — | $V_{CC}$ | V |
| | Output OFF condition | $V_{OFF}$ | 6 | — | 0 | — | 0.8 | V |
| | Input current | $I_{CTL}$ | 9, 10 | CTL1 = CTL2 = 0 V | – 44 | – 35 | – 29 | µA |
| | | | 6 | CTL = 5 V | — | 50 | 75 | µA |
| General | Standby current | $I_{CCS}$ | 24 | CTL = 0 V | — | 0 | 10 | µA |
| | Power-supply current | $I_{CC}$ | 24 | CTL = 5 V | — | 15 | 23 | mA |

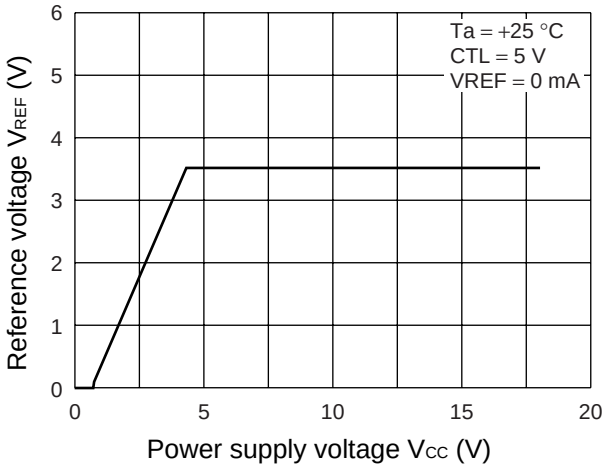
*: Standard design value

## ■ TYPICAL CHARACTERISTICS

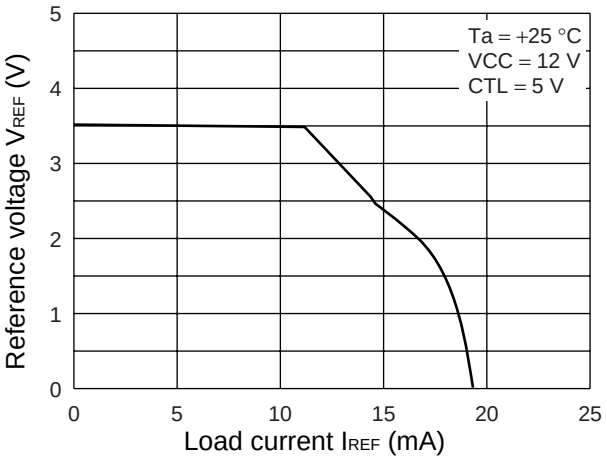
Power Supply Current vs. Power Supply Voltage



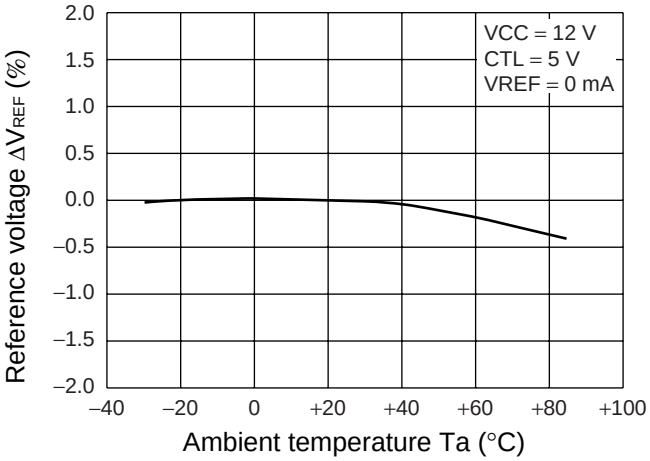

Reference Voltage vs. Power Supply Voltage



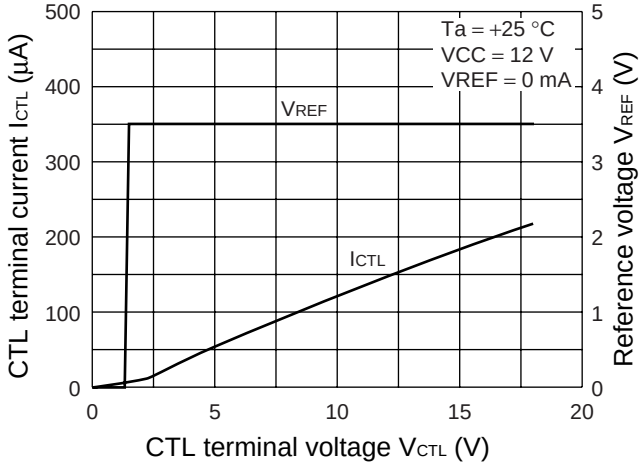

Reference Voltage vs. Load Current



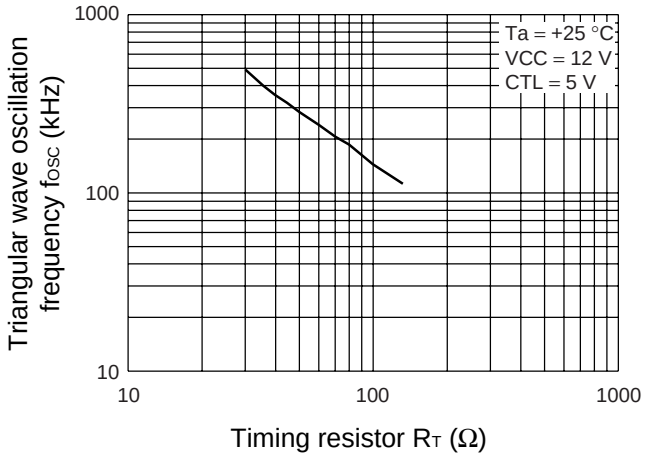

Reference Voltage vs. Ambient Temperature




CTL Terminal Current, Reference Voltage vs. CTL Terminal Voltage




Triangular Wave Oscillation Frequency vs. Timing Resistor

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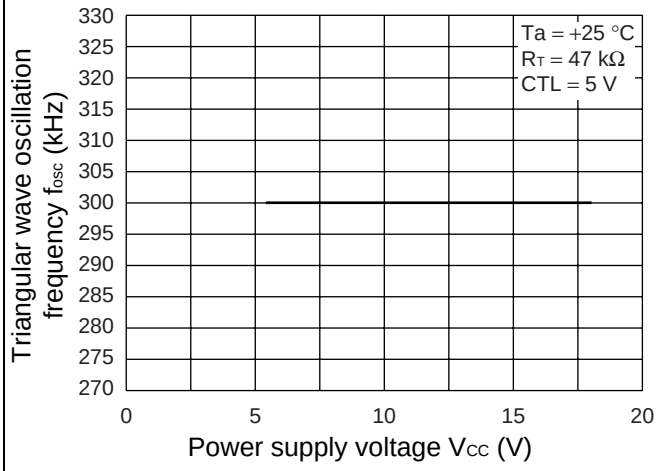
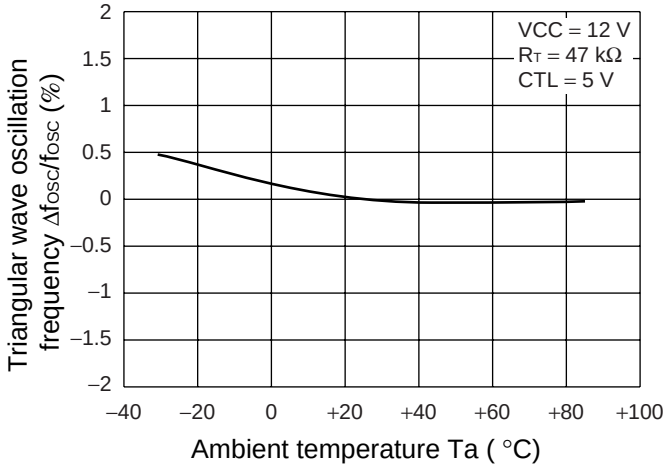
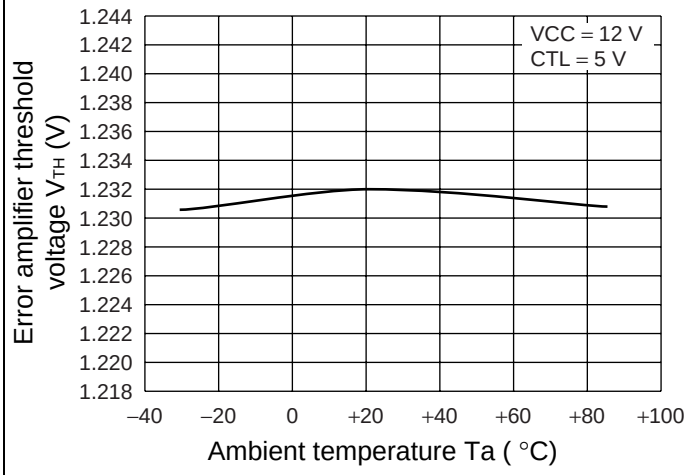
Triangular Wave Oscillation Frequency
vs. Power Supply Voltage



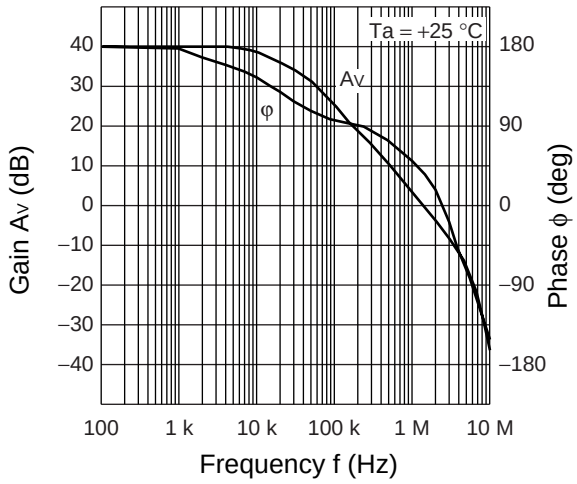

Triangular Wave Oscillation Frequency
vs. Ambient Temperature

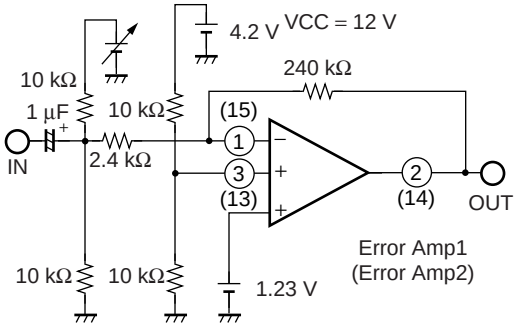



Error Amplifier Threshold Voltage
vs. Ambient Temperature




Error Amplifier, Gain, Phase
vs. Frequency

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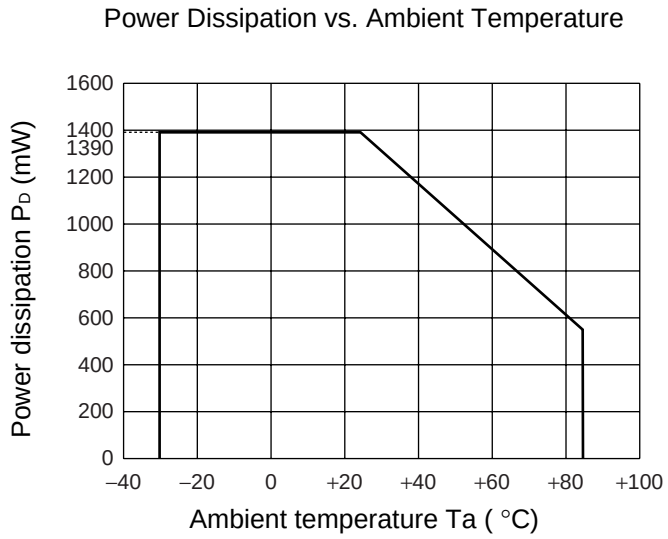

Power Dissipation vs. Ambient Temperature
Power dissipation $P_D$ (mW)
1600
1400
1390
1200
1000
800
600
400
200
0
–40
–20
0
+20
+40
+60
+80
+100
Ambient temperature Ta ( °C)

## ■ FUNCTIONS

### 1. DC/DC Converter Functions

#### (1) Reference voltage block (Ref)

The reference voltage circuit generates a temperature-compensated reference voltage (typically 3.5 V) using the voltage supplied from the power supply terminal (pin 24) . The voltage is used as the reference voltage for the IC's internal circuit.

The reference voltage can be used to supply a load current of up to 1 mA to an external device through the VREF terminal (pin 8) .

#### (2) Triangular-wave oscillator block (OSC)

The triangular waveform oscillator incorporates a triangular oscillation frequency setting capacitor connected respectively to the RT terminal (pin 5) to generate triangular oscillation waveforms CT1 (amplitude of 1.8 V to 3.0 V) and CT2 (amplitude of 1.8 V to 3.0 V in antiphase with CT1). The symmetrical-phase system using the two opposite-phase triangular waves reduces the input ripple current, resulting in a smaller input capacitor.

The triangular oscillation waveforms are input to the IC's internal PWM comparator.

#### (3) Error amplifier block (Error Amp1, Error Amp2)

The error amplifier detects the DC/DC converter output voltage and outputs PWM control signals. By connecting a feedback resistor and capacitor between the output terminal and inverted input terminal, it is possible to create any desired level of loop gain, thereby providing stable phase compensation to the system.

Also, it is possible to prevent rush current at power supply start-up by connecting a soft-start capacitor to the CS1 terminal (pin 3) or CS2 terminal (pin 13), the non-inverted input terminal for Error Amp. The use of Error Amp for soft-start detection makes it possible for a system to operate on a fixed soft-start time that is independent of the output load on the DC/ DC converter.

#### (4) PWM comparator block (PWM Comp.)

The PWM comparator is a voltage-pulse width modulator that controls the output duty depending on the input/output voltage.

Main side : Turns the output transistor on in the intervals in which the error amplifier output voltage is higher than the triangular wave voltage.

Synchronous rectification side : Turns the output transistor on in the intervals in which the error amplifier output voltage is lower than the triangular wave voltage.

#### (5) Output block

The output circuits on the main side and on the synchronous rectification side are both in the totem pole configuration, capable of driving an external N-ch MOS FET.

In addition, because the output drive ability (700 mA Max : Duty ≤ 5%) is high, the gate – source capacity is large and the FET of low ON resistor can be used.

## 2. Channel Control Function

Channels, main, VB and PWRGOOD are turned on and off depending on the voltage levels at the CTL terminal (pin 6), CTL1 terminal (pin 9) and CTL2 terminal (pin 10).

Channel On/Off Setting Conditions

| CTL | CTL1 | CTL2 | Power | CH1 | CH2 | VB | PWRGOOD |
|---|---|---|---|---|---|---|---|
| L | —* | —* | OFF | OFF | OFF | OFF | OFF |
| H | L | L | ON | OFF | OFF | ON | ON |
| H | H | L | ON | ON | OFF | ON | ON |
| H | L | H | ON | OFF | ON | ON | ON |
| H | H | H | ON | ON | ON | ON | ON |

*: Undefined

## 3. Protective Functions

### (1) Undervoltage lockout protection circuit (UVLO)

The transient state or a momentary drops in supply voltage, which occurs when the power supply is turned on, may cause the control IC to malfunction, resulting in breakdown or degradation of the system. To prevent such malfunctions, the undervoltage lockout protection circuit detects the internal reference voltage level with respect to the power supply voltage, turns off the output transistor, and sets the dead time to 100% while holding the CSCP terminal (pin 11) at the “L” level and setting the PWRGOOD terminal (pin 12) to the “L” level.

The system is restored when the supply voltage reaches the threshold voltage of the undervoltage lockout protection circuit.

### (2) Timer-latch overcurrent protection circuit block (OCP)

The timer-latch overcurrent protection circuit is actuated upon completion of the soft-start period. When an overcurrent flows, the circuit detects the increase in the voltage between the main-side FET’s drain and source using the main-side FET ON resistor, actuates the timer circuit, and starts charging the capacitor $C_{SCP}$ connected to the CSCP terminal (pin 11). If the overcurrent remains flowing beyond the predetermined period of time, the circuit sets the latch to turn off the FETs on the main side and synchronous rectification side of each channel while setting the PWRGOOD terminal (pin 12) to the “L” level. The detection current value can be set by resistor $R_{LIM1}$ connected between the main-side FET’s drain and the ILIM1 terminal (pin 25) and resistor $R_{LIM2}$ connected between the drain and the ILIM2 terminal (pin 23).

To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the “L” level to lower the VREF terminal (pin 8) voltage to 1.7 V (Min) or less. It can also be reset by setting both of the CTL1 terminal (pin 9) and CTL2 terminal (pin 10) to the “L” level. (Refer to “1. Setting Timer-Latch Overcurrent Detection Current” in ■ ABOUT TIMER-LATCH PROTECTION CIRCUIT.)

### (3) Timer-latch short-circuit protection circuit (SCP)

The short-circuit detection comparator (SCP Comp.) detects the output voltage level and, if the error amplifier output voltage of either channel reaches the short-circuit detection voltage (typically 3.1 V), the timer circuit is actuated to start charging the external capacitor Cscp connected to the CSCP terminal (pin 11).

When the capacitor voltage reaches about 0.7 V, the circuit turns off the output transistor and sets the dead time to 100%.

The PWRGOOD terminal (pin 12) is fixed at the “L” level.

To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the “L” level to lower the VREF terminal (pin 8) voltage to 1.7 V (Min) or less. It can also be reset by setting both of the CTL1 terminal (pin 9) and CTL2 terminal (pin 10) to the “L” level. (Refer to “2. Setting Time Constant for Timer-Latch Short-Circuit Protection Circuit” in ■ ABOUT TIMER-LATCH PROTECTION CIRCUIT.)

**(4) Timer-latch overvoltage protection circuit block (OVP)**

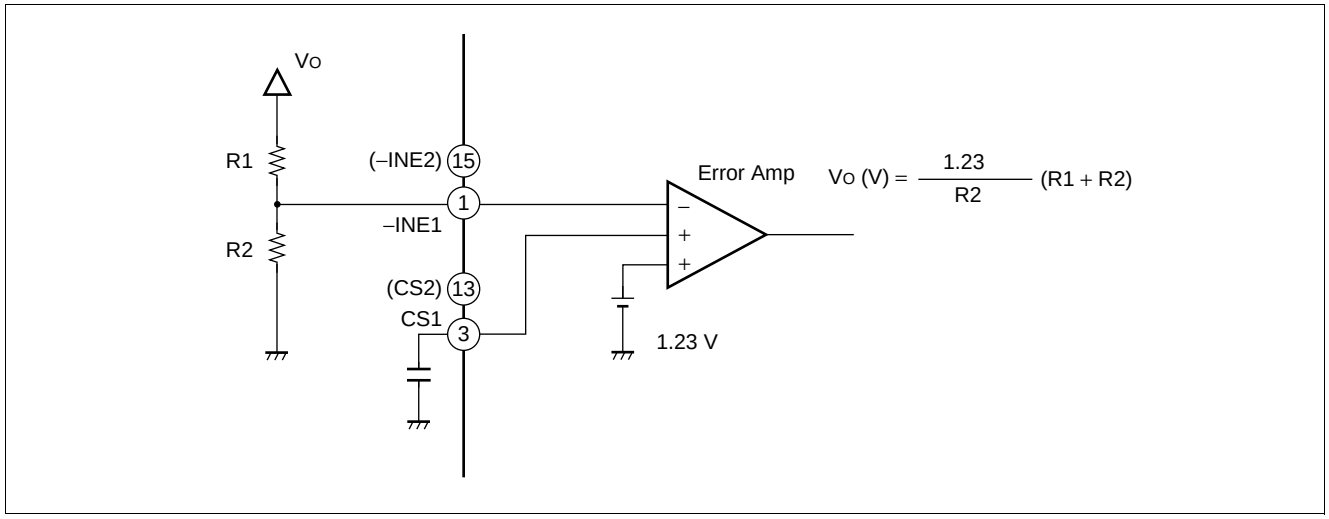
When the overvoltage detection comparator (OVP Comp.) provided for each channel detects the DC/DC converter's output voltage level exceeding its threshold voltage, the timer-latch overvoltage protection circuit actuates the timer circuit and starts charging the capacitor $C_{SCP}$ connected to the CSCP terminal (pin 11). If the overvoltage remains applied beyond the predetermined period of time, the circuit sets the latch to turn off the FET on the main side of each channel while setting the PWRGOOD terminal (pin 12) to the "L" level.

To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the "L" level to lower the VREF terminal (pin 8) voltage to 1.7 V (Min) or less. It can also be reset by setting both of the CTL1 terminal (pin 9) and CTL2 terminal (pin 10) to the "L" level. (Refer to "3. Setting Overvoltage Detection by the Timer-Latch Overvoltage Protection Circuit" in ■ ABOUT TIMER-LATCH PROTECTION CIRCUIT.)

**(5) Protection status output circuit block (PWRGOOD)**

The protection status output circuit outputs the "L" level signal to the PWRGOOD terminal (pin 12) when each protection circuit is actuated.

## ■ SETTING THE OUTPUT VOLTAGE




< CH1, CH2 >

## ■ SETTING THE TRIANGULAR OSCILLATION FREQUENCY

The triangular oscillation frequency is determined by the timing resistor ($R_T$) connected to the RT terminal (pin 5).

Triangular oscillation frequency: $f_{OSC}$

$$f_{OSC}\ (kHz) \fallingdotseq \frac{14100}{R_T\ (k\Omega)}$$

## ■ SETTING THE SOFT-START AND DISCHARGE TIMES

To prevent rush currents when the IC is turned on, you can set a soft-start by connecting soft-start capacitors ($C_{S1}$ and $C_{S2}$) to the CS1 terminal (pin 3) for channel 1 and the CS2 terminal (pin 13) for channel 2, respectively.

Setting the each control terminals (CTL1 and CTL2) from “L” to “OPEN” switches SW1 and SW2 from B to A to charge the external soft-start capacitors ($C_{S1}$ and $C_{S2}$) connected to the CS1 and CS2 terminals at 3 μA.

The error amplifier output (FB1 or FB2) is determined by comparison between the lower one of the potentials at two noninverted input terminals (1.23 V, CS terminal voltages) and the inverted input terminal voltage (-INE).

The FB terminal voltage during the soft-start period is therefore determined by comparison between the -INE terminal and CS terminal voltages. The DC/DC converter output voltage rises in proportion to the CS terminal voltage as the soft-start capacitor connected to the CS terminal is charged.

The soft-start time is obtained from the following equation:

Soft-start time: ts (time to output 100%)

$ts\ (s) \fallingdotseq 0.41 \times C_S\ (\mu F)$

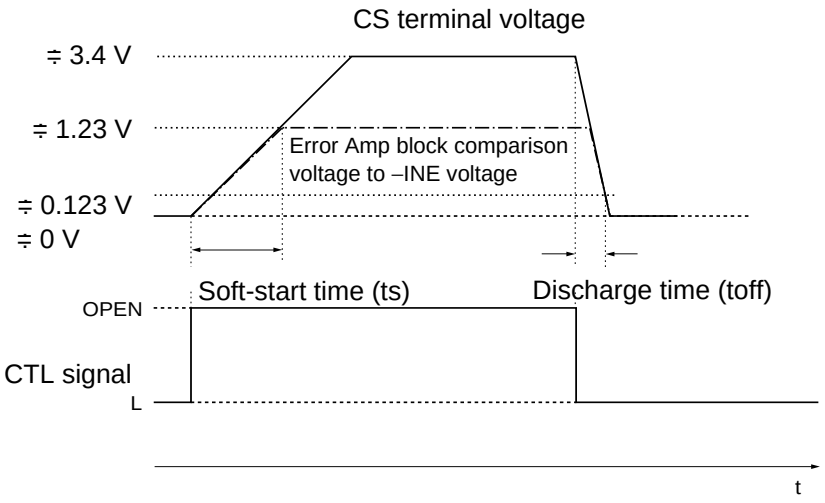
Setting the each control terminals (CTL1 and CTL2) from “OPEN” to “L” switches SW1 and SW2 from A to B.

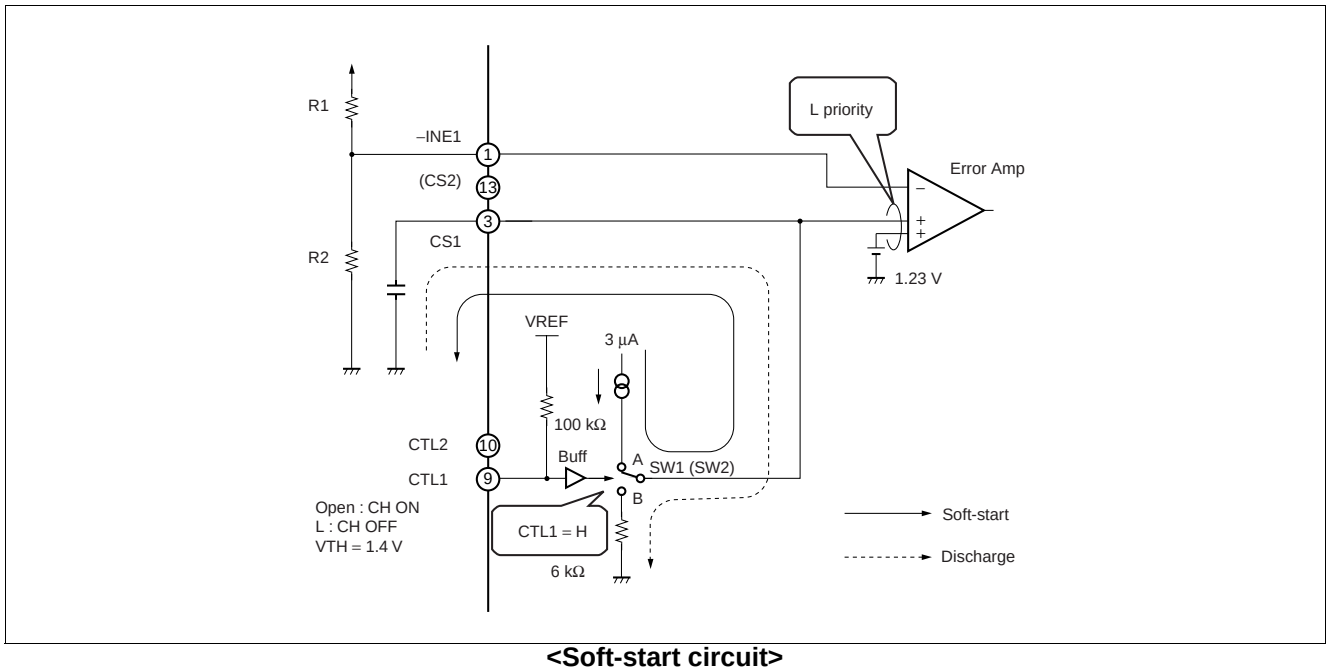
Then the IC discharges the soft-start capacitors ($C_{S1}$ and $C_{S2}$) charged at about 3.4 V using the internally set discharge resistor ($R_S \fallingdotseq 6\ k\Omega$) and lowers the output voltage regardless of the DC/DC converter load current.

The discharge time is obtained from the following equation:

Discharge time: toff (time to output 10%)

$toff\ (s) \fallingdotseq 0.020 \times C_S\ (\mu F)$

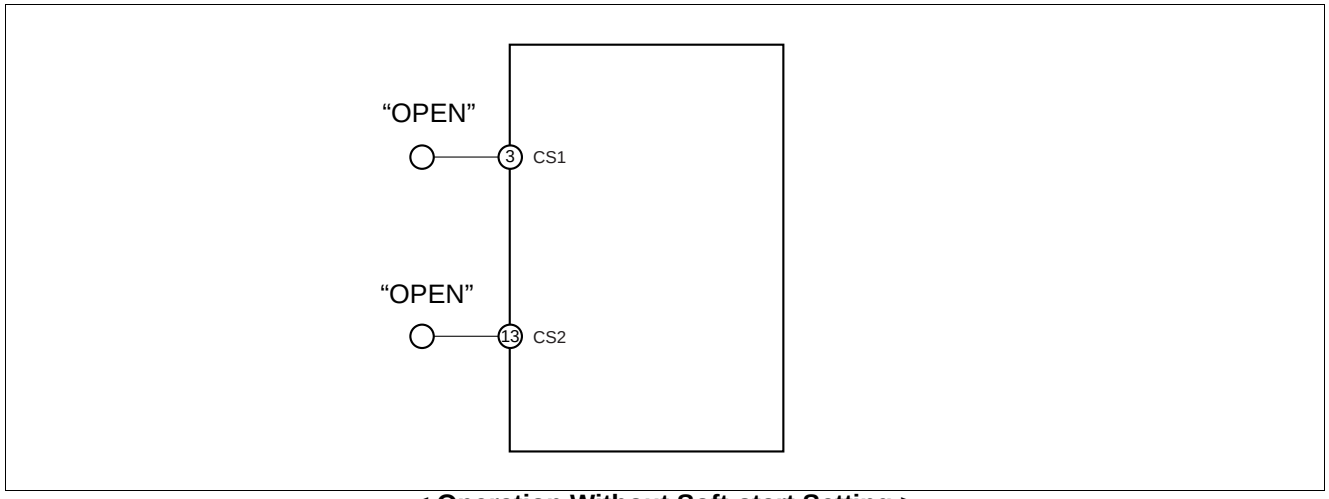





**<Soft-start circuit>**

## ■ TREATMENT OF UNUSED CS TERMINALS

When the soft-start function is not used, the CS1 terminal (pin 3) and CS2 terminal (pin 13) should be left open.




**< Operation Without Soft-start Setting >**

## ■ ABOUT TIMER-LATCH PROTECTION CIRCUIT

### 1. Setting Timer-Latch Overcurrent Detection Current

The overcurrent protection circuit is actuated upon completion of the soft-start period. When an overcurrent flows, the circuit detects the increase in the voltage between the main-side FET's drain and source using the main-side FET ON resistor ($R_{ON}$), actuates the timer circuit, and starts charging the capacitor $C_{SCP}$ connected to the CSCP terminal (pin 11). If the overcurrent remains flowing beyond the predetermined period of time, the circuit sets the latch to turn off the FETs on the main side and synchronous rectification side of each channel while setting the PWRGOOD terminal (pin 12) to the "L" level. The detection current value can be set by the resistors ($R_{LIM1}$ and $R_{LIM2}$) connected between the main-side FET's drain and the ILIM1 terminal (pin 25) and between the drain and the ILIM2 terminal (pin 23), respectively.

The internal current ($I_{LIM}$) can be set by the timing resistor ($R_T$) connected to the RT terminal (pin 5).

Internal current value: $I_{LIM}$

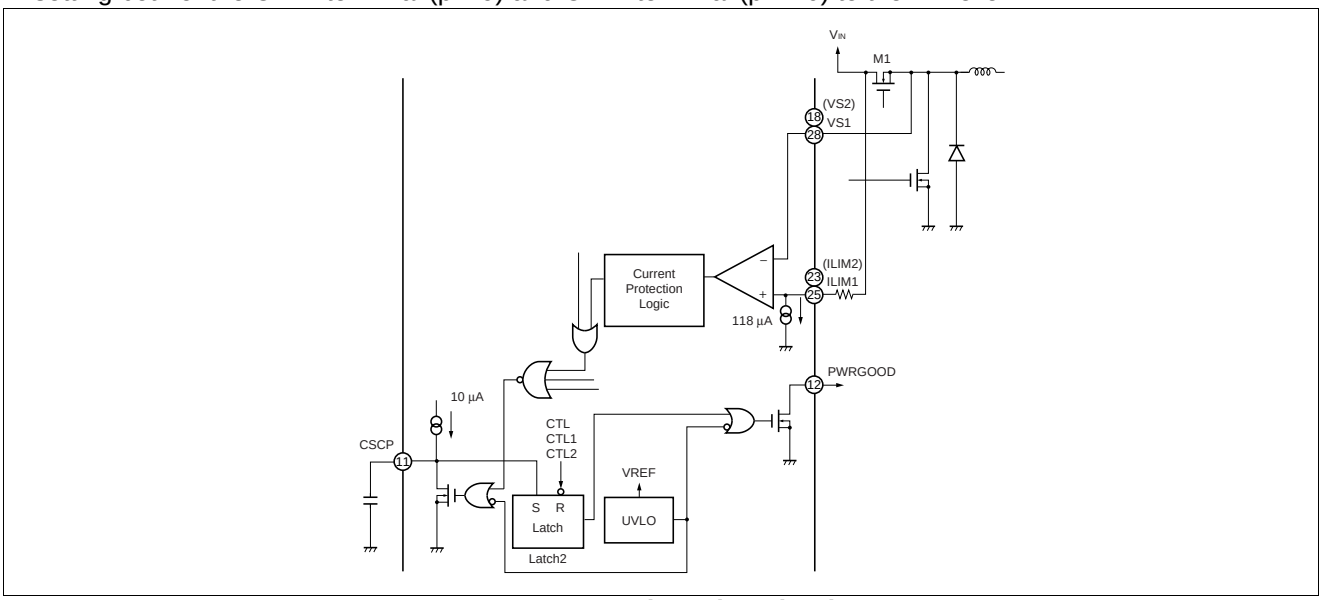
$$I_{LIM}\ (\mu A) \fallingdotseq \frac{5546}{R_T\ (k\Omega)}$$

Detection current value: $I_{OCP}$

$$I_{OCP}\ (A) \fallingdotseq \frac{I_{LIM}(A) \times R_{LIM}(\Omega)}{R_{ON}\ (\Omega)} - \frac{(V_{IN}(V) - V_O(V)) \times V_O(V)}{2 \times V_{IN}(V) \times f_{OSC}(Hz) \times L(H)}$$

$R_{LIM}$: Overcurrent detection resistor
$R_{ON}$: Main-side FET ON resistor
$V_{IN}$: Input voltage
$V_O$: DC/DC converter output voltage
$f_{OSC}$: Oscillation frequency
L: Coil inductance

To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the "L" level to lower the VREF terminal (pin 8) voltage to 1.7 V (Min) or less. It can also be reset by setting both of the CTL1 terminal (pin 9) and CTL2 terminal (pin 10) to the "L" level.




**<Overcurrent detection circuit>**

## 2. Setting Time Constant for Timer-Latch Short-Circuit Protection Circuit

Each channel uses the short-circuit detection comparator (SCP Comp.) to always compare the error amplifier's output level to the reference voltage.

While the DC/DC converter load conditions are stable on both channels, the short-circuit detection comparator keeps its output at the "H" level and the CSCP terminal (pin 11) remains at the "L" level.

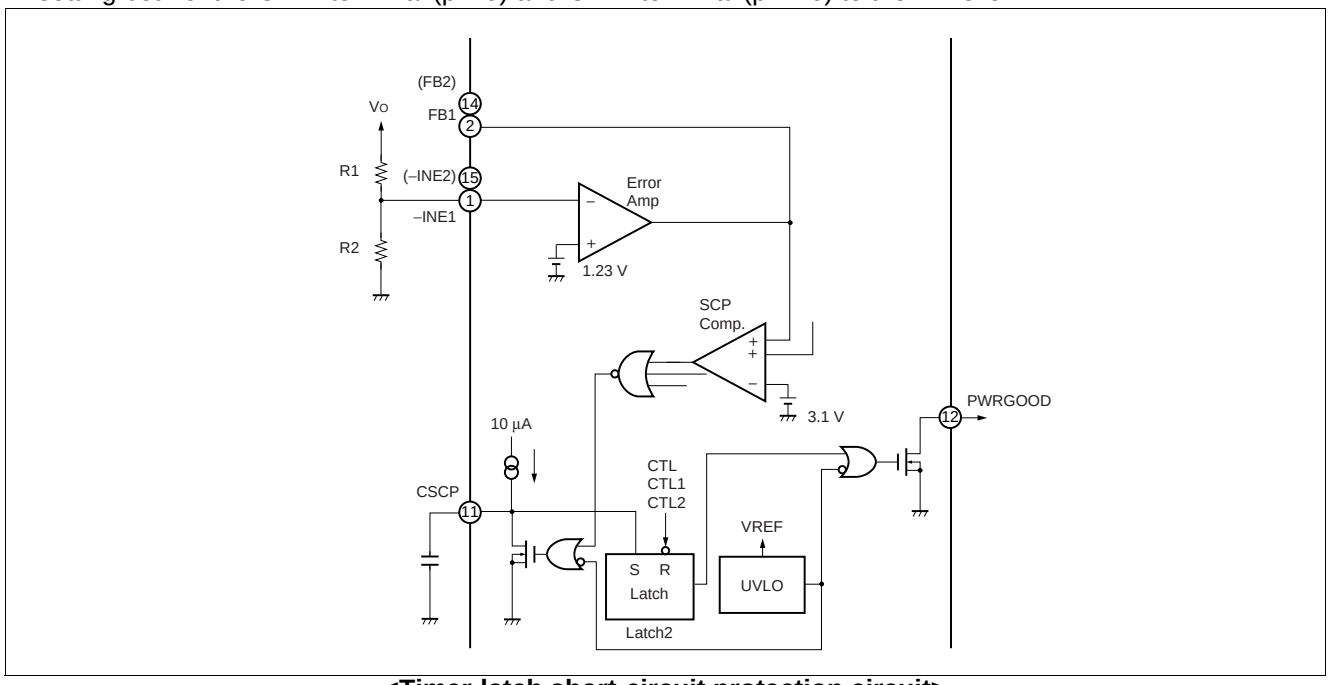
If a load condition changes rapidly due to a short-circuit of the load, causing the output voltage to drop, the short-circuit detection comparator changes its output to the "L" level. This causes the external short-circuit protection capacitor Cscp connected to the CSCP terminal to be charged at 10 µA.

Short-circuit detection time ($t_{SCP}$)

$t_{SCP}$ (s) ≒ 0.070 × $C_{SCP}$ (µF)

When capacitor Cscp is charged to the threshold voltage ($V_{TH}$ ≒ 0.70 V), the protection circuit sets the latch and turns off the external FET (setting the dead time to 100%). At this time, the latch input is closed. As the result, the CSCP terminal is held at the "L" level and the PWRGOOD terminal is set to "L" level. The protection circuit closes both channels even when a short-circuit is detected on only either.

To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the "L" level to lower the VREF terminal (pin 8) voltage to 1.7 V (Min) or less. It can also be reset by setting both of the CTL1 terminal (pin 9) and CTL2 terminal (pin 10) to the "L" level.




**<Timer-latch short-circuit protection circuit>**

### 3. Setting Overvoltage Detection by the Timer-Latch Overvoltage Protection Circuit

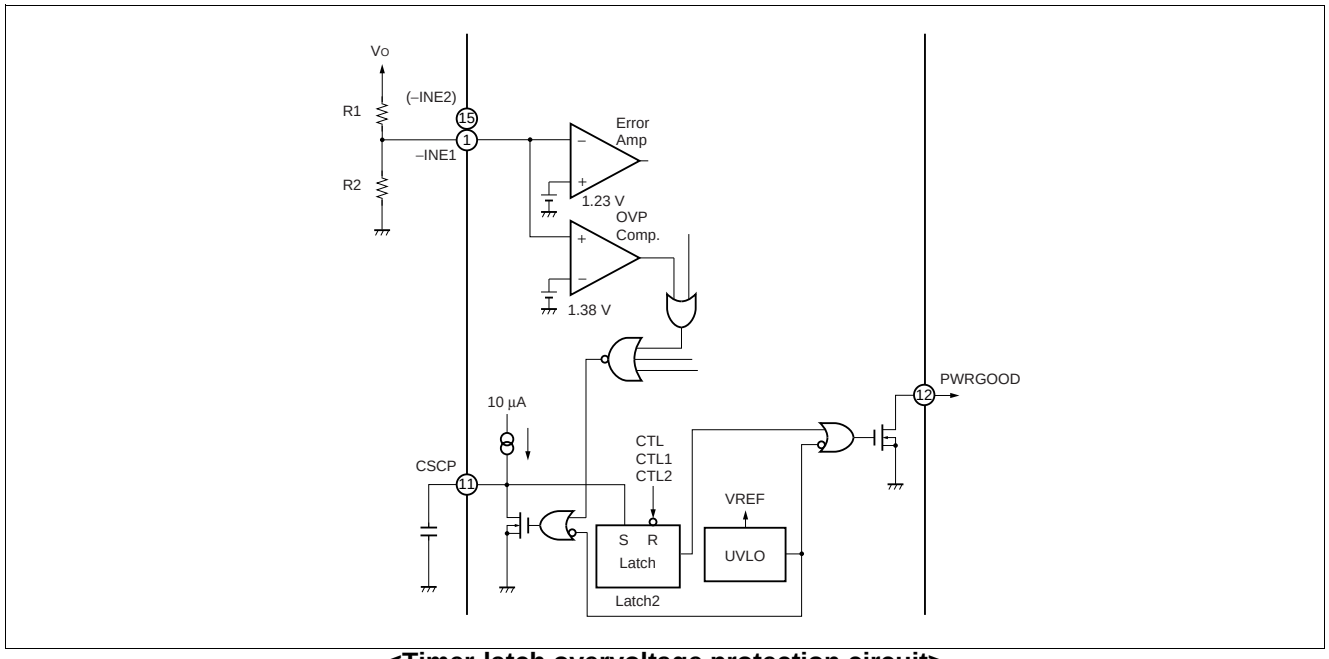
An overvoltage output from the DC/DC converter can be detected by connecting external resistors from the DC/DC converter output to the noninverted input terminal (-INE1 terminal (pin 1) and -INE2 terminal (pin 15)) of the overvoltage comparators (OVP Comp. 1 and OVP Comp. 2).

When the DC/DC converter output voltage exceeds the overvoltage detection level, the output of the overvoltage comparator (OVP Comp. 1 and OVP Comp. 2) becomes the “H” level and the overvoltage protection circuit actuates the timer circuit to start charging the external capacitor Cscp connected to the CSCP terminal (pin 11). If the overvoltage remains applied beyond setting time, the circuit sets the latch to turn off the FET on the main side of each channel while setting the PWRGOOD terminal (pin 12) to the “L” level. The protection circuit closes both channels even when an overvoltage is detected on only either.

Overvoltage detection voltage : $V_{OVP}$

$V_{OVP}$ (V) ≒ 1.38 × (R1 (Ω) + R2 (Ω)) / R2 (Ω) ≒ 1.12 × $V_O$

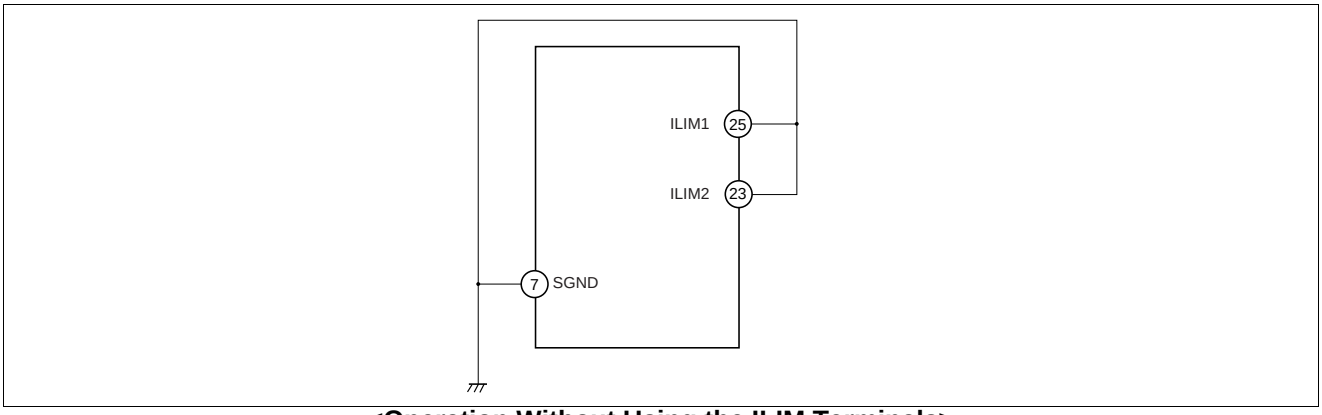
To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the "L" level to lower the VREF terminal (pin 8) voltage to 1.7 V (Min) or less. It can also be reset by setting both of the CTL1 terminal (pin 9) and CTL2 terminal (pin 10) to the "L" level.




**<Timer-latch overvoltage protection circuit>**

## ■ TREATMENT OF UNUSED ILIM TERMINALS

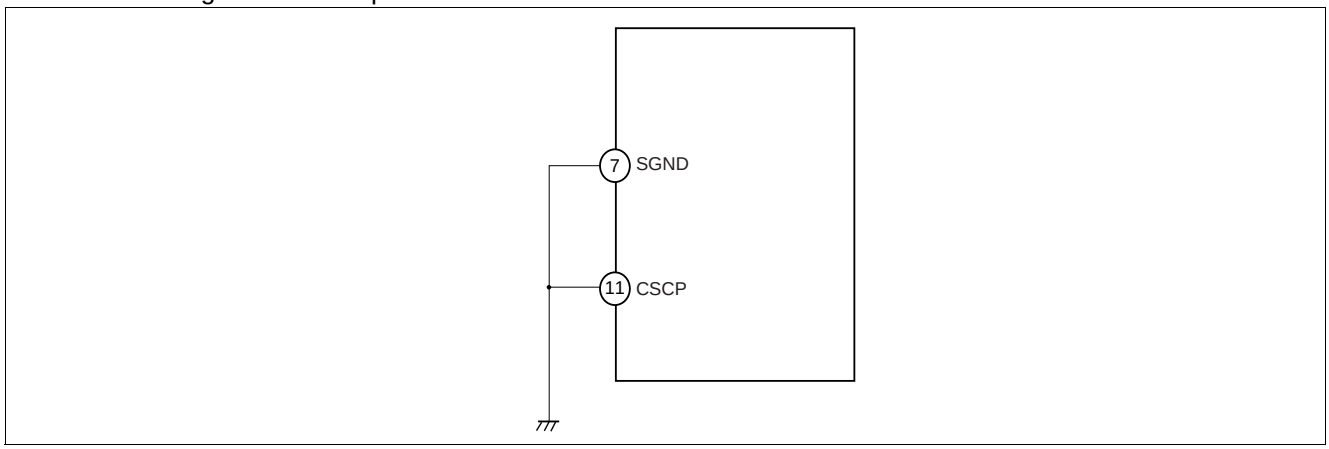
When the overcurrent protection circuit is not used, the ILIM1 terminal (pin 25) and ILIM2 terminal (pin 23) should be shorted to the SGND terminal.




**<Operation Without Using the ILIM Terminals>**

## ■ PROCESSING WITHOUT USING THE CSCP TERMINAL

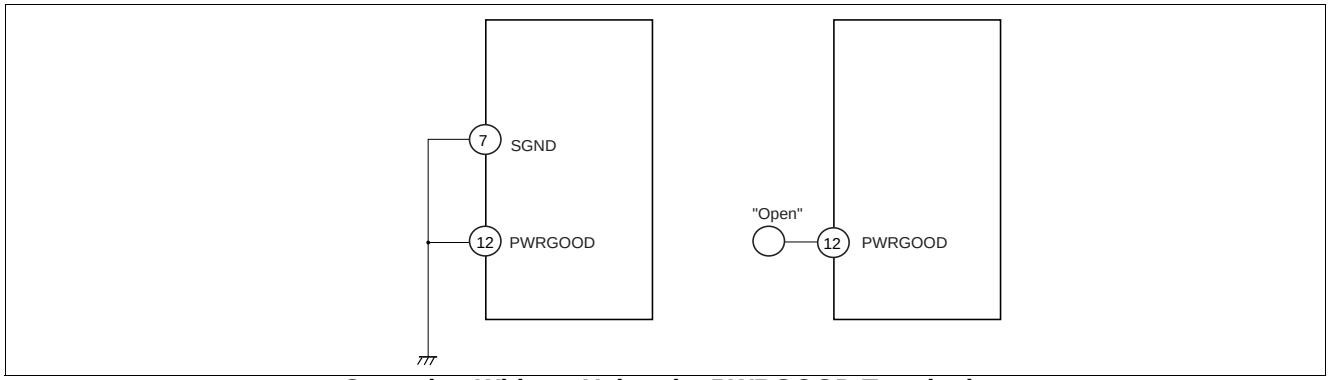
When the timer-latch short-circuit protection circuit is not used, the CSCP terminal (pin 11) should be shorted to SGND using the shortest possible connection.




**<Operation Without Using the CSCP Terminal>**

## ■ TREATMENT OF UNUSED PWRGOOD TERMINALS

When the PWRGOOD terminal is not used, the PWRGOOD terminal (pin 12) should be shorted or open to the SGND terminal.




**<Operation Without Using the PWRGOOD Terminals>**

## ■ OUTPUT STATES DURING PROTECTION CIRCUIT OPERATION

The table below lists the output states with each protection circuit actuated.

| Protection circuit \ Output terminal | | CH1 | | CH2 | | PWRGOOD |
|---|---|---|---|---|---|---|
| | | OUT1-1 | OUT2-1 | OUT1-2 | OUT2-2 | |
| Overcurrent protection circuit | CH1 | L | L | L | L | L |
| | CH2 | L | L | L | L | L |
| Overvoltage protection circuit | CH1 | L | H | L | H | L |
| | CH2 | L | H | L | H | L |
| Short-circuit protection | CH1 | L | L | L | L | L |
| | CH2 | L | L | L | L | L |
| Under voltage lockout protection circuit | | L | L | L | L | L |

## ■ RESETTING THE LATCH OF EACH PROTECTION CIRCUIT

When the overvoltage, overcurrent, or short-circuit protection circuit detects each abnormality, it sets the latch to fix the output at the "L" level. The PWRGOOD terminal (pin 12) is fixed at the "L" level upon abnormality detection by each protection circuit.

To reset the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the "L" level to lower the VREF terminal (pin 8) voltage to 1.7 V (Min) or less. It can also be reset by setting both of the CTL1 terminal (pin 9) and CTL2 terminal (pin 10) to the "L" level.

## ■ NOTE ON IC'S INTERNAL POWER CONSUMPTION

The oscillation frequency of an IC and the total gate charge of FETs largely affects the internal dissipation of the IC.

Pay attention to the following point with respect to the internal power consumption of the IC when applications are used.

$I_B$ (mean current) is obtained from the following equation, assuming Qg1 and Qg2 as the total gate charges applied to the gate capacitors ($Ciss_1$, $Ciss_2$, $Crss_1$, $Crss_2$) of external FETs Q1 and Q2.

Current per channel

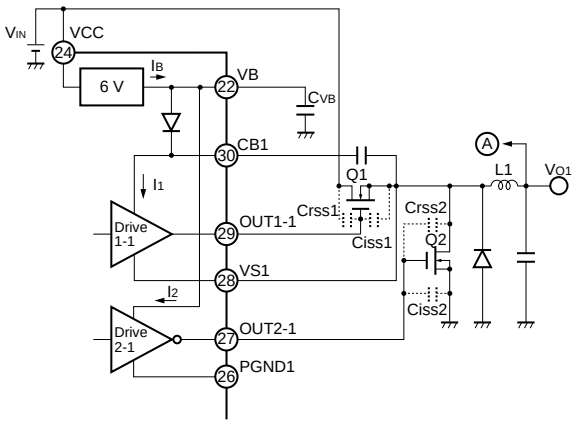
$$I_B\,(A) = I_1 + I_2$$

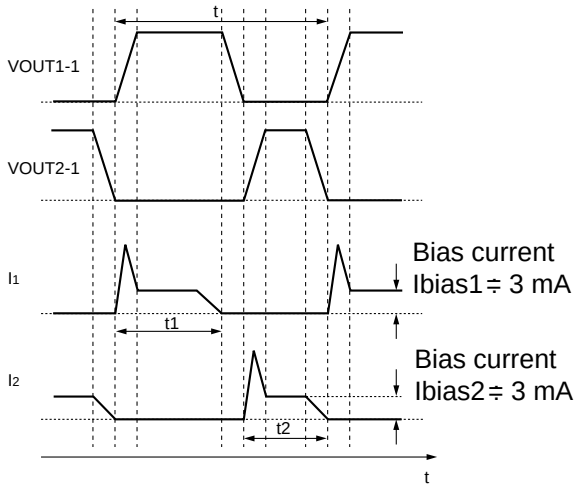
$$\fallingdotseq \text{Ibias1} \times \frac{t1}{t} + \frac{Qg_1}{t} + \text{Ibias2} \times \frac{t2}{t} + \frac{Qg_2}{t} \quad (\text{Ibias1} = \text{Ibias2} \fallingdotseq 3\ \text{mA})$$

As the current consumption by the IC, excluding $I_B$, is about 15 mA, the power consumption is obtained from the following equation :

Power consumption : Pc

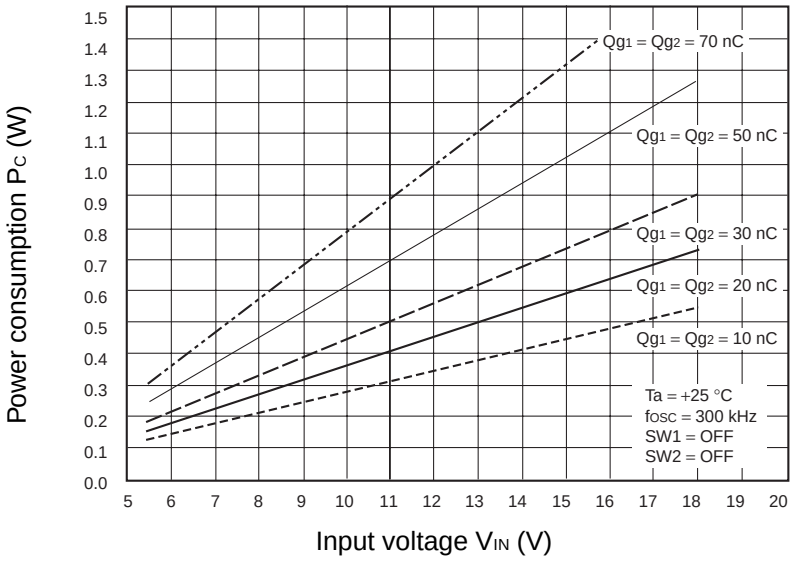
$$Pc\,(W) = 0.015 \times V_{CC}\,(V) + 2 \times V_{CC}\,(V) \bullet I_B\,(A) - V_B\,(V) \bullet I_B\,(A)$$



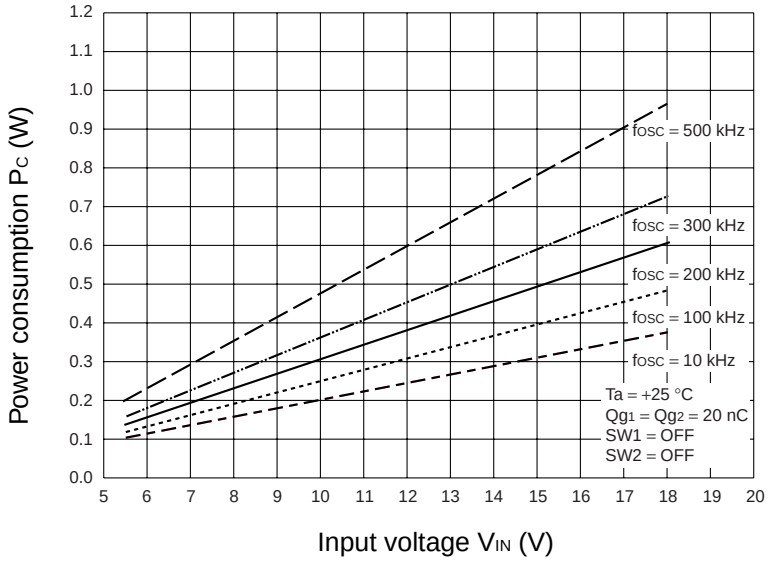




Refer to "Power Consumption vs. Input Voltage" on the next page as a reference and use the above method of obtaining the power consumption to design your application of the IC taking account of the "Power Dissipation vs. Ambient Temperature" characteristic in the ■ TYPICAL CHARACTERISTICS.

Power Consumption vs. Input Voltage (Qg Parameter)

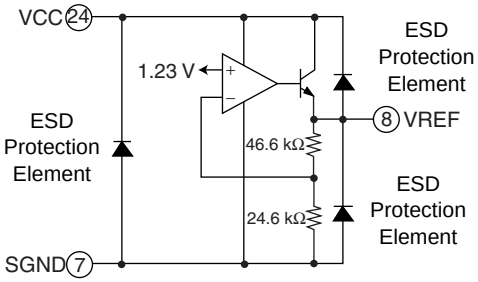



Power Consumption vs. Input Voltage ($f_{OSC}$ Parameter)

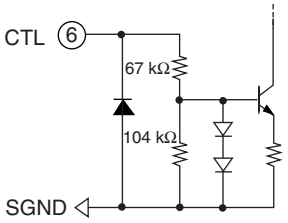


## ■ I/O EQUIVALENT CIRCUIT

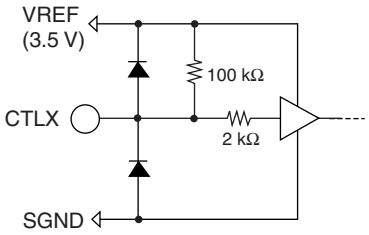
<Reference voltage block>



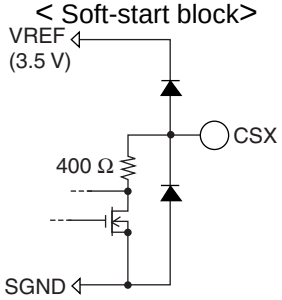

< Control block>



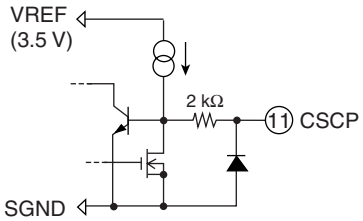

< Channel control block>



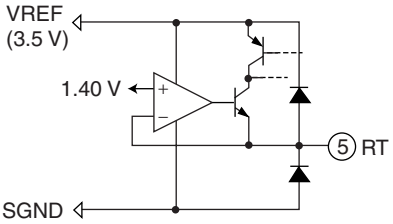

< Soft-start block>



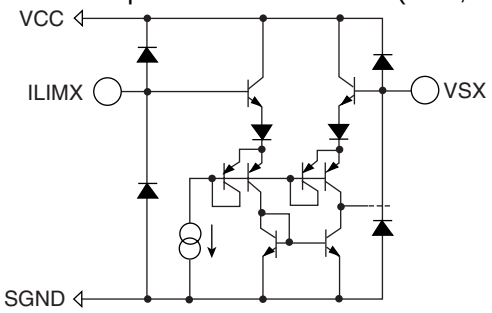

< Short-circuit protection circuit block>



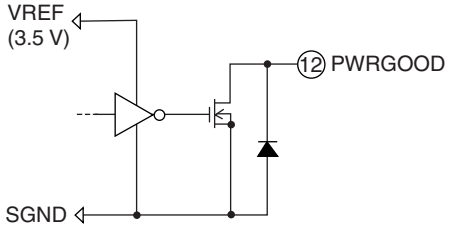

< Triangular wave oscillator block (RT) >



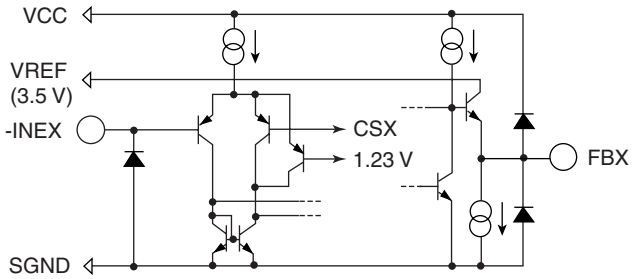

< Overcurrent protection circuit block (CH1, CH2) >



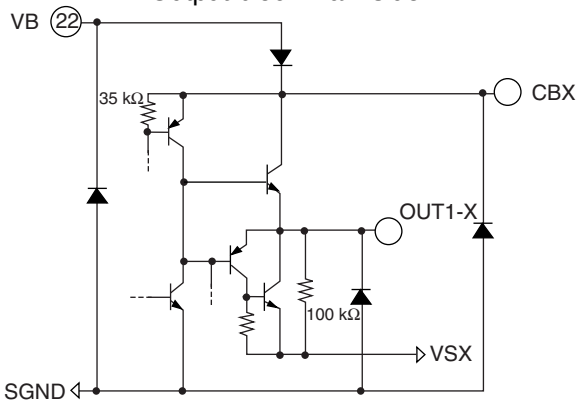

< Protection status output circuit block>



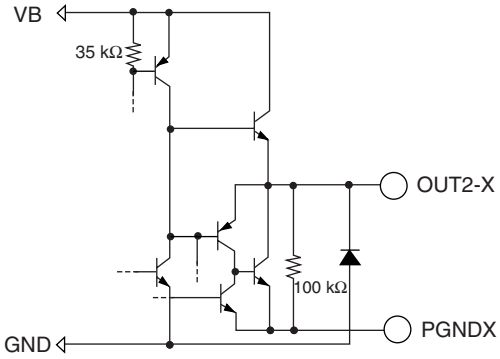

< Error amplifier block (CH1, CH2) >




< Output block main side>

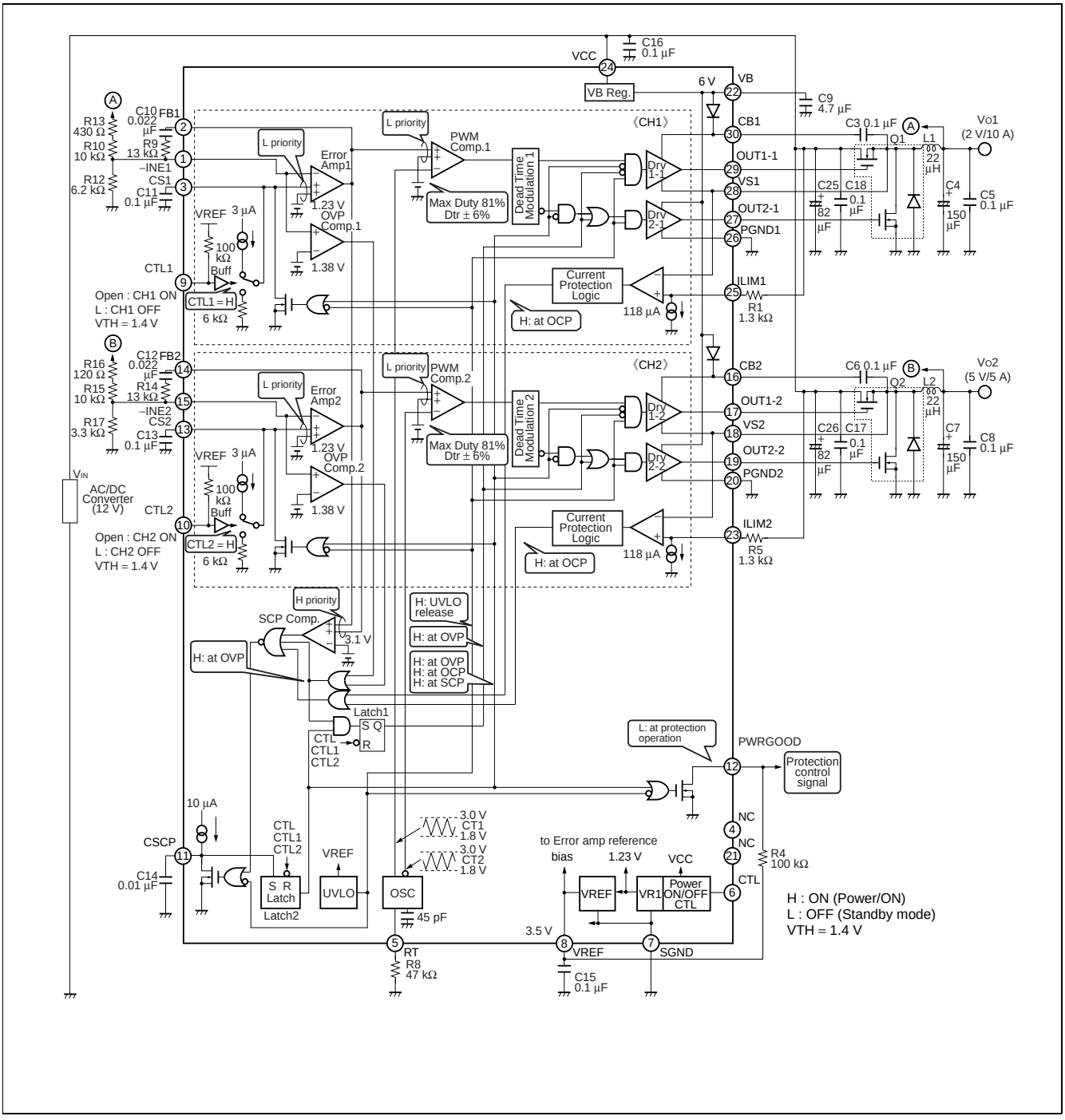



< Output block synchronous rectification side (CH1, CH2) >




X : Each channel No.

## ■ APPLICATION EXAMPLE



## ■ PARTS LIST

| COMPONENT | ITEM | SPECIFICATION | | VENDOR | PARTS NO. |
|---|---|---|---|---|---|
| Q1, Q2 | Dual FETKY™ | Main sides:<br>VDS = 30 V, Qg = 9.9 nC (Max)<br>Synchronous sides:<br>VDS = 30 V, Qg = 20.7 nC (Max)<br>SBD: VF = 0.52 V (Max)<br>at IF = 1 A | | IR | IRF7901D1 |
| L1, L2 | Coil | 22 µH | 3.5 A, 31.6 mΩ | TDK | SLF12565T-220M3R5 |
| C3, C6 | Ceramics Condenser | 0.1 µF | 50 V | TDK | C1608JB1H104K |
| C4 | OS-CON™ | 150 µF | 6.3 V | SANYO | 6SVP150M |
| C5, C8 | Ceramics Condenser | 0.1 µF | 50 V | TDK | C1608JB1H104K |
| C7 | OS-CON™ | 150 µF | 6.3 V | SANYO | 6SVP150M |
| C9 | Ceramics Condenser | 4.7 µF | 10 V | TDK | C3216JB1A475M |
| C10 | Ceramics Condenser | 0.022 µF | 50 V | TDK | C1608JB1H223K |
| C11, C13 | Ceramics Condenser | 0.1 µF | 50 V | TDK | C1608JB1H104K |
| C12 | Ceramics Condenser | 0.022 µF | 50 V | TDK | C1608JB1H223K |
| C14 | Ceramics Condenser | 0.01 µF | 50 V | TDK | C1608JB1H103K |
| C15, C16 | Ceramics Condenser | 0.1 µF | 50 V | TDK | C1608JB1H104K |
| C17, C18 | Ceramics Condenser | 0.1 µF | 50 V | TDK | C1608JB1H104K |
| C25, C26 | OS-CON™ | 82 µF | 16 V | SANYO | 16SVP82M |
| R1, R5 | Resistor | 1.3 Ω | 0.5 % | ssm | RR0816P132D |
| R4 | Resistor | 100 kΩ | 0.5 % | ssm | RR0816P104D |
| R8 | Resistor | 47 kΩ | 0.5 % | ssm | RR0816P473D |
| R9 | Resistor | 13 kΩ | 0.5 % | ssm | RR0816P133D |
| R10 | Resistor | 10 kΩ | 0.5 % | ssm | RR0816P103D |
| R12 | Resistor | 6.2 kΩ | 0.5 % | ssm | RR0816P622D |
| R13 | Resistor | 430 Ω | 0.5 % | ssm | RR0816P434D |
| R14 | Resistor | 13 kΩ | 0.5 % | ssm | RR0816P133D |
| R15 | Resistor | 10 kΩ | 0.5 % | ssm | RR0816P103D |
| R16 | Resistor | 120 Ω | 0.5 % | ssm | RR0816P124D |
| R17 | Resistor | 3.3 kΩ | 0.5 % | ssm | RR0816P332D |

Note : IR : International Rectifier Corp.
TDK : TDK Corporation
SANYO : SANYO Electric Co., Ltd.
ssm : SUSUMU Electronics Corp.
Dual FETKY is a trademark of International Rectifier Corp.
OS-CON is a trademark of SANYO Electric Co., Ltd.

## ■ SELECTION OF COMPONENTS

**• N-ch MOS FET**

The N-ch MOS FET for switching use should be rated for at least 20% more than the maximum input voltage. To minimize continuity loss, use a FET with low $R_{DS(ON)}$ between the drain and source. For high input voltage and high frequency operation, on/off-cycle switching loss will be higher so that power dissipation must be considered. In this application, the IR IRF7901D1 is used. Continuity loss, on/off switching loss, and total loss are determined by the following formulas. The selection must ensure that peak drain current does not exceed rated values, and also must be in accordance with overcurrent detection levels.

Continuity loss : $P_C$

$$P_C = I_D^2 \times R_{DS\,(ON)} \times \text{Duty}$$

On-cycle switching loss : $P_{S\,(ON)}$

$$P_{S\,(ON)} = \frac{V_{D\,(Max)} \times I_D \times tr \times f_{OSC}}{6}$$

Off-cycle switching loss : $P_{S\,(OFF)}$

$$P_{S\,(OFF)} = \frac{V_{D\,(Max)} \times I_{D\,(Max)} \times tf \times f_{OSC}}{6}$$

Total loss : $P_T$

$$P_T = P_C + P_{S\,(ON)} + P_{S\,(OFF)}$$

Example: Using the IR IRF7901D1

CH1 Main side

Input voltage $V_{IN\,(Max)} = 15$ V, output voltage $V_O = 3.3$ V, drain current $I_D = 3$ A, Oscillation frequency $f_{OSC} = 300$ kHz, L = 22 µH, drain-source on resistance $R_{DS\,(ON)} \fallingdotseq 33$ mΩ, tr = 13.8 ns, tf = 8 ns.

Drain current (Max) : $I_{D\,(Max)}$

$$I_{D\,(Max)} = I_O + \frac{V_{IN\,(Max)} - V_O}{2L} \text{ ton}$$

$$= 3 + \frac{15 - 3.3}{2 \times 22 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.22$$

$$\fallingdotseq \underline{3.20\ (A)}$$

Drain current (Min) : $I_{D\,(Min)}$

$$I_{D\,(Min)} = I_O - \frac{V_{IN\,(Max)} - V_O}{2L} \text{ ton}$$

$$= 3 - \frac{15 - 3.3}{2 \times 22 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.22$$

$$\fallingdotseq \underline{2.80\ (A)}$$

$$P_{C1} = I_D^2 \times R_{DS\,(ON)} \times Duty_{(ON)}$$
$$= 3^2 \times 0.033 \times 0.22$$
$$\fallingdotseq \underline{0.065\ W}$$

$$P_{S1\,(ON)} = \frac{V_{D\,(Max)} \times I_D \times tr \times f_{OSC}}{6}$$
$$= \frac{15 \times 3 \times 13.8 \times 10^{-9} \times 300 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.031\ W}$$

$$P_{S1\,(OFF)} = \frac{V_{D\,(Max)} \times I_{D\,(Max)} \times tf \times f_{OSC}}{6}$$
$$= \frac{15 \times 3.2 \times 8 \times 10^{-9} \times 300 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.019\ W}$$

$$P_{T1} = P_{C1} + P_{S1\,(ON)} + P_{S1\,(OFF)}$$
$$\fallingdotseq 0.065 + 0.031 + 0.019$$
$$\fallingdotseq \underline{0.115\ W}$$

CH1 (Synchronous rectification side)

Input voltage $V_{IN\,(Max)}$ = 15 V, output voltage $V_O$ = 3.3 V, drain current $I_D$ = 3 A, oscillation frequency $f_{OSC}$ = 300 kHz, L = 22 µH, drain-source on resistance $R_{DS\,(ON)} \fallingdotseq 28\ m\Omega$, tr = 16.4 ns, tf = 5.2 ns.

Drain current (Max) : $I_{D\,(Max)}$

$$I_{D\,(Max)} = I_O + \frac{V_O}{2L} toff$$
$$= 3 + \frac{3.3}{2 \times 22 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times (1-0.22)$$
$$\fallingdotseq \underline{3.20\ (A)}$$

Drain current (Min) : $I_{D\,(Min)}$

$$I_{D\,(Min)} = I_O - \frac{V_O}{2L} toff$$
$$= 3 - \frac{3.3}{2 \times 22 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times (1-0.22)$$
$$\fallingdotseq \underline{2.80\ (A)}$$

$$P_{C2} = I_D^2 \times R_{DS}(ON) \times Duty_{(OFF)}$$
$$= 3^2 \times 0.028 \times (1-0.22)$$
$$\fallingdotseq \underline{0.197\ W}$$

$$P_{S2}(ON) = \frac{V_D(Max) \times I_D \times tr \times f_{OSC}}{6}$$
$$= \frac{15 \times 3 \times 16.4 \times 10^{-9} \times 300 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.037\ W}$$

$$P_{S2}(OFF) = \frac{V_D(Max) \times I_D(Max) \times tf \times f_{OSC}}{6}$$
$$= \frac{15 \times 3.2 \times 5.2 \times 10^{-9} \times 300 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.012\ W}$$

$$P_{T2} = P_{C2} + P_{S2}(ON) + P_{S2}(OFF)$$
$$\fallingdotseq 0.197 + 0.037 + 0.012$$
$$\fallingdotseq \underline{0.246\ W}$$

$$P_T = P_{T1} + P_{T2}$$
$$\fallingdotseq 0.115 + 0.246$$
$$\fallingdotseq \underline{0.361\ W}$$

The above power dissipation figures for the IRF7901D1 are satisfied with ample margin at 2W (Ta = +100 °C) .

CH2 (Main side)

Input voltage $V_{IN}$ (Max) = 15 V, output voltage $V_O$ = 5 V, drain current $I_D$ = 3 A, Oscillation frequency $f_{OSC}$ = 300 kHz, L = 22 µH, drain-source on resistance $R_{DS}$ (ON) ≒ 33 mΩ, tr = 13.8 ns, tf = 8 ns.

Drain current (Max) : $I_D$ (Max)

$$I_D\,(Max) = I_O + \frac{V_{IN}\,(Max) - V_O}{2L}\,ton$$

$$= 3 + \frac{15-5}{2 \times 22 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.33$$

$$\fallingdotseq \underline{3.25\ (A)}$$

Drain current (Min) : $I_D$ (Min)

$$I_D\,(Min) = I_O + \frac{V_{IN}\,(Max) - V_O}{2L}\,ton$$

$$= 3 - \frac{15-5}{2 \times 22 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.33$$

$$\fallingdotseq \underline{2.75\ (A)}$$

$$P_{C1} = I_D^2 \times R_{DS}\,(ON) \times Duty_{(ON)}$$

$$= 3^2 \times 0.033 \times 0.33$$

$$\fallingdotseq \underline{0.098\ W}$$

$$P_{S1}\,(ON) = \frac{V_D\,(Max) \times I_D \times tr \times f_{OSC}}{6}$$

$$= \frac{15 \times 3 \times 13.8 \times 10^{-9} \times 300 \times 10^3}{6}$$

$$\fallingdotseq \underline{0.031\ W}$$

$$P_{S1}\,(OFF) = \frac{V_D\,(Max) \times I_D\,(Max) \times tf \times f_{OSC}}{6}$$

$$= \frac{15 \times 3.25 \times 8 \times 10^{-9} \times 300 \times 10^3}{6}$$

$$\fallingdotseq \underline{0.020\ W}$$

$$P_{T1} = P_{C1} + P_{S1}\,(ON) + P_{S1}\,(OFF)$$

$$\fallingdotseq 0.098 + 0.031 + 0.020$$

$$\fallingdotseq \underline{0.149\ W}$$

CH2 (Synchronous rectification side)

Input voltage $V_{IN}$ (Max) = 15 V, output voltage $V_O$ = 5 V, drain current $I_D$ = 3 A, Oscillation frequency $f_{OSC}$ = 300 kHz, L = 22 µH, drain-source on resistance $R_{DS}$ (ON) ≒ 28 mΩ, tr = 16.4 ns, tf = 5.2 ns.

Drain current (Max) : $I_D$ (Max)

$$I_D\,(Max) = I_O + \frac{V_O}{2L}\,toff$$

$$= 3 + \frac{5}{2 \times 22 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times (1-0.33)$$

$$\fallingdotseq \underline{3.25\ (A)}$$

$$I_D\,(Min) = I_O - \frac{V_O}{2L}\,toff$$

$$= 3 - \frac{5}{2 \times 22 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times (1-0.33)$$

$$\fallingdotseq \underline{2.75\ (A)}$$

$$P_{C2} = I_D^2 \times R_{DS}\,(ON) \times Duty\,(OFF)$$

$$= 3^2 \times 0.028 \times (1-0.33)$$

$$\fallingdotseq \underline{0.169\ W}$$

$$P_{S2}\,(ON) = \frac{V_D\,(Max) \times I_D \times tr \times f_{OSC}}{6}$$

$$= \frac{15 \times 3 \times 16.4 \times 10^{-9} \times 300 \times 10^3}{6}$$

$$\fallingdotseq \underline{0.037\ W}$$

$$P_{S2}\,(OFF) = \frac{V_D\,(Max) \times I_D\,(Max) \times tf \times f_{OSC}}{6}$$

$$= \frac{15 \times 3.25 \times 5.2 \times 10^{-9} \times 300 \times 10^3}{6}$$

$$\fallingdotseq \underline{0.013\ W}$$

$$P_{T2} = P_{C2} + P_{S2}\,(ON) + P_{S2}\,(OFF)$$

$$\fallingdotseq 0.169 + 0.037 + 0.013$$

$$\fallingdotseq \underline{0.219\ W}$$

$$P_T = P_{T1} + P_{T2}\,(OFF)$$

$$\fallingdotseq 0.149 + 0.219$$

$$\fallingdotseq \underline{0.368\ W}$$

The above power dissipation figures for the IRF7901D1 are satisfied with ample margin at 2W (Ta = +100 °C) .

**• Inductors**

In selecting inductors, it is of course essential not to apply more current than the rated capacity of the inductor, but also to note that the lower limit for ripple current is a critical point that if reached will cause discontinuous operation and a considerable drop in efficiency. This can be prevented by choosing a higher inductance value, which will enable continuous operation under light loads. Note that if the inductance value is too high, however, direct current resistance (DCR) is increased and this will also reduce efficiency. The inductance must be set at the point where efficiency is greatest.
Note also that the DC superimposition characteristics become worse as the load current value approaches the rated current value of the inductor, so that the inductance value is reduced and ripple current increases, causing loss of efficiency. The selection of rated current value and inductance value will vary depending on where the point of peak efficiency lies with respect to load current.
Inductance values are determined by the following formulas.

The L value for all load current condition is set so that the peak to peak value of the ripple current is 1/2 the load current or less.

Inductance value : L

$$L \geq \frac{2\,(V_{IN}-V_O)}{I_O}\ ton$$

Example:

CH1

$$L \geq \frac{2\,(V_{IN\,(Max)}-V_O)}{I_O}\ ton$$

$$\geq \frac{2\times\,(15-3.3)}{3}\times\frac{1}{300\times10^3}\times\ 0.22$$

$$\geq\ \underline{5.7\ \mu H}$$

CH2

$$L \geq \frac{2\,(V_{IN\,(Max)}-V_O)}{I_O}\ ton$$

$$\geq \frac{2\times\,(15-5)}{3}\times\frac{1}{300\times10^3}\times\ 0.33$$

$$\geq\ \underline{7.3\ \mu H}$$

Inductance values derived from the above formulas are values that provide sufficient margin for continuous operation at maximum load current, but at which continuous operation is not possible at light loads. It is therefore necessary to determine the load level at which continuous operation becomes possible. In this application, the TDK SLF12565T-220M3R5 is used. At 22 µH, the load current value under continuous operating conditions is determined by the following formula.

Load current value under continuous operating conditions : $I_O$

$$I_O \geq \frac{V_O}{2L}\ toff$$

Example : Using the SLF12565T-220M3R5
22 µH (allowable tolerance ±20%) , rated current = 3.5 A

CH1

$$I_O \geq \frac{V_O}{2L} \text{ toff}$$

$$\geq \frac{3.3}{2 \times 22 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times (1-0.22)$$

$$\geq \underline{195 \text{ mA}}$$

CH2

$$I_O \geq \frac{V_O}{2L} \text{ toff}$$

$$\geq \frac{5}{2 \times 22 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times (1-0.33)$$

$$\geq \underline{254 \text{ mA}}$$

To determine whether the current through the inductor is within rated values, it is necessary to determine the peak value of the ripple current as well as the peak-to-peak values of the ripple current that affect the output ripple voltage. The peak value and peak-to-peak value of the ripple current can be determined by the following formulas.

Peak value : $I_L$

$$I_L \geq I_O + \frac{V_{IN} - V_O}{2L} \text{ ton}$$

Peak-to-peak value : $\Delta I_L$

$$\Delta I_L = \frac{V_{IN} - V_O}{L} \text{ton}$$

Example: Using the SLF12565T-220M3R5

22 µH (allowable tolerance ±20%) , rated current = 3.5 A

Peak value

CH1

$$I_L \geq I_O + \frac{V_{IN\,(Max)} - V_O}{2L} \text{ ton}$$

$$\geq 3 + \frac{15-3.3}{2 \times 22 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.22$$

$$\geq \underline{3.20 \text{ A}}$$

CH2

$$I_L \geq I_O + \frac{V_{IN\,(Max)} - V_O}{2L} \text{ ton}$$

$$\geq 3 + \frac{15-5}{2 \times 22 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.33$$

$$\geq \underline{3.25 \text{ A}}$$

Peak-to-peak value:

CH1

$$\Delta I_L = \frac{V_{IN}\,(Min) - V_O}{L}\ ton$$

$$= \frac{15-3.3}{22 \times 10^{-6}} \times \frac{1}{300 \times 10^{3}} \times 0.22$$

$$\fallingdotseq \underline{0.39\ A}$$

CH2

$$\Delta I_L = \frac{V_{IN}\,(Max) - V_O}{L}\ ton$$

$$= \frac{15-5}{22 \times 10^{-6}} \times \frac{1}{300 \times 10^{3}} \times 0.33$$

$$\fallingdotseq \underline{0.5\ A}$$

**• Smoothing Capacitor**

The smoothing capacitor is an indispensable element for reducing ripple voltage in output. In selecting a smoothing capacitor it is essential to consider equivalent series resistance (ESR) and allowable ripple current. Higher ESR means higher ripple voltage, so that to reduce ripple voltage it is necessary to select a capacitor with low ESR. However, the use of a capacitor with low ESR can have substantial effects on loop phase characteristics, and therefore requires attention to system stability. Care should also be taken to use a capacity with sufficient margin for allowable ripple current. This application uses the 6SVP150M (OS-CON™ : SANYO) . The ESR, capacitance value, and ripple current can be calculated from the following formulas.

Equivalent Series Resistance : ESR

$$ESR \leq \frac{\Delta V_O}{\Delta I_L} - \frac{1}{2\pi f C_L}$$

Capacitance value : $C_L$

$$C_L \geq \frac{\Delta I_L}{2\pi f\,(\Delta V_O - \Delta I_L \times ESR)}$$

Ripple current : $IC_{Lrms}$

$$IC_{Lrms} \geq \frac{(V_{IN} - V_O)}{2\sqrt{3}L}\ ton$$

Example: Using the 6SVP150M
Rated voltage = 6.3 V, ESR = 35 mΩ, maximum allowable ripple current = 2.35 Arms

Equivalent series resistance

CH1

$$ESR \leq \frac{\Delta V_O}{\Delta I_L} - \frac{1}{2\pi f C_L}$$

$$\leq \frac{0.033}{0.39} - \frac{1}{2\pi \times 300 \times 10^{3} \times 150 \times 10^{-6}}$$

$$\leq \underline{81.1\ m\Omega}$$

CH2

$$ESR \leq \frac{\Delta V_O}{\Delta I_L} - \frac{1}{2\pi f C_L}$$

$$\leq \frac{0.05}{0.5} - \frac{1}{2\pi \times 300 \times 10^3 \times 150 \times 10^{-6}}$$

$$\leq \underline{96.5\ m\Omega}$$

Capacitance value

CH1

$$C_L \geq \frac{\Delta I_L}{2\pi f\ (\Delta V_O - \Delta I_L \times ESR)}$$

$$\geq \frac{0.39}{2\pi \times 300 \times 10^3 \times\ (0.033 - 0.39 \times 0.035)}$$

$$\geq \underline{10.7\ \mu F}$$

CH2

$$C_L \geq \frac{\Delta I_L}{2\pi f\ (\Delta V_O - \Delta I_L \times ESR)}$$

$$\geq \frac{0.5}{2\pi \times 300 \times 10^3 \times\ (0.05 - 0.5 \times 0.035)}$$

$$\geq \underline{8.2\ \mu F}$$

Ripple current

CH1

$$I_{CLrms} \geq \frac{(V_{IN\ (Max)} - V_O)}{2\sqrt{3}L}\ ton$$

$$\geq \frac{(15 - 3.3)\ \times 0.22}{2\sqrt{3}L \times 22 \times 10^{-6} \times 300 \times 10^3}$$

$$\geq \underline{112.6\ mArms}$$

CH2

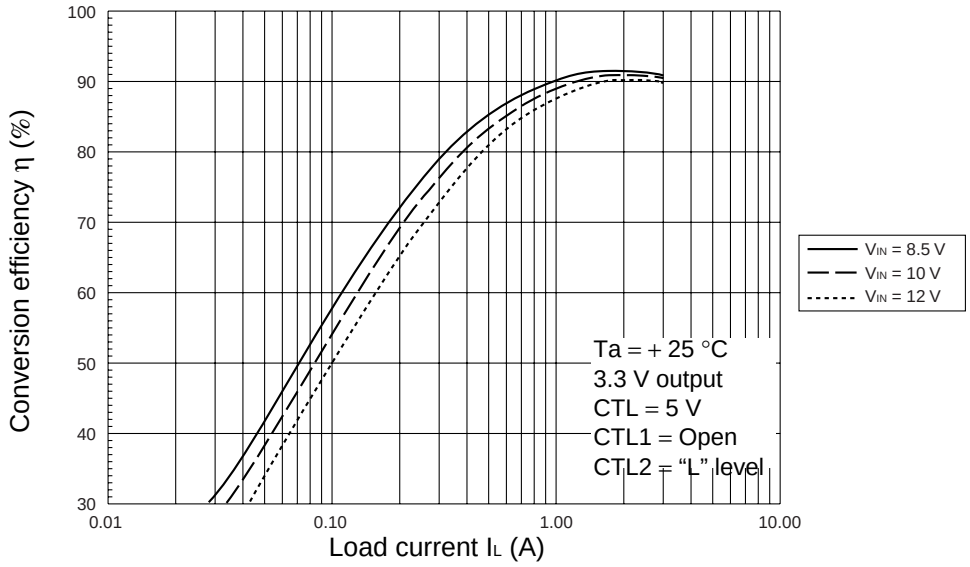
$$I_{CLrms} \geq \frac{(V_{IN\ (Max)} - V_O)\ ton}{2\sqrt{3}L}$$

$$\geq \frac{(15 - 5)\ \times 0.33}{2\sqrt{3}L \times 22 \times 10^{-6} \times 300 \times 10^3}$$

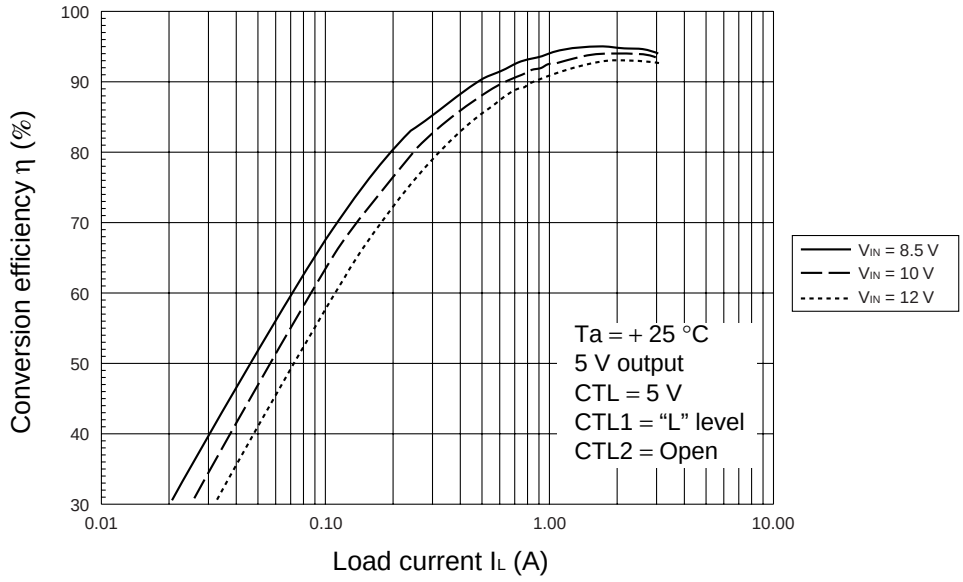
$$\geq \underline{114.3\ mArms}$$

## ■ REFERENCE DATA

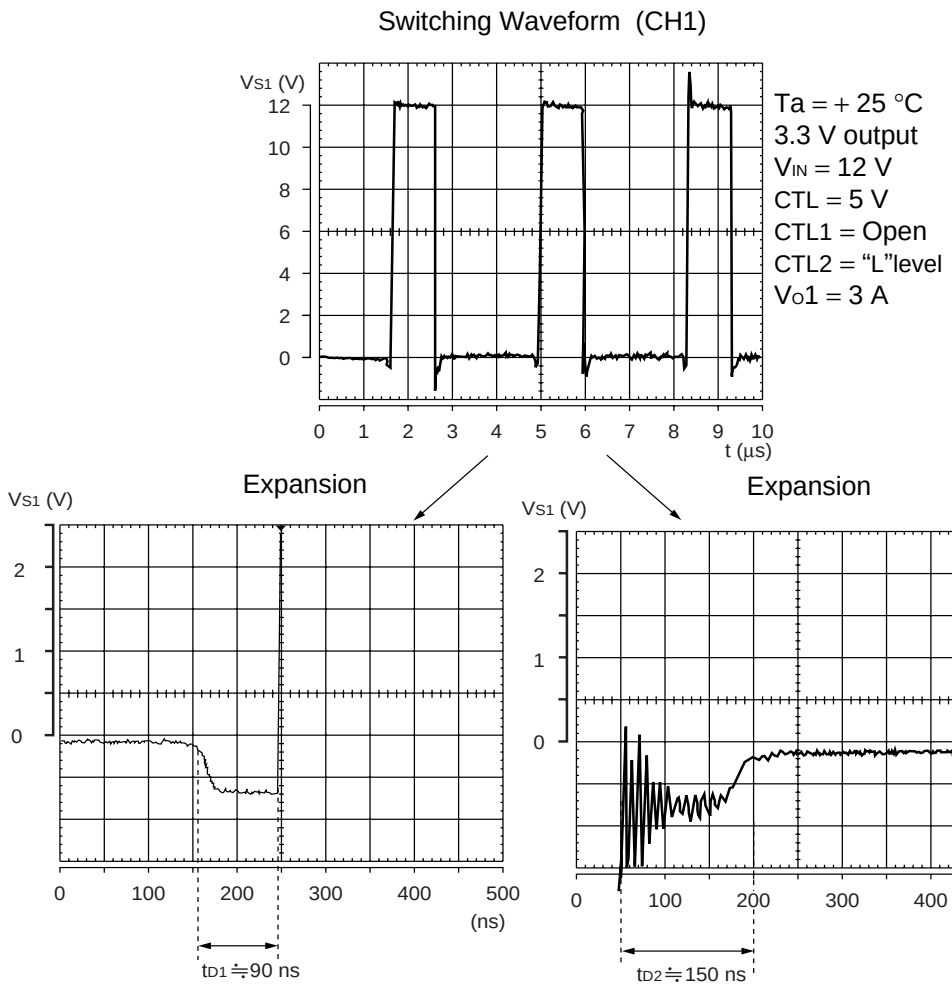
Conversion Efficiency vs. Load Current (CH1)



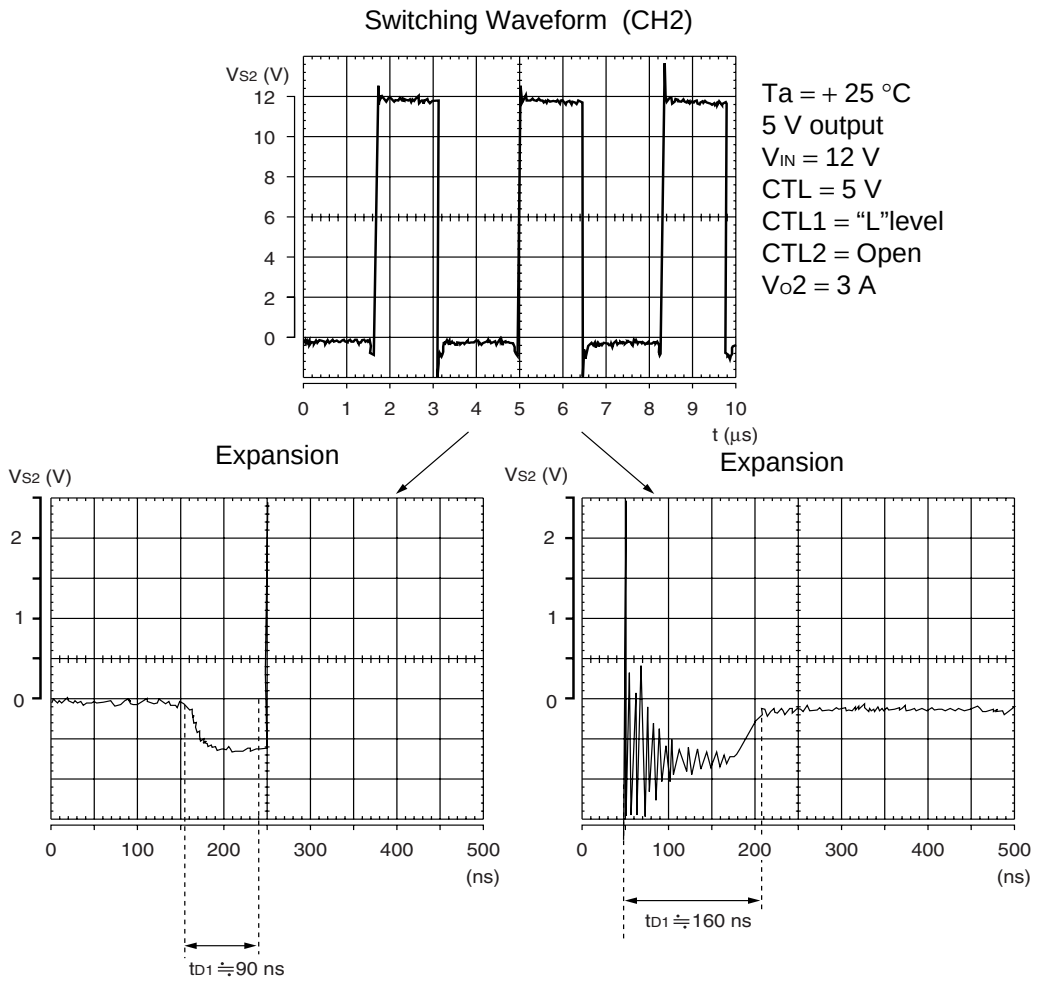

Conversion Efficiency vs. Load Current (CH2)




*(Continued)*


Switching Waveform (CH1)
VS1 (V)
12
10
8
6
4
2
0
0 1 2 3 4 5 6 7 8 9 10
t (µs)
Ta = + 25 °C
3.3 V output
VIN = 12 V
CTL = 5 V
CTL1 = Open
CTL2 = "L"level
VO1 = 3 A
Expansion
Expansion
VS1 (V)
2
1
0
0 100 200 300 400 500
(ns)
tD1 ≒ 90 ns
VS1 (V)
2
1
0
0 100 200 300 400 500
(ns)
tD2 ≒ 150 ns

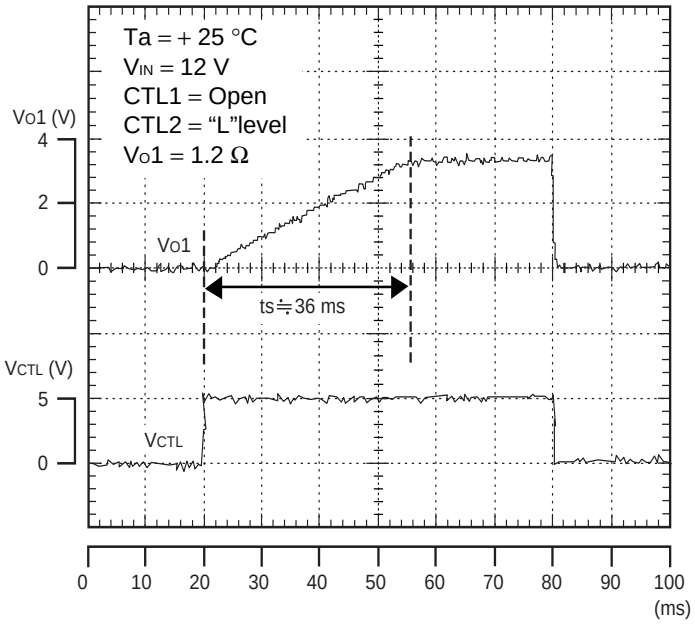
*(Continued)*


Switching Waveform (CH2)
VS2 (V)
12
10
8
6
4
2
0
0 1 2 3 4 5 6 7 8 9 10
t (µs)
Ta = + 25 °C
5 V output
VIN = 12 V
CTL = 5 V
CTL1 = "L"level
CTL2 = Open
VO2 = 3 A
Expansion
Expansion
VS2 (V)
2
1
0
0 100 200 300 400 500
(ns)
tD1 ≒90 ns
VS2 (V)
2
1
0
0 100 200 300 400 500
(ns)
tD1 ≒160 ns

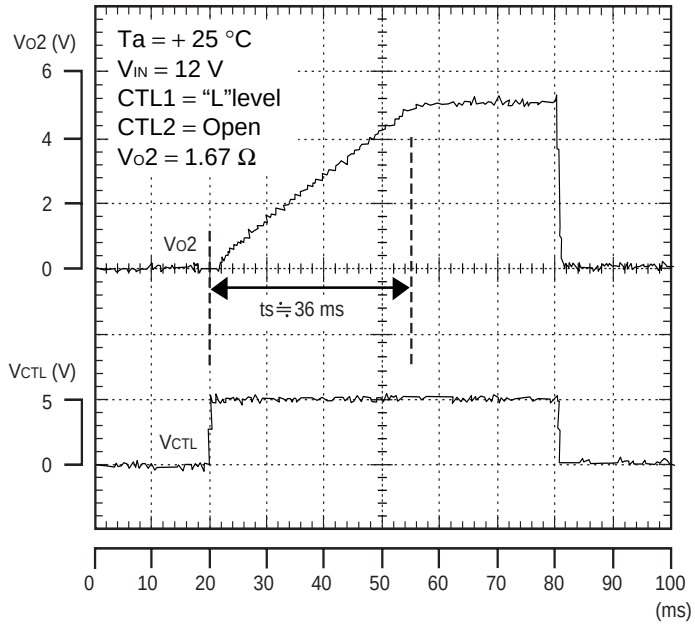
*(Continued)*

*(Continued)*

Soft-start Operating Waveform (CH1)




Soft-start Operating Waveform (CH2)



## ■ NOTES ON USE

- Take account of common impedance when designing the earth line on a printed wiring board.

- Take measures against static electricity.
  - For semiconductors, use antistatic or conductive containers.
  - When storing or carrying a printed circuit board after chip mounting, put it in a conductive bag or container.
  - The work table, tools, and measuring instruments must be grounded.
  - The worker must put on a grounding device containing 250 kΩ to 1 MΩ resistors in series.

- Do not apply a negative voltage.
  - Applying a negative voltage of −0.3 V or less to an LSI may generate a parasitic transistor, resulting in malfunction.

## ■ PRECAUTIONS ON HANDLING THIS PRODUCT

This product has obtained US patents for patent numbers of 6,147,477.

## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB39A106PFT-❑❑❑E1 | 30-pin plastic TSSOP<br>(FPT-30P-M04) | Lead Free version |

## ■ EV BOARD ORDERING INFORMATION

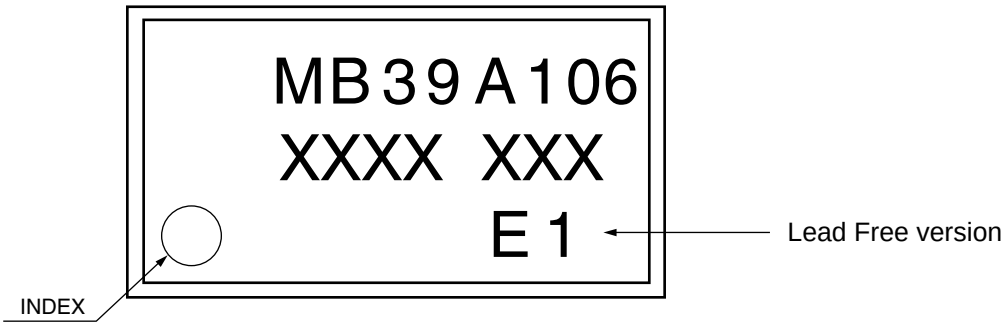
| EV board part No. | EV board version No. | Remarks |
|---|---|---|
| MB39A106EVB | Board Rev. 2.0 | TSSOP-30P |

## ■ RoHS COMPLIANCE INFORMATION OF LEAD (Pb) FREE VERSION

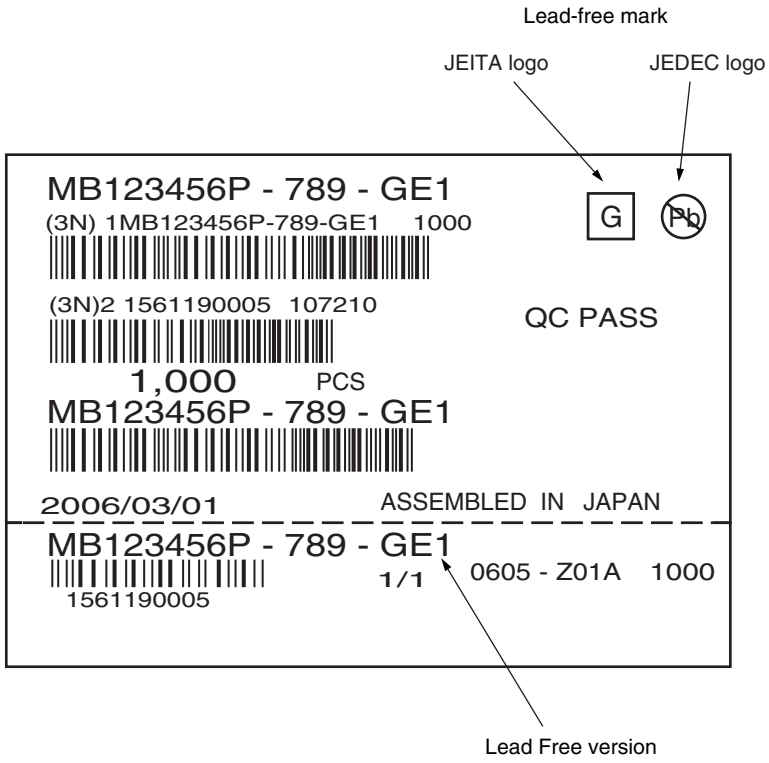
The LSI products of Fujitsu with “E1” are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB) , and polybrominated diphenyl ethers (PBDE) .

The product that conforms to this standard is added “E1” at the end of the part number.

## ■ MARKING FORMAT (LEAD FREE VERSION)



## ■ LABELING SAMPLE (LEAD FREE VERSION)



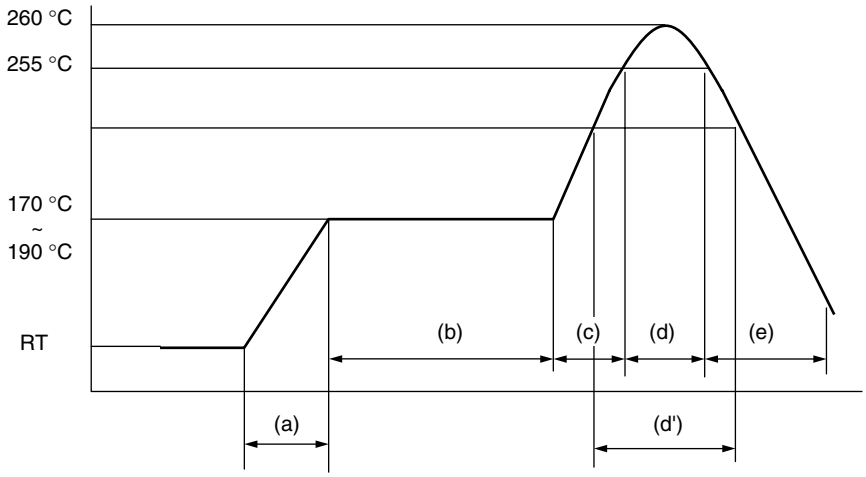
## ■ MB39A106PFT-❑❑❑E1
## RECOMMENDED CONDITIONS OF MOISTURE SENSITIVITY LEVEL

| Item | Condition | |
|---|---|---|
| Mounting Method | IR (infrared reflow) , Manual soldering (partial heating method) | |
| Mounting times | 2 times | |
| Storage period | Before opening | Please use it within two years after Manufacture. |
| | From opening to the 2nd reflow | Less than 8 days |
| | When the storage period after opening was exceeded | Please processes within 8 days after baking (125 °C, 24H) |
| Storage conditions | 5 °C to 30 °C, 70%RH or less (the lowest possible humidity) | |

**[Temperature Profile for FJ Standard IR Reflow]**

**(1) IR (infrared reflow)**

H rank : 260 °C Max



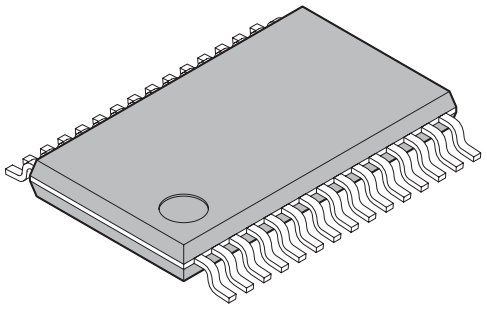

(a) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(b) Preliminary heating : Temperature 170 °C to 190 °C, 60 s to 180 s
(c) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(d) Actual heating : Temperature 260 °C Max; 255 °C or more, 10 s or less
(d') : Temperature 230 °C or more, 40 s or less
or
Temperature 225 °C or more, 60 s or less
or
Temperature 220 °C or more, 80 s or less
(e) Cooling : Natural cooling or forced cooling

Note : Temperature : the top of the package body

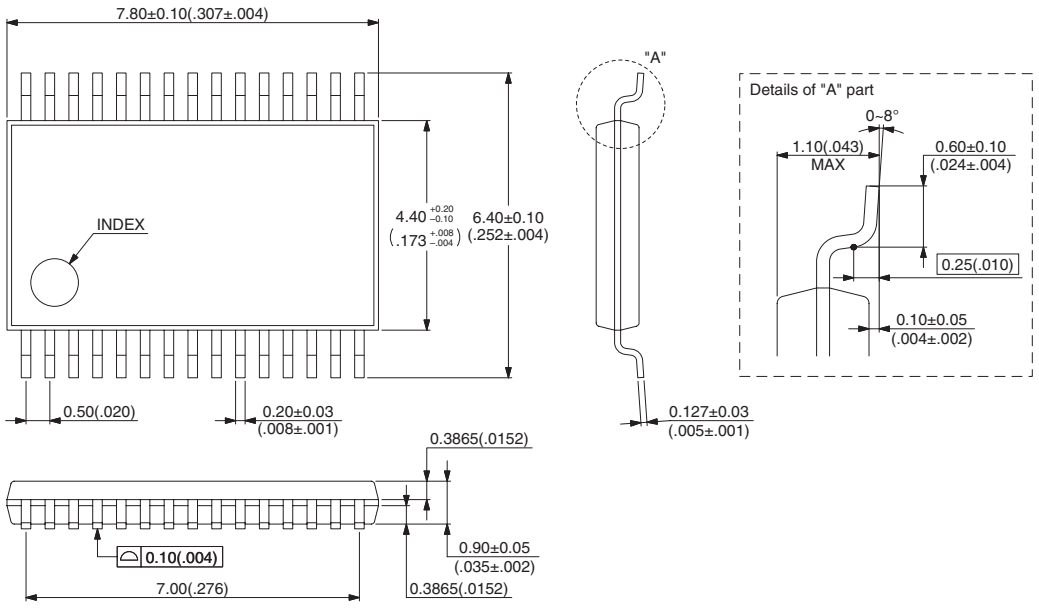
**(2) Manual soldering (partial heating method)**

Conditions : Temperature 400 °C Max
Times : 5 s max/pin

## ■ PACKAGE DIMENSION

| 30-pin plastic TSSOP | | |
|---|---|---|
|  | Lead pitch | 0.50 mm |
| | Package width × package length | 4.40 × 7.80 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.10 mm MAX |
| | | |
| (FPT-30P-M04) | | |

30-pin plastic TSSOP
(FPT-30P-M04)






Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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