PRELIMINARY

256x16 & 512x16 Parallel-to-Serial FIFOs

FEATURES

- 25ns parallel port access time
- 50MHz serial output port shift rate
- Easily expandable in both word width and depth
- Asynchronous and simultaneous read/write operation
- Five memory status flags: Empty, Full, Half-full, Almost-empty and Almost-full
- Least Significant or Most Significant bit first read selectable for two sided printing
- Low power, power down capability
- Dual port RAM architecture with zero fall through time
- Available in 28-pin 300mil plastic DIP or 330mil SOIC gull wing

DESCRIPTION

The MS72105 and MS72115 are high-speed, low power 16-bit parallel-to-serial FIFOs. These FIFOs are well suited for any serial date output buffering such as are found in laser printers, FAX machines, local area networks, video frame buffers, disk and tape controllers. They are fully asynchronous and allow simultaneous read and write operations.

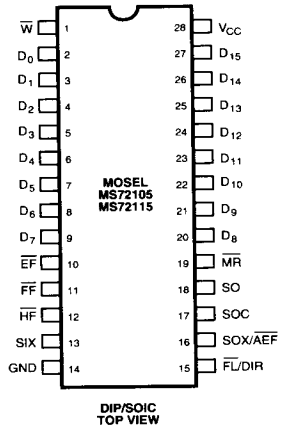
Wider and deeper FIFOs can be assembled using multiple devices. MOSEL's on-chip expansion logic (SIX, SOX & $\overline{FL}$/DIR) makes this possible and requires no external components. The serial output is clocked out by signalling the serial output clock pin (SOC) and data is available on the serial out pin (SO). The Least Significant or Most Significant bit can be read first by programming the DIR pin after Reset.

The device has five flags: empty, full, half full, almost-empty and almost-full. The empty and full flags prevent data underflow or overflow. The empty, full and half-full flags are available in both single device and expansion configurations. The almost-empty and almost-full are only available in the single device configuration.

The MS72105 and MS72115 designs are based on a self addressing dual port RAM architecture. This allows for a zero fall through delay and quick flag logic response. The MS72105 and MS72115 are fabricated on MOSEL's full CMOS process.

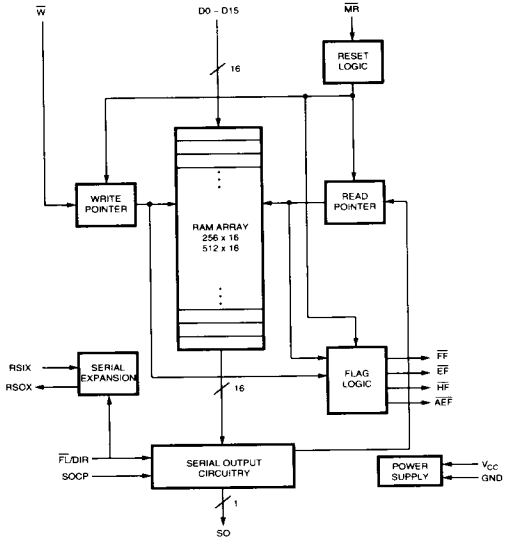
6

PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

D_0 - D_{15} Inputs

Data inputs for 16-bit wide data.

$\overline{MR}$ Master Reset

When $\overline{MR}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{FF}$ and $\overline{HF}$ go HIGH. $\overline{EF}$ and $\overline{AEF}$ go LOW. A master reset is required before an initial WRITE after power-up. $\overline{W}$ must be high during the $\overline{MR}$ cycle. Also the First Load pin ($\overline{FL}$/) is progammed only during Reset.

$\overline{W}$ Write

A write cycle is initiated on the falling edge of WRITE if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation.

SOC Serial Output Clock

A serial bit read cycle is initiated on the rising edge of SOC if the Empty Flag ($\overline{EF}$) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOC pins are tied together.

$\overline{FL}$/DIR First Load/Direction

This is a dual purpose input used in the width and depth expansion configurations. The First Load ($\overline{FL}$) function is programmed only during Master Reset ($\overline{MR}$) and a LOW on $\overline{FL}$ indicates the first device to be loaded with a byte of data. All other devices should be programmed HIGH. The Direction (DIR) function is programmed during operation after MASTER Reset and tells the device whether to read out the Least Significant or Most Significant bit first.

SIX Read Serial in Expansion

In the single device configuration, SIX is set HIGH. In depth expansion or daisy chain expansion. SIX is connected to SOX (expansion out) of the previous device.

SO Serial Output

Serial data is output on the Serial Output (SO) pin. Data is clocked out LSB or MSB depending on the Direction pin programming. During Expansion the SO pins are tied together.

$\overline{FF}$ Full Flag

When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full.

$\overline{EF}$ Empty Flag

When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty.

$\overline{HF}$ Half Full Flag

When $\overline{HF}$ is LOW, the device is more than half full. When $\overline{HF}$ is HIGH, the device is empty to half full.

SOX/$\overline{AEF}$ Serial Out Expansion, Almost Empty, Almost Full Flag

This is a dual purpose output. In the single device configuration (RSIX HIGH), this is an $\overline{AEF}$ output pin. When $\overline{AEF}$ is LOW, the device is empty to 1/8 full - 1 or 7/8 full + 1 to full. When $\overline{AEF}$ is HIGH, the device is 1/8 full up to 7/8 full. In the Expansion configuration (SOX connected to SIX of the next device) a pulse is sent from SOX to SIX to coordinate the width, depth or daisy chain expansion.

V_{cc} Power Supply

Single power supply of 5V.

GND Ground

Single ground of 0V.

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	COMMERCIAL	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	-	-	V
V_{IL}(1)	Input Low Voltage	-	-	0.8	V

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	MS72105 MS72115 MIN.	TYP.	MIAX.	UNITS
I_{IL} (1)	Input Leakage Current (Any Input)	–1	-	1	µA
I_{OL} (2)	Output Leakage Current	–10	-	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = –2mA (5)	-	-	-	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA (6)	-	-	0.4	V
I_{CC1} (3)	Power Supply Current	-	90	140	mA
I_{CC2} (3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = FL/DIR = V_H)	-	8	12	mA
I_{CC3} (L)(3, 4)	Power Down Current	-	-	8	mA

1. Measurements with $0.4 \le V_{IN} \le V_{OUT}$.
2. $\overline{MR} \le V_{IL}$, $0.4 \le V_{OUT} \le V_{CC}$
3. I_{CC} measurements are made with outputs open.
4. $\overline{MR}$ = $\overline{FL}$/DIR = $\overline{W}$ = $\overline{SOC}$ = V_{CC} –0.2V; all other inputs ≥ V_{CC} –0.2V or ≤ 0.2V.
5. For SO, I_{OUT} = –4mA
6. For SO, I_{OUT} = 16mA

STATUS FLAGS

NUMBER OF WORDS IN FIFO		$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
MS72105	MS72115				
0	0	H	L	H	L
1–31	1–63	H	L	H	H
32–128	64–256	H	H	H	H
129–224	257–448	H	H	L	H
225–255	449–511	H	L	L	H
256	512	L	L	L	H

AC ELECTRICAL CHARACTERISTICS (Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	MS72105 MS72115 25		MS72105 MS72115 50		MS72105 MS72115 80		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_S	Parallel Shift Frequency	-	22.2	-	15	-	10	MHz
t_{SOCP}	Serial Shift Frequency	-	50	-	40	-	28	MHz
t_{WC}	Write Cycle Time	35	-	65	-	100	-	ns
t_{WPW}	Write Pulse Width	25	-	50	-	80	-	ns
t_{WR}	Write Recovery Time	10	-	15	-	20	-	ns
t_{DS}	Data Set-up Time	10	-	15	-	15	-	ns
t_{DH}	Data Hold Time	0	-	5	-	5	-	ns
t_{SOCP}	Serial Clock Cycle Time	20	-	25	-	35	-	ns
t_{SOCW}	Serial Clock Width High/Low	8	-	10	-	15	-	ns
t_{SOPD}	SOC Rising Edge to SO Valid Data	-	10	-	12	-	17	ns
t_{SOHZ}	SOC Rising Edge to SO at High Z[1]	3	10	3	12	3	17	ns
t_{SOLZ}	SOC Rising Edge to SO at Low Z[1]	3	10	3	12	3	17	ns
t_{WEF}	Write High to $\overline{EF}$ High	-	20	-	25	-	35	ns
t_{WFF}	Write Low to $\overline{FF}$ Low	-	30	-	40	-	50	ns
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	-	30	-	40	-	50	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ High	25	-	50	-	80	-	ns
t_{SOCEF}	SOC Rising Edge to $\overline{EF}$ Low	-	20	-	25	-	35	ns
t_{SOCFF}	SOC Rising Edge to $\overline{FF}$ High	-	30	-	40	-	50	ns
t_{SOCF}	SOC Rising Edge to Transitioning $\overline{HF}$, $\overline{AEF}$	-	30	-	40	-	50	ns
t_{REFSO}	SOC Delay After $\overline{EF}$ High	35	-	65	-	100	-	ns
t_{RSC}	Reset Cycle Time	35	-	65	-	100	-	ns
t_{RS}	Reset Pulse Width	25	-	50	-	80	-	ns
t_{RSS}	Reset Set-up Time	25	-	50	-	80	-	ns
t_{RSR}	Reset Recovery Time	10	-	15	-	20	-	ns
t_{FLS}	$\overline{FL}$ Set-up Time to $\overline{RS}$ Rising Edge	5	-	7	-	10	-	ns
t_{FLH}	$\overline{FL}$ Hold Time to $\overline{RS}$ Rising Edge	0	-	0	-	5	-	ns
t_{DIRS}	DIR Set-up Time to SOCPRising Edge	5	-	7	-	10	-	ns
t_{DIRH}	DIR Hold Time from SOC Rising Edge	0	-	0	-	5	-	ns
t_{SOXD1}	SOC Rising Edge to SOX Rising Edge	3	11	3	15	3	20	ns
t_{SOXD2}	SOC Rising Edge to SOX Falling Edge	3	11	3	15	3	20	ns
t_{SIXS}	SIX Set-up Time to SOC Rising Edge	5	-	7	-	10	-	ns
t_{SIXH}	SIX Hold Time from SOC Rising Edge	0	-	0	-	5	-	ns

1. Guaranteed by design minimum times, not tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

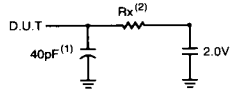


Figure A. Output Load

1. Includes jig and scope capacitances.
2. For SO, Rx = 100Ω. For all other outputs, Rx = 200Ω

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER (1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

1. This parameter is sampled and not 100% tested.

FUNCTIONAL DESCRIPTION

Parallel Data Input

The device must be reset before beginning operation so that all flags are set to location zero. In width or depth expansion the First Load pin ($\overline{FL}$) must be programmed to indicate the first device.

The data is written into the FIFO in parallel through the D_{0-15} input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full Flag ($\overline{FF}$) is already set, the write line is inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. The data is written to the RAM at the write pointer. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

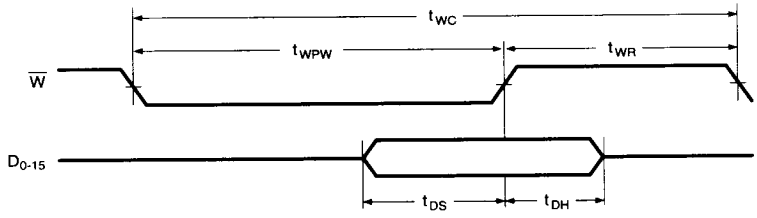


Figure 1. Write Operation

Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOC providing the Empty Flag ($\overline{EF}$) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOC.

The serial word is shifted out Least Significant Bit or Most Significant Bit first depending on the $\overline{FL}$/DIR level during operation. A LOW on DIR will cause the Least Significant Bit to be read out first. A HIGH on DIR will cause the Most Significant Bit to be read out first.

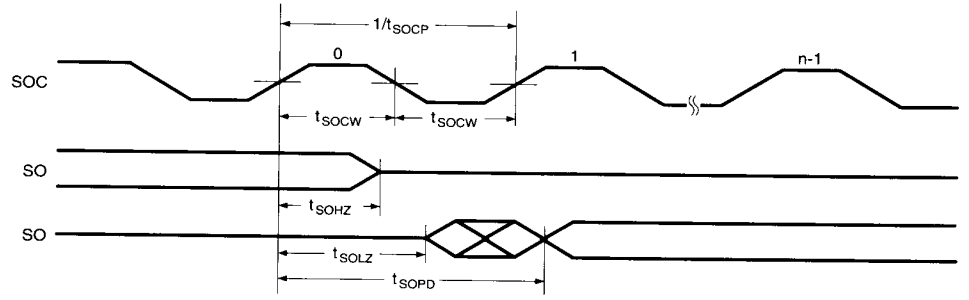


Figure 2. Read Operation

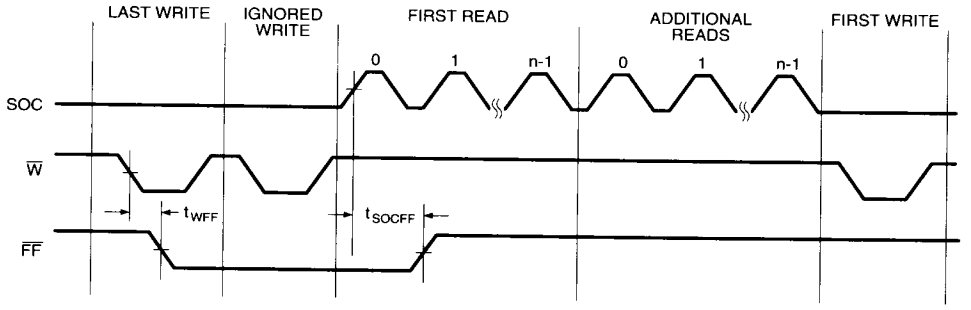


Figure 3. Full Flag from Last Write to First Read

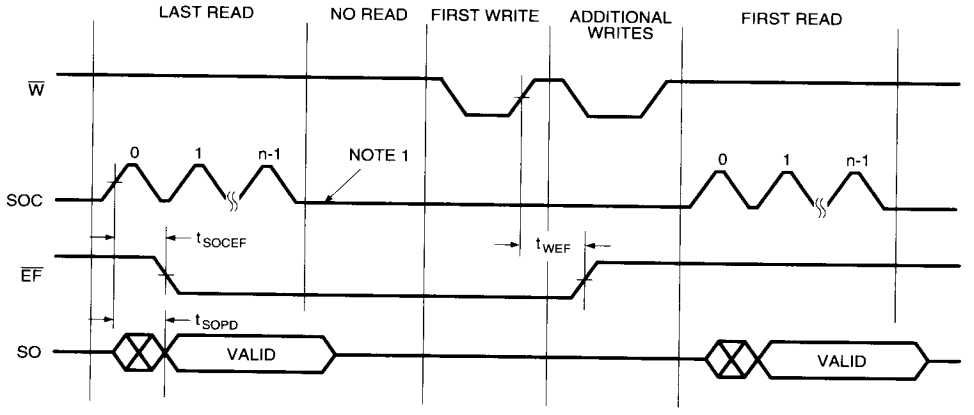


Figure 4. Empty Flag from Last Read to First Write

Note:
1. SOC should not be clocked until $\overline{EF}$ goes high.

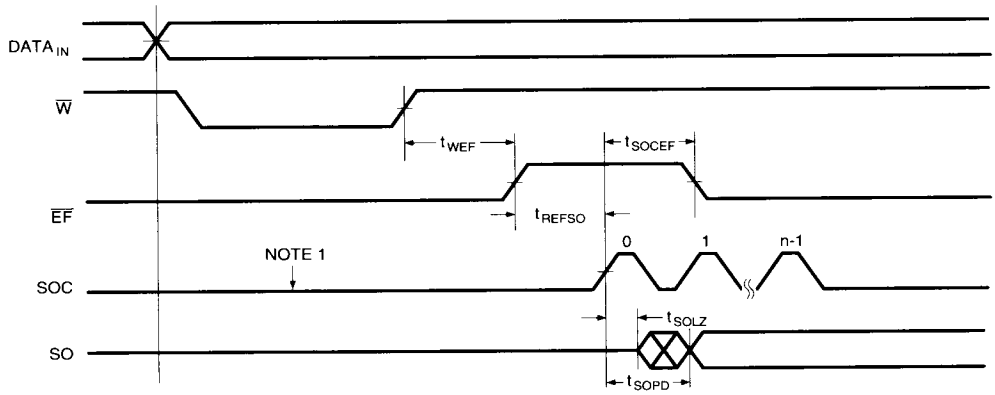


Figure 5. Empty Boundry Condition Timing

Note:
1. SOC should not be clocked until $\overline{EF}$ goes high.

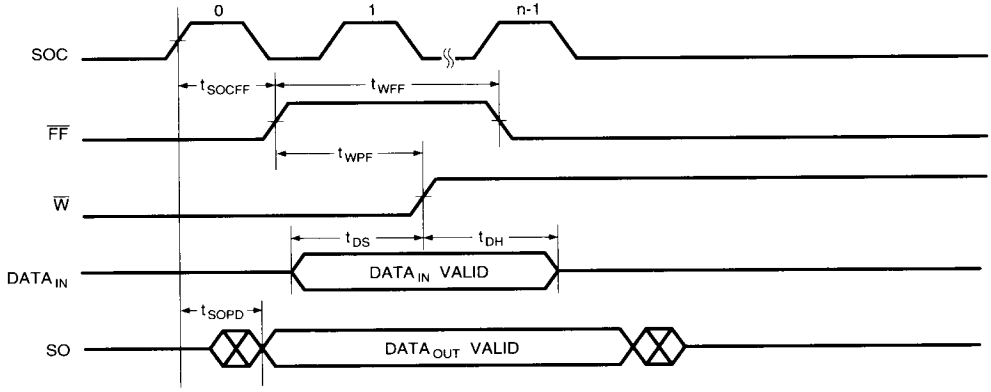


Figure 6. Full Boundary Condition Timing

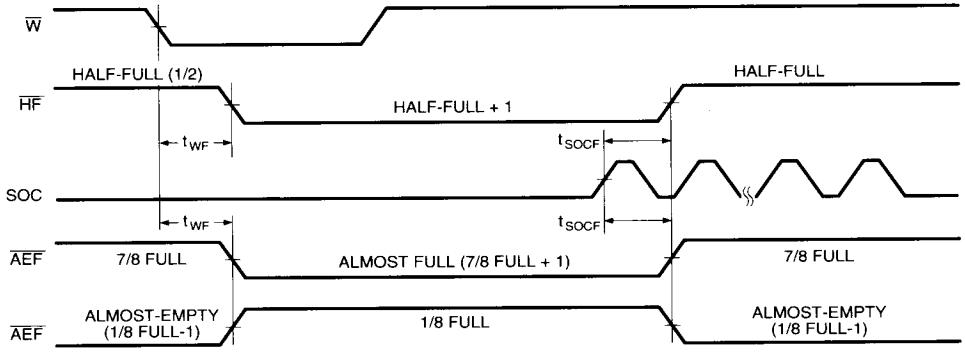


Figure 7. Half Full, Almost Full and Almost Empty Timings

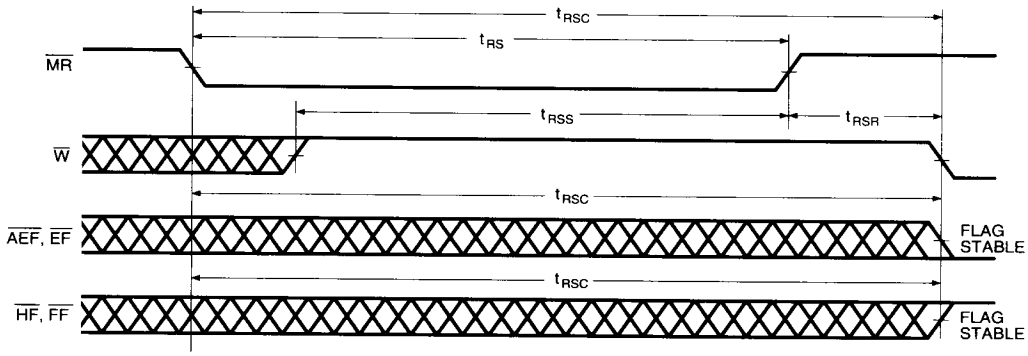


Figure 8. Master Reset

Note:
1. EF, FF, HF and AEF may change status during Master Reset, but flags will be valid at t_{RSC}.

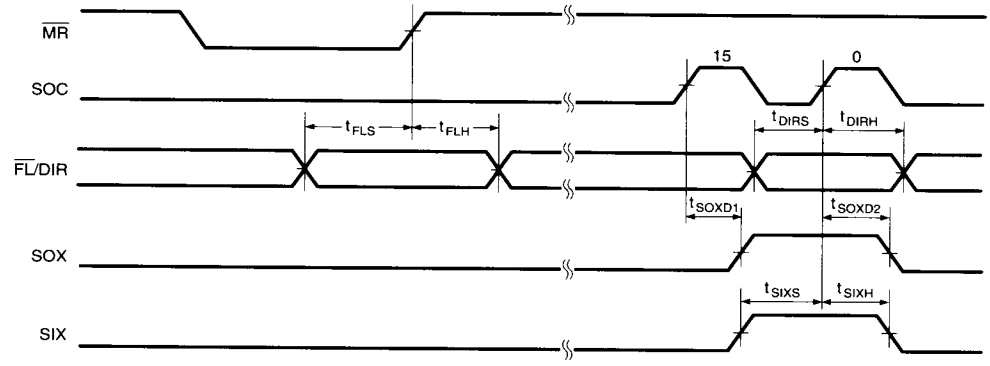


Figure 9. Serial Read Expansion

OPERATING CONFIGURATIONS

Single Device Mode

The device must be reset before beginning operation so that all flags are set to location zero. In the standalone case, the SIX line is tied HIGH and indicates single device operation to the device. The SOX/$\overline{AEF}$ pin defaults to $\overline{AEF}$ and outputs the Almost Empty and Almost Full Flag.

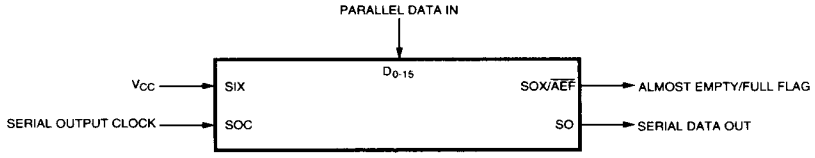


Figure 10. Single Device Configuration

TABLE 1: MASTER RESET AND FIRST LOAD TRUE TABLE– SINGLE DEVICE CONFIGURATION

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{MR}$	$\overline{FL}$	DIR	READ POINTER	WRITE POINTER	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	X	Location Zero	Location Zero	0	1	1
Read/Write	1	X	0, 1	Increment (1)	Increment (1)	X	X	X

1. Pointer will increment if appropriate flag is HIGH.

6

Width Expansion Mode

In the cascaded case, word widths of more than 16 bits can be achieved by using more than one device. By tying the SOX and SIX pins together as shown in Figure 11 and programming which is the Least Significant Device, a cascaded serial word is achieved. The Least Significant Device is programmed by a LOW on the $\overline{FL}$/DIR pin during reset. All other devices should be programmed HIGH on the $\overline{FL}$/DIR pin at reset.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit bus. NOTE: After reset, the level on the $\overline{FL}$/DIR pin decides if the Least Significant or Most Significant Bit is read first out of each device.

The three flag outputs, Empty ($\overline{EF}$), Half Full ($\overline{HF}$) and Full ($\overline{FF}$), should be taken from the Most Significant Device (in the example, FIFO #2). The Almost Empty and Almost Full Flag is not available due to using the SOX pin for expansion.

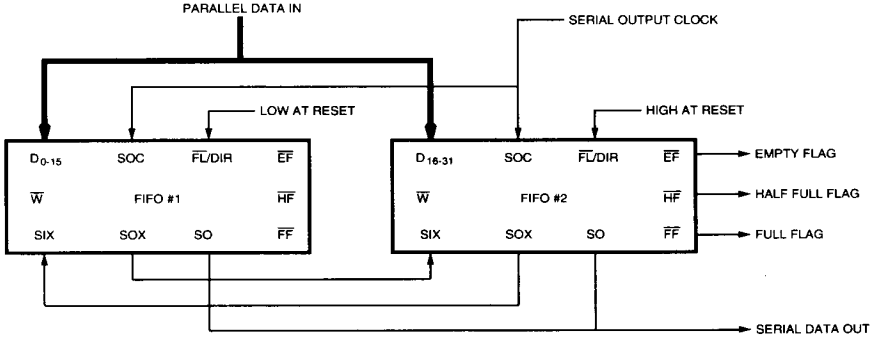


Figure 11. Width Expansion for 32-bit Parallel Data In

Depth Expansion (Daisy Chain) Mode

The MS72105/72115 can easily be adapted to applications where the requirements are for greater than 512 words. Figure 12 demonstrates Depth Expansion using three MS72115 and an Address Decoder. Any depth can be attained by adding additional devices. The Address Decoder is necessary to determine which FIFO to write data into. A byte of data should be written sequentially into each FIFO so that the SOX/SIX handshake can control reading out the data in the correct sequence. The MS72105/72115 operate in the Depth Expansion Mode when the following conditions are met:

1. The first device must be designated by programming $\overline{FL}$ LOW at Reset. All other devices to be programmed HIGH.
2. The Serial Out Expansion (SOX) of each device must be tied to the Serial In Expansion (SIX of the next device in the manner shown).
3. External logic is needed to generate composite Empty, Half Full and Full Flags. This requires the OR-ing of all $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ Flags.
4. The Almost Empty and Almost Full Flag is not available due to using the SOX pin for expansion.

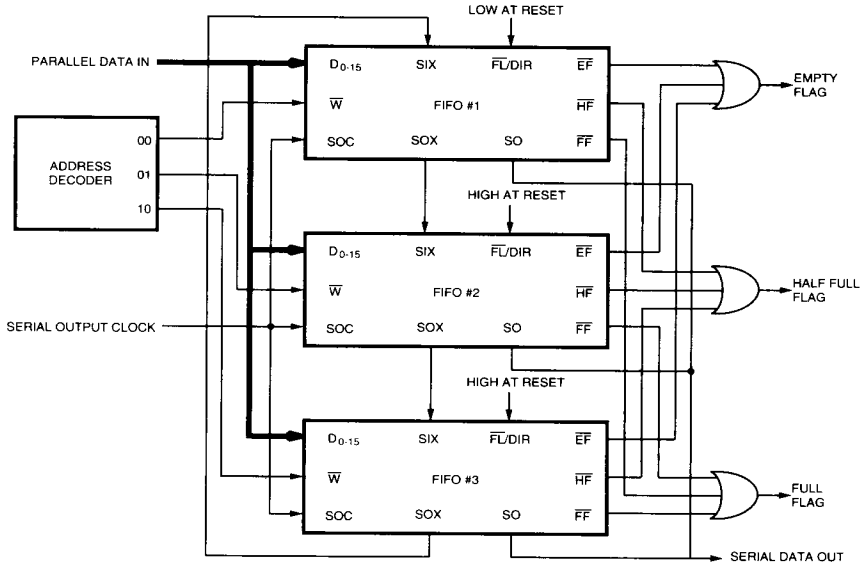


Figure 12. A 1536 x 16 Parallel-to-Serial FIFO using the MS72115

TABLE 2: MASTER RESET AND FIRST LOAD TRUE TABLE– WIDTH/DEPTH COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{MR}$	$\overline{FL}$	$\overline{DIR}$	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{HF}$, $\overline{FF}$
Reset-First Device	0	0	X	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	X	Location Zero	Location Zero	0	1
Read/Write	1	X	0, 1	X	X	X	X

1. $\overline{MR}$ = Master Reset , $\overline{FL}$/DIR = First Load/Direction, $\overline{EF}$ = Empty Flag Output, $\overline{HF}$ = Half Full Flag Output, $\overline{FF}$ = Full Flag Output

Compound Expansion (Daisy Chain) Mode

The MS72105/72115 can be expanded in both depth and width as Figure 13 indicates:

1. The SOX-to-SIX expansion signals are wrapped around sequentially.
2. The write ($\overline{W}$) signal is expanded in width.
3. Flag signals are only taken from the Most Significant Devices.
4. The Least Significant device in the array must be programmed with a LOW on $\overline{FL}$/DIR during reset.

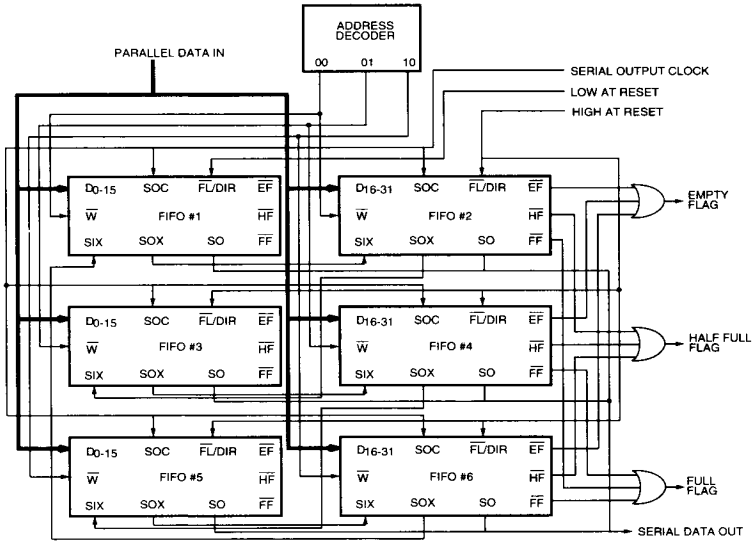


Figure 13. A 1536 x 32 Parallel-to-Serial FIFO using the MS72115

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
25	MS72105-25NC	P28-2	0°C to + 70°C
25	MS72115-25NC		0°C to + 70°C
25	MS72105-25FC	S28-2	0°C to + 70°C
25	MS72115-25FC		0°C to + 70°C
50	MS72105-50NC	P28-2	0°C to + 70°C
50	MS72115-50NC		0°C to + 70°C
50	MS72105-50FC	S28-2	0°C to + 70°C
50	MS72115-50FC		0°C to + 70°C
80	MS72105-80NC	P28-2	0°C to + 70°C
80	MS72115-80NC		0°C to + 70°C
80	MS72105-80FC	S28-2	0°C to + 70°C
80	MS72115-80FC		0°C to + 70°C