NJU26040 Series Data Sheet

■ General Description

The NJU26040 Series a Digital Signal Processor with built-in OTP (One Time Programmable).

By the DSP with built-in OTP, customization is possible from various sound technology.

The NJU26040 Series is suitable for TV, mini-component, speakers system and other audio products. This DSP can constitute a small system by combining a CODEC.

■ Package

NJU26040V

■ FEATURES

- 24bit Fixed-point Digital Signal Processing
- System Clock Frequency : Maximum 38MHz
- Digital Audio Interface : 3 Input ports / 3Output ports
- Digital Audio Format : I^2S 24bit, Left- justified, Right-justified, BCK : 32/64fs
- Master / Slave Mode : In Master mode, MCK : 768/384/256fs
- Serial Host Interface : I^2C bus (Standard-mode/100kbps, First-mode/400kbps)
  : 4-Wire Serial bus (Clock, Enable, Input data, Output data)
- Power Supply : 3.3 V
- Input terminal : 5.0V Input tolerant
- Package : SSOP32 (Pb-Free)

■ Block Diagram

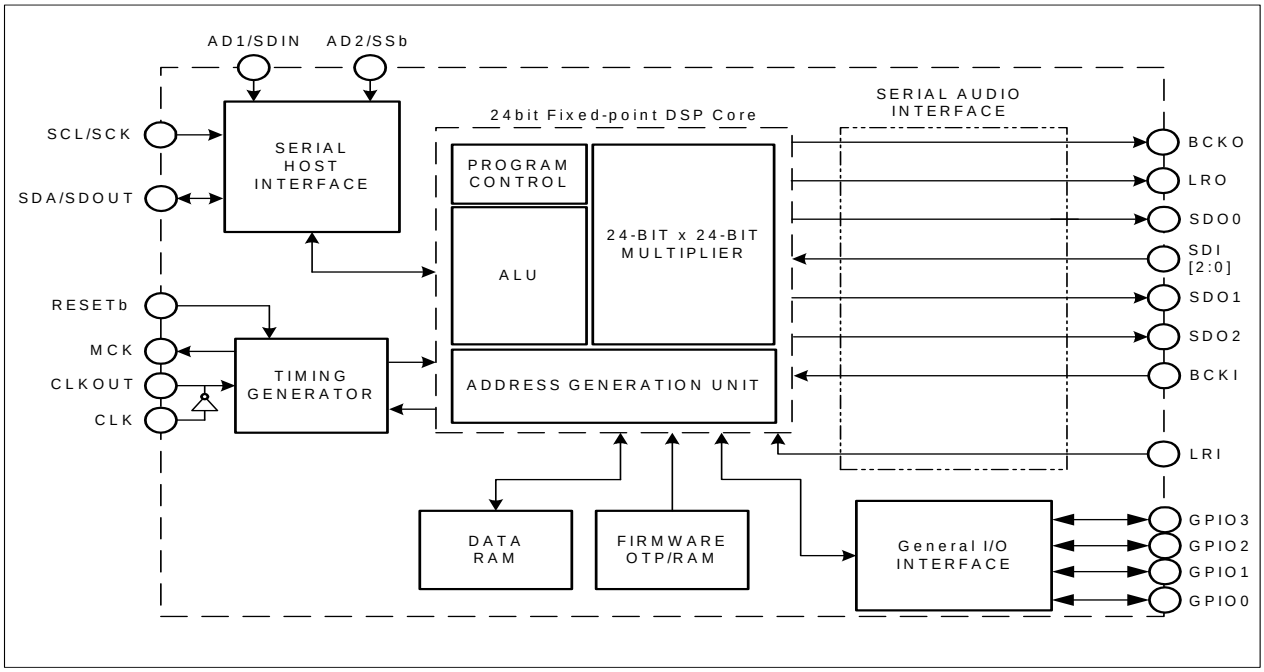


Fig.1 NJU26040 Hardware Block Diagram

■ Pin Configuration

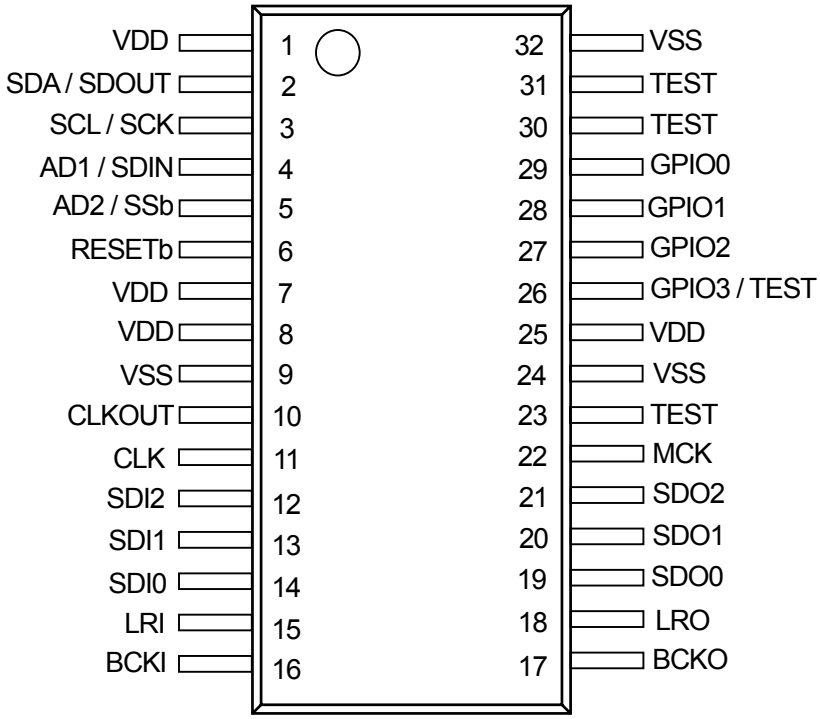


Fig. 2 Pin Configuration

■ Pin Description

Table 1 Pin Description

Pin No.	Symbol	I/O	Description
1, 7, 8, 25	VDD	-	Power Supply +3.3V
2	SDA / SDOUT	OD	I^2C I/O / 4-Wire Serial Output This pin requires a pull-up resistance in both I^2C bus and 4-Wire serial mode.
3	SCL / SCK	I	I^2C Clock / Serial Clock
4	AD1 / SDIN	I	I^2C Address / Serial Input
5	AD2 / SSb	I	I^2C Address / Serial Enable
6	RESETb	I	Reset (RESETb='Low' : DSP Reset)
9, 24, 32	VSS	-	GND
10	CLKOUT	O	OSC Output
11	CLK	I	OSC Clock Input
12	SDI2	I	Audio Data Input 2
13	SDI1	I	Audio Data Input 1
14	SDI0	I	Audio Data Input 0
15	LRI	I	LR Clock Input
16	BCKI	I	Bit Clock Input
17	BCKO	O	Bit Clock Output
18	LRO	O	LR Clock Output
19	SDO0	O	Audio Data Output 0
20	SDO1	O	Audio Data Output 1
21	SDO2	O	Audio Data Output 2
22	MCK	O	Master Clock Output for A/D, D/A
23, 30, 31	TEST	I -	for Test (connected to VSS)
26	GPIO3/ TEST	I/O +	General Purpose IO 3 / for Test (Not connected : OPEN)
27	GPIO2	I/O -	General Purpose IO 2
28	GPIO1	I/O -	General Purpose IO 1
29	GPIO0	I/O -	General Purpose IO 0

Note : I : Input
I - : Input (Pull-down)
O : Output
OD : Bi-directional (Open Drain) This pin requires a pull-up resistance.
I/O+ : Bi-directional (with Pull-up resistance)
I/O - : Bi-directional (with Pull-down resistance)

■ Absolute Maximum Ratings

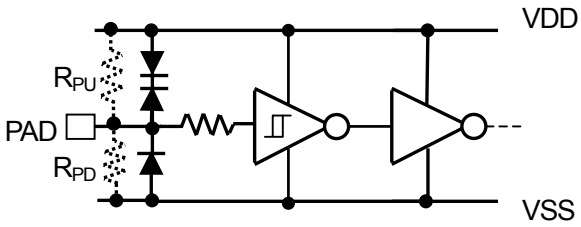
Table 2 Absolute Maximum Ratings **(V_{SS}=0V=GND, Ta=25°C)**

Parameter		Symbol	Rating	Units
Supply Voltage		V_{DD}	-0.3 to 3.8	V
Pin Voltage *	In, OD	$V_{x(IN)}$,$V_{x(OD)}$	-0.3 to 5.5 ($V_{DD}\geq$ 3.0V) -0.3 to 3.8 (V_{DD} < 3.0V)	V
	I/O	$V_{x(I/O)}$	-0.3 to 3.8	
	Out	$V_{x(OUT)}$	-0.3 to 3.8	
	CLK	$V_{x(CLK)}$	-0.3 to 3.8	
	CLKOUT	$V_{x(CLKOUT)}$	-0.3 to 3.8	
Power Dissipation		P_D	500	mW
Operating Voltage		T_{OPR}	-40 to 85	°C
Storage Temperature		T_{STR}	-40 to 125	°C

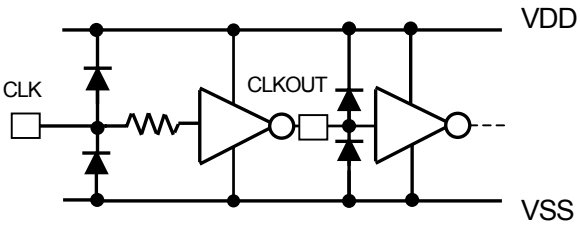
* The LSI must be used inside of the “Absolute maximum ratings”. Otherwise, a stress may cause permanent damage to the LSI.

* $V_{x(IN)}$: 3, 4, 5, 6, 12,13,14,15,16, 23, 30, 31 pin
* $V_{x(OD)}$: 2 pin
* $V_{x(I/O)}$: 26, 27, 28, 29 pin
* $V_{x(OUT)}$: 17, 18, 19, 20, 21, 22 pin
* $V_{x(CLK)}$: 11 pin
* $V_{x(CLKOUT)}$: 10 pin

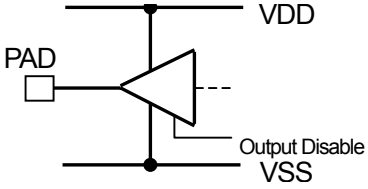
■ Terminal equivalent circuit diagram



Input, I/O (Input part)
(With R_{PU}: 26 pin)
(With R_{PD} : 23, 27 to 31pin)



CLK / CLKOUT
(No.10, 11 pin)



Output, I/O (Output part)
(No.2pin: Open Drain Output)

Fig.3 NJU26040 Terminal equivalent circuit diagram

■ Electric Characteristics

Table 3 Electric Characteristics **(V_{DD}=3.3V, f_{OSC}=36.864MHz, Ta=25°C)**

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}	V_{DD} pin	3.0	3.3	3.6	V
Operating Current	I_{DD}	V_{DD}=3.3V *1	-	42	-	mA
High Level Input Voltage	V_{IH}		V_{DD} x 0.7	-	V_{DD} *2	V
Low Level Input Voltage	V_{IL}		0	-	V_{DD} x 0.3	
High Level Output Voltage	V_{OH}	I_{OH}= -1mA *3	V_{DD} x 0.8	-	V_{DD}	
Low Level Output Voltage	V_{OL}	I_{OL}= 1mA	0	-	V_{DD} x 0.2	
Leakage Current *4	I_{IN}	V_{IN} = V_{SS} to V_{DD}	-10	-	10	μA
	$I_{IN(PU)}$		-100	-	10	
	$I_{I(PD)N}$		-10	-	100	
Input Transition Time *5	t_r / t_f		-	-	100	ns
Clock Frequency	f_{OSC}	No.11pin (CLK) *6	20	36.864	38	MHz
Clock Duty Cycle	r_{EC}	No.11pin (CLK)	45	50	55	%

*1 Current of operation is at the starting time.
It is an actual measurement (reference value) in the room temperature in standard firmware in the default state.

*2 Open-Drain input/output pins are +5.0V tolerant except GPIO0,GPIO1/GPIO2,GPIO3 and CLK input pin at supply voltage V_{DD} = 3.3V.

*3 Except No.2pin: SDA/SDOUT (Open-Drain).

*4 $I_{IN(PU)}$: 26pin, $I_{IN(PD)}$: 27,28,29,30,31 pin

*5 The tr / tf of No.2,3,4,5 pins are specified separately. Refer to the software specification.

*6 Use it by the clock frequency united with the specification of firmware. Refer to the software specification.
Usually, the sampling frequency of 768 Fs is supplied to CLK pin.

1. Power Supply, Input/Output terminal, Clock, Reset

1.1 Power Supply

The NJU26040 Series has a power supply V_{DD}. To setup good power supply condition, the decoupling capacitors should be implemented at the all power supply terminals.

1.2 Input/Output terminal

It restricts, when the input terminals (SCL/SCK, AD1/SDIN, AD2/SSb, RESETb, SDI2, SDI1, SDI0, LRI, BCKI pins) and bi-directional Open-drain terminal (SDA/SDOUT pin) of NJU26040 Series, and V_{DD} are supplied on regular voltage (V_{DD}=3.3V), and it becomes +5V Input tolerant.

1.3 Clock

The NJU26040 Series CLK pin requires the system clock that should be related to the sample frequency768 Fs. The clock frequency of 36.864MHz(48kHz x 768) should be supplied to the NJU26040. Refer to the software specification.

(For example : Fs=48kHz CLK=36.864MHz)

Note :

The clock frequency of 36.864MHz(48kHz x 768) should be supplied to the NJU26040.

Out of 36.864MHz(48kHz x 768) in Master mode. The NJU26040 Series can't process the decoding correctly. Please consult with manufacture of crystal oscillator / ceramic resonator enough in use of these parts. NJRC would not take the responsibility on the external parts of clock generating.

1.4 Reset

To initialize the NJU26040 Series, RESETb pin should be set Low level during some period. After some period of Low level, RESETb pin should be High level. This procedure starts the initialization of the NJU26040 Series. After the power supply and the oscillation of the NJU26040 Series becomes stable, RESETb pin must be kept Low-level more than t_{RESETb} period. (Fig.4)

If RESETb terminal is fixed “Low” level, SDA /SDOUT pin is Hi-Z state compulsorily. A Hi-Z state is continued until a Serial Host Interface (SHI) is decided. Therefore, communication by SHI cannot be performed until a setup of internal hardware is completed.

After RESETb pin level goes to "High" (after reset release), a setup of the internal hardware of a Serial Host Interface completes NJU26040 Series within 25ms. Then, it will be in the state which can communicate. How to select a Serial Host Interface,I^2C bus or 4-Wire serial bus. Refer to the software specification.

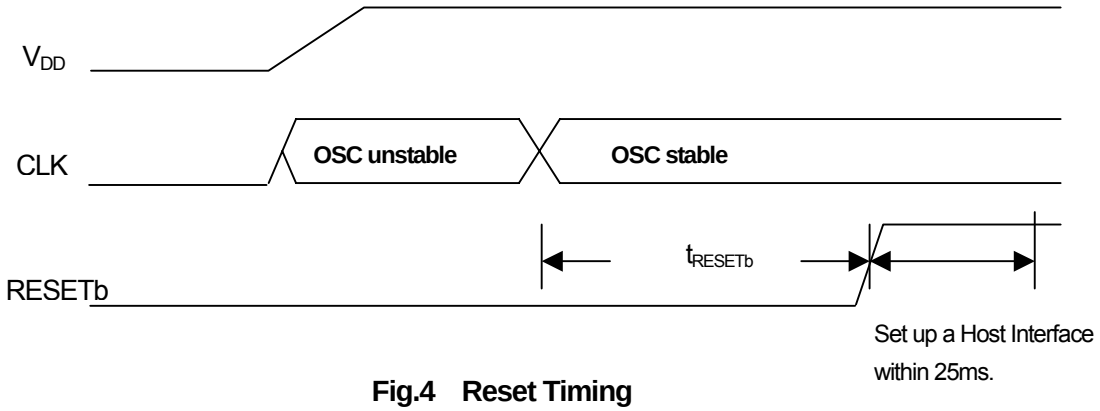


Fig.4 Reset Timing

Table 4 Reset Time

Symbol	Time
t_{RESETb}	≥ 300μs

Note :

If supply of a clock is stopped or the NJU26040 is reset again, putting a normal clock into CLK terminal, the period RESETb terminal of t_{RESETb} is kept “Low” level.(Table 4) Next, the NJU26040 is reset. Then redo from initial setting.

2. Digital Audio Clock

Digital audio data needs to synchronize and transmit between digital audio systems.
The NJU26040 Series - master mode / slave mode - both of the modes are supported.

- In Master mode;
  Use the clock of BCKO and a LRO pin output clock for digital audio data transfer.
- In Slave mode;
  The clock output from a master device is needed for the input terminal of BCKI and LRI.

2.1 Audio Clock

Three kinds of clocks are needed for digital audio data transfer.

(1) LR clock (LRI, LRO) is needed by serial-data transmission. It is the same as the sampling frequency of a digital audio signal.
(2) Bit clock (BCKI, BCKO) is needed by serial-data transmission. It becomes the multiple of LR clock.
(3) Master clock (MCK) is needed by A/D, D/A converter, etc. It becomes the multiple of LR clock. It is not related to serial audio data transmission.

Bit clock (BCKI, BCKO) of NJU26040 Series is supporting 32fs and 64fs of LR clock rate. (Table 5, 6, 7)
Moreover, regardless of the master mode / slave mode of NJU26040 Series, MCK clock pin outputs the clock which carried out 256fs (1/3 x CLK) after NJU26040 reset release. "STOP", "Buffer output (768 fs = 1/1 x CLK)", and an output setup of a "384fs(1/2 x CLK)" are possible by control command.(Table 7) Refer to the software specification.

Table 5 Sampling Frequency and BCK, MCK, clock (In Slave mode)

Mode	Clock Signal	Multiple Frequency	32kHz	44.1kHz	48kHz
DSP Slave	LRI	1fs	32kHz	44.1kHz	48kHz
	BCKI (32fs)	32fs	1.024MHz	1.4112MHz	1.536MHz
	BCKI (64fs)	64fs	2.048MHz	2.822MHz	3.072MHz

* In Slave mode : BCKO / LRO output data is same as input data of BCKI / LRI.

Table 6 Sampling Frequency and BCK, MCK, clock (In Master mode)

Mode	Clock Signal	Multiple Frequency	CLK pin frequency		
			24.576MHz	33.8688MHz	36.864MHz
DSP Master	LRO	1fs	32kHz	44.1kHz	48kHz
	BCKO (32fs)	32fs	1.024MHz	1.4112MHz	1.536MHz
	BCKO (64fs)	64fs	2.048MHz	2.822MHz	3.072MHz

Table 7 Sampling Frequency and BCK, MCK, clock (In Master/Slave mode)

Mode	Clock Signal	Multiple Frequency	CLK pin frequency		
			24.576MHz	33.8688MHz	36.864MHz
DSP Master/ Slave	MCK	256fs (1/3 CLK)	8.192MHz	11.2896MHz	12.288MHz
		384fs (1/2 CLK)	12.288MHz	16.9344MHz	18.432MHz
		768fs (1/1 CLK)	24.576MHz	33.8688MHz	36.864MHz
		"STOP"	Fixed "Low" level		

3. Digital Audio Interface

3.1 Digital Audio Data Format

The NJU26040 Series can use three kinds of formats hereafter as industry-standard digital audio data format.

(1) I^2S : MSB is put on the 2nd bit of LR clock change rate.(1 bit is delayed to left stuffing)
(2) Left-justified : LR clock -- MSB is placed for changing.
(3) Right-justified : LSB is placed just before LR clock change rate.
The main differences among three kinds of formats are in the position relation between LR clock (LRI, LRO) and an audio data (SDI, SDO).

- In every format: : a left channel is transmitted previously.
- In Right/Left-justified : LR clock ='High' shows a left channel.
- I^2S : LR clock="Low" shows a left channel.
- The Bit clock BCK (BCKI, BCKO) is used as a shift clock of transmission data. The number of clocks more than the number of sum total transmission bits of a L/R channel is needed at least.
- One cycle of LR clock is one sample of a stereo audio data. The frequency of LR clock becomes equal to a sample rate (Fs).
- The NJU26040 supports serial data format which includes 32(32fs) or 64(64fs) BCK clocks. This serial data format is applied to both MASTER and SLAVE mode.

3.2 Serial Audio Data Input/output

The NJU26040 Series audio interface includes 3 data input lines: SDI0, SDI1 and SDI2 (Table 8). 3 data output lines: SDO0, SDO1 and SDO2. (Table 9). Refer to software specification.

Table 8 Serial Audio Input Pin Description

Pin No.	Symbol	Description
14	SDI0	Audio Data Input 0
13	SDI1	Audio Data Input 1
12	SDI2	Audio Data Input 2

Table 9 Serial Audio Output Pin Description

Pin No.	Symbol	Description
19	SDO0	Audio Data Output 0
20	SDO1	Audio Data Output 1
21	SDO2	Audio Data Output 2

The NJU26040 Series can use three kinds of formats hereafter as industry-standard digital audio data format; (1) I^2S (2) Left-Justified (3) Right-justified and 16 / 18 / 20 / 24bits data length. (Fig.5-1 to Fig5-12) An audio interface input and output data format become the same data format.

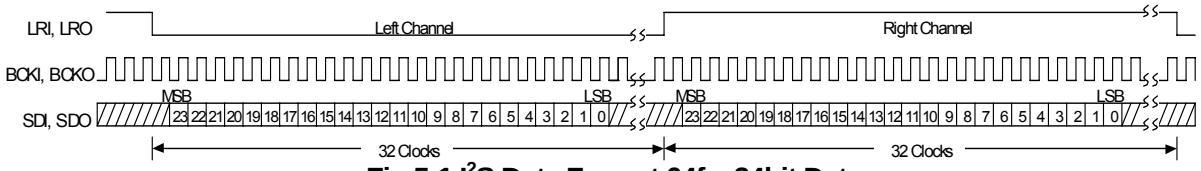


Fig.5-1 I^2S Data Format 64fs, 24bit Data

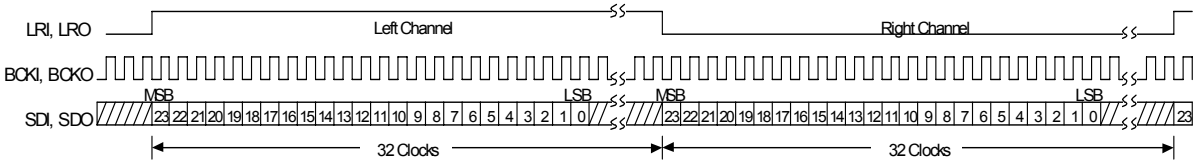


Fig.5-2 Left-Justified Data Format 64fs, 24bit Data

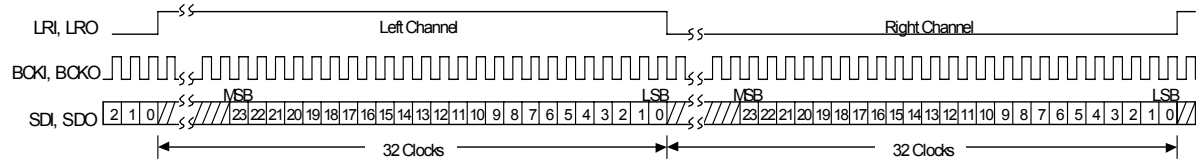


Fig.5-3 Right-Justified Data Format 64fs, 24bit Data

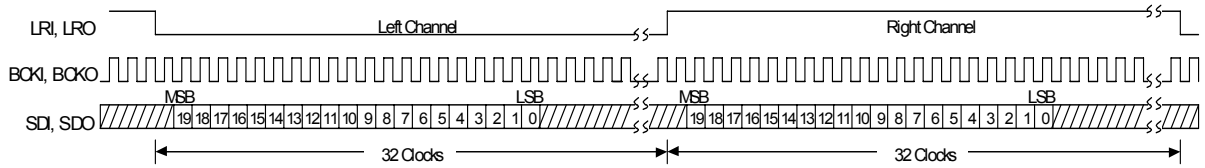


Fig.5-4 I^2S Data Format 64fs, 20bit Data

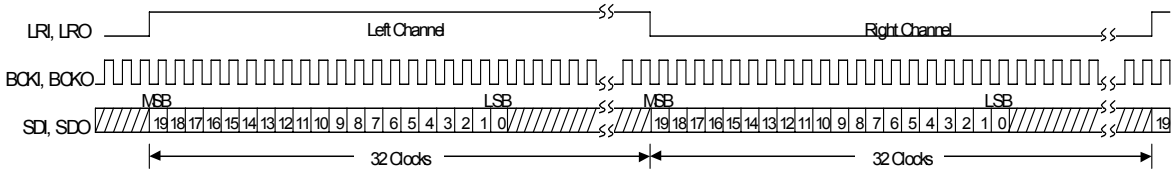


Fig.5-5 Left-Justified Data Format 64fs, 20bit Data

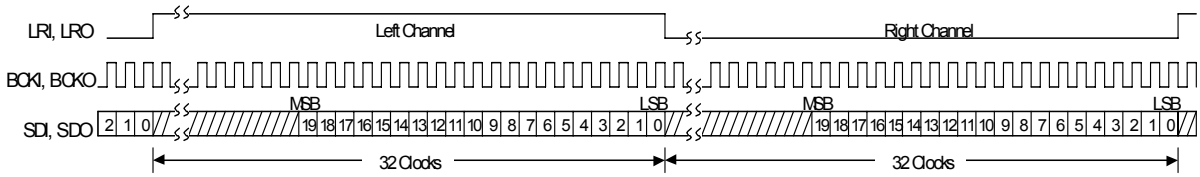


Fig.5-6 Right-Justified Data Format 64fs, 20bit Data

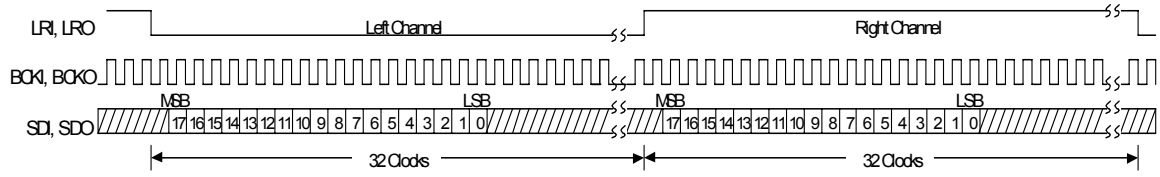


Fig.5-7 I²S Data Format 64fs, 18bit Data

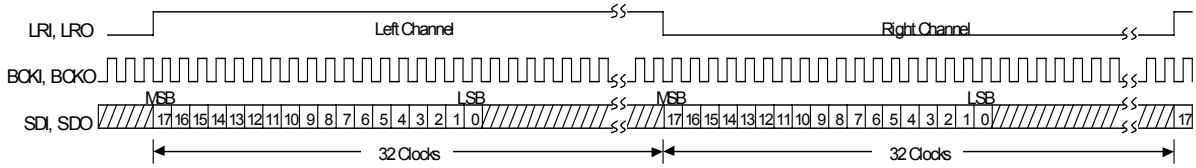


Fig.5-8 Left-Justified Data Format 64fs, 18bit Data

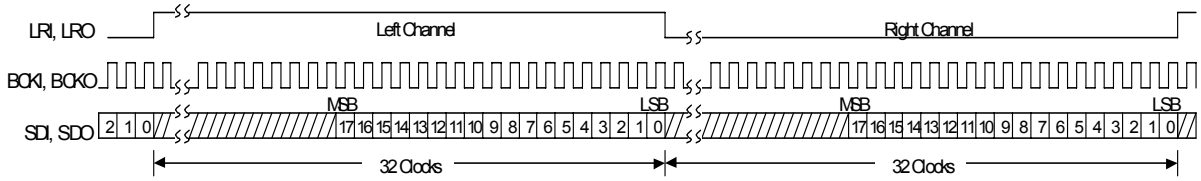


Fig.5-9 Right-Justified Data Format 64fs, 18bit Data

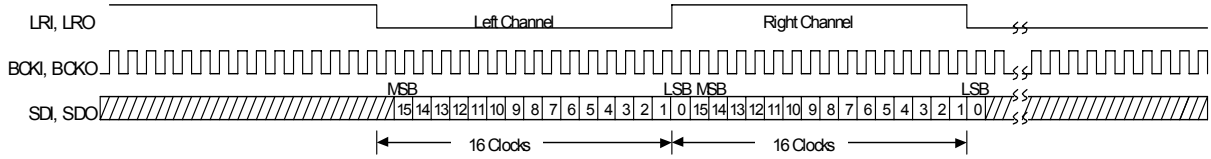


Fig.5-10 I²S Data Format 32fs, 16bit Data

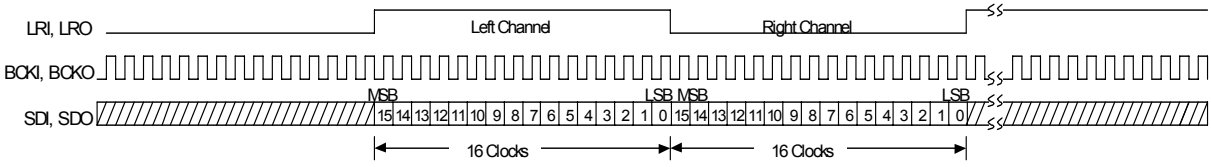


Fig.5-11 Left-Justified Data Format 32fs, 16bit Data

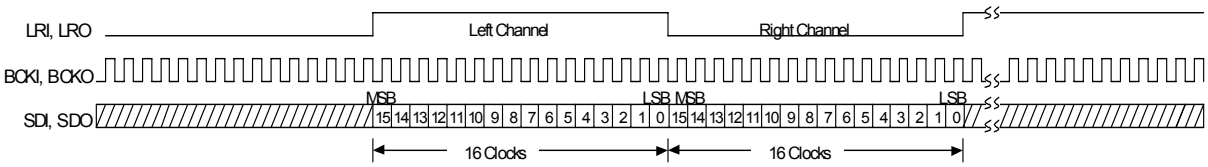


Fig.5-12 Right-Justified Data Format 32fs, 16bit Data

3.3 Serial Audio Input Timing

Table 10 Serial Audio Input Timing Parameters **(V_{DD}=3.3V, Ta=25°C)**

Parameter	Symbol	Test Condition	Min	Typ.	Max	Units
BCKI Frequency *	f_{BCKI}		-	-	6.5	MHz
BCKI Period *						
Low Pulse Width	t_{SIL}		75	-	-	ns
High Pulse Width	t_{SIH}		75			
BCKI to LRI Time *	t_{SLI}		40	-	-	ns
LRI to BCKI Time *	t_{LSI}		40	-	-	ns
Data Setup Time **	t_{DS}		15	-	-	ns
Data Hold Time **	t_{DH}		15	-	-	ns

* It is the regulation in slave mode.
** It is the regulation to BCKI in slave mode and to BCKO in master mode.

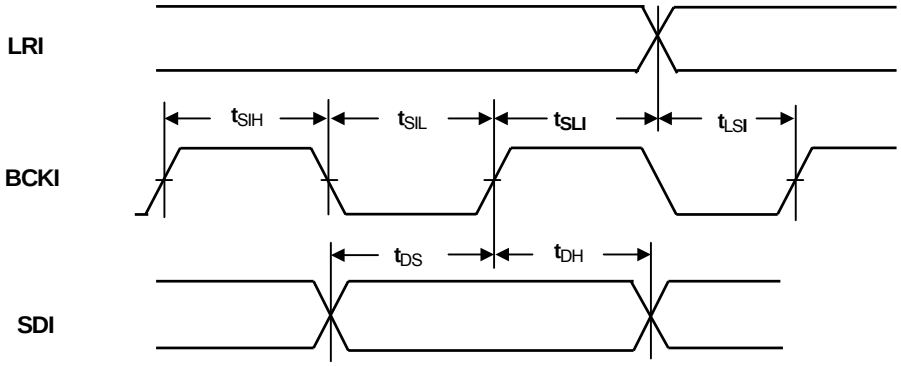


Fig.6 Serial Audio Input Timing

Table 11 Serial Audio Output Timing Parameters **(V_{DD}=3.3V, Ta=25°C)**

Parameter	Symbol	Test Condition	Min	Typ.	Max	Units
BCKO to LRO Time *	t_{SLO}	C_L:LRO, BCKO, SDO=25pF	-15	-	15	ns
Data Output Delay	t_{DOD}		-	-	15	ns

* It is the regulation in Master mode.

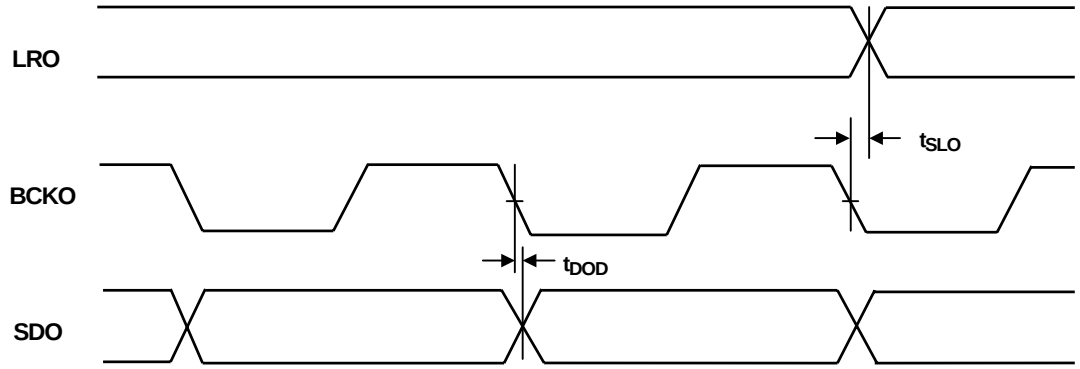


Fig.7 Serial Audio Input Timing

Table 12 Serial Audio Clock Timing (In slave mode) **(V_{DD}=3.3V, Ta=25°C)**

Parameter	Symbol	Test Condition	Min	Typ.	Max	Units
Clock Output Delay (LRI --> LRO)	t_{PDL}	C_L:LRO, BCKO, SDO=25pF DSP Slave Mode	-	-	15	ns
Clock Output Delay (BCKI --> BCKO)	t_{PDB}		-	-	15	ns

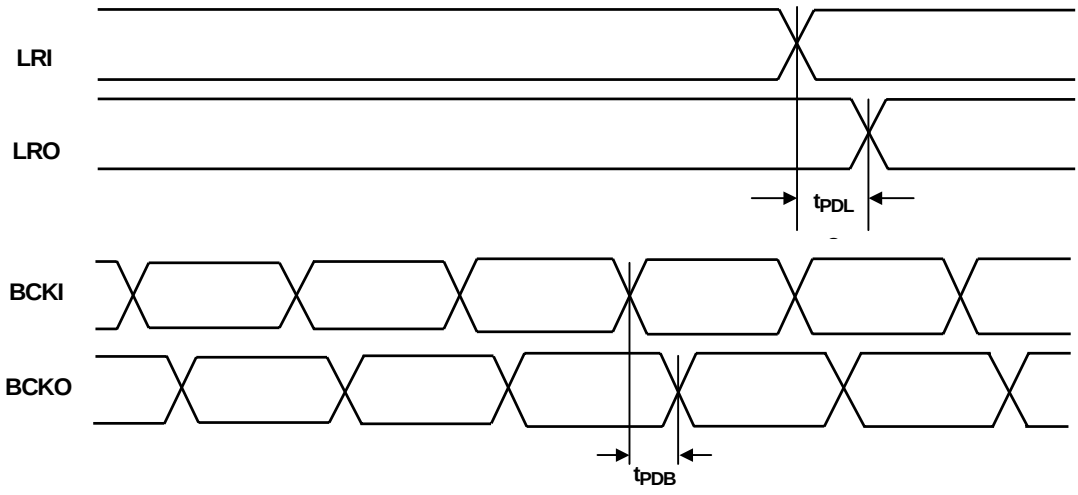


Fig.8 Serial Audio clock Timing (In slave mode)

4. Serial Host Interface

The NJU26040 Series can be controlled via Serial Host Interface (SHI) using either of two serial bus formats: I^2C bus or 4-Wire serial bus.(Table 13)

How to select a Serial Host Interface, I^2C bus or 4-Wire serial bus. Refer to the software specification.

Table 13 Serial Host Interface Pin Description

Pin No.	Symbol (I^2C bus / Serial)	I^2C bus Format	4-Wire Serial bus Format
2	SDA / SDOUT *	Serial Data Input/Output (Open Drain Input/Output)	Serial Data Output (Open-Drain Output)
3	SCL / SCK *	Serial Clock	Serial Clock
4	AD1 / SDIN *	I^2C bus address Bit1	Serial Data Input
5	AD2 / SSb *	I^2C bus address Bit2	Serial enable

Note : SDA /SDOUT pin is a bi-directional open drain.
This pin requires a pull-up resistance in both I^2C bus and 4-Wire serial mode.
* When the power supply (V_{DD}= +3.3V) is supplied to NJU26040, these pins become +5.0V Input tolerant.

4.1 I^2C bus

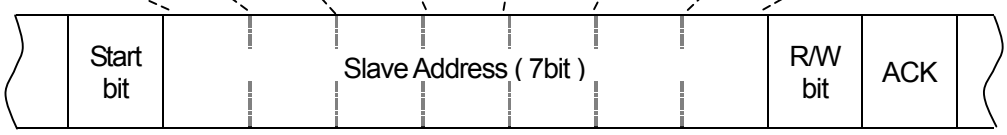
When the NJU26040 Series is configured for I^2C bus communication during the Reset initialization sequence. I^2C bus interface transfers data to the SDA pin and clocks data to the SCL pin.

AD1 and AD2 pins are used to configure the seven-bit SLAVE address of the serial host interface. (Table 14) This offers additional flexibility to a system design by four different SLAVE addresses of the NJU26040. An address can be arbitrarily set up by the AD1 and AD2 pins. The I^2C address of AD1/AD2 is decided by connection of AD1/AD2 pins. The I^2C address should be the same level of AD1/AD2 pins. The real I^2C address is described in the software specification.

Both “Standard-Mode (100kbps)” and “Fast-Mode (400kbps)” data transfer rate are supported.

Table 14 I^2C bus SLAVE Address

bit7	bit6	*1 bit5	bit4	bit3	AD2 bit2 *2	AD1 bit1 *2	R/W bit0
0	0	1	1	1	0	0	R/W
0	0	1	1	1	0	1	
0	0	1	1	1	1	0	
0	0	1	1	1	1	1	



*1 : Refer to the software specification.
*2 : SLAVE address is 0 when AD1/AD2 is “Low”. SLAVE address is 1 when AD1/AD2 is “High”.

Table 15 I²C bus Interface Timing Parameters **(V_{DD}=3.3V, f_{OSC}=36.864MHz, Ta=25°C)**

Parameter	Symbol	Min	Max	Units
SCL Clock Frequency	f_{SCL}	0	400	kHz
Start Condition Hold Time	$t_{HD:STA}$	0.6	-	μs
SCL "Low" Duration	t_{LOW}	1.3	-	μs
SCL "High" Duration	t_{HIGH}	0.6	-	μs
Start Condition Setup Time	$t_{SU:STA}$	0.6	-	μs
Data Hole Time *1	$t_{HD:DAT}$	0	0.9	μs
Data Setup Time	$t_{SU:DAT}$	250	-	ns
Rising Time	t_R	-	1000	ns
Falling Time	t_F	-	300	ns
Stop Condition Setup Time	$t_{SU:STO}$	0.6	-	μs
Bus Release Time *2	t_{BUF}	1.3	-	μs

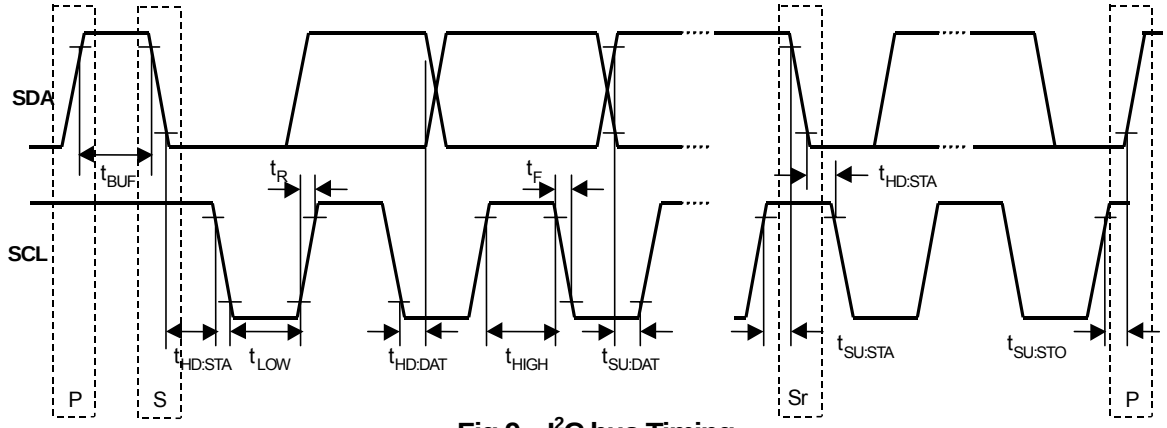


Fig.9 I²C bus Timing

Note :

*1 $t_{HD:DAT}$: Keep data 100ns hold time to avoid indefinite state by SCL falling edge.

*2 This item shows the interface specification. The interval of a continuous command is specified separately.

4.2 4-Wire Serial Interface

When the NJU26040 Series is configured for 4-Wire Serial bus communication during the reset initialization sequence. 4-Wire Serial interface communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin.

Data transfers are MSB first and are enabled by setting the Slave Select pin Low (SSb = 0). Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte (MSB) which is latched on the falling transitions of SSb.(Table16, Fig.10)

Table 16 4-Wire Serial Interface Timing Parameters (V_{DD}=3.3V, f_{OSC}=36.864MHz ,SDOUT=25pF, Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Units
Input Data Rising Time	t_{MSDr}	-	-	100	ns
Input Data Falling Time	t_{MSDf}	-	-	100	ns
Serial Clock Rising Time	t_{MSCr}	-	-	100	ns
Serial Clock Falling Time	t_{MSCf}	-	-	100	ns
Serial Strobe Rising Time	t_{MSSr}	-	-	100	ns
Serial Strobe Falling Time	t_{MSSf}	-	-	100	ns
Serial Clock High Duration	t_{MSCa}	0.5	-	-	µs
Serial Clock Low Duration	t_{MSCn}	0.5	-	-	µs
Serial Clock Period	t_{MSCc}	1.0	-	-	µs
Serial Strobe Setup Time	t_{MSSs}	0.5	-	-	µs
Serial Strobe Hold Time	t_{MSSh}	0.5	-	-	µs
Serial Strobe Low Duration *1	t_{MSSa}	-	8.5	-	µs
Serial Strobe High Duration *1	t_{MSSn}	-	1.0	-	µs
Input Data Setup Time	t_{MSDis}	0.1	-	-	µs
Input Data Hold Time	t_{MSDih}	0.1	-	-	µs
Output Data Hold Time	t_{MSDoh}	-	-	0.25	µs
Output Data Turn off Time (Hi-Z)	t_{MSDov}	-	-	0.25	µs

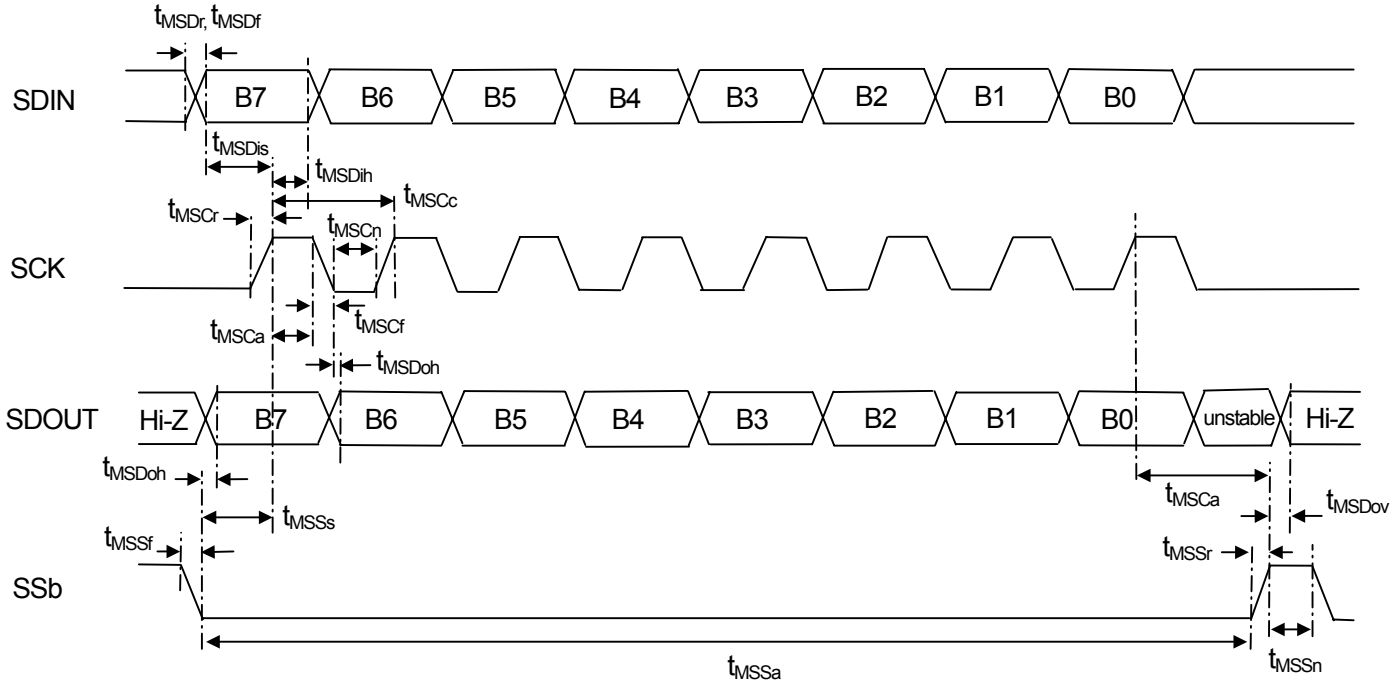


Fig.10 4-Wire Serial Interface Timing

Note : When the data-clock is less than 8 clocks, the input data is shifted to LSB side.
*1 : It is not a continuous command interval.

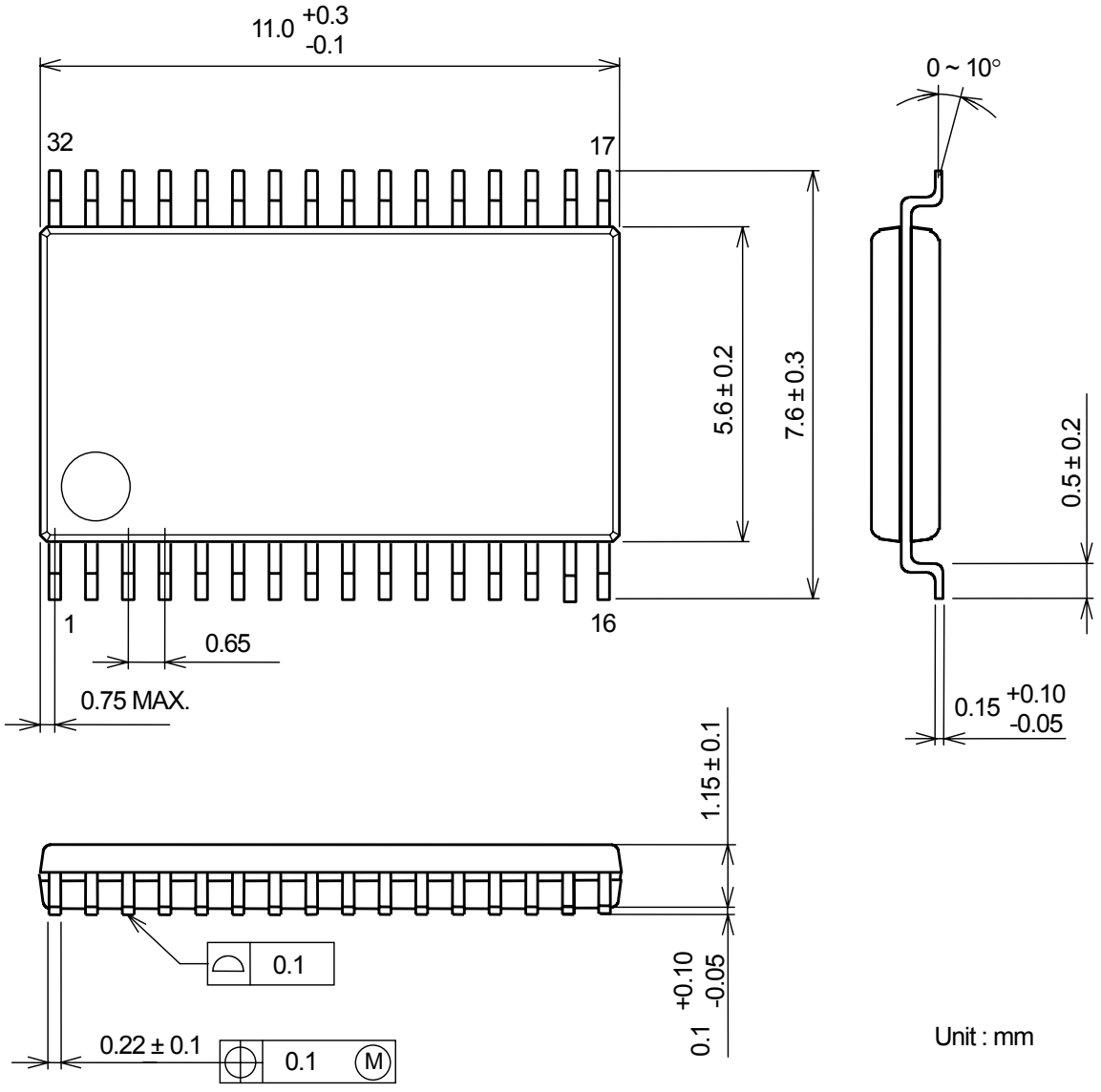
5. General Purpose I/O (GPIO) Ports

NJU26040 Series has four general purpose Input/Output (GPIO) ports.
- GPIO0, GPIO1, GPIO2 : Bi-directional (with Pull-down resistance)
- GPIO3 : Bi-directional (with Pull-Up resistance)

Note :

Until firmware starts, please set GPIO3/TEST1 pin should be “High” level after NJU26040 reset release.
In case of GPIO3/TEST1 pin is “Low” level. The NJU26040 can’t operate.
GPIO3/TEST1 pin is must be not connected (OPEN).

6. Package Dimensions (SSOP32, Pb-Free)



Unit : mm