OP-07

Ultra-Low Offset Voltage Op Amp

FEATURES

- Ultra-low V_{OS} (10μV typ.)
- Ultra-low V_{OS} drift (0.2μV/°C)
- Ultra-stable vs time (0.2μV/month)
- Ultra-low noise (0.35μV_{p-p})
- No external components required
- Large input voltage range (±14.0V)
- Wide supply voltage range (±3V to ±18V)
- Fits 725, 108A/308A, 741, AD510 sockets

GENERAL DESCRIPTION

The OP-07 series of monolithic operational amplifiers provides high performance through the use of a low noise, chopper-less bipolar input transistor amplifier circuit. The elimination of external components for offset nulling, frequency compensation and device protection permits optimization of system design, while excellent device interchangeability provides reduced system assembly time and eliminates or reduces field recalibrations.

The outstanding common-mode rejection provides maximum flexibility and performance in high noise environments and non-inverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range.

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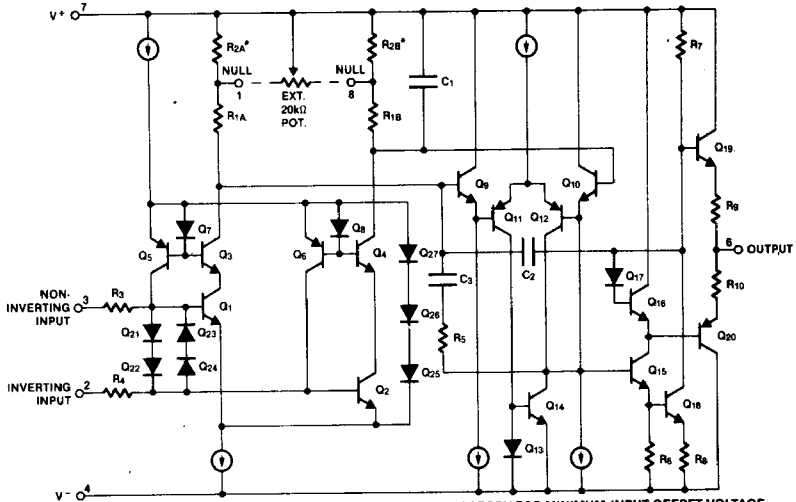
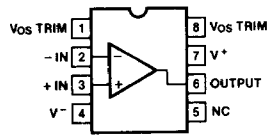
SIMPLIFIED SCHEMATIC Pin numbers for 8-pin packages only

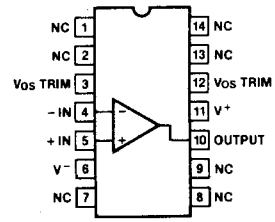


NOTE: R_{2A} AND R_{2B} ARE ELECTRONICALLY ADJUSTED ON-CHIP AT FACTORY FOR MINIMUM INPUT OFFSET VOLTAGE.

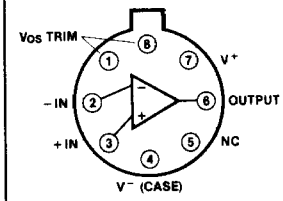
PIN CONFIGURATIONS



(outline dwgs JA, PA)



(outline dwg JD)



(outline dwg TY)

ORDERING INFORMATION

PART	PACKAGE			
	TO-99	8-PIN CERDIP	8-PIN MiniDIP	14-PIN* CERDIP
TEMPERATURE RANGE: −55°C to +125°C				
OP-07 OP-07A	OP-07J OP-07AJ	OP-07Z OP-07AZ	— —	OP-07Y OP-07AY
TEMPERATURE RANGE: 0°C to +70°C				
OP-07C OP-07D OP-07E	OP-07CJ OP-07DJ OP-07EJ	OP-07CZ — OP-07EZ	OP-07CP OP-07DP OP-07EP	OP-07CY — OP-07EY

For dice order # OP-07/D

*Not directly interchangeable with LM108A

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±22V
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
OP-07A, OP-07 ..... −55°C to +125°C
OP-07E, OP-07C, OP-07D ..... 0°C to +70°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1: Maximum package power dissipation vs ambient temperature.

Package Type	Max. Amb. Temp. for Full Rating	Derate Above Max. Ambient Temp.
TO-99 (J)	80°C	7.1mW/°C
Dual-In-Line (Y)	100°C	10.0mW/°C
MiniDIP (P)	36°C	5.6mW/°C
8-Pin CERDIP (Z)	75°C	6.7mW/°C

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS

These specifications apply for V_{SUPP} = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	OP-07A			OP-07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)		10	25		30	75	µV
Long Term Input Offset Voltage Stability	$\Delta V_{OS}/\Delta t$	(Note 2)		0.2	1.0		0.2	1.0	µV/mo
Input Offset Current	I_{OS}			0.3	2.0		0.4	2.8	nA
Input Bias Current	I_{BIAS}			±0.7	±2.0		±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)		0.35	0.6		0.35	0.6	µVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3) f_O = 100Hz (Note 3) f_O = 1000Hz (Note 3)		10.3 10.0 9.6	18.0 13.0 11.0		10.3 10.0 9.6	18.0 13.0 11.0	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)		14	30		14	30	pAp-p
Input Noise Current Density	i_n	f_O = 10Hz (Note 3) f_O = 100Hz (Note 3) f_O = 1000Hz (Note 3)		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.14 0.12	0.80 0.23 0.17	pA/√Hz
Input Resistance Differential Mode Common-Mode	 R_{diff} R_{CM}		 30 	 80 200	 	 20 	 60 200	 	 MΩ GΩ
Input Common-Mode Voltage Range	CMVR		±13.0	±14.0		±13.0	±14.0		V
Common-Mode Rejection Ratio	CMRR	CMVR = ±13.0V	110	126		110	126		dB
Power Supply Rej. Ratio	PSRR	V_{SUPP} = ±3V to ±18V	100	110		100	110		dB
Large Signal Voltage Gain	A_{VOL}	$R_L \geq 2k\Omega$, V_O = ±10V $R_L \geq 500\Omega$, V_O = ±0.5V, V_{SUPP} = ±3V	300 150	500 500		200 150	500 500		V/mV
Maximum Output Voltage Swing	±V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.17		0.1	0.17		V/µs
Closed Loop Bandwidth	BW	A_V = +1.0 (Note 3)	0.4	0.6		0.4	0.6		MHz
Open Loop Output Res.	R_O	V_O = 0, $I_O \doteq 0$		60			60		Ω
Power Consumption	Pd	 V_{SUPP} = ±3V		75 4	120 6		75 4	120 6	mW
Offset Adjustment Range		R_P = 20kΩ		±4			±4		mV

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OPERATING CHARACTERISTICS (Continued)

These specifications apply for $V_{SUPP} = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	OP-07E			OP-07C			OP-07D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)		30	75		60	150		60	150	μV
Long Term Input Offset Voltage Stability	$\Delta V_{OS}/\Delta t$	(Note 2)		0.3	1.5		0.4	2.0		0.5	3.0	μV/mo
Input Offset Current	I_{OS}			0.5	3.8		0.8	6.0		0.8	6.0	nA
Input Bias Current	I_{BIAS}			±1.2	±4.0		±1.8	±7.0		±2.0	±12	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)		0.35	0.6		0.38	0.65		0.38	0.65	μVp-p
Input Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 3) $f_O = 100Hz$ (Note 3) $f_O = 1000Hz$ (Note 3)		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5		10.5 10.2 9.8	20.0 13.5 11.5	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)		14	30		15	35		15	35	pAp-p
Input Noise Current Density	i_n	$f_O = 10Hz$ (Note 3) $f_O = 100Hz$ (Note 3) $f_O = 1000Hz$ (Note 3)		0.32 0.14 0.12	0.80 0.23 0.17		0.35 0.15 0.13	0.90 0.27 0.18		0.35 0.15 0.13	0.90 0.27 0.18	pA/√Hz
Input Resistance Differential Mode	R_{diff}		15	50		8	33		7	31		MΩ
Input Resistance Common-Mode	R_{CM}			160			120			120		GΩ
Input Common-Mode Voltage Range	CMVR		±13.0	±14.0		±13.0	±14.0		±13.0	±14.0		V
Common-Mode Rejection Ratio	CMRR	CMVR = ±13.0V	106	123		100	120		94	110		dB
Power Supply Rejection Ratio	PSRR	$V_{SUPP} = \pm 3V$ to ±18V	94	107		90	104		90	104		dB
Large Signal Voltage Gain	A_{VOL}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_{SUPP} = \pm 3V$	200 150	500 500		120 100	400 400		120 —	400 —		V/mV
Maximum Output Voltage Swing	$\pm V_O$	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.0 ±11.5 —	±13.0 ±12.8 ±12.0		±12.0 ±11.5 —	±13.0 ±12.8 —		V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.17		0.1	0.17		0.1	0.17		V/μs
Closed Loop Bandwidth	BW	$A_{VOL} = +1.0$ (Note 3)	0.4	0.6		0.4	0.6		0.4	0.6		MHz
Open Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$		60			60			60		Ω
Power Consumption	Pd			75	120		80	150		80	150	mW
		$V_{SUPP} = \pm 3V$		4	6		4	8		4	8	
Offset Adjustment Range		$R_P = 20k\Omega$		±4			±4			±4		mV

Note 1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, OP-07A offset voltage is measured 5 minutes after power supply application at −55°C, +25°C and +125°C.

Note 2: Long term input offset voltage stability refers to the average trend line of V_{OS} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, the change in V_{OS} during the first 30 operating days is typically 25μV. Parameter is not 100% tested; 90% of units meet this specification.

Note 3: Parameter is not 100% tested; at least 90% of units meet this specification.

OPERATING CHARACTERISTICS (Continued)

These specifications apply for $V_{SUPP} = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	OP-07A			OP-07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)		25	60		60	200	μV
Input Offset Voltage Drift Without External Trim With External Trim	$\Delta V_{OS}/\Delta T$	(Average Tested) $R_P = 20k\Omega$ (Note 3)		 0.2 0.2	 0.6 0.6		 0.3 0.3	 1.3 1.3	μV/°C
Input Offset Current	I_{OS}			0.8	4.0		1.2	5.6	nA
Input Offset Current Drift	$\Delta I_{OS}/\Delta T$	(Average Tested)		5	25		8	50	pA/°C
Input Bias Current	I_{BIAS}			±1.0	±4.0		±2.0	±6.0	nA
Input Bias Current Drift	$\Delta I_{BIAS}/\Delta T$	(Average Tested)		8	25		13	50	pA/°C
Input Common-Mode Voltage Range	CMVR		±13.0	±13.5		±13.0	±13.5		V
Common-Mode Rej. Ratio	CMRR	CMVR = ±13.0	106	123		106	123		dB
Power Supply Rej. Ratio	PSRR	$V_{SUPP} = \pm 3V$ to $\pm 18V$	94	106		94	106		dB
Large Signal Voltage Gain	A_{VOL}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	400		150	400		V/mV
Output Voltage Swing	$\pm V_O$	$R_L \geq 2k\Omega$	±12.0	±12.6		±12.0	±12.6		V

OPERATING CHARACTERISTICS

These specifications apply for $V_{SUPP} = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	OP-07E			OP-07C			OP-07D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)		45	130		85	250		85	250	μV
Input Offset Voltage Drift Without External Trim With External Trim	$\Delta V_{OS}/\Delta T$	(Average Tested) $R_P = 20k\Omega$		 0.3 0.3	 1.3 1.3		 0.5 0.4	(Note 3) 1.8 1.6 (Note 3)		 0.7 0.7	(Note 3) 2.5 2.5 (Note 3)	μV/°C
Input Offset Current	I_{OS}			0.9	5.3		1.6	8.0		1.6	8.0	nA
Input Offset Current Drift	$\Delta I_{OS}/\Delta T$	(Average Tested) (Note 3)		8	35		12	50		12	50	pA/°C
Input Bias Current	I_{BIAS}			±1.5	±5.5		±2.2	±9.0		±3.0	±14	nA
Input Bias Current Drift	$\Delta I_{BIAS}/\Delta T$	(Average Tested) (Note 3)		13	35		18	50		18	50	pA/°C
Input Common-Mode Voltage Range	CMVR		±13.0	±13.5		±13.0	±13.5		±13.0	±13.5		V
Common-Mode Rej. Ratio	CMRR	CMVR = ±13.0	103	123		97	120		94	106		dB
Power Supply Rej. Ratio	PSRR	$V_{SUPP} = \pm 3V$ to $\pm 18V$	90	104		86	100		86	100		dB
Large Signal Voltage Gain	A_{VOL}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	180	450		100	400		100	400		V/mV
Output Voltage Swing	$\pm V_O$	$R_L \geq 2k\Omega$	±12.0	±12.6		±11.0	±12.6		±11.0	±12.6		V

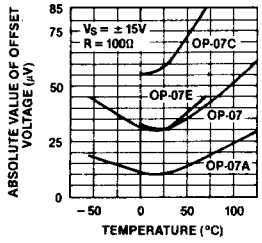
Note 1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, OP-07A offset voltage is measured 5 minutes after power supply application at −55°C, +25°C and +125°C.

Note 2: Long term input offset voltage stability refers to the average trend line of V_{OS} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, the change in V_{OS} during the first 30 operating days is typically 25μV. Parameter is not 100% tested; 90% of units meet this specification.

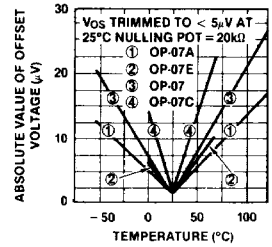
Note 3: Parameter is not 100% tested; at least 90% of units meet this specification.

TYPICAL PERFORMANCE CURVES

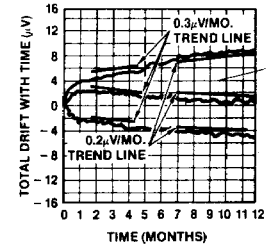
Untrimmed Offset Voltage vs Temperature



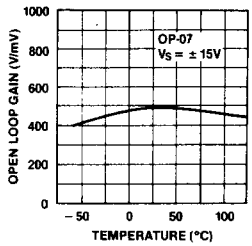
Trimmed Offset Voltage vs Temperature



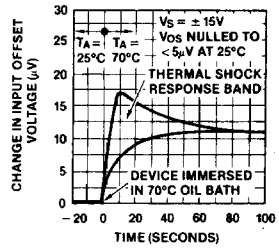
Typical Offset Voltage Stability vs Time



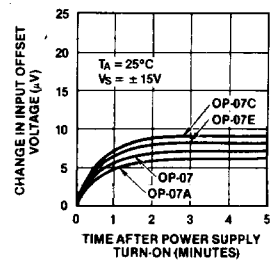
Open Loop Gain vs Temperature



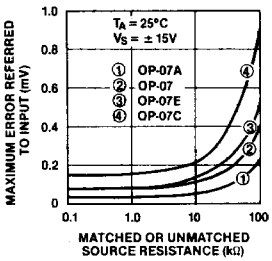
Offset Voltage Change Due to Thermal Shock



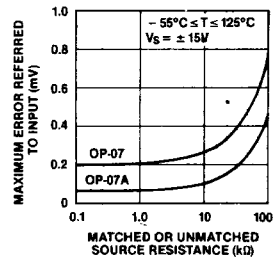
Warm-Up Drift



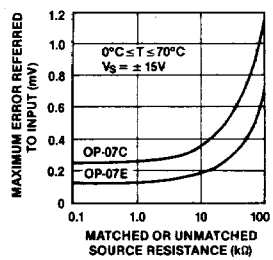
Maximum Error vs Source Resistance



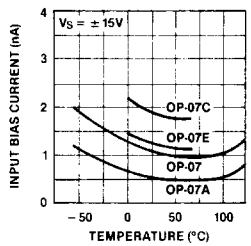
Maximum Error vs Source Resistance



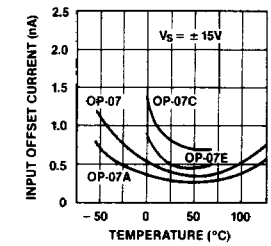
Maximum Error vs Source Resistance



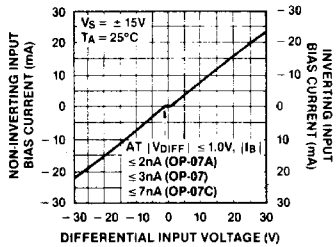
Input Bias Current vs Temperature



Input Offset Current vs Temperature

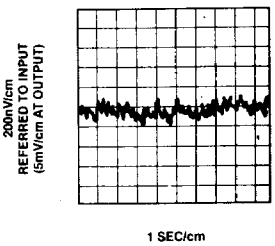


Input Bias Current vs Differential Input Voltage

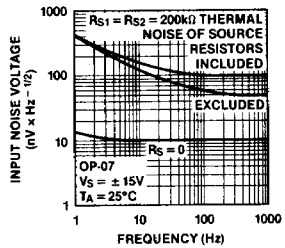


TYPICAL PERFORMANCE CURVES (Continued)

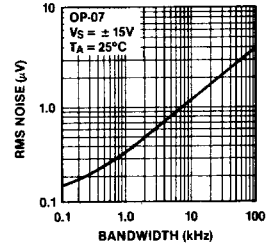
OP-07 Low Frequency Noise



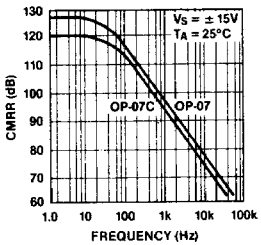
Total Input Noise Voltage vs Frequency



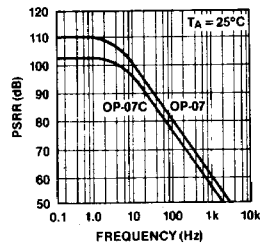
Input Wideband Noise vs Bandwidth (0.1Hz to Frequency Indicated)



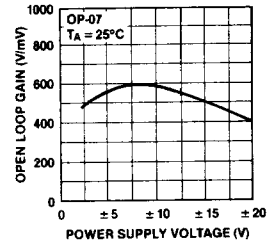
CMRR vs Frequency



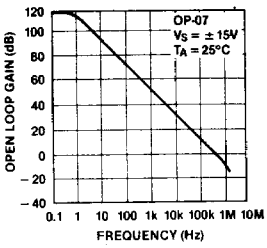
PSRR vs Frequency



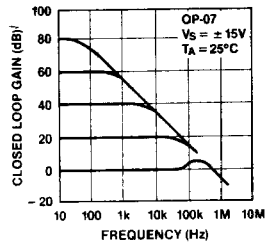
Open Loop Gain vs Power Supply Voltage



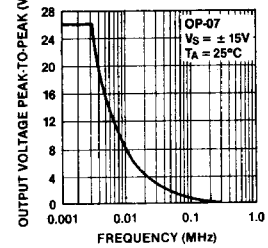
Open Loop Frequency Response



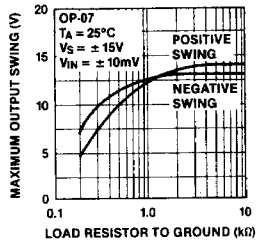
Closed Loop Response for Various Gain Configurations



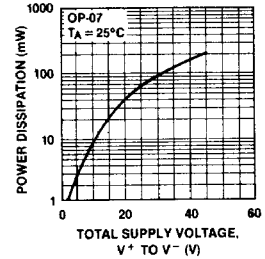
Maximum Undistorted Output vs Frequency



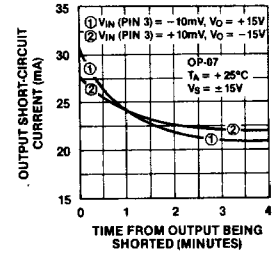
Output Voltage vs Load Resistance



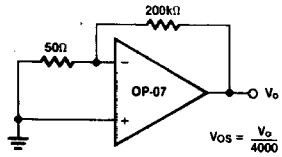
Power Consumption vs Power Supply



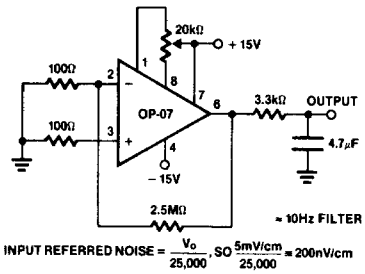
Output Short-Circuit Current vs Time



TEST CIRCUITS



Offset Voltage Test Circuit



Low Frequency Noise Test Circuit

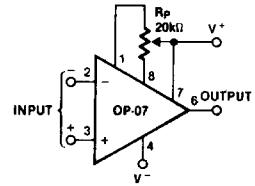


Figure 1. Offset Nulling Circuit

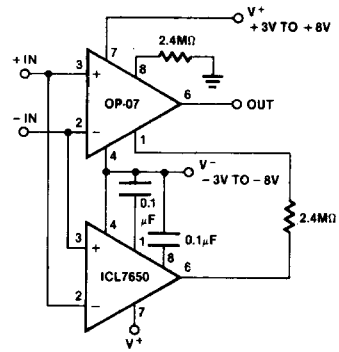


Figure 2. Auto-Nulling Circuit for OP-07

APPLICATIONS

OP-07 series devices may be inserted directly in 725 and 108/108A* series sockets with or without removal of external compensation components. Additionally, the OP-07 may be fitted to unnulled 741 series sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-07 operation (see Figure 1). The OP-07 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with a 50Ω decoupling resistor. The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

*except "Y" package

Figure 2 shows how it is possible to combine the low noise and output drive capability of the OP-07 with the low offset and drift of the ICL7650 chopper stabilized op-amp to yield a circuit which has a V_{OS} of less than 5μV (typically 1μV), temperature drift of <0.01μV/°C, long term drift of less than 1μV per year and input noise voltage of 10nV/√Hz, while at the same time driving loads of up to 2kΩ.

The exceptional input characteristics of the OP-07 are used to advantage in Figure 3 with the ICL7134B 14-bit monolithic DAC. Both the reference inversion amplifier, A_3, and the output amplifier, A_1, require offset voltages and input currents of around 25μV and 2nA respectively, to maintain the required accuracy.

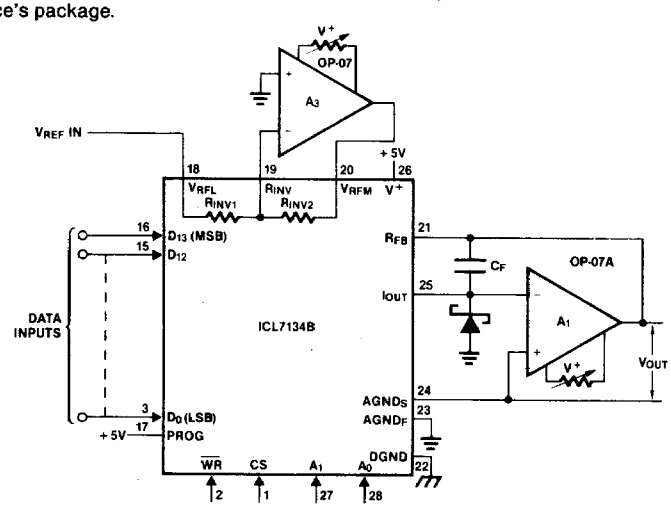
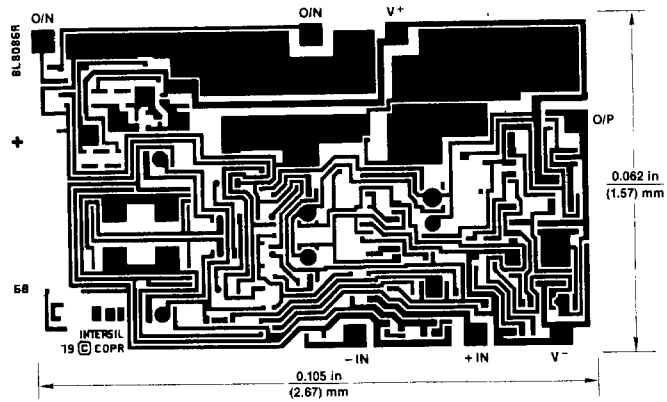


Figure 3. OP-07s Used for Reference Inversion and Voltage Output with ICL7134B DAC

OP-07

CHIP TOPOGRAPHY



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