

DATA SHEET

TEA5757HL; TEA5759HL Self Tuned Radio (STR)

Product specification
File under Integrated Circuits, IC01

2000 Feb 02

Self Tuned Radio (STR)

TEA5757HL; TEA5759HL

FEATURES

- The tuning system has an optimized IC partitioning both from application (omitting interferences) and flexibility (removable front panel option) point of view: the tuning synthesizer is on-chip with the radio
- The tuning quality is superior and requires no IF-counter for stop-detection; it is insensitive to ceramic filter tolerances
- In combination with the microcontroller, fast, low-power operation of preset mode, manual-search, auto-search and auto-store are possible
- The local (internal) controller function facilitates reduced and simplified microcontroller software
- The high integration level (radio and tuning synthesizer on one chip) means fewer external components with regard to the communication between the radio and the microcontroller (90% less components compared to the digital tuning application of a radio IC with external PLL tuning function) and a simple and small Printed-Circuit Board (PCB)
- There will be no application considerations for the tuning system, with regards to quality and high integration level, since there will be no external 110 MHz buffers, loop filter or false lock elimination
- The inherent FUZZY LOGIC behaviour of the Self Tuned Radio (STR), which mimics hand tuning and yields a potentially fast yet reliable tuning operation
- The level of the incoming signal at which the radio must lock is software programmable
- Two programmable ports
- FM-on/off port to control an external FM front-end

- High selectivity with distributed IF gain
- Soft mute
- Signal dependent stereo-blend
- High impedance MOSFET input on AM
- Wide supply voltage range of 2.5 to 12 V
- Low current consumption 18 mA at AM and FM (including tuning synthesizer)
- High input sensitivity
- Low output distortion
- Due to the new tuning concept, the tuning is independent of the channel spacing.

GENERAL DESCRIPTION

The TEA5757HL; TEA5759HL is a 48-pin integrated AM/FM stereo radio circuit including a novel tuning concept. The radio part is based on the TEA5712.

The TEA5757HL is used in FM-standards in which the local oscillator frequency is above the radio frequency (e.g. european and american standards).

The TEA5759HL is the version in which the oscillator frequency is below the radio frequency (e.g. Japanese standard).

The new tuning concept combines the advantages of hand tuning with electronic facilities and features. User 'intelligence' is incorporated into the tuning algorithm and an improvement of the analog signal processing is used for the AFC function.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA5757HL	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
TEA5759HL	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage		2.5	–	12	V
V_{CC2}	supply voltage for tuning		–	–	12	V
V_{tune}	tuning voltage		0.7	–	$V_{CC2} - 0.75$	V
I_{CC1}	supply current	AM mode	12	15	18	mA
		FM mode	13	16	19	mA
I_{DD}	supply current	AM mode	2.8	3.3	3.7	mA
		FM mode	2.4	2.7	3.0	mA
I_{CC2}	supply current for tuning in preset mode (band-end to band-end)		–	–	800	μ A
T_{amb}	ambient temperature		–15	–	+60	$^{\circ}$ C
AM performance; note 1						
V_{11}	AF output voltage	$V_{i1} = 5$ mV	36	45	70	mV
V_{i1}	RF sensitivity input voltage	$(S+N)/N = 26$ dB	40	55	70	μ V
THD	total harmonic distortion	$V_{i1} = 1$ mV	–	0.8	2.0	%
FM performance; note 2						
V_{11}	AF output voltage	$V_{i5} = 1$ mV	40	48	57	mV
V_{i5}	RF sensitivity input voltage	V_{11} at –3 dB; V_{11} is 0 dB at $V_{i5} = 1$ mV	0.4	1.2	3.8	μ V
THD	total harmonic distortion	IF filter SFE10.7MS3A20K-A	–	0.3	0.8	%
MPX performance; note 3						
α_{cs}	channel separation		26	30	–	dB

Notes

- $V_{CC1} = 3$ V; $V_{CC2} = 12$ V; $V_{DDD} = 3$ V; $f_i = 1$ MHz; $m = 0.3$; $f_m = 1$ kHz; measured in Fig.11 with S1 in position A; S2 in position B; unless otherwise specified.
- $V_{CC1} = 3$ V; $V_{CC2} = 12$ V; $V_{DDD} = 3$ V; $f_i = 100$ MHz; $\Delta f_m = 22.5$ kHz; $f_m = 1$ kHz; measured in Fig.11 with S2 in position A; S3 in position A and S5 in position A; unless otherwise specified.
- $V_{CC1} = 3$ V; $V_{CC2} = 12$ V; $V_{DDD} = 3$ V; $V_{i3(L+R)} = 155$ mV; $V_{pilot} = 15.5$ mV; $f_i = 1$ kHz; measured in Fig.11 with S2 in position B; S3 in position B; unless otherwise specified.

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BLOCK DIAGRAM

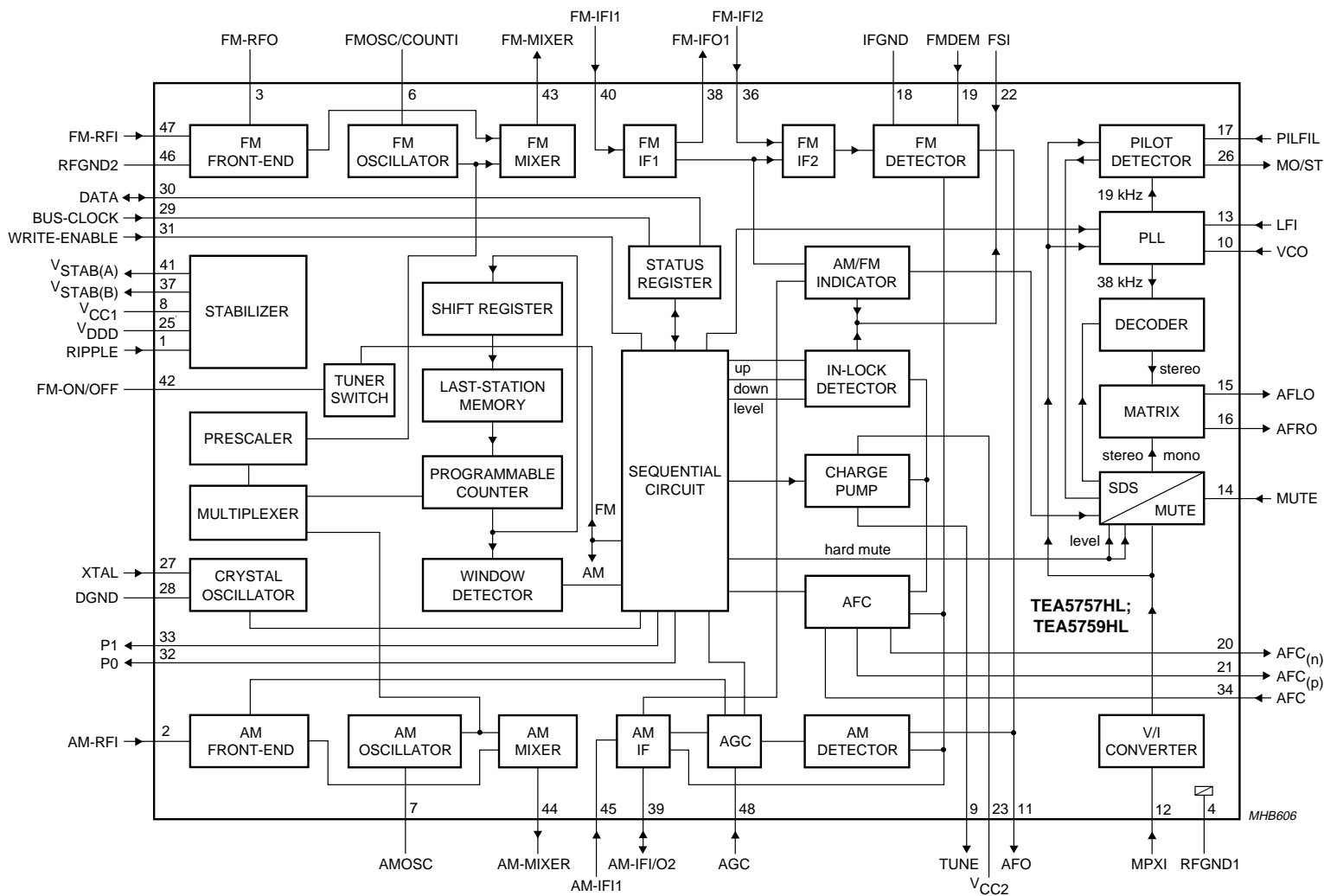


Fig.1 Block diagram.

Self Tuned Radio (STR)

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PINNING

SYMBOL	PIN	DESCRIPTION
RIPPLE	1	ripple capacitor input
AM-RFI	2	AMRF input
FM-RFO	3	parallel tuned FMRF circuit to ground
RFGND1	4	RF ground 1 and substrate
CGND	5	counter ground
FMOSC/COUNTI	6	parallel tuned FM-oscillator circuit to ground/counter input
AMOSC	7	parallel tuned AM-oscillator circuit to ground
V _{CC1}	8	supply voltage
TUNE	9	tuning current output
VCO	10	voltage controlled oscillator input
AFO	11	AM/FM AF output (output impedance typical 5 k Ω)
MPXI	12	stereo decoder input (input impedance typical 150 k Ω)
LFI	13	loop filter input
MUTE	14	mute input
AFLO	15	left channel output (output impedance typical 4.3 k Ω)
AFRO	16	right channel output (output impedance typical 4.3 k Ω)
PILFIL	17	pilot detector filter input
IFGND	18	ground of IF, detector and MPX stage
FMDEM	19	ceramic discriminator input
AFC _(n)	20	AFC negative output
AFC _(p)	21	AFC positive output
FSI	22	field strength indicator
V _{CC2}	23	supply voltage for tuning
n.c.	24	not connected
V _{DDD}	25	digital supply voltage
MO/ST	26	mono/stereo and tuning indication output
XTAL	27	crystal input
DGND	28	digital ground
BUS-CLOCK	29	bus-clock input
DATA	30	bus data input/output
WRITE-ENABLE	31	bus write-enable input
P0	32	programmable output port (P0)
P1	33	programmable output port (P1)
AFC	34	450 kHz LC circuit
n.c.	35	not connected
FM-IFI2	36	FMIF input 2 (input impedance typical 330 Ω)
V _{STAB(B)}	37	internal stabilized supply voltage (B)
FM-IFO1	38	FMIF output 1 (output impedance typical 330 Ω)
AM-IFI/O2	39	input/output to IF-Tank (IFT); output: current source
FM-IFI1	40	FMIF input 1 (input impedance typical 330 Ω)

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SYMBOL	PIN	DESCRIPTION
V _{STAB(A)}	41	internal stabilized supply voltage (A)
FM-ON/OFF	42	FM ON/OFF port
FM-MIXER	43	ceramic filter output (output impedance typical 330 Ω)
AM-MIXER	44	open-collector output to IFT
AM-IFI1	45	IFT or ceramic filter input (input impedance typical 3 kΩ)
RFGND2	46	FMRF ground 2
FM-RFI	47	FMRF aerial input (input impedance typical 40 Ω)
AGC	48	AGC capacitor input

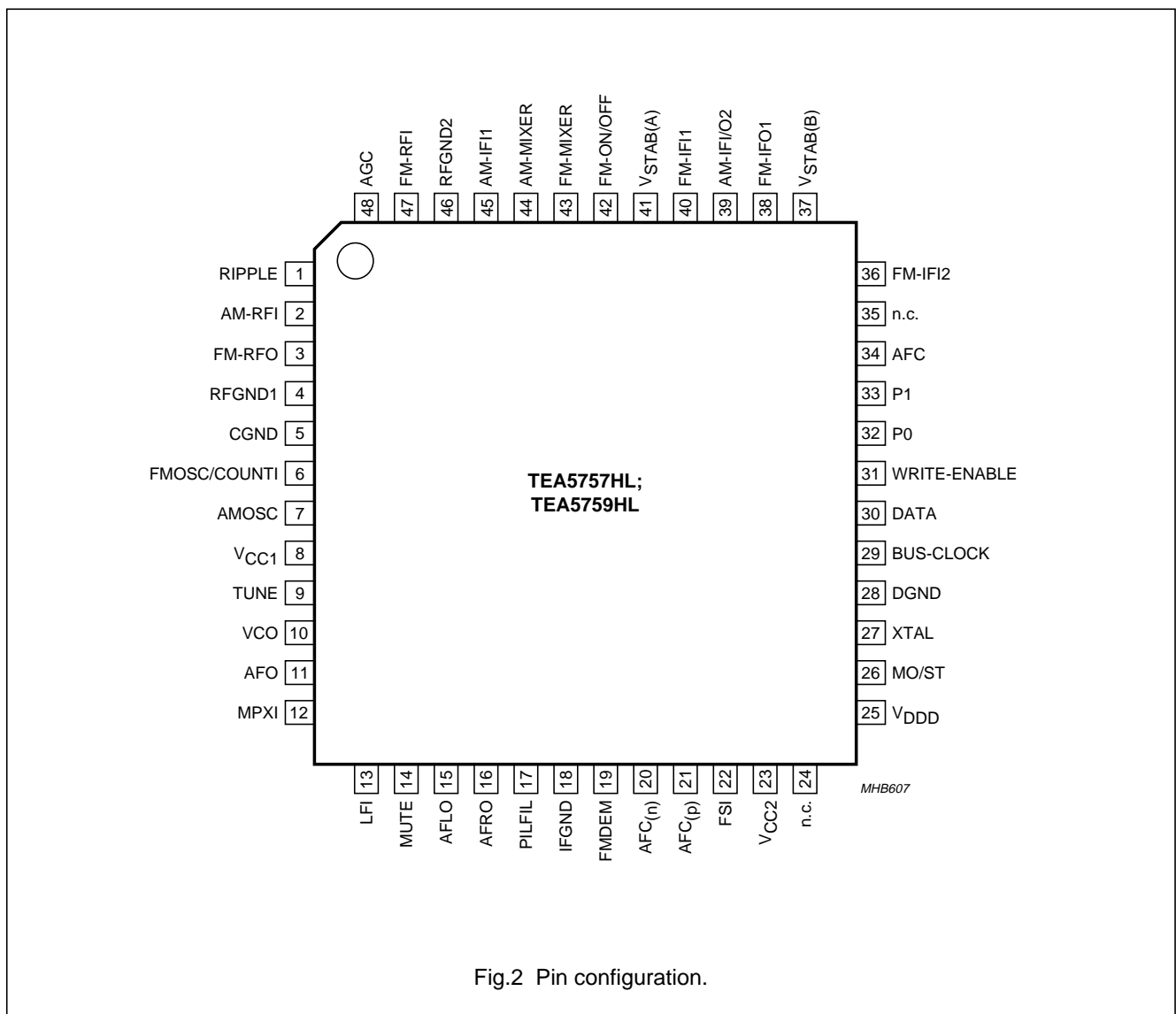


Fig.2 Pin configuration.

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FUNCTIONAL DESCRIPTION

The TEA5757HL; TEA5759HL is an integrated AM/FM stereo radio circuit including digital tuning and control functions.

The radio

The AM circuit incorporates a double balanced mixer, a one-pin low-voltage oscillator (up to 30 MHz) and is designed for distributed selectivity.

The AM input is designed to be connected to the top of a tuned circuit. AGC controls the IF amplification and for large signals it lowers the input impedance of the AM front-end.

The first AM selectivity can be an IF-Tank (IFT) as well as an IFT combined with a ceramic filter; the second one is an IFT.

The FM circuit incorporates a tuned RF stage, a double balanced mixer, a one-pin oscillator and is designed for distributed IF ceramic filters. The FM quadrature detector uses a ceramic resonator.

The TEA5757HL; TEA5759HL can also be used with an external FM front-end circuit. The external front-end is activated by the FM-ON/OFF signal. The AFC circuit in the TEA5757HL; TEA5759HL provides a tuning voltage to drive the VCO of the external FM front-end. The frequency of the external VCO is counted in the Self Tuned Radio (STR) tuning system.

The PLL stereo decoder incorporates a signal dependent stereo-blend circuit and a soft-mute circuit.

Tuning

The tuning concept of Self Tuned Radio (STR) is based on FUZZY LOGIC: it mimics hand tuning (hand tuning is a combination of coarse and fine tuning to the qualitatively best frequency position). As a consequence the tuning system is very fast.

The tuning algorithm, which is controlled by the sequential circuit (see Fig.1), is completely integrated; so there are only a few external components needed.

The bus and the microcontroller can be kept very simple. The bus only consists of three wires (BUS-CLOCK, DATA and WRITE-ENABLE). The microcontroller must basically give two instructions:

- Preset operation
- Search operation.

PRESET OPERATION

In preset mode, the microcontroller has to load information such as frequency band, frequency and mono/stereo. This information has to be sent via the bus to the STR.

The internal algorithm controls the tuning sequence as follows:

1. The information is loaded into a shift register, a last-station memory and the counter.
2. The Automatic Frequency Control (AFC) is switched off.
3. The counter starts counting the frequency and the tuning voltage is varied until the desired frequency roughly equals the real frequency.
4. The AFC is then switched on and the counter is switched off.
5. The real frequency is more precisely tuned to the desired frequency.

After the AFC has tuned the real frequency to the desired frequency an in-lock signal can be generated. In order to get a reliable in-lock signal, there are two parameters measured: the field strength and the S-curve. The field strength indicates the strength of the station and by looking at the S-curve the system can distinguish false in-locks from real in-locks (false in-locks occur on the wrong slope of the S-curve).

In the event of fading or pulling the in-lock signal becomes logic 0 and the synthesizer will be switched on again and the algorithm will be repeated.

SEARCH OPERATION

During a search operation, the only action the microcontroller has to take is: sending the desired band plus the direction and the search sensitivity level to the STR. The search operation is performed by the charge pump until an in-lock signal is generated (combination of measuring the field strength and the S-curve). The AFC then fine tunes to the station. The frequency belonging to the found station will be counted by the counter and written into the last-station memory and the shift register of the counter. At this time the frequency is available in the shift register and can be read by the microcontroller.

The microcontroller decides whether the frequency is within the desired frequency band. If so, this frequency can be stored under a preset and if not, a new search action should be started.

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To ensure that the search function operates correctly under all conditions the following search sequence must be applied:

- Store the current frequency in the memory
- Issue the search command
- Wait for data valid and read the new frequency
- If the new frequency is the same as the stored frequency, issue a preset step (e.g. 50 kHz) and start the search sequence again.

TUNING CURRENTS FOR DIFFERENT CONDITIONS

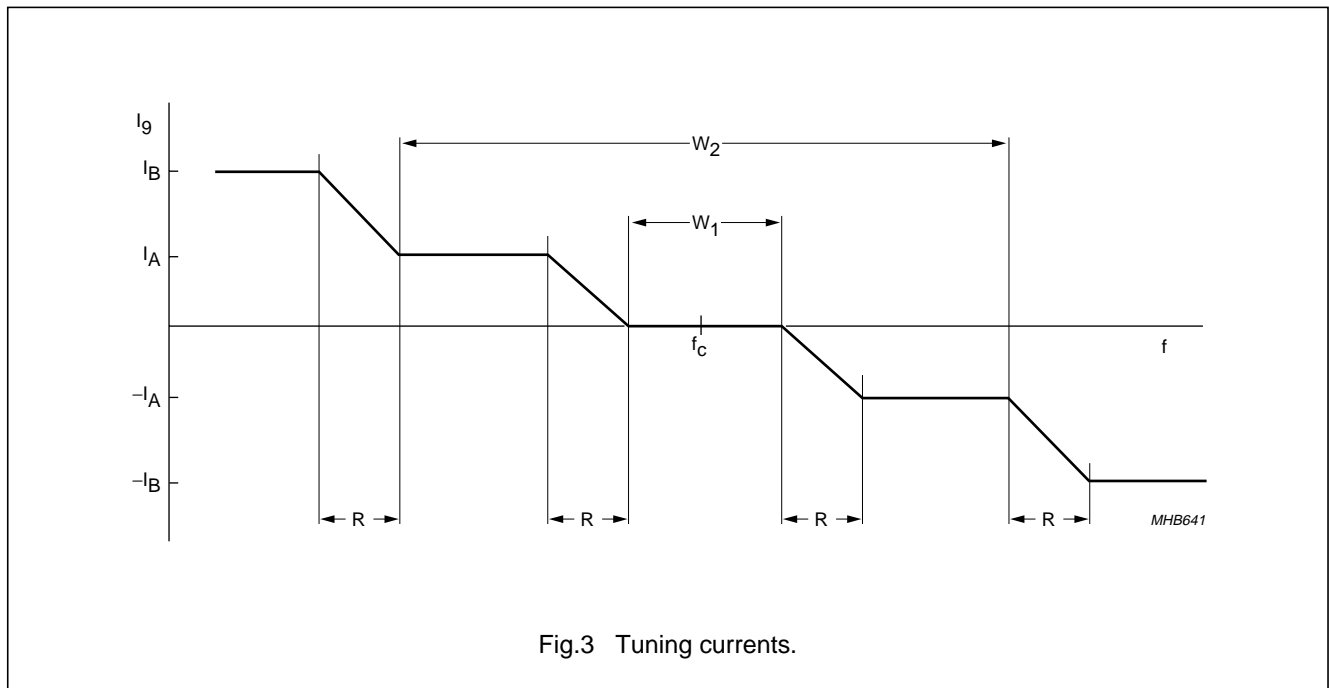


Fig.3 Tuning currents.

Table 1 Tuning currents

BAND SELECT	W ₁ (kHz)	W ₂ (kHz)	R (kHz)	I _A (μA)			I _B (μA)		
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FM	25	200	12.5	2	2.5	3	54	80	100
MW	3	64	1	2	2.5	3	54	80	100
LW	1	64	1	2	2.5	3	54	80	100
SW	1	64	1	0.4	0.5	0.7	12	16	20

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Description of the bus

The TEA5757HL; TEA5759HL radio has a bus which consists of three wires, as shown in Table 2.

Table 2 Bus signals

SIGNAL	DESCRIPTION	PIN
BUS-CLOCK	software driven clock input	29
DATA	data input/output	30
WRITE-ENABLE	write/read input	31

These three signals, together with the mono/stereo pin (MO/ST; pin 26), communicate with the microcontroller. The mono/stereo indicator has two functions, which are controlled by the BUS-CLOCK, as shown in Table 3.

Table 3 Bus-clock functions

BUS-CLOCK	MO/ST (PIN 26)	RESULT
LOW	LOW	stereo
LOW	HIGH	mono
HIGH	LOW	tuned
HIGH	HIGH	not tuned

The TEA5757HL; TEA5759HL has a 25-bit shift register; see Table 4 for an explanation of the shift register bits.

If in search mode no transmitter can be found, all frequency bits of the shift register are set to logic 0.

The bus protocol is illustrated in Figs 4 and 5.

Table 4 Explanation of the shift register bits

BIT	DESCRIPTION	LOGIC STATE	RESULT
S.24 (MSB)	search start/end	0	after a search when a station is found or after a preset
		1	during the search action
D.23	search up/down	0	indicates if the radio has to search down
		1	indicates if the radio has to search up
M.22	mono/stereo	0	stereo is allowed
		1	mono is required (radio switched to forced mono)
B0.21	band	see Table 5	selects FM/MW/LW/SW band
B1.20	band	see Table 5	selects FM/MW/LW/SW band
P0.19	port	note 1	user programmable bits which e.g. can be used as band switch driver
P1.18	port	note 1	user programmable bits which e.g. can be used as band switch driver
S0.17	search-level of station	see Table 6	determines the locking field strength during an automatic search, automatic store or manual search
S1.16	search-level of station	see Table 6	determines the locking field strength during an automatic search, automatic store or manual search
15	dummy	–	buffer
F.14 to F.0 (LSB)	frequency	–	determine the tuning frequency of the radio; see Table 7 for the bit values

Note

1. The output pins 32 and 33 can drive currents up to 5 mA; bits P0.19 and P1.18 control the output voltage of the control pins P0 (pin 32) and P1 (pin 33):
 - a) Bit P0.19 LOW sets P0 (pin 32) to LOW.
 - b) Bit P0.19 HIGH sets P0 (pin 32) to HIGH.
 - c) Bit P1.18 LOW sets P1 (pin 33) to LOW.
 - d) Bit P1.18 HIGH sets P1 (pin 33) to HIGH.

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Table 5 Truth table for bits B0.21 and B1.20

B0.21	B1.20	BAND SELECT
0	0	FM ⁽¹⁾
0	1	MW
1	0	LW
1	1	SW

Note

- When FM is selected, the control output FM-ON/OFF (pin 42) is pulled to ground to switch-on the external FM front-end. Pin 42 is an open-collector pin with a series resistor R = 500 Ω.

Table 6 Truth table for bits S1.16 and S0.17

S1.16	S0.17	SIGNAL RECEPTION		
		FM IF INPUT (μV)	FM RF INPUT (μV)	AM RF INPUT (μV)
0	0	>50	>5	>28
0	1	>100	>10	>40
1	0	>300	>30	>63
1	1	>1500	>150	>1000

Table 7 Values for bits F.14 to F.0

BIT	BIT VALUE	FM VALUE ⁽¹⁾ (kHz)	AM VALUE ⁽²⁾ (kHz)
F.14	2 ¹⁴	–	16384
F.13	2 ¹³	102400	8192
F.12	2 ¹²	51200	4096
F.11	2 ¹¹	25600	2048
F.10	2 ¹⁰	12800	1024
F.9	2 ⁹	6400	512
F.8	2 ⁸	3200	256
F.7	2 ⁷	1600	128
F.6	2 ⁶	800	64
F.5	2 ⁵	400	32
F.4	2 ⁴	200	16
F.3	2 ³	100	8
F.2	2 ²	50	4
F.1	2 ¹	25	2
F.0	2 ⁰	12.5	1

Notes

- FM value of the affected oscillators:
 - FM VALUE = FMRF + FMIF (for TEA5757HL).
 - FM VALUE = FMRF – FMIF (for TEA5759HL).
- AM value of the affected oscillators:

AM VALUE = AMRF + AMIF.

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READING DATA

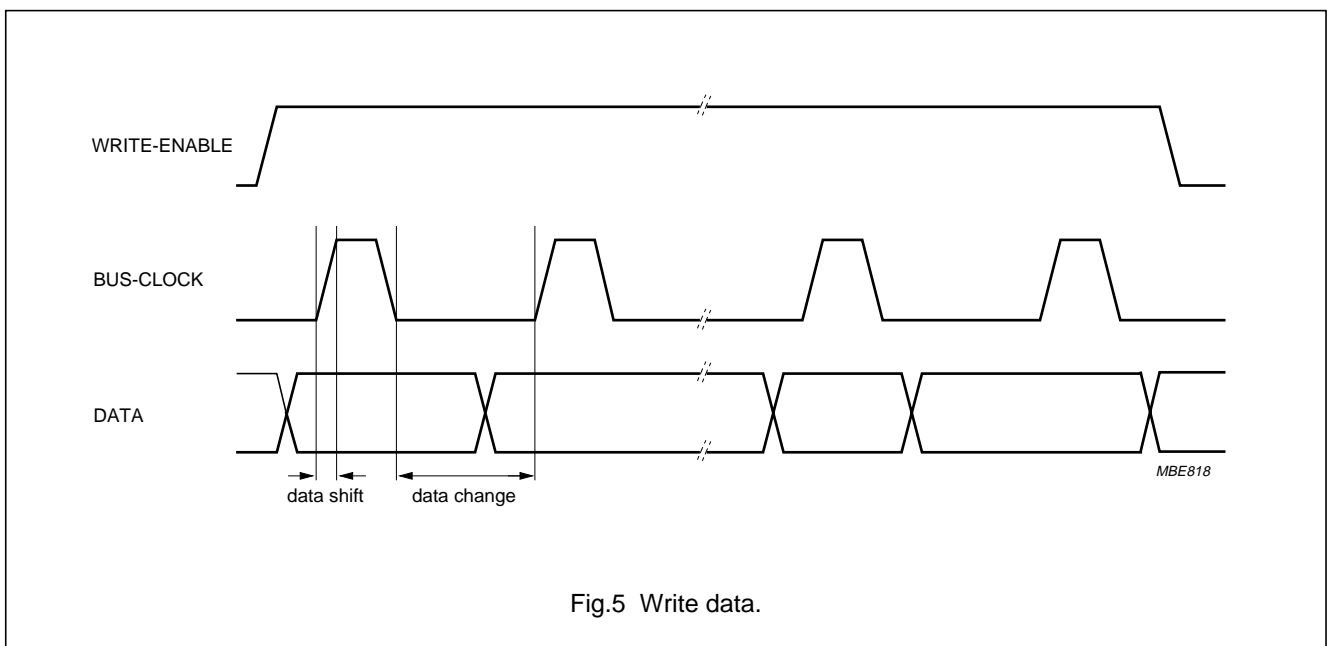
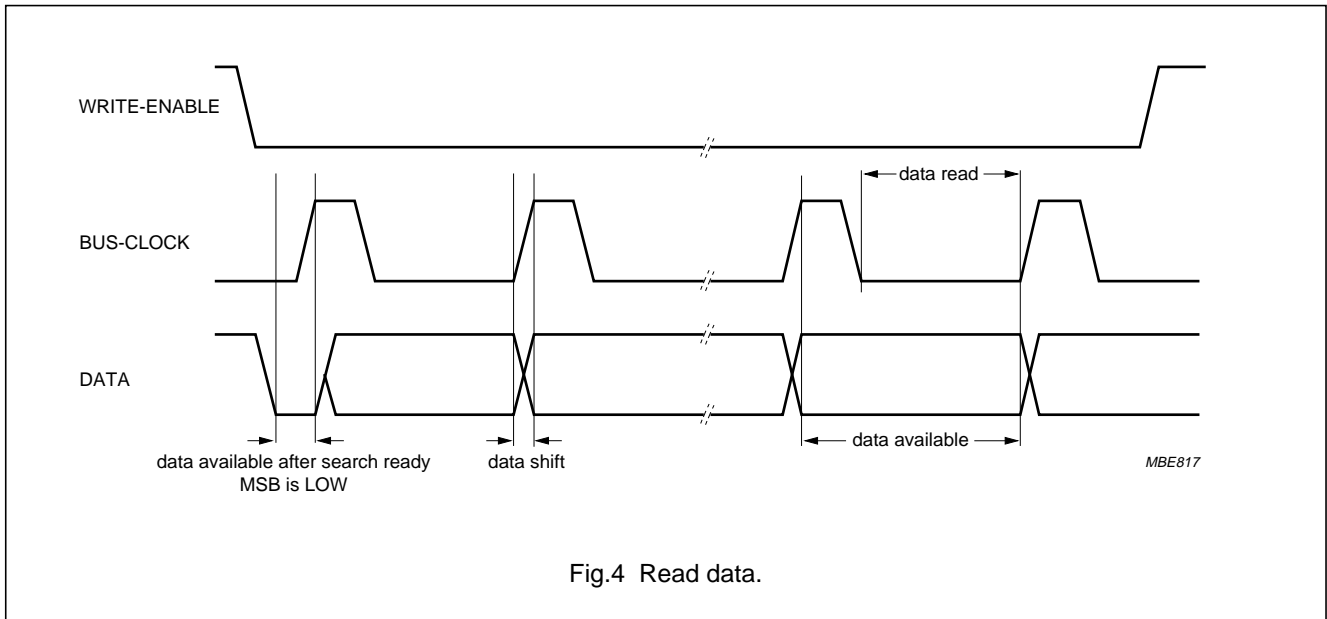
While WRITE-ENABLE is LOW data can be read by the microcontroller. At a rising edge of the BUS-CLOCK, data is shifted out of the register. This data is available from the point where the BUS-CLOCK is HIGH until the next rising edge of the BUS-CLOCK occurs (see Fig.4).

To read the entire shift register 24 clock pulses are necessary.

WRITING DATA

While WRITE-ENABLE is HIGH the microcontroller can transmit data to the TEA5757HL; TEA5759HL (hard mute is active). At a rising edge of the BUS-CLOCK, the register shifts and accepts one bit into LSB. At clock LOW the microcontroller writes data (see Fig.5).

To write the entire shift register 25 clock pulses are necessary.



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BUS TIMING

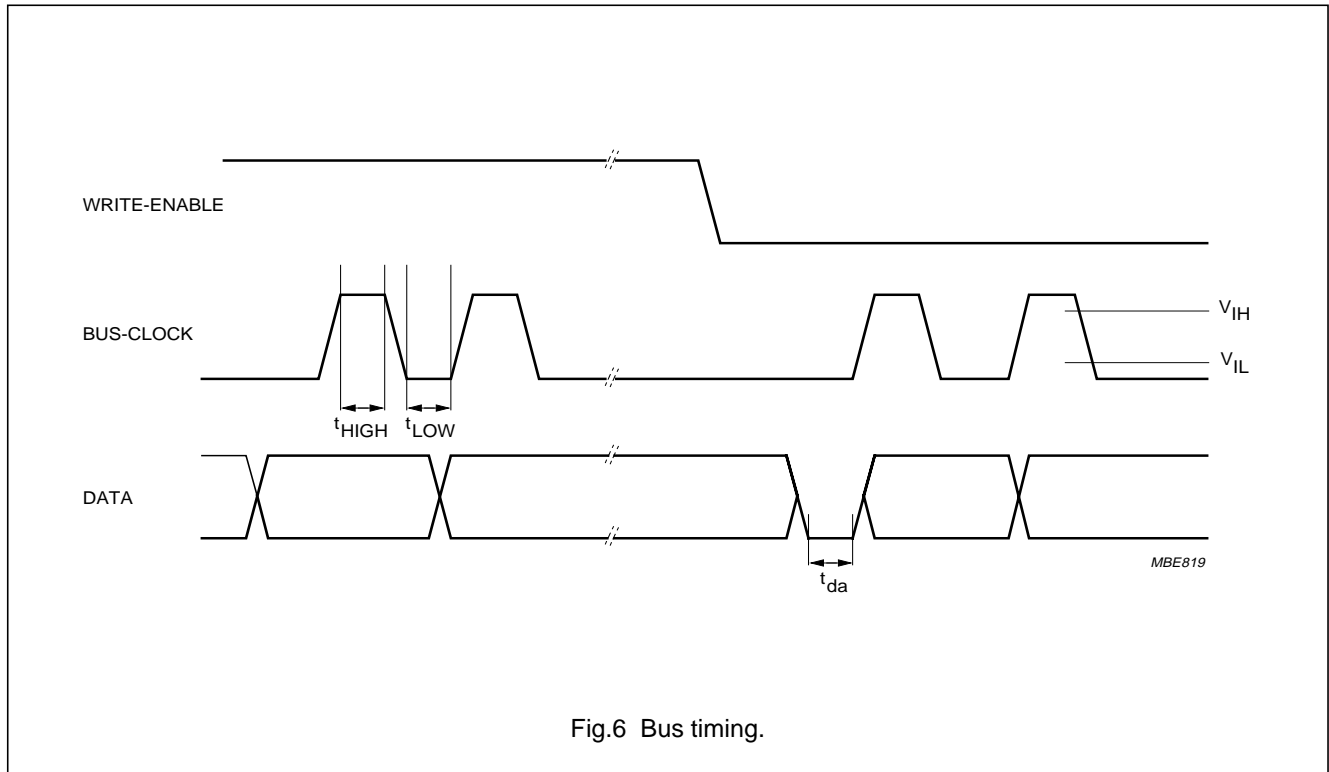


Fig.6 Bus timing.

Table 8 Digital inputs

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Digital inputs					
V_{IH}	HIGH-level input voltage		1.4	–	V
V_{IL}	LOW-level input voltage		–	0.6	V
Digital outputs (open-collector)					
I_{OL}	LOW-level output current		–	1 000	μA
V_{OL}	LOW-level output voltage	$I_{OL} = 600 \mu A$	–	0.6	V
Timing					
f_{clk}	clock input		–	300	kHz
t_{HIGH}	clock HIGH time		1.67	–	μs
t_{LOW}	clock LOW time		1.67	–	μs
t_{da}	shift register available after 'search ready'		–	14	μs

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC1}	supply voltage		0	13.2	V
P_{tot}	total power dissipation	$T_{amb} = 70\text{ °C}$	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature		–15	+60	°C
T_j	junction temperature		–15	+150	°C
V_{es}	electrostatic handling voltage for all pins	note 1	–	±200	V

Note

1. Charge device model; equivalent to discharging a 200 pF capacitor via a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	75	K/W

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CHARACTERISTICS

$V_{CC1} = 3\text{ V}$; $T_{amb} = 25\text{ °C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage		2.5	–	12	V
V_{CC2}	supply voltage for tuning		–	–	12	V
V_{DDD}	supply voltage for digital part		2.5	–	12	V
V_{tune}	tuning voltage		0.7	–	$V_{CC2} - 0.75$	V
I_{CC2}	supply current for tuning in preset mode (band-end to band-end)		–	–	800	μA
$f_{\text{BUS-CLOCK(max)}}$	maximum BUS-CLOCK frequency		–	–	300	kHz
I_{CC1}	current consumption during acquisition of V_{CC1}	AM mode	12	15	18	mA
		FM mode	12.5	15.5	18.5	mA
I_{DD}	current consumption during acquisition of I_{DD}	AM mode	–	4.8	–	mA
		FM mode	–	5.5	–	mA
I_{CC1}	current consumption after acquisition of V_{CC1}	AM mode	12	15	18	mA
		FM mode	13	16	19	mA
I_{DD}	current consumption after acquisition of I_{DD}	AM mode	–	3.3	–	mA
		FM mode	–	2.7	–	mA
t_{search}	synthesizer auto-search time for empty band	FM mode	–	–	10	s
t_{acq}	synthesizer preset acquisition time between two band limits	FM	–	100	–	ms
		MW	–	100	–	ms
		LW	–	200	–	ms
		SW	–	500 ⁽¹⁾	–	ms
f_{band}	frequency band range of the synthesizer	AM mode	0.144	–	30	MHz
		FM mode	50	–	150	MHz
Δf_{FM}	AFC inaccuracy of FM	note 2	–	–	1	kHz
Δf_{AM}	AFC inaccuracy of AM		–	–	100	Hz
$I_{P0(\text{sink})}$	sink current of software programmable output P0	$V_{32} = 3\text{ V}$	4	6	–	mA
$I_{P1(\text{sink})}$	sink current of software programmable output P1	$V_{33} = 3\text{ V}$	4	6	–	mA
$I_{P0(\text{source})}$	source current of software programmable output P0	$V_{32} = 0\text{ V}$	5	9	–	mA
$I_{P1(\text{source})}$	source current of software programmable output P1	$V_{33} = 0\text{ V}$	5	9	–	mA
$I_{42(\text{sink})}$	sink current of FM-ON/OFF switch	FM ON	4	6	–	mA

Notes

1. Depending on band.
2. In the application with external front-end the inaccuracy depends on the front-end.

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AM CHARACTERISTICS

Input frequency $f_i = 1$ MHz; $m = 0.3$; $f_m = 1$ kHz; measured in test circuit at pin 11 (see Fig.11); S2 in position B; V_{i1} measured at input of matching network at pin 2; matching network adjusted to maximum output voltage at low input level; $V_{i(n)}$ refers to test circuit (see Fig.11); V_n refers to pin voltages; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{11}	AF output voltage	$V_{i1} = 5$ mV	36	45	70	mV
		$V_{i2} = 0.2$ mV	12	30	45	mV
V_{i1}	RF sensitivity input voltage	(S+N)/N = 26 dB	40	55	70	μ V
V_{i1}	large signal voltage handling capacity	$m = 0.8$; THD $\leq 8\%$	150	300	–	mV
PSRR	power supply ripple rejection $\left(\frac{V_{11}}{\Delta V_8}\right)$	$\Delta V_8 = 100$ mV (RMS); 100 Hz; $V_8 = 3.0$ V	–	–47	–	dB
I_i	input current (pin 2)	$V_{48} = 0.2$ V	–	0	–	μ A
C_i	input capacitance (pin 2)	$V_{48} = 0.2$ V	–	–	4	pF
G_c	front-end conversion gain	$V_{48} = 0.2$ V	5	10	14	dB
		$V_{48} = 0.9$ V	–26	–14	0	dB
(S+N)/N	signal plus noise-to-noise ratio		–	50	–	dB
		$V_{i2} = 0.32$ mV	–	32	–	dB
THD	total harmonic distortion	$V_{i1} = 1$ mV	–	0.8	2.0	%
α_{450}	IF suppression	$V_{11} = 30$ mV	–	56	–	dB
I_{22}	indicator current	$V_{i2} = 0$ V; $V_{22} = 0$ V	–60	–50	–40	μ A
		$V_{i2} = 100$ mV; $V_{22} = 0$ V	–330	–285	–240	μ A
I_{14}	muting current	S4 in position B; $V_{14} = 1.4$ V; $V_{i2} = 100$ mV	12	16	20	μ A

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FM CHARACTERISTICS

Input frequency $f_i = 100$ MHz; $\Delta f = 22.5$ kHz; $f_m = 1$ kHz; measured in test circuit (see Fig.11) at pin 11; S2 in position B; $V_{i(n)}$ refers to test circuit (see Fig.11); V_n refers to pin voltages; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{11}	AF output voltage	$V_{i5} = 1$ mV	40	48	57	mV
V_{i5}	RF sensitivity input voltage	$(S+N)/N = 26$ dB	1	2	3.8	μ V
	RF limiting sensitivity	V_{11} at -3 dB; V_{11} is 0 dB at $V_{i5} = 1$ mV	0.4	1.2	3.8	μ V
V_{i1}	large signal voltage handling capacity	THD $\leq 5\%$	–	500	–	mV
PSRR	power supply ripple rejection $\left(\frac{V_{11}}{\Delta V_8}\right)$	$\Delta V_8 = 100$ mV (RMS); 100 Hz; $V_8 = 3.0$ V	–44	–	–	dB
G_c	front-end conversion gain $\left(\frac{V_{40}}{V_{i5}}\right)$		12	18	22	dB
$(S+N)/N$	signal plus noise-to-noise ratio	$V_{i5} = 2$ μ V	–	26	–	dB
		$V_{i5} = 1$ mV	–	62	–	dB
		$V_{i4} = 30$ μ V	33	38	–	dB
		$V_{i4} = 10$ mV	62	–	–	dB
THD	total harmonic distortion	IF filter SFE10.7MS3A20K-A detector CDA10.7MG40-A $\Delta f = 22.5$ kHz	–	0.3	0.8	%
		$\Delta f = 75$ kHz	–	1.5	3	%
I_{22}	indicator current	$V_{i4} = 0$ V; $V_{22} = 0$ V	–90	–60	–30	μ A
		$V_{i4} = 100$ mV; $V_{22} = 0$ V	–330	–285	–240	μ A
I_{14}	muting current	$V_{14} = 1.4$ V; $V_{i2} = 0$ mV	3	4.5	6	μ A
		$V_{14} = 1.4$ V; $V_{i2} = 100$ mV	8	12	17	μ A

Self Tuned Radio (STR)

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STEREO DECODER CHARACTERISTICS

$V_{i3(L+R)} = 155 \text{ mV}$; $V_{\text{pilot}} = 15.5 \text{ mV}$; $f = 1 \text{ kHz}$; apply unmodulated RF-signal of 100 mV to front-end to set radio to maximum channel separation; soft mute off (S4 in position A); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_o	output resistance (pins 15 and 16)		–	4.3	–	$k\Omega$
R_i	input resistance (pin 12)		–	180	–	$k\Omega$
$V_{15/16}$	AF output voltage		–	160	–	mV
$V_{\text{pilot}(s)}$	switch to stereo		–	8	12	mV
$V_{\text{pilot}(m)}$	switch to mono		2	5	–	mV
$\Delta f/f$	capture range	$V_{\text{pilot}} = 15 \text{ mV}$	3	4	8	%
V_{AF-L}/V_{i3}	MPX voltage gain		–1.5	–	+1.5	dB
$(S+N)/N$	signal plus noise-to-noise ratio	$V_{\text{pilot}} = 15.5 \text{ mV}$ (stereo)	–	74	–	dB
		$V_{\text{pilot}} = 0 \text{ mV}$ (mono)	–	80	–	dB
THD	total harmonic distortion		–	0.5	1.0	%
α_{cs}	channel separation		26	30	–	dB
α_{cub}	channel unbalance		–	0	1	dB
I_{26}	stereo indicator current	$V_{26} = V_{CC1}$; clock = LOW				
		$V_{\text{pilot}} = 15.5 \text{ mV}$	600	800	–	μA
		$V_{\text{pilot}} = 0 \text{ mV}$	–	15	30	μA
α_{19}	carrier and harmonic suppression	19 kHz (200 mV) = 0 dB	27	32	–	dB
α_{38}		38 kHz	16	21	–	dB
α	stereo-blend	$V_{i5} = 200 \mu\text{V}$	22	30	–	dB
		$V_{i5} = 20 \mu\text{V}$	–	1	2	dB
mute(s)	soft mute depth	$V_{i5} = 3 \mu\text{V}$; $V_{15} = V_{16}$	–1	0	–	dB
		$V_{i5} = 1 \mu\text{V}$; $V_{15} = V_{16}$	–10	–6	–	dB

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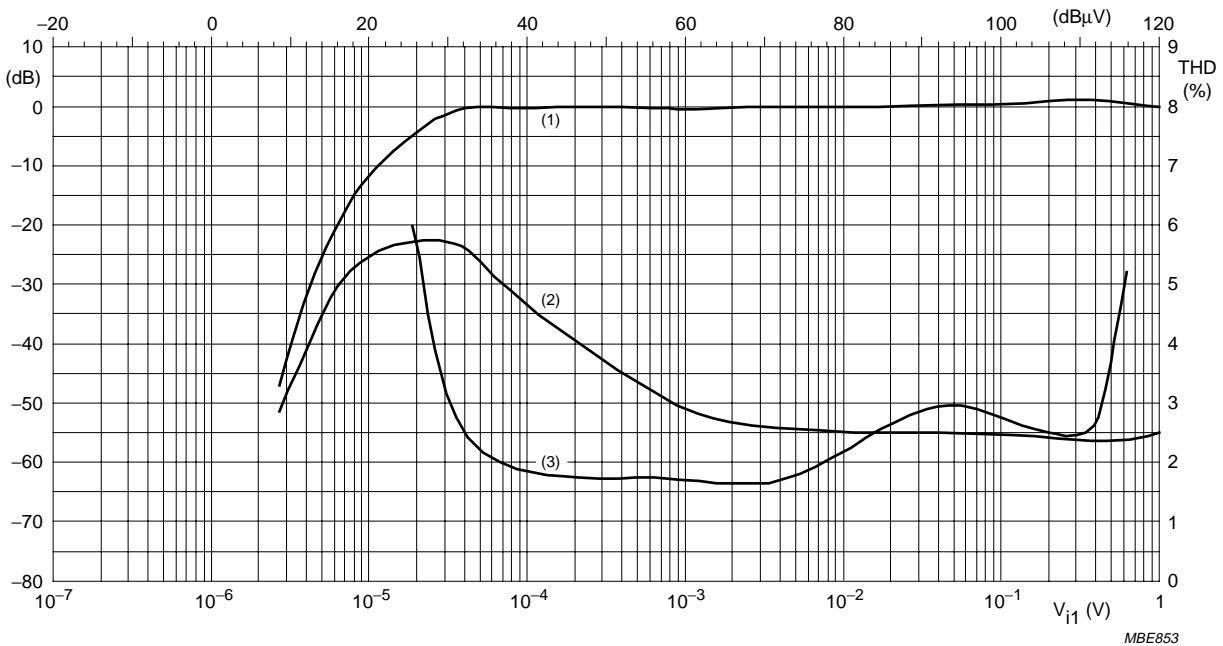
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TUNING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{FM(IF)}$	FM IF voltage levels	α_{-3} dB-point at $V_{i4} = 20 \mu V$				
	high (auto-store/search)	$S0 = 1; S1 = 1$	600	1500	5000	μV
	medium (auto-store/search)	$S0 = 0; S1 = 1$	100	300	550	μV
	low (auto-store/search)	$S0 = 1; S1 = 0$	40	100	200	μV
$V_{FM(RF)}$	FM RF voltage levels	α_{-3} dB-point at $V_{i5} = 2 \mu V$				
	high (auto-store/search)	$S0 = 1; S1 = 1$	60	150	500	μV
	medium (auto-store/search)	$S0 = 0; S1 = 1$	10	30	55	μV
	low (auto-store/search)	$S0 = 1; S1 = 0$	4	10	20	μV
V_{AM}	AM voltage levels	α_{-3} dB-point at $V_{i5} = 2 \mu V$				
	high (auto-store/search)	$S0 = 1; S1 = 1$	400	1000	2500	μV
	medium (auto-store/search)	$S0 = 0; S1 = 1$	50	63	80	μV
	low (auto-store/search)	$S0 = 1; S1 = 0$	32	40	50	μV
$V_{AFC(off)}$	AFC voltage off mode	α_{-3} dB-point at $V_{i5} = 2 \mu V$				
		FM mode	–	3	–	μV
		AM mode	–	25	–	μV
mute(h)	hard mute depth	WRITE-ENABLE = HIGH	–	60	–	dB
mute(p)	pull mute depth		–	15	–	dB
f_{max}	maximum frequency of FM prescaler		–	150	–	MHz
I_{26}	lock-in indicator current	$V_{26} = V_{CC1};$ clock = HIGH				
		tuning system locked	1200	1800	–	μA
		tuning system not locked	–	12	18	μA

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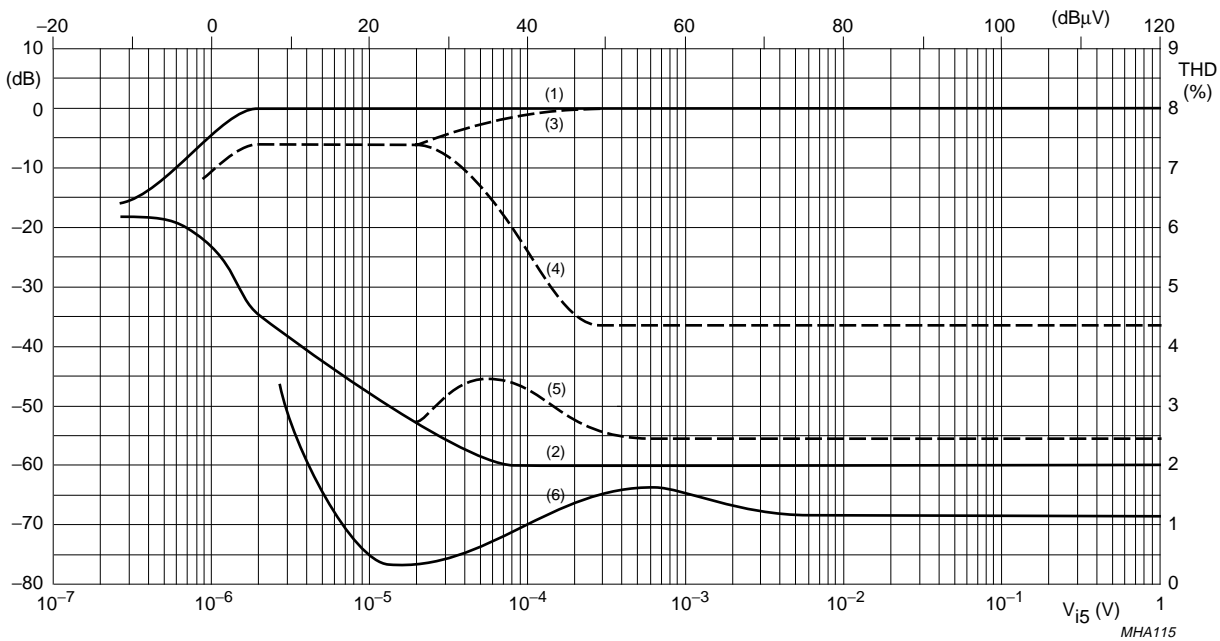


- (1) Audio signal.
- (2) Noise.
- (3) Harmonic distortion.

Fig.7 AM mode.

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- (1) Mono signal.
- (2) Noise in mono mode.
- (3) Left channel with modulation left.
- (4) Right channel with modulation left.
- (5) Noise in stereo mode.
- (6) Total harmonic distortion $\Delta f = 75$ kHz.

Fig.8 FM mode.

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INTERNAL CIRCUITRY

Table 9 Equivalent pin circuits and pin voltages

PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
1	RIPPLE	2.1	2.1	
2	AM-RFI	0	0	
3	FM-RFO	0	0	
4	RFGND1	-	-	
5	CGND	-	-	
6	FMOSC/ COUNTI	0	0	

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PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
7	AMOSC	0	0	
8	V _{CC1}	3.0	3.0	
9	TUNE	–	–	
10	VCO	1.3	0.95	
11	AFO	0.6	0.7	

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PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
12	MPXI	1.23	1.23	<p>MHB615</p>
13	LFI	0.1	0.8	<p>MHB616</p>
14	MUTE	0.7	0.7	<p>MHB617</p>
15	AFLO	0.65	0.65	<p>MHB618</p>

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PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
16	AFRO	0.65	0.65	
17	PILFIL	0.95	0.95	
18	IFGND	-	-	
19	FMDEM	-	1.0	
20	AFC _(n)	-	-	
21	AFC _(p)	-	-	

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PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
22	FSI	-	-	<p>MHB623</p>
23	V _{CC2}	-	-	
24	n.c.	-	-	
25	V _{DDD}	3.0	3.0	
26	MO/ST	-	-	<p>MHB624</p>
27	XTAL	-	-	<p>MHB625</p>
28	DGND	-	-	
29	BUS-CLOCK	-	-	<p>MHB626</p>

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PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
30	DATA	-	-	
31	WRITE-ENABLE	-	-	
32	P0	-	-	
33	P1	-	-	
34	AFC	-	-	
35	n.c.	-	-	
36	FM-IF12	-	0.73	

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PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
37	V _{STAB(B)}	1.4	1.4	
38	FM-IFO1	–	0.69	
39	AM-IFI/O2	1.4	1.4	
40	FM-IFI1	–	0.73	
41	V _{STAB(A)}	1.4	1.4	

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PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
42	FM-ON/OFF	-	-	
43	FM-MIXER	-	1.0	
44	AM-MIXER	1.4	1.4	
45	AM-IF1I	1.4	1.4	

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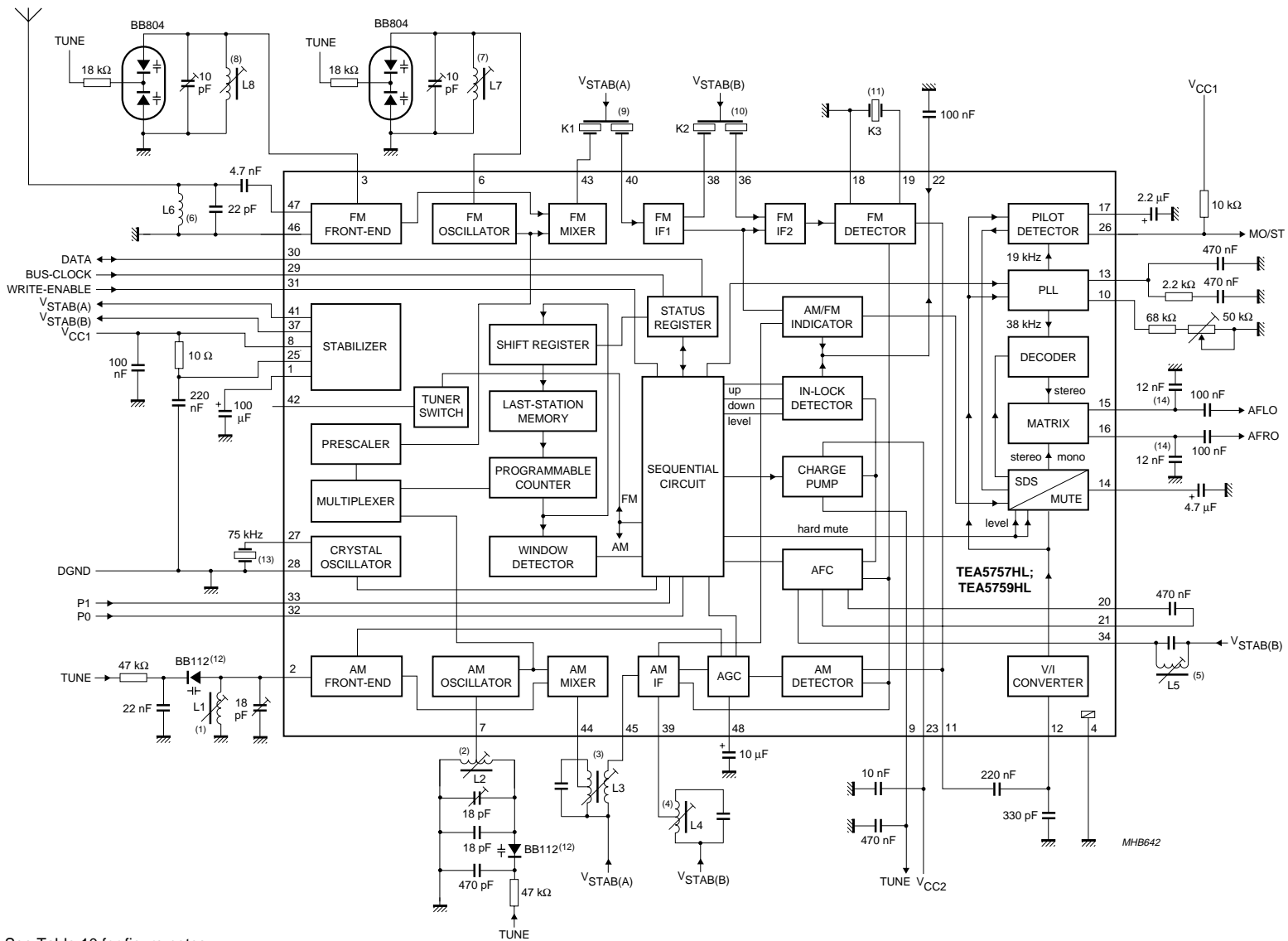
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PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
46	RFGND2	-	-	
47	FM-RFI	-	0.73	
48	AGC	0.1	0.7	

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TEST AND APPLICATION INFORMATION

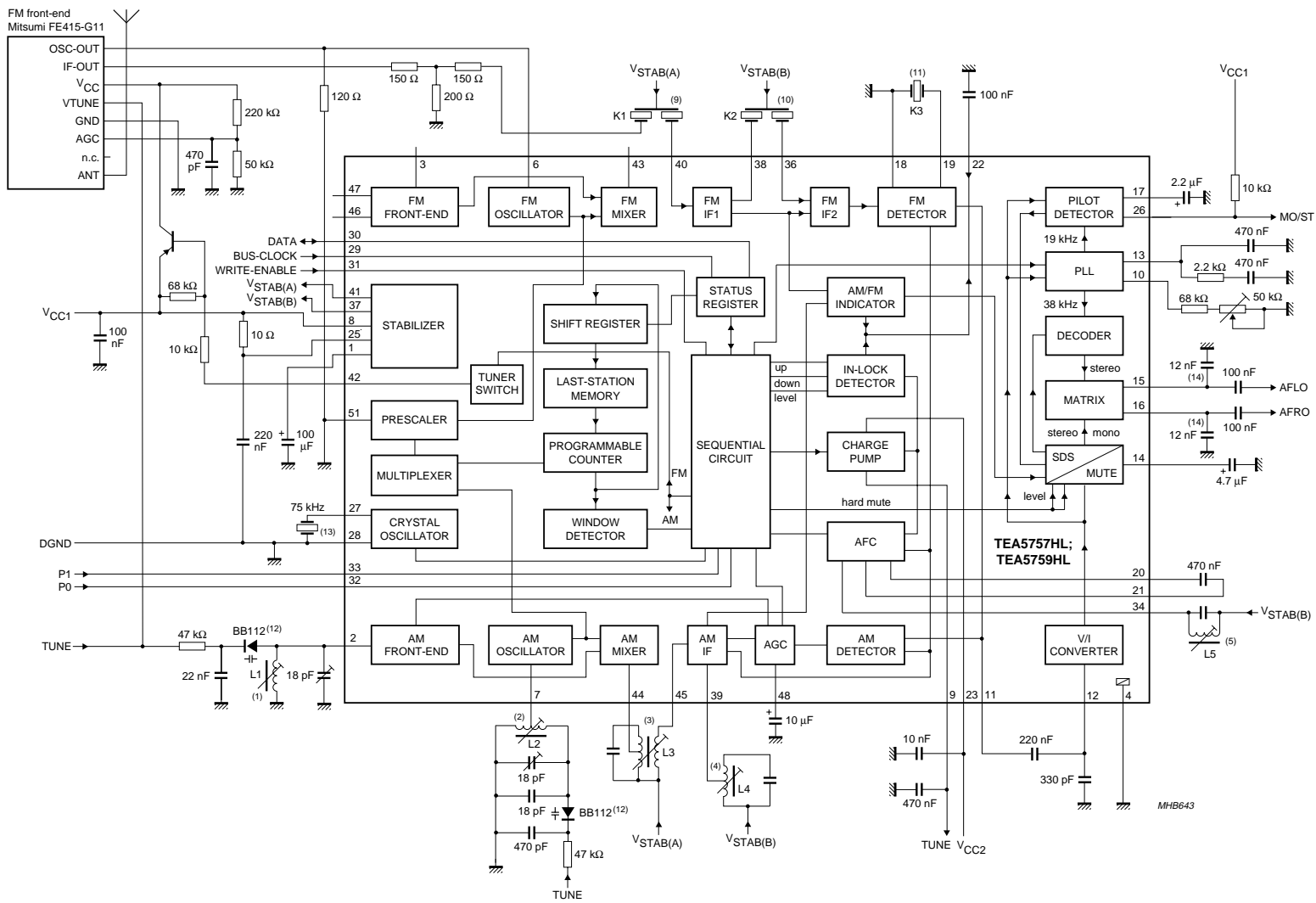


See Table 10 for figure notes.

Fig.9 Application diagram.

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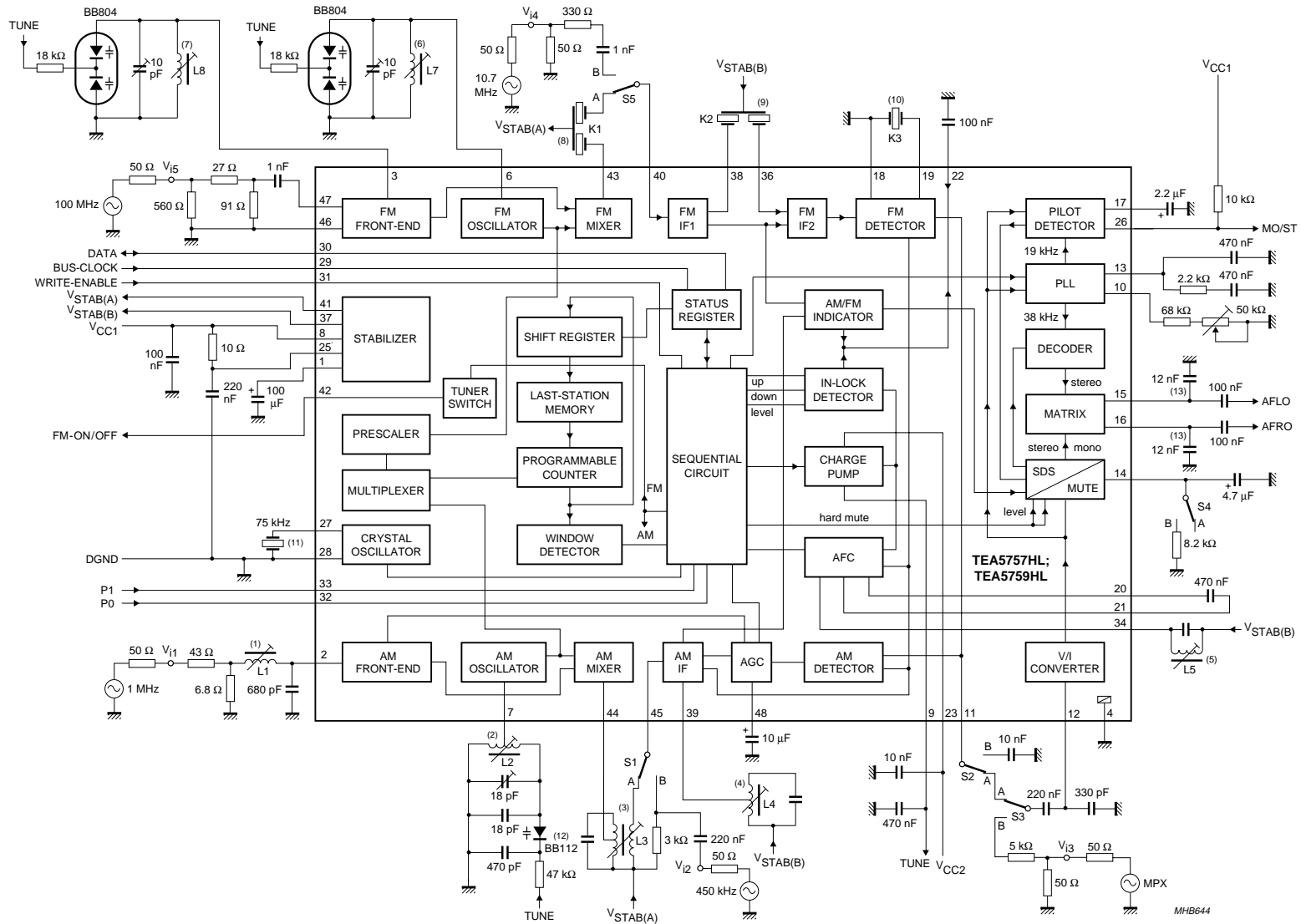


See Table 10 for figure notes.

Fig.10 Application diagram with external FM front-end.

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See Table 10 for figure notes.

Fig.11 Test circuit.

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Table 10 Test and application components

FIGURE NOTE	DESCRIPTION
Application diagrams; see Figs 9 and 10	
1	L1 = 250 μ H ferroceptor
2	L2 = 7P 7DRS-11459N, 110 μ H at 796 kHz, Q = 80, TOKO
3	L3 = 7P A7MCS-11844N, C = 180 pF, Q = 90, TOKO
4	L4 = 7P A7MCS-11845Y, C = 180 pF, Q = 90, TOKO
5	L5 = 7P A7MCS-11845Y, C = 180 pF, Q = 90, TOKO
6	L6 = 60 nH
7	L7 = MC117E523FN-2000242, 38 pF \pm 3%, TOKO
8	L8 = MC117E523FN-2000242, 38 pF \pm 3%, TOKO
9	K1 = SFE10.7MS3, MURATA
10	K2 = SFE10.7MS3, MURATA
11	K3 = CDA10.7-MC40-A, MURATA
12	alternatively BB512, Siemens or KV1561A, TOKO
13	standard application: \pm 30 ppm at $T_{amb} = 25$ °C short wave application: \pm 20 ppm at $T_{amb} = 25$ °C
14	de-emphasis time constant is 50 μ s: $C_{deem} = 12$ nF de-emphasis time constant is 75 μ s: $C_{deem} = 18$ nF
Test circuit; see Fig.11	
1	L1 = 22281-30091
2	L2 = 7P 7DRS-11459N, 110 μ H at 796 kHz, Q = 80, TOKO
3	L3 = 7P A7MCS-11844N, C = 180 pF, Q = 90, TOKO
4	L4 = 7P A7MCS-11845Y, C = 180 pF, Q = 90, TOKO
5	L5 = 7P A7MCS-11845Y, C = 180 pF, Q = 90, TOKO
6	L7 = MC117E523FN-2000242, 38 pF \pm 3%, TOKO
7	L8 = MC117E523FN-2000242, 38 pF \pm 3%, TOKO
8	K1 = SFE10.7MS3, MURATA
9	K2 = SFE10.7MS3, MURATA
10	K3 = CDA10.7-MG40-A, MURATA or CDACV10.7MG61-A, MURATA
11	standard application: \pm 30 ppm at $T_{amb} = 25$ °C short wave application: \pm 20 ppm at $T_{amb} = 25$ °C
12	alternatively BB512, Siemens or KV1561A, TOKO
13	de-emphasis time constant is 50 μ s: $C_{deem} = 12$ nF de-emphasis time constant is 75 μ s: $C_{deem} = 18$ nF

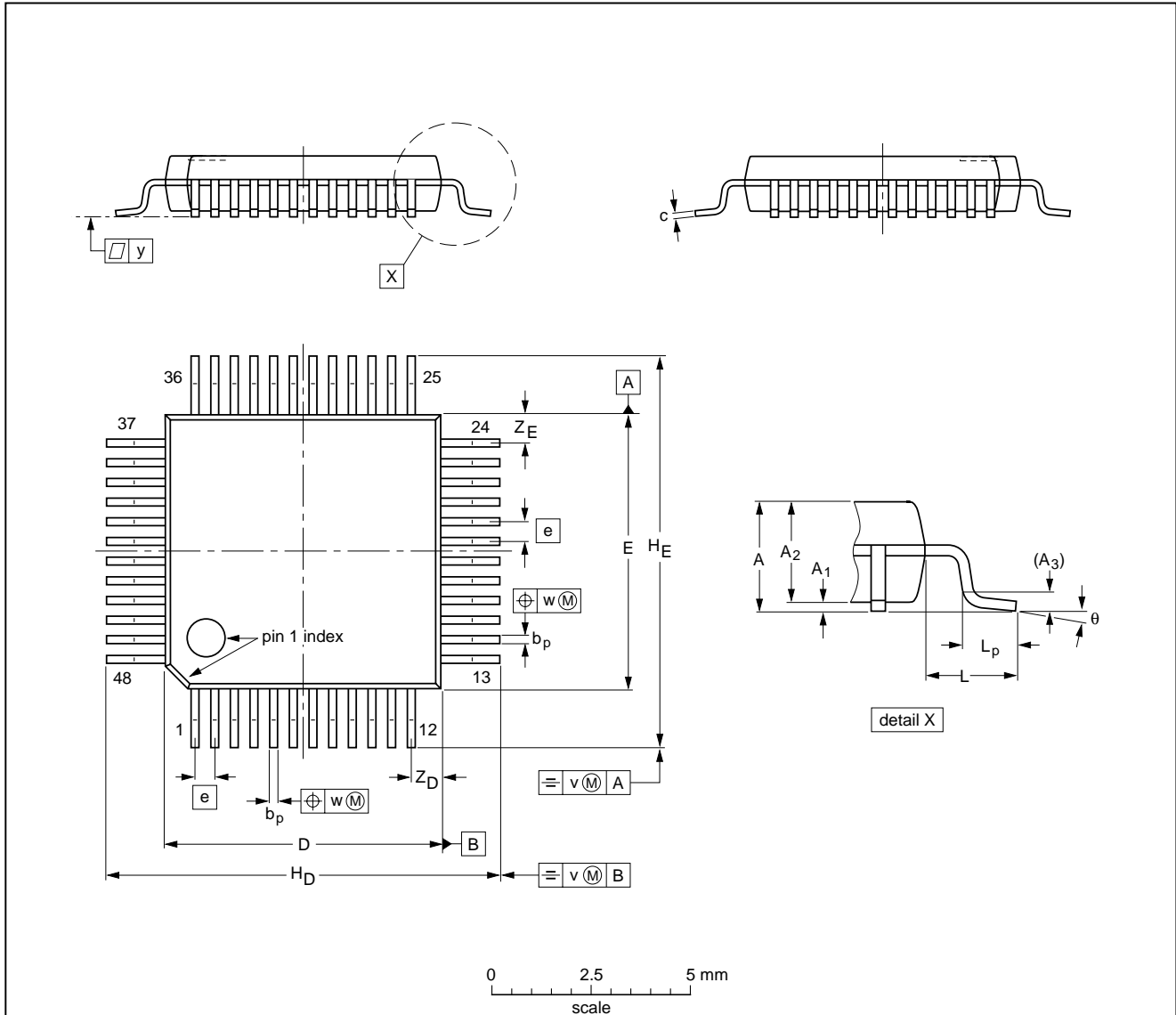
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PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

SOT313-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2	136E05	MS-026				99-12-27 00-01-19

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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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