SANYO Semiconductors
DATA SHEET

CMOS IC

LE25FW808 — 8M-bit (1024K×8) Serial Flash Memory with High-Density Read Mode

Overview

The LE25FW808 is 1024K×8bit Serial flash memory by 3.0V single power supply operation, and support serial peripheral interface (S.P.I.). There are three kinds of erase functions, Small Sector (8K bytes) erase, Sector (64K bytes) erase and Chip erase. If those erase is used properly according to the application, you can efficiently use the memory space. Page program can program the arbitrary data from 1 byte to 256 bytes. LE25FW808 has our original high-speed program function, page program time is 0.3ms (Typ.). Therefore, the overall rewriting time of 8M bit is 1.5s (Typ.), when combining with Chip erase. Moreover, LE25FW808 is stored in 8 pin very small package by making the best use of the feature of serial interface. According to these features, LE25FW808 is the best suited for applications in the portable electronic devices, that require re-programmable nonvolatile storage of program memory.

LE25FW808 has also the High-Density read mode (hereafter, HD_READ mode) that is the most high-speed data transfer in the world as the flash memory with serial interface. About eight times the data-transfer velocity can be achieved without changing the clock frequency used in a usual serial flash memory by using this mode. For instance, it is possible to read with 240Mbit/s in the maximum by using the HD_READ mode of 30MHz though a standard serial flash memory read with 30Mbit/s or less.

Features

- Read/write operations enabled by single 3.0V power supply: 2.7 to 3.6V supply voltage range
- Operating frequency : 50MHz
- Temperature range : 0 to 70°C
  –40 to +85°C (Planning)

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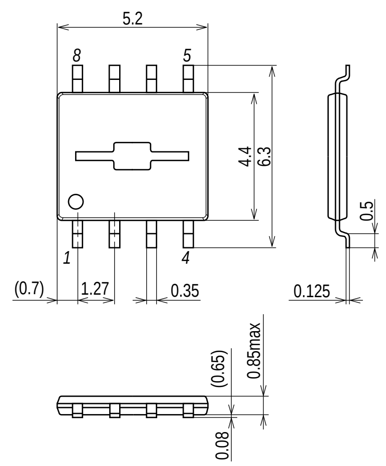
- Serial interface : SPI mode 0, mode 3 supported
- Sector size : 8K bytes/small sector, 64K bytes/sector
- Small sector erase, sector erase, chip erase functions
- Page program function (256 bytes/page)
- High-Density read mode (HD_READ)
- Block protect function
- Highly reliable read/write
  Number of rewrite times : 100,000 times
  Small sector erase time : 80ms (typ.), 300ms (max.)
  Sector erase time : 100ms (typ.), 400ms (max.)
  Chip erase time : 250ms (typ.), 3s (max.)
  Page program time : 0.3ms/256 bytes (typ.), 0.5ms/256 bytes (max.)
- Status functions
  Ready/busy information, protect information
- Data retention period : 20 years
- Package : LE25FW808TT MSOP8 (225mil)

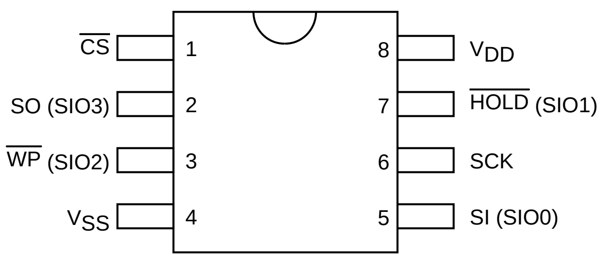
Package Dimensions

unit:mm (typ)
3276



SANYO : MSOP8(225mil)

Figure 1 Pin Assignments



Top view

Figure 2 Block Diagram

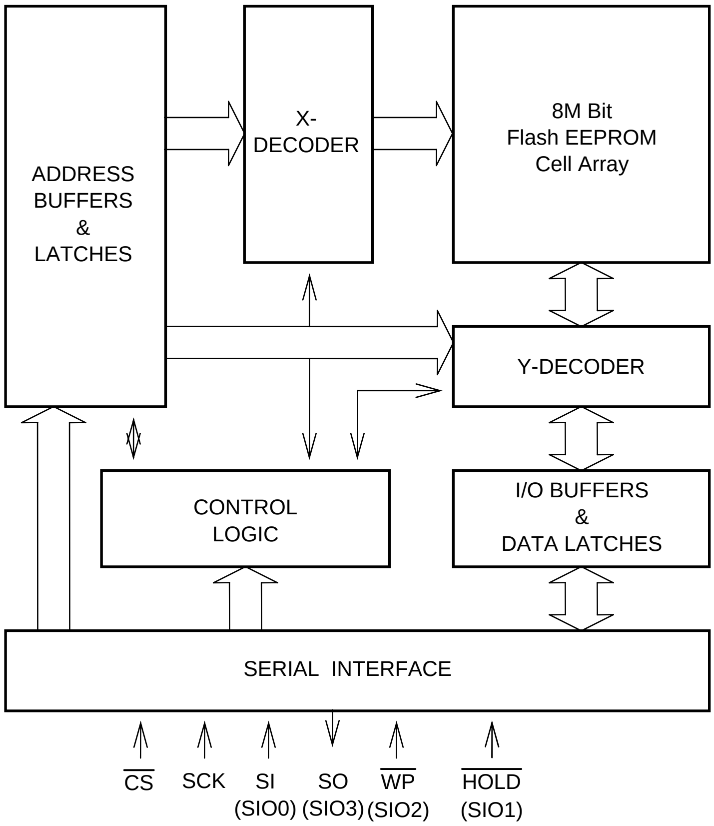


Table 1 Pin Description

***( )** HD_READ mode

Symbol	Pin Name	Description
SCK	Serial clock	This pin controls the data input/output timing.
SI (SIO0)	Serial data input (Serial data I/O0)	To input data or addresses serially from MSB to LSB (Least Significant Bit). (To input data or addresses and to output data serially in the HD_READ mode)
SO (SIO3)	Serial data output (Serial data I/O3)	To output data serially from MSB to LSB. (To input data or addresses and to output data serially in the HD_READ mode)
$\overline{CS}$	Chip select	The device becomes active when the logic level of this pin is low; it is deselected and placed in standby status when the logic level of the pin is high.
$\overline{WP}$ (SIO2)	Write-protect (Serial data I/O2)	To write-protect the block protect bits (BP0, BP1, BP2) and the status register write protect bit (SRWP) of the status register in co-operation with the status register write protect bit (SRWP). (To input data or addresses and to output data serially in the HD_READ mode)
$\overline{HOLD}$ (SIO1)	Hold (Serial data I/O1)	To pause any serial communications with the device without deselecting the device. (To input data or addresses and to output data serially in the HD_READ mode)
V_{DD}	Power supply	This pin supplies the 2.7 to 3.6V supply voltage.
V_{SS}	Ground	This pin supplies the 0V supply voltage.

Table 2 Command Settings

Command	1st bus cycle	2nd bus cycle	3rd bus cycle	4th bus cycle	5th bus cycle	6th bus cycle	Nth bus cycle
Read	03h	A23-A16	A15-A8	A7-A0			
	0Bh	A23-A16	A15-A8	A7-A0	X		
Set HD_READ mode	D4h	MD *1					
Small sector erase	D7h	A23-A16	A15-A8	A7-A0			
Sector erase	D8h	A23-A16	A15-A8	A7-A0			
Chip erase	C7h						
Page program	02h	A23-A16	A15-A8	A7-A0	PD *2	PD *2	PD *2
Write enable	06h						
Write disable	04h						
Power down	B9h						
Status register read	05h						
Status register write	01h	DATA					
Read silicon ID 1 *2	9Fh						
Read silicon ID 2 *4	ABh	X	X	A7-A0			
Exit power down mode	ABh						

Explanatory notes for Table 2

"X" signifies "don't care" (that is to say, any value may be input).

The "h" following each code indicates that the number given is in hexadecimal notation.

Addresses A23 to A20 for all commands are "Don't care".

In order for commands other than the read command to be recognized, $\overline{\text{CS}}$ must rise after all the bus cycle input.

*1. MD: mode register data. Various operation methods of the HD_READ mode such as the operation frequencies and the clock latency. Please refer to Table 3 for details.

*2: "PD" stands for page program data. Any amount of data from 1 to 256 bytes in 1-byte unit is input.

*3: Of the two silicon ID commands, it is for the command with the 9Fh setting that the manufacturer code 62h is first output. For as long as the clock input is continued, 20h of the device code is output continuously, followed by the repeated output of 62h and 20h.

*4: Read ID2 (ABh) A7 to A1 are don't care. A read cycle from address A0=‘0’ outputs the manufacture code (SANYO: 62h). A read cycle at address A0=‘1’ outputs the device code (20h).

Device Operation

The LE25FW808 features electrical on-chip erase functions using a single 3.0V power supply, that have been added to the EPROM functions of the industry standard that support serial interfaces. Interfacing and control are facilitated by incorporating the command registers inside the chip. The read, erase, program and other required functions of the device are executed through the command registers. The command addresses and data input in accordance with "Table 2 Command Settings" are latched inside the device in order to execute the required operations. "Figure 3 Serial Input Timing" shows the timing waveforms of the serial data input. First, at the falling $\overline{CS}$ edge the device is selected, and serial input is enabled for the commands, addresses, etc. These inputs are introduced internally in sequence starting with bit 7 in synchronization with the rising SCK edge. At this time, output pin SO is in the high-impedance state. The output pin is placed in the low-impedance state when the data is output in sequence starting with bit 7 synchronized to the falling clock edge during read, status register read and silicon ID. Refer to "Figure 4 Serial Output Timing" for the serial output timing.

The LE25FW808 supports both serial interface SPI mode 0 and SPI mode 3. At the falling $\overline{CS}$ edge, SPI mode 0 is automatically selected if the logic level of SCK is low, and SPI mode 3 is automatically selected if the logic level of SCK is high.

Figure 3 Serial Input Timing

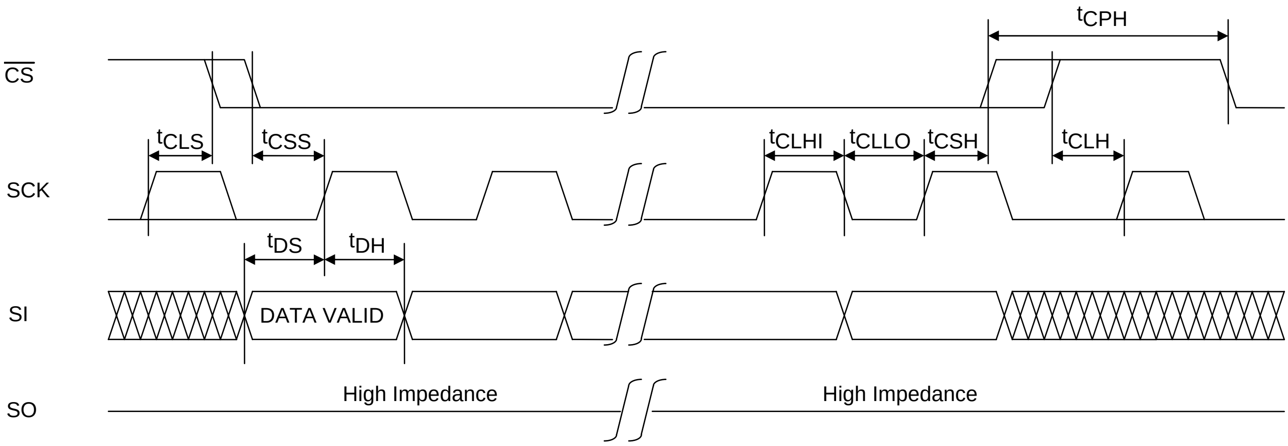
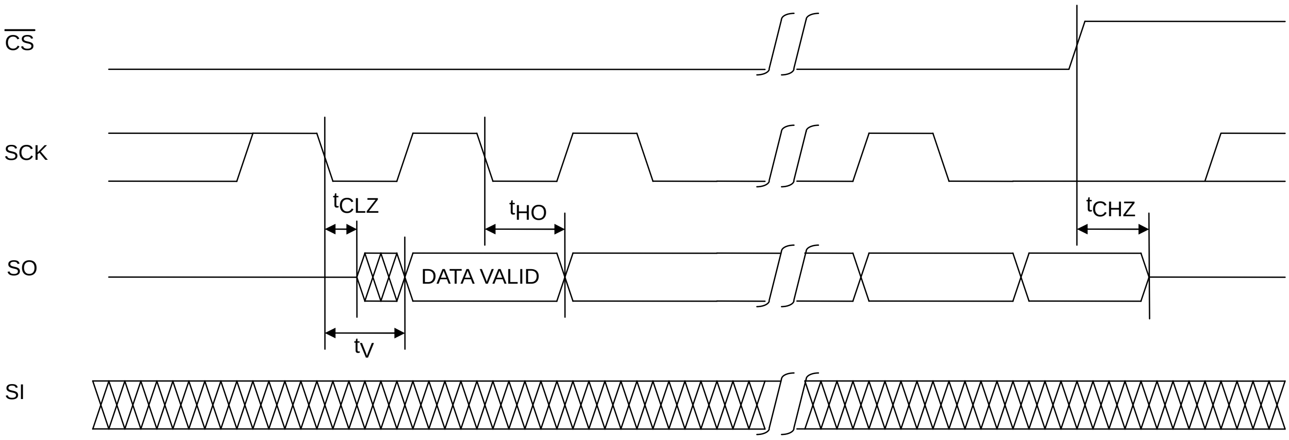


Figure 4 Serial Output Timing



Outline of High-Density read mode (HD_READ mode) operation

LE25FW808 has the HD_READ mode in addition to two kinds of normal read (4 bus read and 5 bus read). The HD_READ mode is greatly different from the normal mode in three points.
The first is the difference of the role of pins. Four pins (SO, WP, HOLD, SI) become I/O pins (SIO3 to SIO0) in the HD_READ mode while the input pin (SI) and the output pin (SO) are only one in the normal mode respectively as shown in Figure 2. Because SO, WP, HOLD and SI operate as I/O pin in the HD_READ mode, the setting of read address and the outputting read data become to be done from four pins.
The second is the difference of the relation between the clock and the data output. The rising edge of SCK is made a trigger for the address input and the falling edge of SCK is made a trigger for the data output in the normal mode. However, both edges of rising and falling of SCK will be done to the address taking and the data outputting in the HD_READ mode.
The third is the difference of the data composition at the time of reading. It is read by the ×16 bit in the HD_READ mode though it is read by the ×8 bit in the normal read. Therefore, please fix least significant bit (LSB) : A0 to L in the address input in HD_READ mode.

Pin Assignments

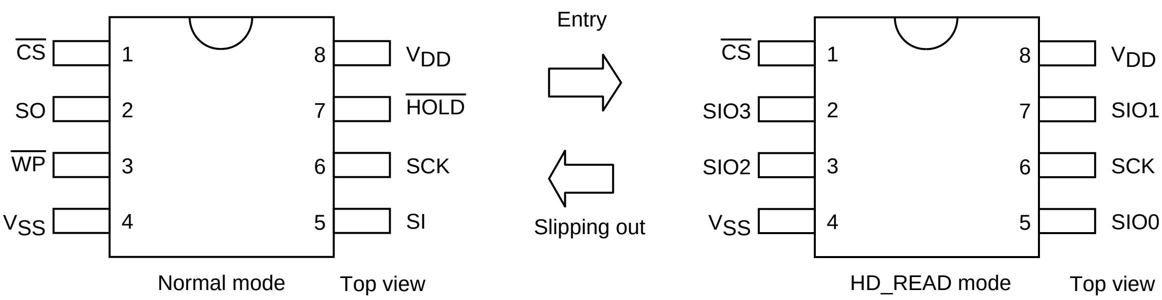
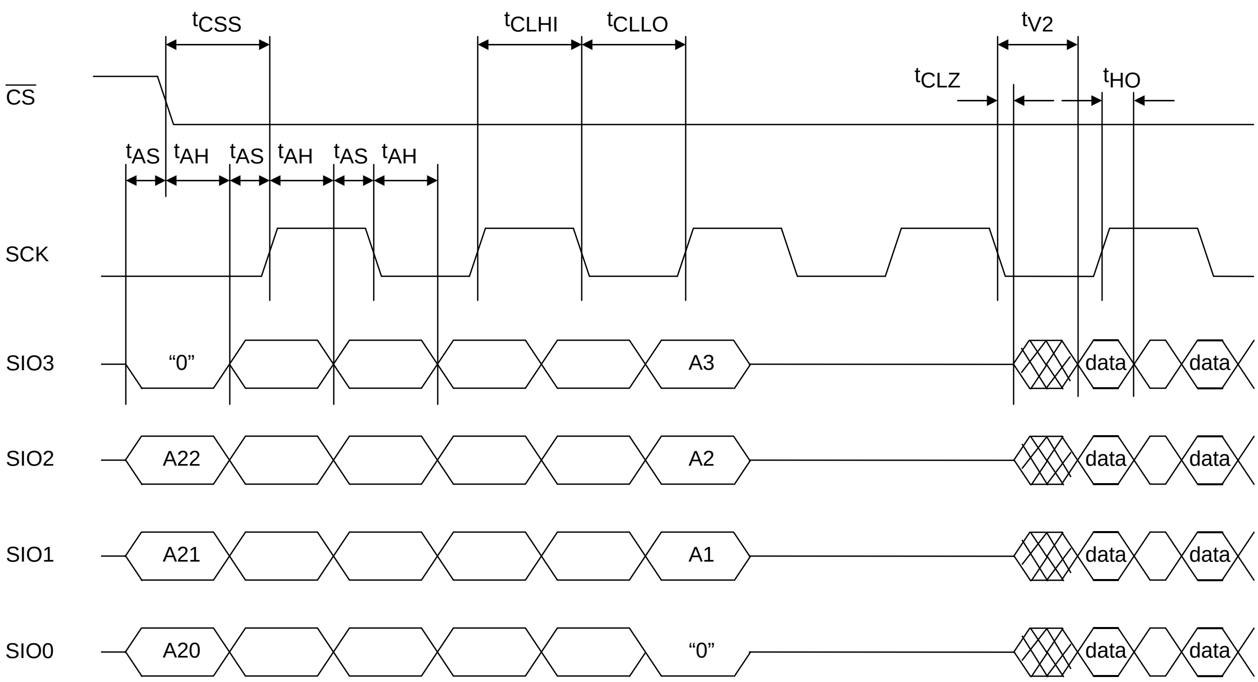


Figure 5: Serial input / output timing diagram for HD_READ mode (CL=1.0)



Command Definition

"Table 2 Command Settings" provides a list and overview of the commands. A detailed description of the functions and operations corresponding to each command is presented below.

1. Conventional Read

There are two read commands, the 4 bus cycle read command and 5 bus cycle read command. Consisting of the first through fourth bus cycles, the 4 bus cycle read command inputs the 24-bit addresses following (03h), and the data in the designated addresses is output synchronized to SCK. The data is output from SO on the falling clock edge of fourth bus cycle bit 0 as a reference. "Figure 6-a 4 Bus Read" shows the timing waveforms.
Consisting of the first through fifth bus cycles, the 5 bus cycle read command inputs the 24-bit addresses and 8 dummy bits following (0Bh). The data is output from SO using the falling clock edge of fifth bus cycle bit 0 as a reference. "Figure 6-b 5 Bus Read" shows the timing waveforms. The only difference between these two commands is whether the dummy bits in the fifth bus cycle are input.
When SCK is input continuously after the read command has been input and the data in the designated addresses has been output, the address is automatically incremented inside the device while SCK is being input, and the corresponding data is output in sequence. If the SCK input is continued after the internal address arrives at the highest address (FFFFFh), the internal address returns to the lowest address (00000h), and data output is continued. By setting the logic level of $\overline{CS}$ to high, the device is deselected, and the read cycle ends. While the device is deselected, the output pin SO is in a high-impedance state.

Figure 6-a 4 Bus Read

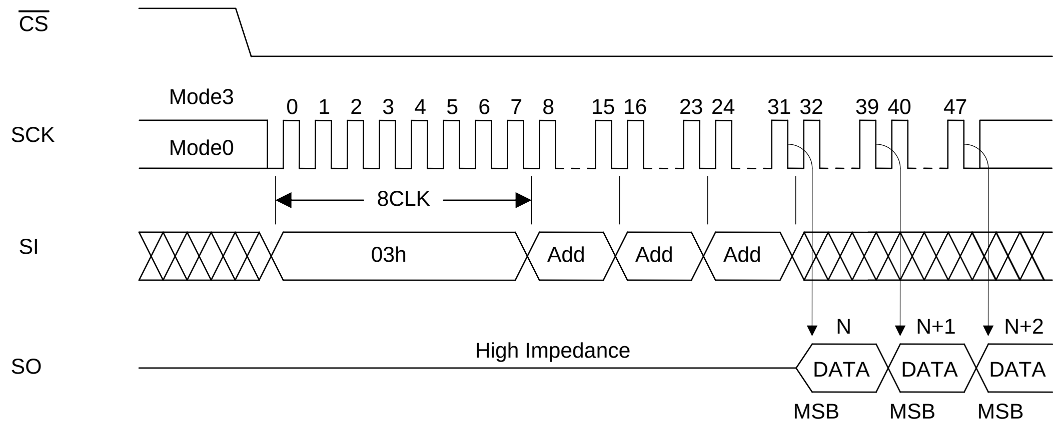
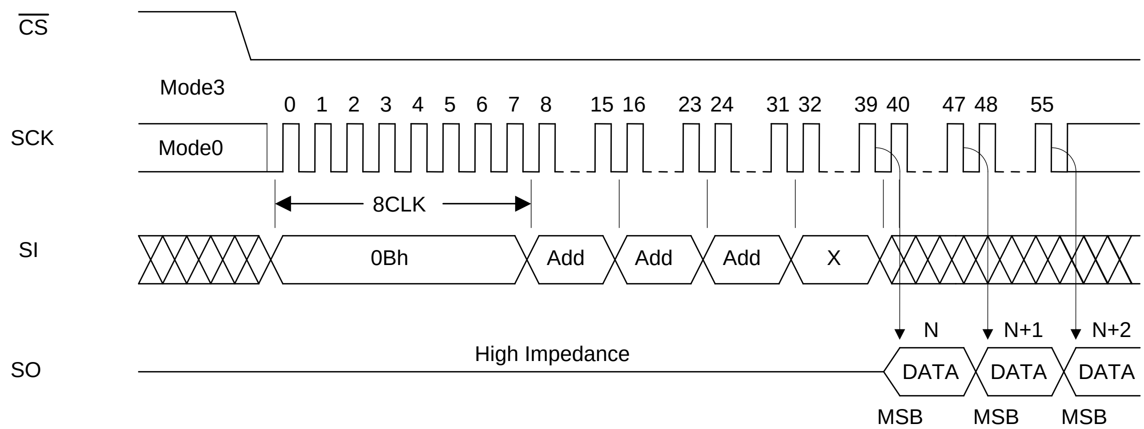


Figure 6-b 5 Bus Read

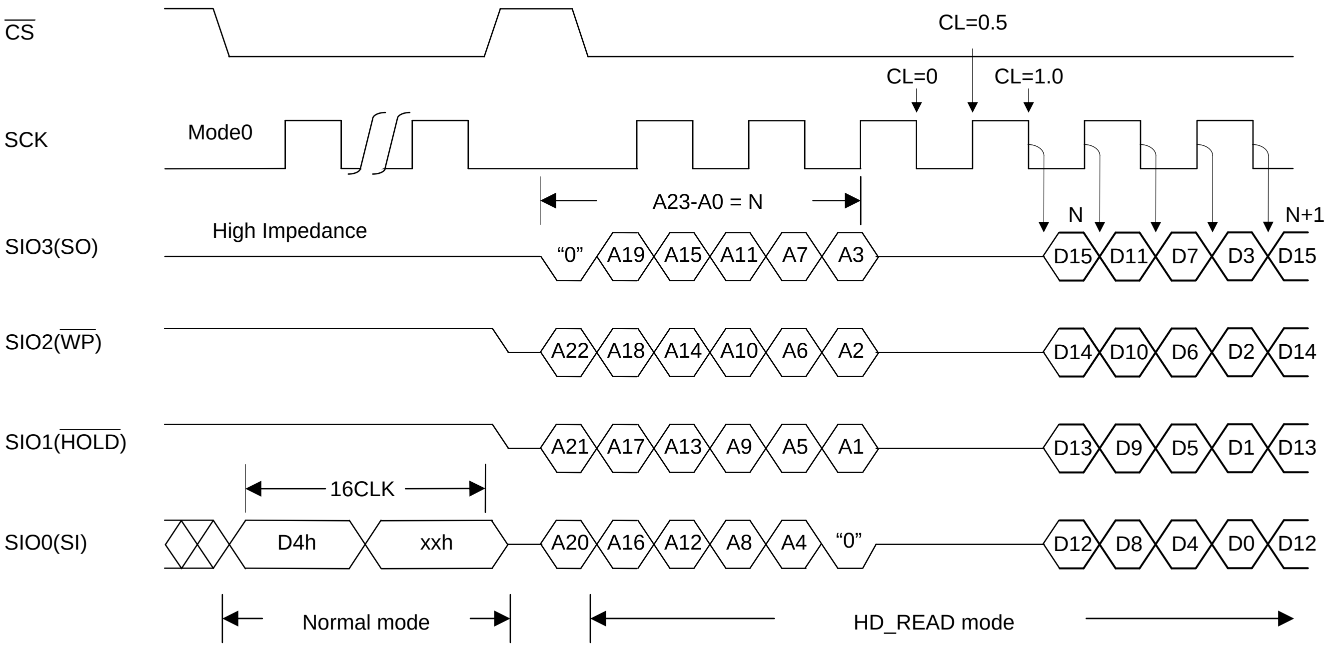


2. High-Density Read

LE25FW808 has the HD_READ mode in addition to two kinds of normal read (4 bus read and 5 bus read). The HD_READ mode is greatly different from the normal mode in three points.
The first is the difference of the role of pins. Four pins (SO, $\overline{WP}$, $\overline{HOLD}$, SI) become I/O pins (SIO3 – SIO0) in the HD_READ mode while the input pin (SI) and the output pin (SO) are only one in the normal mode respectively as shown in Figure 2. Because SO, $\overline{WP}$, $\overline{HOLD}$ and SI operate as I/O pin in the HD_READ mode, the setting of read address and the outputting read data become to be done from four pins.
The second is the difference of the relation between the clock and the data output. The rising edge of SCK is made a trigger for the address input and the falling edge of SCK is made a trigger for the data output in the normal mode. However, both edges of rising and falling of SCK will be done to the address taking and the data outputting in the HD_READ mode.
The third is the difference of the data composition at the time of reading. It is read by the ×16 bit in the HD_READ mode though it is read by the ×8 bit in the normal read. Therefore, please fix least significant bit (LSB): A0 to L in the address input in HD_READ mode.
When the HD_READ mode is used with LE25FW808, it is necessary to input the HD_READ mode command first according to the usual serial input specification. Please refer to Table 1 for the command input to set of the HD_READ mode. The command is composed at two bus cycles, and various operation methods of the HD_READ mode can be set at the second bus cycle. Please refer to Table 2 for a set content.

Please refer to Figure 7 for the input waveform when the HD_READ mode is set. The HD_READ mode becomes effective by making $\overline{CS}$ to H after the command is input. It keeps maintaining the HD_READ mode until the power supply is cut or the above-mentioned release command is input after entering the HD_READ mode once.

Figure 7: HD_READ mode setting waveform (CL=1.0)



Because the HD_READ mode entry is an input in the normal mode, either input of SPI mode 0/3 is possible. However, there is no concept of SPI mode for the period when the HD_READ mode is set. Please control $\overline{CS}$ according to timing that provides with this specifications.

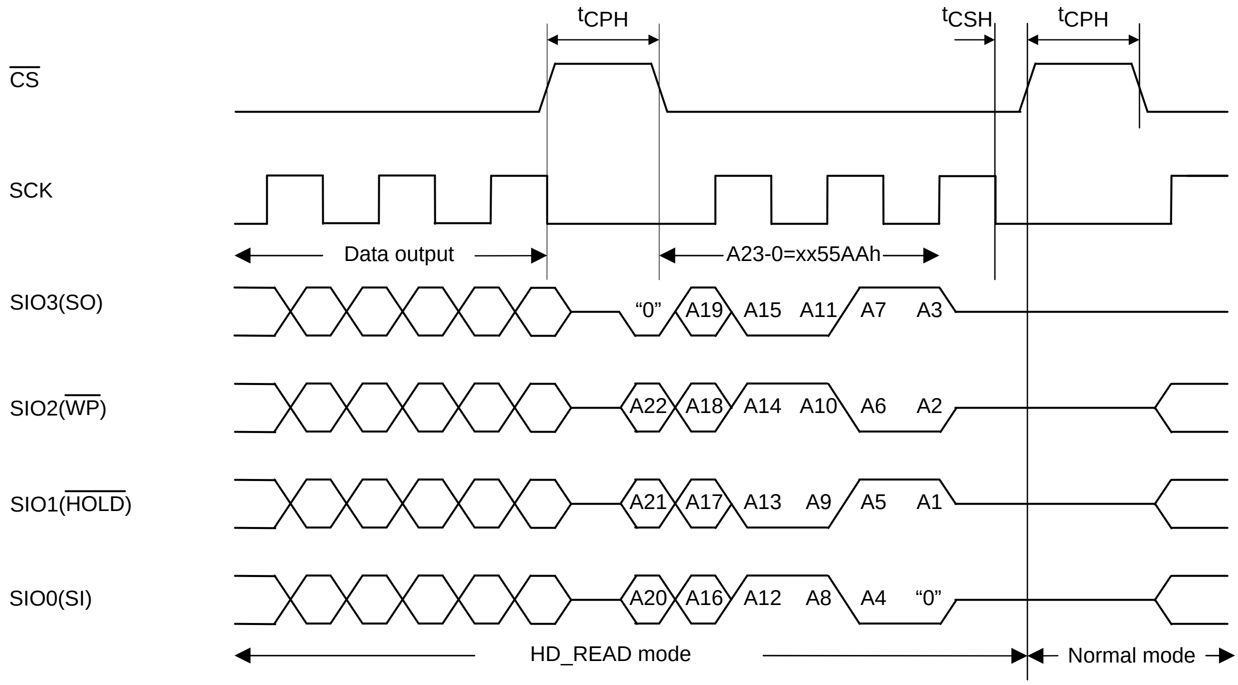
The composition of one input pin and one output pin changes into the composition of four I/O pins if it enters in the HD_READ mode. Therefore, the start address of reading in HD_READ mode is set from four I/O pins (SIO0 - SIO3). At this time, the address from A23 to A0 are latched internally by rising edge of $\overline{CS}$, rising and falling edge of SCK. Please refer to Figure 7. However, it is necessary to note the following points.

- Even if $\overline{CS}$ is fixed at H, four I/O pins become the input waiting states in the HD_READ mode. Therefore, please fix the state of four I/O pins at H or L for this period as much as possible. The input level changes or it becomes middle potential, the penetration current will flow in the pin input buffer inside the flash.
- The address that can be input is only an even number address because output data is read in each x16 bit in the HD_READ mode.
- Please input L to most significant bit (A23) of the address.
- The input address from A22 to A20 is don't care. Those are for the serial flash memory that exceeds 8Mbit (planning).

Please rise $\overline{CS}$ to H in arbitrary timing when you want to stop reading in the HD_READ mode temporarily. The level of SCK at this time doesn't ask H or L. The output is be the state of Hi-Z after t_{CHZ} by rising $\overline{CS}$, and four I/O pins (SIO0 - SIO3) become the input waiting states. Therefore, please fix the state of four I/O pins for this period at H level or L level. Afterwards, please execute it from the address input again when you restart reading.

Address A23-A0 is set to xx55AAh to release from the HD_READ mode to the normal mode, and then the operation that makes $\overline{CS}$ to H immediately when SCK becomes L after the address input is done. Please refer to Figure 8.

Figure 8: HD_READ mode release waveform



3. HD_READ Mode Register Setting

Various operation methods of the HD_READ mode can be set to an internal register in the HD_READ mode command input at the second bus cycle. The register are eight bits in all, and shows the meaning of each bit in the table 3: HD_READ mode register table. This register setting is effective until the release from HD_READ mode to the normal mode. It is not necessary to set it again at each temporary stop of reading in the HD_READ mode.

Table 3: HD_READ Mode Register Table

MSB							LSB
REGBL2	REGBL1	REGBL0	REGFCLK1	REGFCLK0	REGCL2	REGCL1	REGCL0

BIT	Name	Function	Set value : Set content
7	REGBL2	Burst length [REGBL2, REGBL1, REGBL0]	[0, 0, 0]: continuous [1, 0, 0]: 4words wrap around [1, 0, 1]: 8 words wrap around [1, 1, 0]: 16 words wrap around [1, 1, 1]: 32 words wrap around
6	REGBL1		
5	REGBL0		
4	REGFCLK1	Clock frequency [REGFCLK1, REGFCLK0]	[0, 0]: 16MHz or less + power save mode [0, 1]: 25MHz or less [1, 0]: 50MHz or less [1, 1]: 51MHz or more (1)
3	REGFCLK0		
2	REGCL2	Clock latency [REGCL2, REGCL1, REGCL0]	[0, 0, 0]: Clock latency = 0.5 (2) [0, 0, 1]: Clock latency = 1.0 [0, 1, 0]: Clock latency = 1.5 [0, 1, 1]: Clock latency = 2.0 [1, 0, 0]: Clock latency = 2.5 [1, 0, 1]: Clock latency = 3.0
1	REGCL1		
0	REGCL0		

(1) The specification that exceeds f_{CLK}=50MHz is planning.
(2) When f_{CLK} exceeds 30MHz, it is necessary to adjust the CL to 1.0 or more.

Burst length setting

In this model, two kinds of reading methods of "Continuous reading" and "Wrap around reading" in the HD_READ mode can be set alternately. And, the delimitation of the address can be set to four kinds (every 4 words, 8 words, 16 words, and 32 words (one word =16 bits)) in "Wrap around reading".

- Continuous reading

  When the burst length is set, the Continuous reading is set by specifying (0, 0, 0) the register bit.
  The Continuous reading method automatically continues to read as long as the SCK is input. Reading is begun from the input address, and an internal address is automatically count up by two addresses (every 16 bits). If the internal address reaches to the final address (FFFFEh), it returns to the first address (00000h) and reading is continued. If it wants to shift to an arbitrary address on the way, the operation that makes $\overline{CS}$ to H once and makes to L again is done.

- Wrap around reading

When the burst length is set, the wrap around reading method is set by specifying (1, X, X) the register bit. The wrap around reading method automatically continues to read as long as the SCK is input. Reading is begun from the input address, and an internal address is automatically count up by two addresses (every 16 bits). If the internal address reaches to the delimitation of the address set beforehand, it returns to the head of the delimitation of the address and reading is repeated.
The delimitation of the address can be set to four kinds (every 4 words, 8 words, 16 words and 32 words (one word =16 bits)) by two subordinate position bits of the register bit.

For instance, 16 words becomes a unit of the address delimitation for reading by 16 word wrap around. After it reaches the final word of the address delimitation by 16 words, it returns to the first word and reading is done even if reading is started from which address.
The order of reading for 20 words when the address of the third word from the head is read as a start address is as follows.

The order of reading	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
address	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	0000	0001	0010

The order of reading	17	18	19	20
address	0011	0100	0101	0110

Mark address is A4 to A1

Clock frequency setting

In this model, it is necessary to set the register bit of the clock frequency according to the operation frequency used .The clock of 50MHz or less can be input at present. Especially, the power saving mode that decreases the power consumption at HD_READ can be selected by specifying (0, 0) the register bit. However, this power saving mode use with operation frequency 16MHz or less. Moreover, spec (t_{V2}) of the output data time from SCK changes in this case.

Clock latency setting

In this model, CL (= clock latency: number of clocks from the setting of the address to the output of the first data) can be set by setting the clock latency register bit. Please refer to Figure 7 for the method of counting CL. The falling edge of the first SCK after the address input is assumed to be CL=0, and 0.5 CL is added every half clock of SCK. CL can be set within the range from 0.5 to 3.0. However, when the clock frequency exceeds 30MHz, it is necessary to set CL to 1.0 or more.

4. Status Register

The Status Register's contents are shown in Table 4.
The Status Register can perform detection state of a device and setup of protection.

Table 4 Status Registers

Bit	Name	Logic	Function	Power-on Time Information
Bit0	$\overline{RDY}$	0	Ready	0
		1	Erase/Program	
Bit1	WEN	0	Write disabled	0
		1	Write enabled	
Bit2	BP0	0	Block protect information See status register descriptions on BP0, BP1, and BP2.	Nonvolatile information
		1		
Bit3	BP1	0		Nonvolatile information
		1		
Bit4	BP2	0		Nonvolatile information
		1		
Bit5			Reserved bits	0
Bit6			Reserved bits	0
Bit7	SRWP	0	Status register write enabled	Nonvolatile information
		1	Status register write disabled	

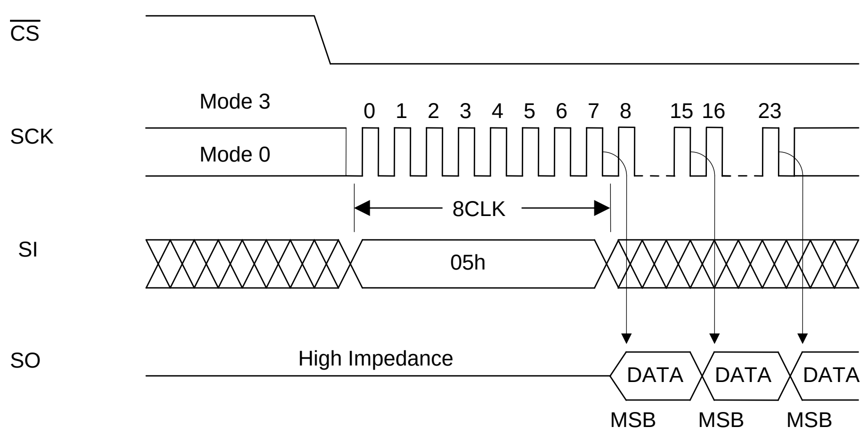
4-1. Status Register Read

The contents of the status registers can be read using the status register read command. This command can be executed even during the following operations.

- Small sector erase, sector erase, chip erase
- Page program
- Status register write

"Figure 9 Status Register Read" shows the timing waveforms of status register read. Consisting only of the first bus cycle, the status register command outputs the contents of the status registers synchronized to the falling edge of the clock (SCK) with which the eighth bit of (05h) has been input. In terms of the output sequence, SRWP (bit 7) is the first to be output, and each time one clock is input, all the other bits up to $\overline{RDY}$ (bit 0) are output in sequence, synchronized to the falling clock edge. If the clock input is continued after $\overline{RDY}$ (bit 0) has been output, the data is output by returning to the bit (SRWP) that was first output, after which the output is repeated for as long as the clock input is continued. The data can be read by the status register read command at any time (even during a program or erase cycle).

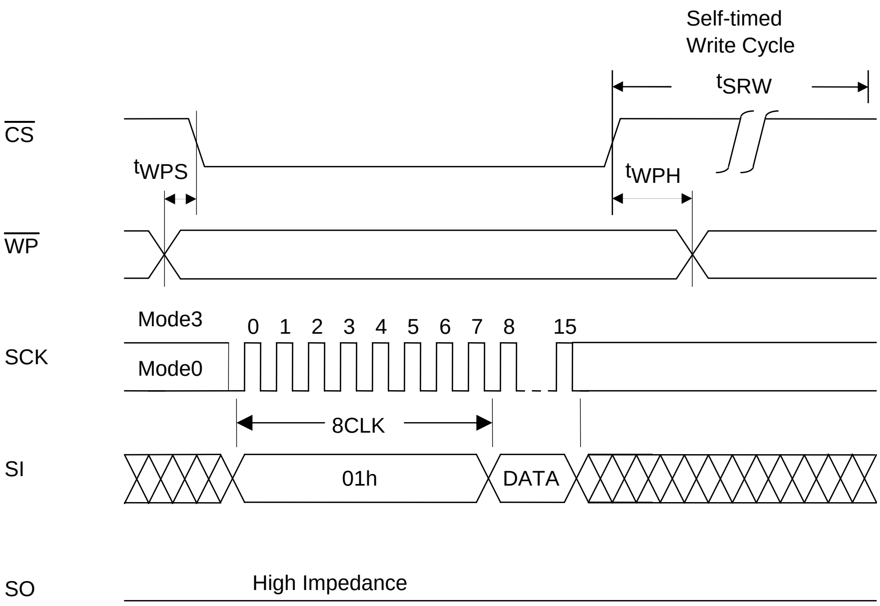
Figure 9 Status Register Read



4-2. Status Register Write

By Status Register Write, BP0, BP1, BP2 and SRWP can be rewritten. $\overline{\text{RDY}}$, WEN, Bit5, and Bit6 are read-only, BP0, BP1, BP2 and SRWP are non-volatile.
A timing waveform is shown in Figure 10 and a flow chart is shown in Figure 23.
Status Register Write command consists of the 1st bus cycle and the 2nd bus cycle, and internal Write operation starts with the rising edge of $\overline{\text{CS}}$ after inputting data after OP-code (01h). Erase and program are automatically performed inside the device and a Status Register Write rewrites BP0, BP1, BP2 and SRWP non-volatilized data. The write-in data to read-only bits ($\overline{\text{RDY}}$, WEN, Bit 5, Bit 6) are don't care.
The end of a Status Register Write is detectable with $\overline{\text{RDY}}$ of a Status Register Read.
The number of times of rewriting of a Status Register Write is 1,000 times (min).
In order to perform a Status Register Write, it is necessary to change WEN of a Status Register into "1" state for $\overline{\text{WP}}$ pin.

Figure 10 Status Register Write



4-3. Contents of Each Status Register

$\overline{\text{RDY}}$ (bit 0)

The $\overline{\text{RDY}}$ register is for detecting the write (program, erase and status register write) end. When it is "1", the device is in a busy state, and when it is "0", it means that write is completed.

WEN (bit 1)

The WEN register is for detecting whether the device can perform write operations. If it is set to "0", the device will not perform the write operation even if the write command is input. If it is set to "1", the device can perform write operations in any area that is not block-protected.
WEN can be controlled using the write enable and write disable commands. By inputting the write enable command (06h), WEN can be set to "1"; by inputting the write disable command (04h), it can be set to "0." In the following states, WEN is automatically set to "0" in order to protect against unintentional writing.

- At power-on
- Upon completion of small sector erase, sector erase or chip erase
- Upon completion of page program
- Upon completion of status register write

* If a write operation has not been performed inside the LE25FW808 because, for instance, the command input for any of the write operations (small sector erase, sector erase, chip erase, page program, or status register write) has failed or a write operation has been performed for a protected address, WEN will retain the status established prior to the issue of the command concerned. Furthermore, its state will not be changed by a read operation.

BP0, BP1, BP2 (bits 2, 3, 4)

Block protect BP0, BP1, and BP2 are status register bits that can be rewritten, and the memory space to be protected can be set depending on these bits. For the setting conditions, refer to "Table 5 Protect level setting conditions".

Table 5 Protect Level Setting Conditions

Protect Level	Status Register Bits			Protected Area
	BP2	BP1	BP0	
0 (Whole area unprotected)	0	0	0	None
1 (1/16 protected)	0	0	1	F0000h to FFFFFh
2 (1/8 protected)	0	1	0	E0000h to FFFFFh
3 (1/4 protected)	0	1	1	C0000h to FFFFFh
4 (1/2 protected)	1	0	0	80000h to FFFFFh
5 (Whole area protected)	1	0	1	00000h to FFFFFh
5 (Whole area protected)	1	1	0	00000h to FFFFFh
5 (Whole area protected)	1	1	1	00000h to FFFFFh

* Chip erase is enabled only when the protect level is 0.

SRWP (bit 7)

Status register write protect SRWP is the bit for protecting the status registers, and its information can be rewritten. When SRWP is "1" and the logic level of the $\overline{WP}$ pin is low, the status register write command is ignored, and status registers BP0, BP1, BP2, and SRWP are protected. When the logic level of the $\overline{WP}$ pin is high, the status registers are not protected regardless of the SRWP state. The SRWP setting conditions are shown in "Table 5 SRWP setting conditions".

Table 6 SRWP Setting Conditions

$\overline{WP}$ Pin	SRWP	Status Register Protect State
0	0	Unprotected
	1	Protected
1	0	Unprotected
	1	Unprotected

Bits 5 and 6 are reserved bits, and have no significance.

5. Write Enable

Before performing any of the operations listed below, the device must be placed in the write enable state. Operation is the same as for setting status register WEN to "1", and the state is enabled by inputting the write enable command. "Figure 11 Write Enable" shows the timing waveforms when the write enable operation is performed. The write enable command consists only of the first bus cycle, and it is initiated by inputting (06h).

- Small sector erase, sector erase, chip erase
- Page program
- Status register write

6. Write Disable

The write disable command sets status register WEN to "0" to prohibit unintentional writing. "Figure 12 Write Disable" shows the timing waveforms. The write disable command consists only of the first bus cycle, and it is initiated by inputting (04h). The write disable state (WEN "0") is exited by setting WEN to "1" using the write enable command (06h).

Figure 11 Write Enable

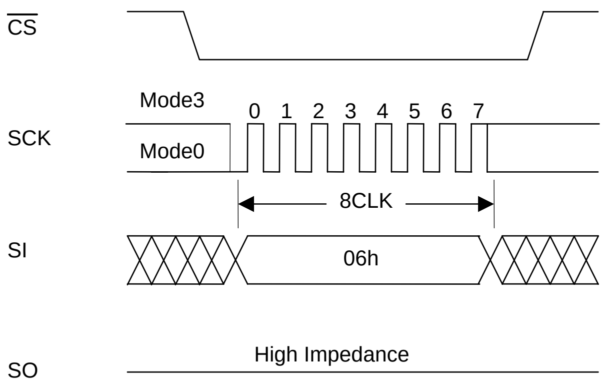
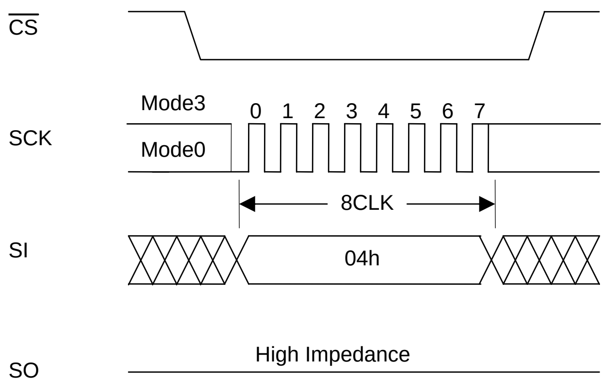


Figure 12 Write Disable



7. Power-down

The power-down command sets all the commands, with the exception of the silicon ID read command and the command to exit from power-down, to the acceptance prohibited state (power-down). "Figure 13 Power-down" shows the timing waveforms. The power-down command consists only of the first bus cycle, and it is initiated by inputting (B9h). However, a power-down command issued during an internal write operation will be ignored. The power-down state is exited using the power-down exit command (power-down is exited also when one bus cycle or more of the silicon ID read command (ABh) has been input). "Figure 14 Exiting from Power-down" shows the timing waveforms of the power-down exit command.

Figure 13 Power-down

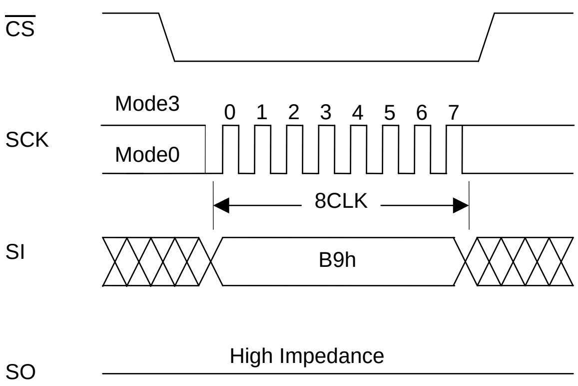
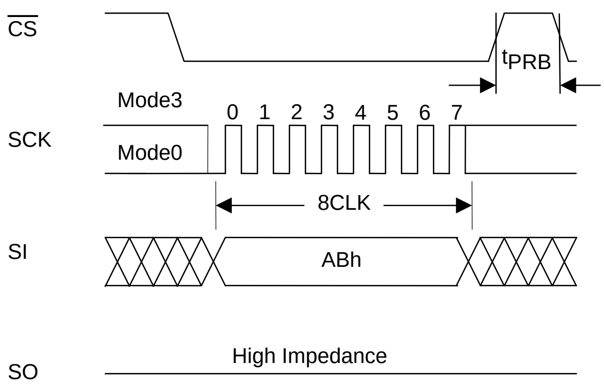


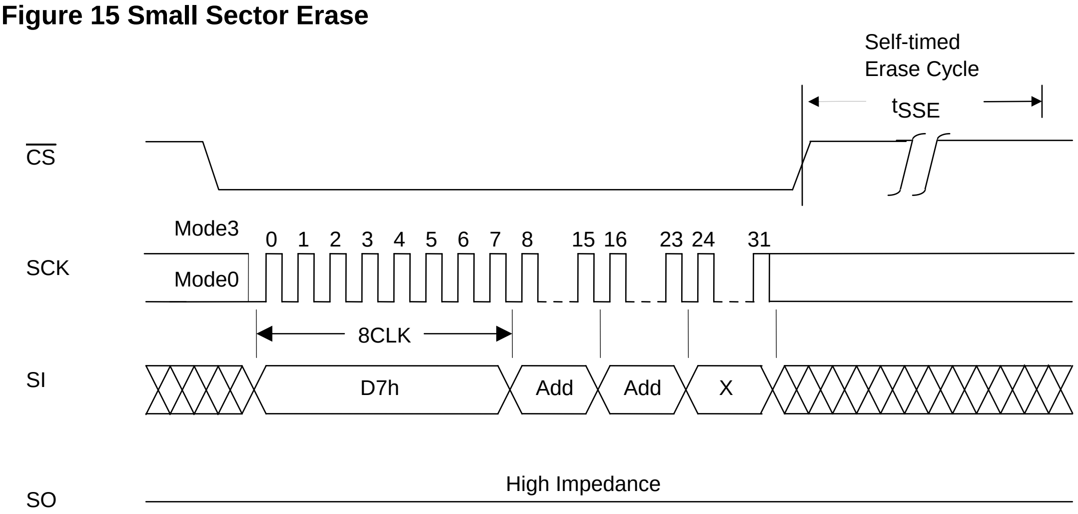
Figure 14 Exiting from Power-down



8. Small Sector Erase

Small sector erase is an operation that sets the memory cell data in any small sector to "1". A small sector consists of 8Kbytes. "Figure 15 Small Sector Erase" shows the timing waveforms, and Figure 24 shows a small sector erase flowchart. The small sector erase command consists of the first through fourth bus cycles, and it is initiated by inputting the 24-bit addresses following (D7h). Addresses A19 to A13 are valid, and Addresses A23 to A20 are "don't care". After the command has been input, the internal erase operation starts from the rising $\overline{CS}$ edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register $\overline{RDY}$.

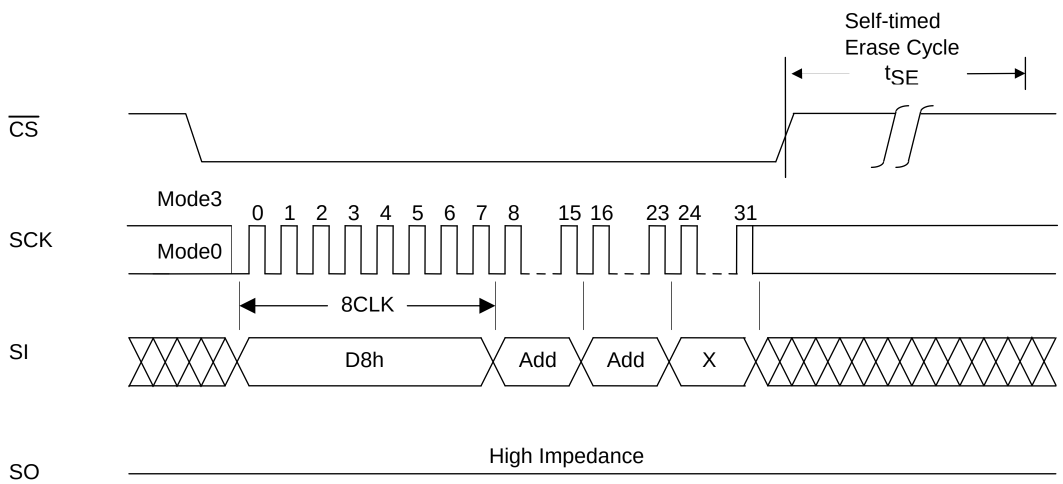
Figure 15 Small Sector Erase



9. Sector Erase

Sector erase is an operation that sets the memory cell data in any sector to "1". A sector consists of 64Kbytes. "Figure 16 Sector Erase" shows the timing waveforms, and Figure 24 shows a sector erase flowchart. The sector erase command consists of the first through fourth bus cycles, and it is initiated by inputting the 24-bit addresses following (D8h). Addresses A19 to A16 are valid, and Addresses A23 to A20 are "don't care". After the command has been input, the internal erase operation starts from the rising $\overline{CS}$ edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register $\overline{RDY}$.

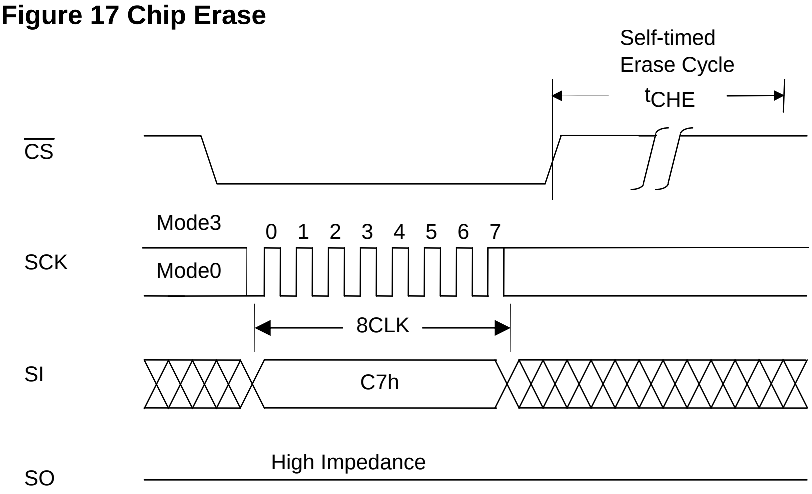
Figure 16 Sector Erase



10. Chip Erase

Chip erase is an operation that sets the memory cell data in all the sectors to "1". "Figure 17 Chip Erase" shows the timing waveforms, and Figure 24 shows a chip erase flowchart. The chip erase command consists only of the first bus cycle, and it is initiated by inputting (C7h). After the command has been input, the internal erase operation starts from the rising $\overline{CS}$ edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register $\overline{RDY}$.

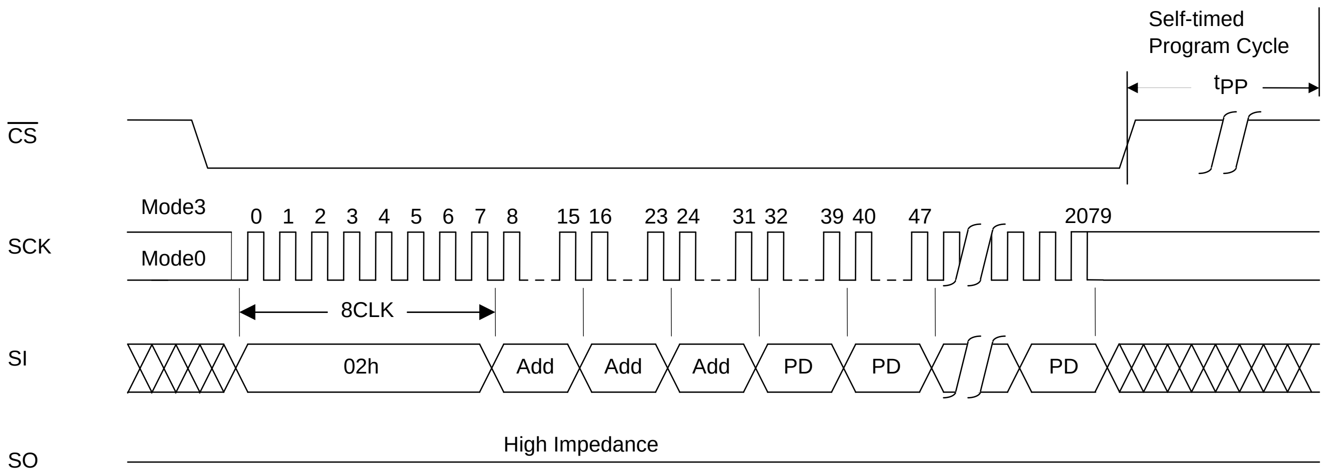
Figure 17 Chip Erase



11. Page Program

Page Program can program the arbitrary numbers of bytes of 1 to 256 bytes into the sector erased in advance.
Figure 18 shows timing waveform and a flow chart is shown in Figure 25.
24-bit address is inputted after OP-code (02H). As for an address A19-A0 are effective. Then, loading is possible for program data during $\overline{CS}$ is low. When the data loaded exceeds 256 bytes, 256 bytes loaded at the end are programmed. It is necessary to load program data per byte, and when it programs by loading the data below a byte unit, a normal Page Program is not performed.

Figure 18 Page Program



12. Silicon ID Read

Silicon ID read is an operation that reads the manufacturer code and device code information. "Table 7 Silicon ID codes table" lists the silicon ID codes. The silicon ID read command is not accepted during writing.
Two methods are used for silicon ID reading. The first method involves inputting the 9Fh command: the setting is completed with only the first bus cycle input, and in subsequent bus cycles the manufacturer code 62h and device code 20h are repeatedly output in succession so long as the clock input is continued. Refer to "Figure 19-a Silicon ID read 1" for the waveforms.
The second method involves inputting the ABh command. This command consists of the first through fourth bus cycles, and the silicon ID can be read when 16 dummy bits and an 8-bit address are input after (ABh). When address A0 is "0", the manufacturer code 62h is read in the fifth bus cycle, and the device code 20h is read in the sixth bus cycle. "Figure 19-b Silicon ID read 2" shows the timing waveforms. If, after the manufacturer code or device code has been read, the SCK input is continued, the manufacturer code and device code are output alternately with each bus cycle. When address A0 is "1", reading starts with device code 20h in the fifth bus cycle.

Table 7 Silicon ID Codes

	Address A0	Output Code
Manufacturer code	0	62h
Device code	1	20h

The data is output starting with the falling clock edge of the fourth bus cycle bit 0, and silicon ID reading ends at the rising $\overline{CS}$ edge.

Figure 19-a Silicon ID Read 1

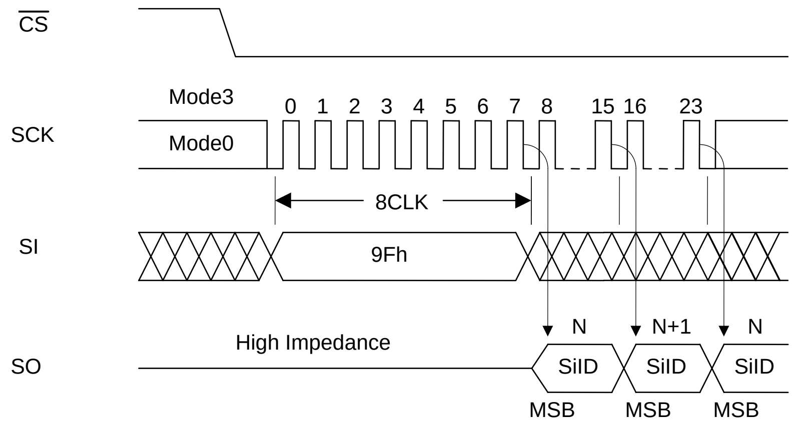
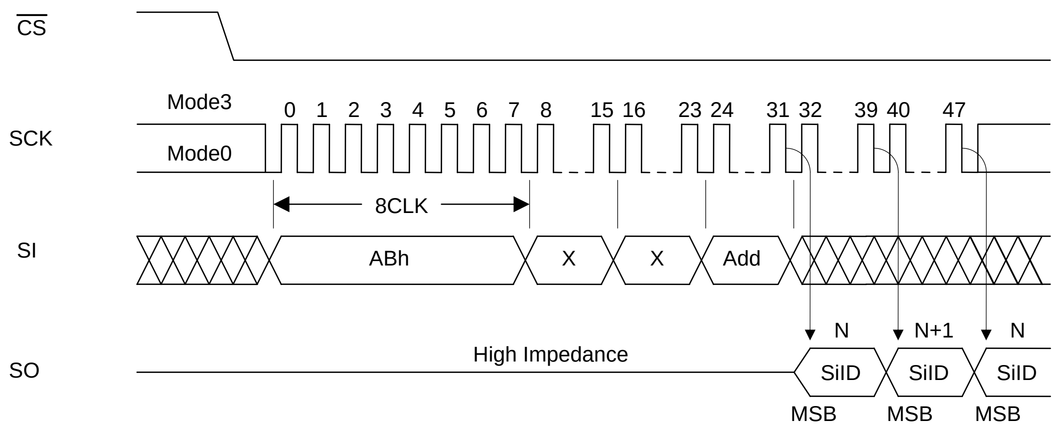


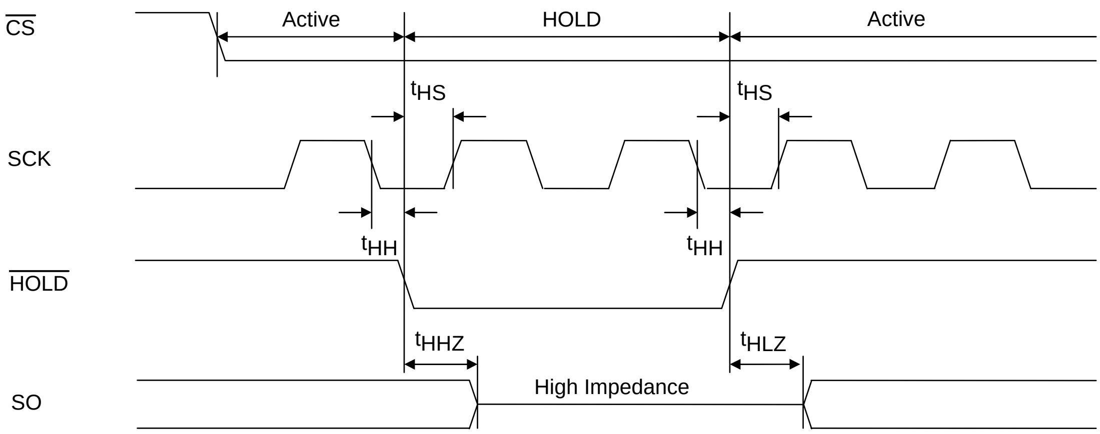
Figure 19-b Silicon ID Read 2



13. Hold Function

Using the $\overline{HOLD}$ pin, the hold function suspends serial communication (it places it in the hold status). "Figure 21 $\overline{HOLD}$" shows the timing waveforms. The device is placed in the hold status at the falling $\overline{HOLD}$ edge while the logic level of SCK is low, and it exits from the hold status at the rising $\overline{HOLD}$ edge. When the logic level of SCK is high, $\overline{HOLD}$ must not rise or fall. The hold function takes effect when the logic level of $\overline{CS}$ is low, the hold status is exited and serial communication is reset at the rising $\overline{CS}$ edge. In the hold status, the SO output is in the high-impedance state, and SI and SCK are "don't care".

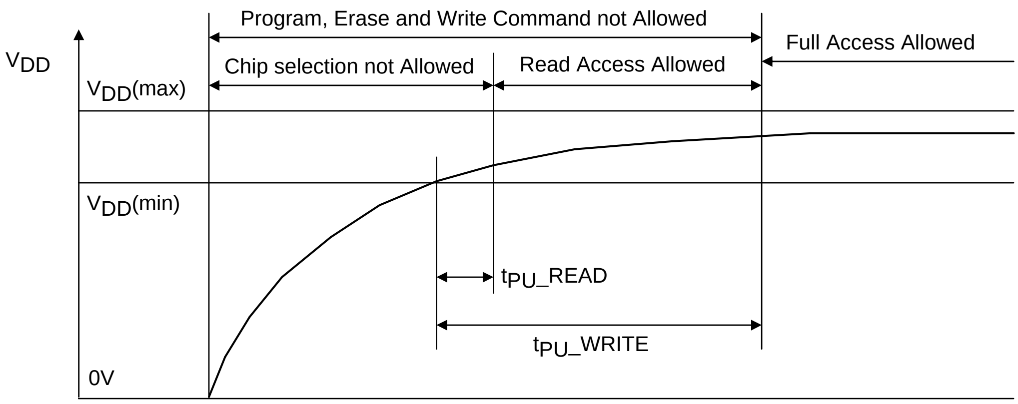
Figure 21 $\overline{HOLD}$



14. Power-on

Please make $\overline{CS}$ to high to prevent a careless writing when you turn on the power supply.
Please begin the command input of the read operation after 100μs (t_{PU}_READ) from the state to which the power-supply voltage is 2.7V or more steady.
Please begin the command input of the program or erase operation after 10ms (t_{PU}_WRITE) from the state to which the power-supply voltage is 2.7V or more steady.

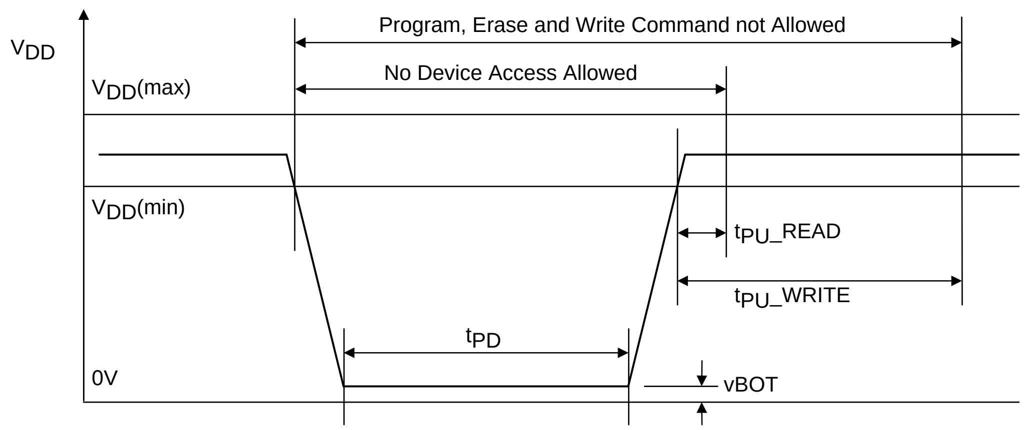
Figure 21 Power-on Timing



15. Hardware Data Protection

In order to protect against unintentional writing at power-on, the LE25FW808 incorporates a power-on reset function. The following conditions must be met in order to ensure that the power reset circuit will operate stably.
No guarantees are given for data in the event of an instantaneous power failure occurring during the writing period.

Figure 22 Power-down Timing



16. Software Data Protection

The LE25FW808 eliminates the possibility of unintentional operations by not recognizing commands under the following conditions.

- When a write command is input and the rising $\overline{CS}$ edge timing is not in a bus cycle (8 CLK units of SCK)
- When the page program data is not in 1-byte increments
- When the status register write command is input for 2 bus cycles or more

17. Decoupling Capacitor

A 0.1µF ceramic capacitor must be provided to each device and connected between V_{DD} and V_{SS} in order to ensure that the device will operate stably.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage		With respect to V_{SS}	-0.5 to +4.6	V
DC voltage (all pins)		With respect to V_{SS}	-0.5 to V_{DD}+0.5	V
Storage temperature	Tstg		-55 to +150	°C

Operating Conditions

Parameter	Symbol	Conditions	Ratings	unit
Operating supply voltage			2.7 to 3.6	V
Operating ambient temperature			0 to 70	°C
			-40 to +85 (Planning)	°C

Allowable DC Operating Conditions

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Power Supply Current (Normal Mode)	I_{CCR}	$\overline{CS}$ = 0.1V_{DD}, $\overline{HOLD}$ = $\overline{WP}$ = 0.9V_{DD} SI = 0.1V_{DD} / 0.9V_{DD}, SO =open clock frequency = 50MHz, V_{DD} = V_{DD} max			8	mA
Power Supply Current (HD_Read)	I_{CCR}	$\overline{CS}$ = 0.1V_{DD}, SO = $\overline{WP}$ = $\overline{HOLD}$ = SI = open V_{DD} = V_{DD} max. Clock frequency = 16MHz (Power saving mode)		3	6	mA
		$\overline{CS}$ = 0.1V_{DD}, SO = $\overline{WP}$ = $\overline{HOLD}$ = SI = open V_{DD} = V_{DD} max. Clock frequency = 25MHz (frequency setting=0:1)		6	12	mA
		$\overline{CS}$ = 0.1V_{DD}, SO = $\overline{WP}$ = $\overline{HOLD}$ = SI = open V_{DD} = V_{DD} max. Clock frequency = 50MHz (frequency setting=1:0)		10	20	mA
Power Supply Current (Write)	I_{CCW}	V_{DD} = V_{DD} max t_{SSE}=80ms, t_{SE}=100ms, t_{CHE}=250ms, t_{PP}=0.5ms			15	mA
CMOS standby current	ISB	$\overline{CS}$ = $\overline{HOLD}$ = $\overline{WP}$ = V_{DD}-0.3V, SO = open SI = V_{IH} / V_{IL}, V_{DD} = V_{DD} max			10	μA
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}, V_{DD} = V_{DD} max			2	μA
Output Leakage Current	I_{LO}	V_{IN} = V_{SS} to V_{DD}, V_{DD} = V_{DD} max			2	μA
Input Low Voltage	V_{IL}	V_{DD} = V_{DD} max	-0.3		0.3 V_{DD}	V
Input High Voltage	V_{IH}	V_{DD} = V_{DD} min	0.7V_{DD}		V_{DD}+0.3	V
Output low Voltage	V_{OL}	I_{OL} = 100μA, V_{DD} = V_{DD} min			0.2	V
		I_{OL} = 1.6mA, V_{DD} = V_{DD} min			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -100μA, V_{DD} = V_{DD} min	V_{DD}-0.2			V

Power-on Timing

Parameter	Symbol	Ratings		unit
		min	max	
Time from power-on to read operation	t_{PU}_READ	100		μs
Time from power-on to write operation	t_{PU}_WRITE	10		ms
Power-down time	t_{PD}	10		ms
Power-down voltage	v_{BOT}		0.2	V

Pin Capacitance at Ta=25°C, f=1MHz

Parameter	Symbol	Conditions	Ratings	unit
			max	
Output pin capacitance	C_{DQ}	V_{DQ}=0V	12	pF
Input pin Capacitance	C_{IN}	V_{IN}=0V	6	pF

Note: These parameter values do not represent the results of measurements undertaken for all devices but rather values for some of the sampled devices.

AC Characteristics

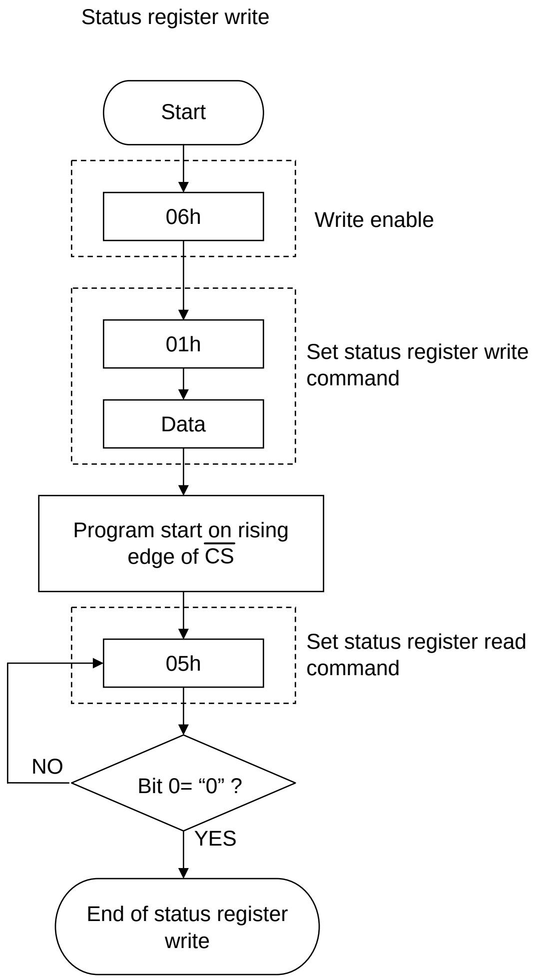
Parameter	Symbol	Ratings			unit
		min	typ	max	
Clock frequency	f_{CLK}			50	MHz
SCK High pulse width	t_{CLHI}	9			ns
SCK Low pulse width	t_{CLLO}	9			ns
Input rising, falling time	t_{RF}			20	ns
$\overline{CS}$ Setup time (Conventional Mode)	t_{CSS}	5			ns
$\overline{CS}$ Setup time (HD_READ Mode)	t_{CSS}	10			ns
SCK Setup time	t_{CLS}	5			ns
Data Setup time	t_{DS}	2			ns
Data Hold time	t_{DH}	5			ns
Address Setup time (HD_READ Mode)	t_{AS}	4			ns
Address Hold time (HD_READ Mode)	t_{AH}	3			ns
SCK to output valid	t_V		5.5	9	ns
SCK to output valid (HD_READ)	t_{V2}		5.5	9	ns
SCK to output valid (HD_READ, power saving mode)			10	15	ns
$\overline{CS}$ Hold time	t_{CSH}	5			ns
SCK Hold time	t_{CLH}	5			ns
$\overline{CS}$ Standby pulse width	t_{CPH}	25			ns
$\overline{CS}$ to High-Z output	t_{CHZ}	1	2.5	8	ns
Output data hold time	t_{HO}	1	2.5		ns
$\overline{HOLD}$ Setup time	t_{HS}	5			ns
$\overline{HOLD}$ Hold time	t_{HH}	3			ns
$\overline{HOLD}$ High to Low-Z Output	t_{HLZ}			8	ns
$\overline{HOLD}$ Low to High-Z Output	t_{HHZ}			8	ns
$\overline{WP}$ Setup time	t_{WPS}	20			ns
$\overline{WP}$ Hold time	t_{WPH}	20			ns
Status Register Write cycle time	t_{SRW}		5	15	ms
Page Program cycle time	t_{PP}		0.5	0.8	ms
Small Sector Erase cycle time	t_{SSE}		0.08	0.3	s
Sector Erase cycle time	t_{SE}		0.1	0.4	s
Chip Erase cycle time	t_{CHE}		0.25	3	s
Power Down recovery time	t_{PRB}	25			ns
SCK to Low-Z output	t_{CLZ}	0			ns

AC Test Conditions

Input pulse level··············· 0V, 3.0V
Input rising/falling time···· 5ns
Input timing level············· $0.3V_{DD}$, $0.7V_{DD}$
Output timing level ·········· $1/2 \times V_{DD}$
Output load ······················· 30pF

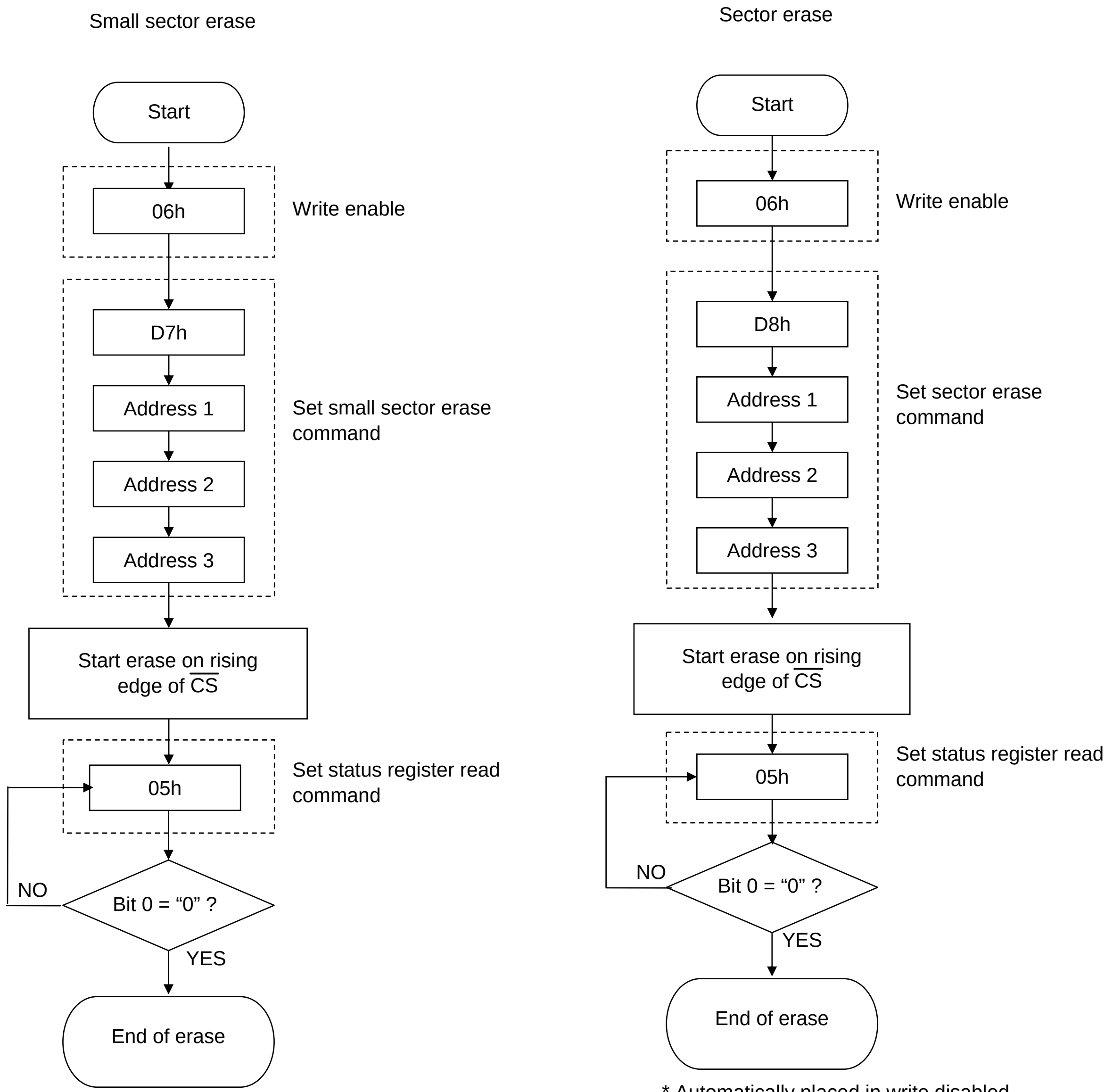
Note: As the test conditions for "typ", the measurements are conducted using 3.0V for V_{DD} at room temperature.

Figure 23 Status Register Write Flowchart



* Automatically placed in write disabled state at the end of the status register write

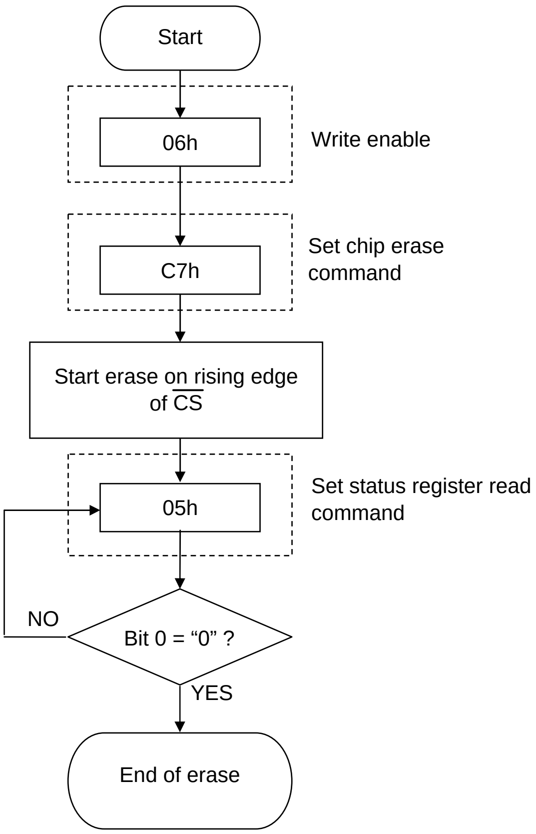
Figure 24 Erase Flowcharts



* Automatically placed in write disabled state at the end of the erase

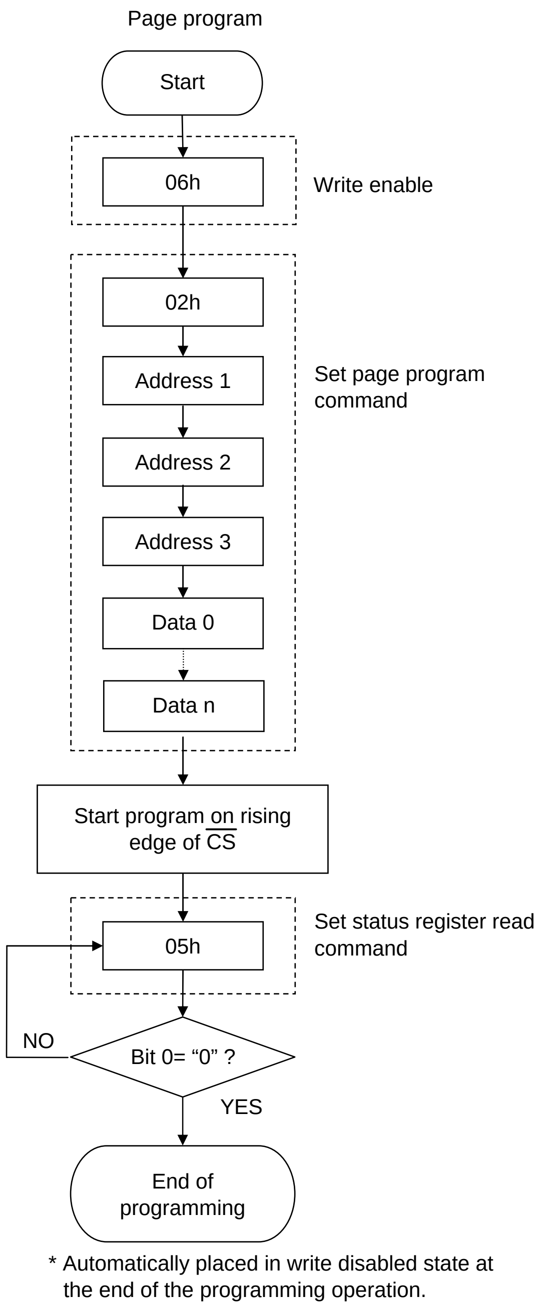
* Automatically placed in write disabled state at the end of the erase

Chip erase



* Automatically placed in write disabled state at the end of the erase

Figure 25 Page Program Flowchart



This catalog provides information as of June, 2009. Specifications and information herein are subject to change without notice.