19-3772; Rev 1; 10/05

Dual-/Triple-Voltage, Power-Supply Sequencers/Supervisors

General Description

The MAX6880–MAX6883 dual-/triple-voltage monitors are designed to sequence power supplies during power-up condition. When all of the voltages exceed their respective thresholds, these devices turn on voltages to the system sequentially, enhancing n-channel MOSFETs used as switches. The time between each sequenced voltage is determined by an external capacitor, thus allowing flexibility in delay timing. The MAX6880/MAX6881 sequence three voltages and the MAX6882/MAX6883 sequence two voltages.

These devices initially monitor all of the voltages and when all of them are within their tolerances, the internal charge pumps enhance external n-channel MOSFETs in a sequential manner to apply the voltages to the system. Internal charge pumps drive the gate voltages 5V above the respective input voltage thereby ensuring the MOSFETs are fully enhanced to reduce the on-resistance.

The MAX6880–MAX6883 feature capacitor-adjustable slew-rate control to provide controlled turn-on characteristics. After all of the voltages reach 92.5% of their final value, a power-good output (MAX6880/MAX6882) signal is active. The power-good output (PG/$\overline{\text{RST}}$) can be delayed with an external capacitor to create a power-on reset delay. After the initial power-up phase, the MAX6880–MAX6883 continue to monitor the voltages. If any of the voltages falls below its threshold, the MOSFETs are quickly turned off and the voltages are tracked down together. An internal 100Ω pulldown resistor ensures that the capacitance at the MOSFET's source is discharged quickly. The power-good output goes low to provide a system reset.

The MAX6880–MAX6883 are available in small 4mm x 4mm 24-pin and 16-pin thin QFN packages and specified over the -40°C to +85°C extended operating temperature range.

Applications

Multivoltage Systems
Networking Systems
Telecom
Storage Equipment
Servers/Workstations

Selector Guide appears at end of data sheet.

Features

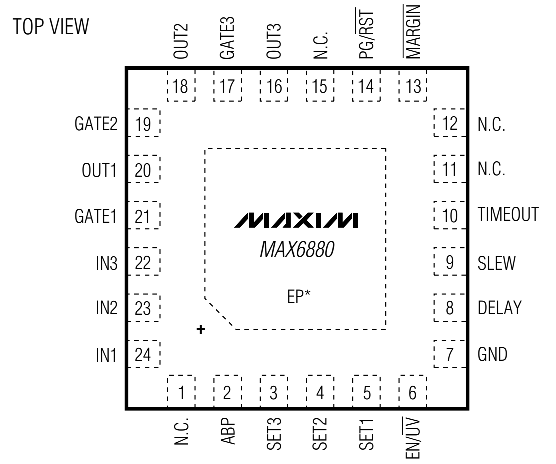
- **Capacitor-Adjustable Power-Up Sequencing Delay**
- **Internal Charge Pumps to Enhance External n-Channel FETs**
- **Capacitor-Adjustable Timeout Period Power-Good Output (MAX6880/MAX6882)**
- **Adjustable Undervoltage Lockout or Logic-Enable Input**
- **Internal 100Ω Pulldown for Each Output to Discharge Capacitive Load Quickly**
- **0.5V to 5.5V Nominal IN_/OUT_ Range**
- **2.7V to 5.5V Operating Voltage Range**
- **Immune to Short Voltage Transients**
- **Small 4mm x 4mm 24-Pin or 16-Pin Thin QFN Packages**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX6880ETG+	-40°C to +85°C	24 Thin QFN	T2444-4
MAX6881ETE+	-40°C to +85°C	16 Thin QFN	T1644-4
MAX6882ETE+	-40°C to +85°C	16 Thin QFN	T1644-4
MAX6883ETE+	-40°C to +85°C	16 Thin QFN	T1644-4

+Denotes lead-free package.

Pin Configurations



4mm x 4mm THIN QFN

*EXPOSED PADDLE CONNECTED TO GND.

Pin Configurations continued at end of data sheet.

Dual-/Triple-Voltage, Power-Supply Sequencers/Supervisors

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)

IN1, IN2, IN3	-0.3V to +6V
ABP	-0.3V to the highest of V_{IN1} - V_{IN3}
SET1, SET2, SET3	-0.3V to +6V
GATE1, GATE2, GATE3	-0.3V to +12V
OUT1, OUT2, OUT3	-0.3V to +6V
$\overline{\text{MARGIN}}$	-0.3V to +6V
PG/$\overline{\text{RST}}$, EN/$\overline{\text{UV}}$	-0.3V to +6V
DELAY, SLEW, TIMEOUT	-0.3V to +6V
OUT_ Current	±50mA
GND Current	±50mA
Input/Output Current (all pins except OUT_ and GND)	±20mA
Continuous Power Dissipation (T_A = +70°C)	
16-Pin 4mm x 4mm Thin QFN (derate 16.9mW/°C above +70°C)	1349mW
24-Pin 4mm x 4mm Thin QFN (derate 20.8mW/°C above +70°C)	1667mW
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(IN1, IN2, or IN3 = +2.7V to +5.5V, EN/$\overline{\text{UV}}$ = $\overline{\text{MARGIN}}$ = ABP, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	IN_	Voltage on the highest of IN_ to ensure that PG/$\overline{\text{RST}}$ is valid and GATE_ = 0	1.4			V
		Voltage on the highest of IN_ to ensure the device is fully operational	2.7		5.5	
Supply Current	I_{CC}	IN1 = 5.5V, IN2 = IN3 = 3.3V, no load		1.1	1.8	mA
SET_ Threshold Range	V_{TH}	SET_ falling, T_A = +25°C	0.4925	0.5	0.5075	V
		SET_ falling, T_A = -40°C to +85°C	0.4875	0.5	0.5125	
SET_ Threshold Hysteresis	V_{TH_HYST}	SET_ rising		0.5		%
SET_ Input Current	I_{SET}	SET_ = 0.5V	-100		+100	nA
EN/$\overline{\text{UV}}$ Input Voltage	V_{EN_R}	Input rising		1.286		V
	V_{EN_F}	Input falling	1.22	1.25	1.28	
EN/$\overline{\text{UV}}$ Input Current	I_{EN}		-5		+5	µA
EN/$\overline{\text{UV}}$ Input Pulse Width	t_{EN}	EN/$\overline{\text{UV}}$ falling, 100mV overdrive	7			µs
DELAY, TIMEOUT Output Current	I_D	(Notes 2, 3)	2.12	2.5	2.88	µA
DELAY, TIMEOUT Threshold Voltage		V_{CC} = 3.3V		1.25		V
SLEW Output Current	I_S	(Note 4)	22.5	25	27.5	µA
Sequence Slew-Rate Timebase Accuracy	SR	C_{SLEW} = 200pF	-15		+15	%
Timebase/C_{SLEW} Ratio		100pF < C_{SLEW} < 1nF		104		kΩ
Slew-Rate Accuracy during Power-Up and Power-Down		C_{SLEW} = 200pF, $V_{IN\_}$ = 5.5V (Note 4)	-50		+50	%

ELECTRICAL CHARACTERISTICS (continued)

(IN1, IN2, or IN3 = +2.7V to +5.5V, EN/$\overline{\text{UV}}$ = $\overline{\text{MARGIN}}$ = ABP, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

Power-Good Threshold	V_{TH_PG}	$V_{OUT\_}$ falling	91.5	92.5	93.5	%
Power-Good Threshold Hysteresis	V_{HYS_PG}	$V_{OUT\_}$ rising		0.5		%
GATE_ Output High	V_{GOH}	I_{SOURCE} = 0.5µA	IN_ + 4.2	IN_ + 5.0	IN_ + 5.8	V
GATE_ Pullup Current	I_{GUP}	During power-up and power-down, $V_{GATE\_}$ = 1V	2.5	4		µA
GATE_ Pulldown Current	I_{GD}	During power-up and power-down, $V_{GATE\_}$ = 5V	2.5	4		µA
	I_{GDS}	When disabled, $V_{GATE\_}$ = 5V, $V_{IN\_} \geq 2.7V$		9.5		mA
		When disabled, $V_{GATE\_}$ = 5V, $V_{IN\_} \geq 4V$		20		
SET_ to GATE_ Delay	t_{D-GATE}	SET falling, 25mV overdrive		10		µs
PG/$\overline{\text{RST}}$ Output Low	V_{OL}	$V_{IN\_} \geq 2.7V$, I_{SINK} = 1mA, output asserted			0.3	V
		$V_{IN\_} \geq 4.0V$, I_{SINK} = 4mA, output asserted			0.4	
Tracking Differential Voltage Stop Ramp	V_{TRK}	Differential between each of the OUT_ and the ramp voltage during power-up and power-down, Figure 1 (Note 5)	75	125	180	mV
Tracking Differential Fault Voltage	V_{TRK_F}	Differential between each of the OUT_ and the ramp voltage, Figure 1 (Note 5)	200	250	310	mV
Power-Low Threshold	V_{TH_PL}	OUT_ falling	125	142	170	mV
Power-Low Hysteresis	V_{TH_PLHYS}	OUT_ rising		10		mV
OUT to GND Pulldown Impedance		IN_ > 2.7V (Note 6)		100		Ω
$\overline{\text{MARGIN}}$ Pullup Current	I_{IN}		7	10	13	µA
$\overline{\text{MARGIN}}$ Input Voltage	V_{IL}				0.8	V
	V_{IH}		2.0			
$\overline{\text{MARGIN}}$ Glitch Rejection				100		ns

Note 1: Specifications guaranteed for the stated global conditions. 100% production tested at T_A = +25°C and T_A = +85°C. Specifications at T_A = -40°C to +85°C are guaranteed by design. These devices meet the parameters specified when at least one of IN1/IN2/IN3 is between 2.7V to 5.5V, while the remaining IN1/IN2/IN3 are between 0 and 5.5V.

Note 2: A current I_D = 2.5µA ±15% is generated internally and is used to set the DELAY and TIMEOUT periods and used as a reference for t_{DELAY} and $t_{TIMEOUT}$.

Note 3: The total DELAY is t_{DELAY} = 200µs + (500kΩ x C_{DELAY}). Leave DELAY unconnected for 200µs delay. The total TIMEOUT is $t_{TIMEOUT}$ = 200µs + (500kΩ x $C_{TIMEOUT}$). Leave TIMEOUT unconnected for 200µs timeout.

Note 4: A current I_S = 25µA ±10% is generated internally and used as a reference for t_{FAULT}, t_{RETRY}, and slew rate.

Note 5: During power-up, only the condition OUT_ < ramp - V_{TRK} is checked in order to stop the ramp. However, both conditions OUT_ < ramp – V_{TRK_F} and OUT_ > ramp + V_{TRK_F} cause a fault. During power-down, only the condition OUT > ramp + V_{TRK} is checked in order to stop the ramp. However, both conditions OUT_ < ramp - V_{TRK_F} and OUT_ > ramp + V_{TRK_F} cause a fault (see Figure 10). Therefore, if OUT1, OUT2, and OUT3 (during power-up tracking and power-down) differ by more than 2 x V_{TRK_F}, a fault condition is asserted.

Note 6: A 100Ω pulldown to GND activated by a fault condition. See the *Internal Pulldown* section.

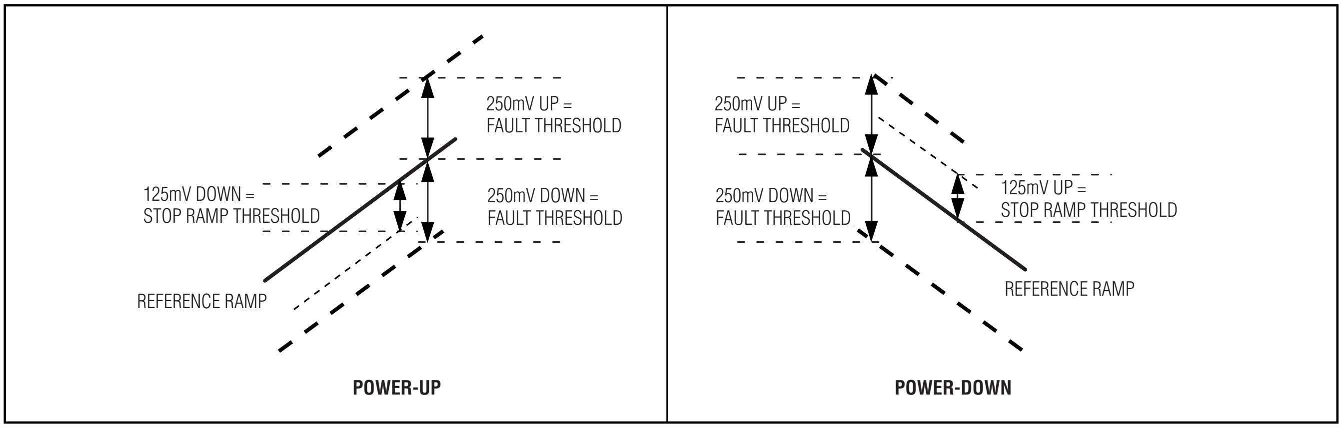


Figure 1. Stop Ramp/Fault Window During Power-Up and Power-Down

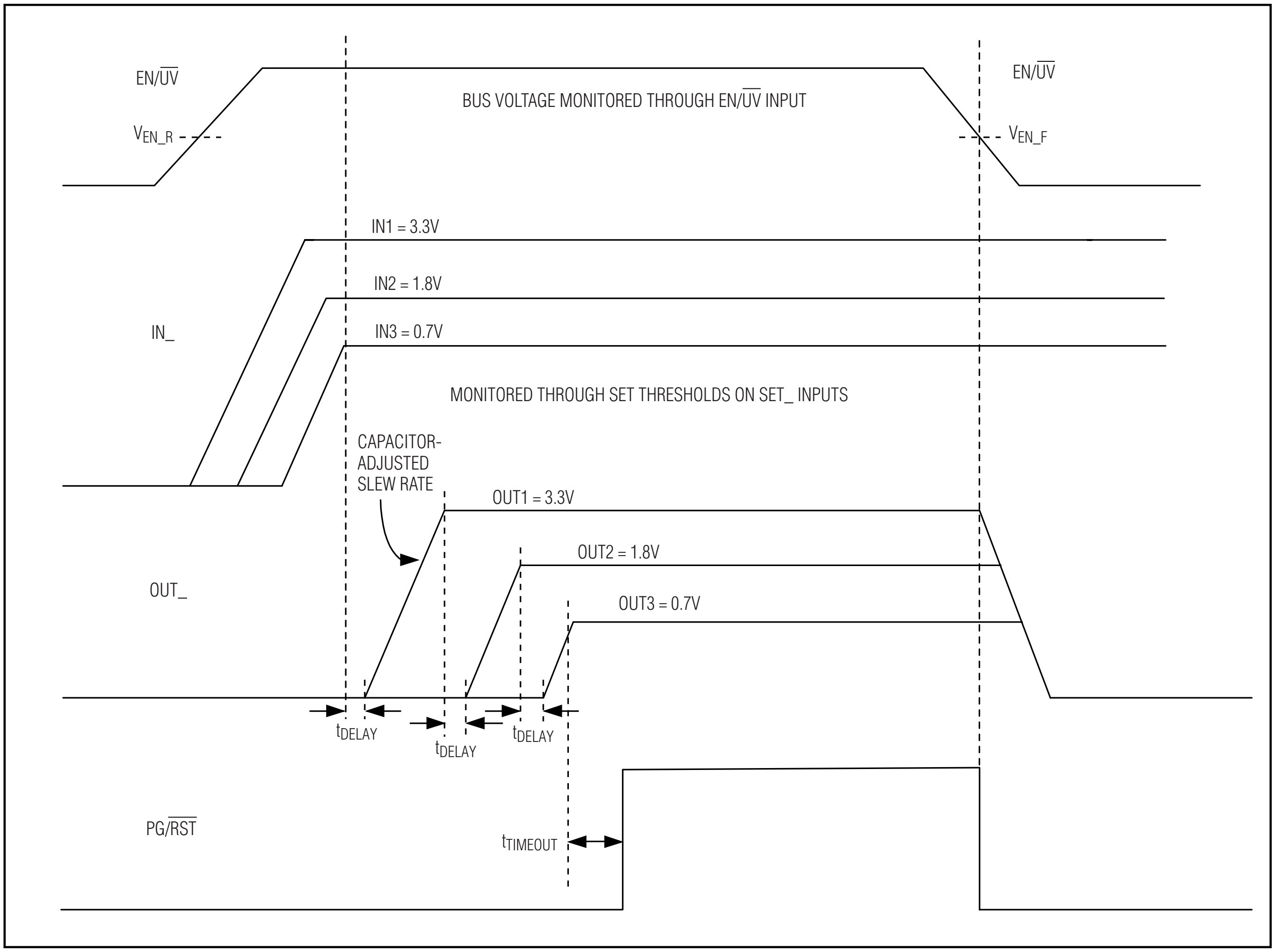


Figure 2. Sequencing In Normal Mode

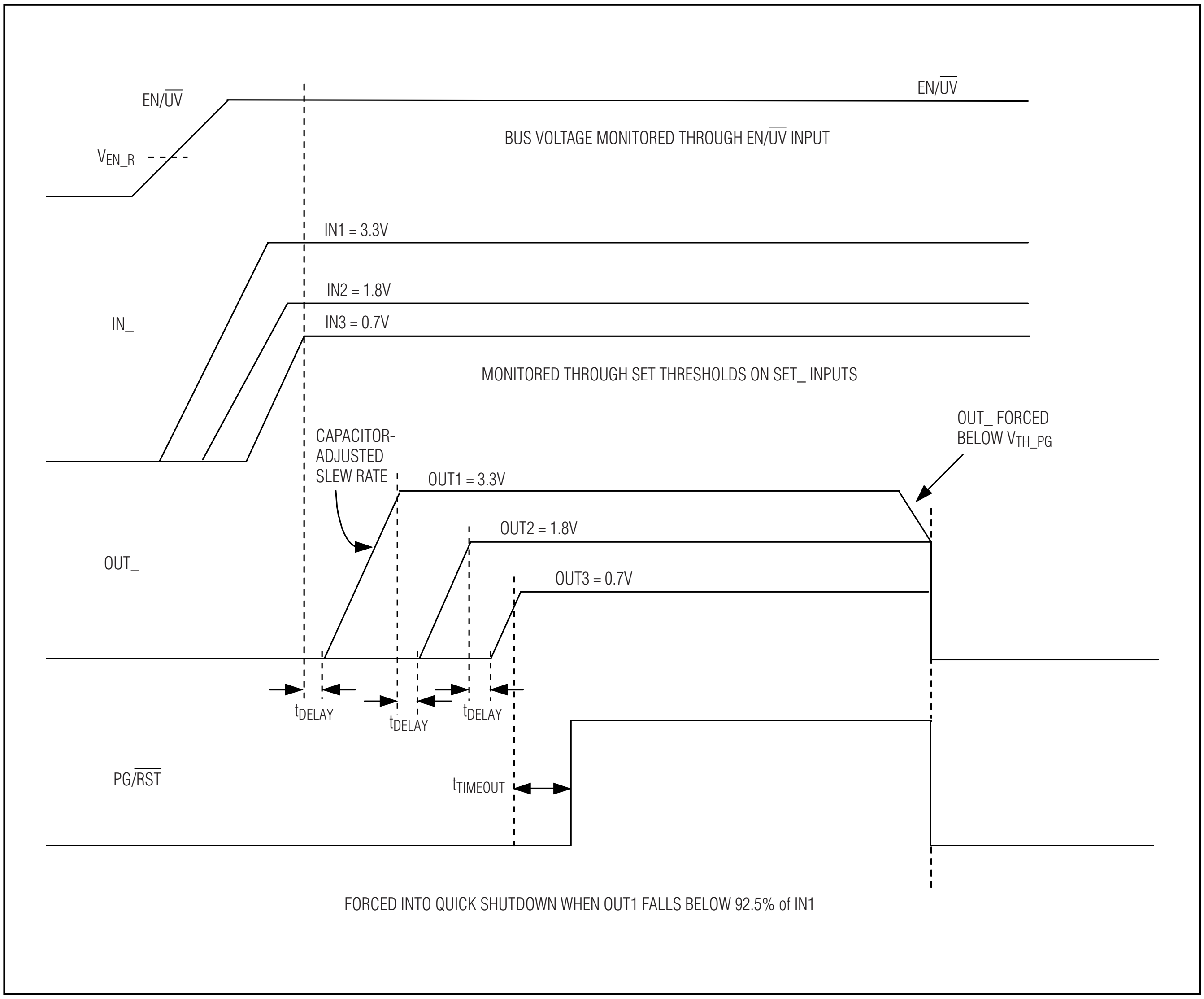


Figure 3. Sequencing In Fast Shutdown Mode

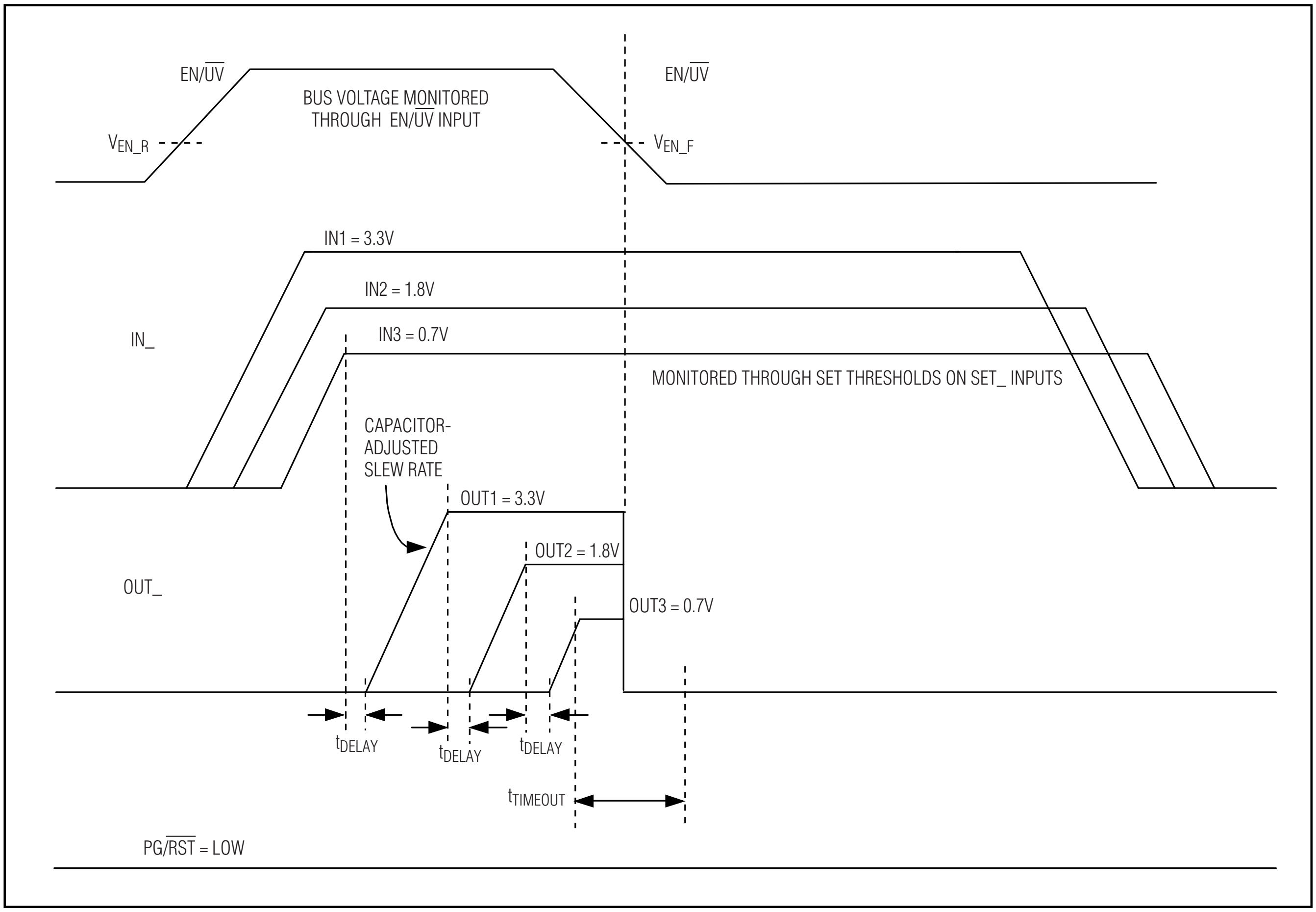


Figure 4. Timing Diagram (Aborted Sequencing)

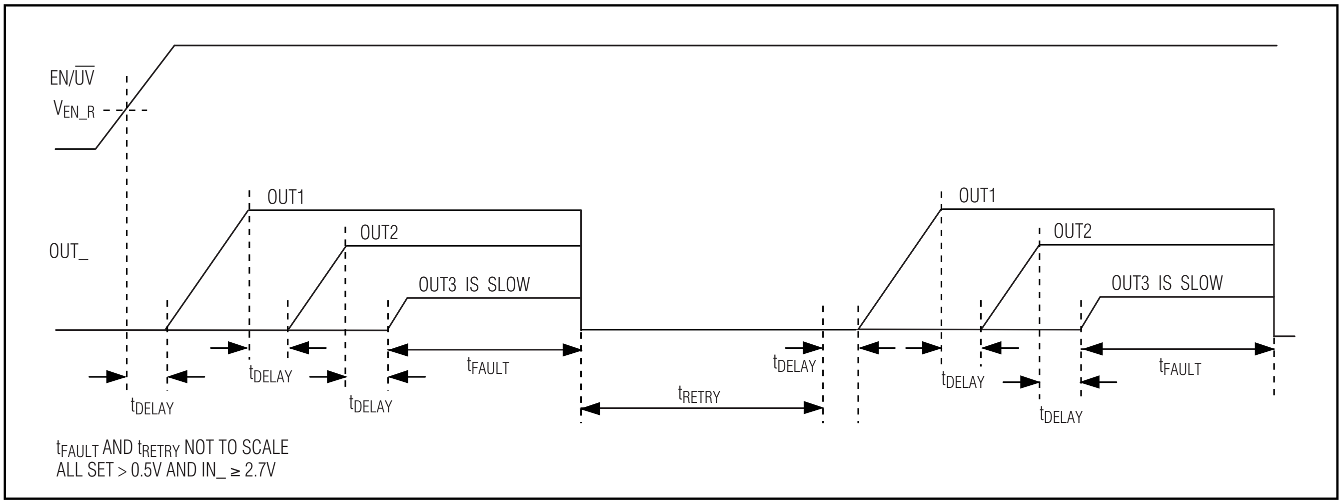
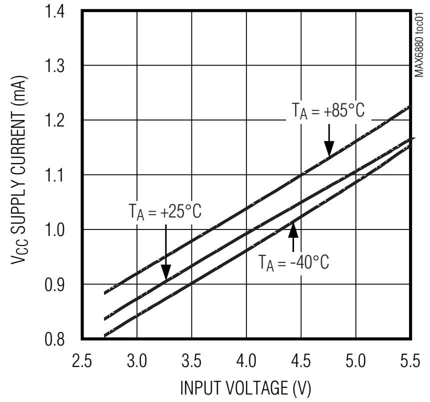


Figure 5. t_{FAULT} and t_{RETRY} Timing Diagram in Sequencing

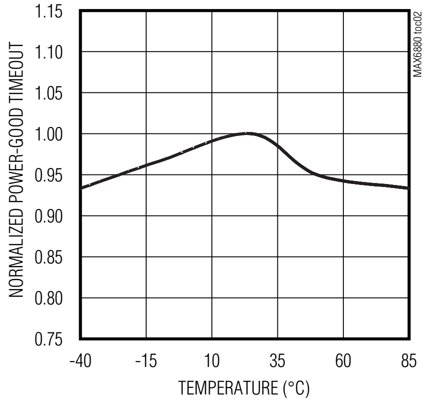
Typical Operating Characteristics

($V_{IN\_}$ = 2.7V to 5.5V, C_{SLEW} = 200pF, EN = $\overline{\text{MARGIN}}$ = ABP, T_A = +25°C, unless otherwise noted.)

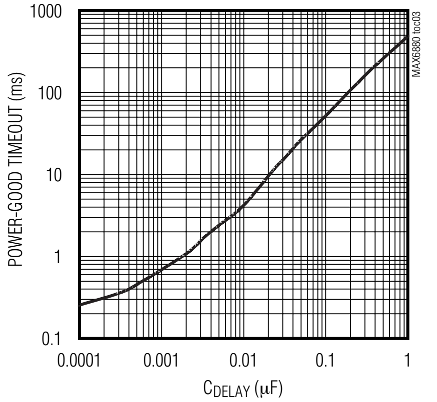
V_{CC} SUPPLY CURRENT vs. INPUT VOLTAGE



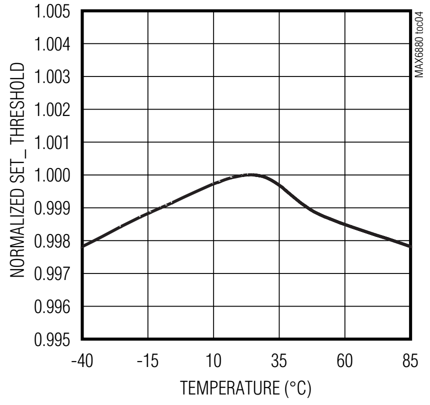
NORMALIZED POWER-GOOD TIMEOUT vs. TEMPERATURE



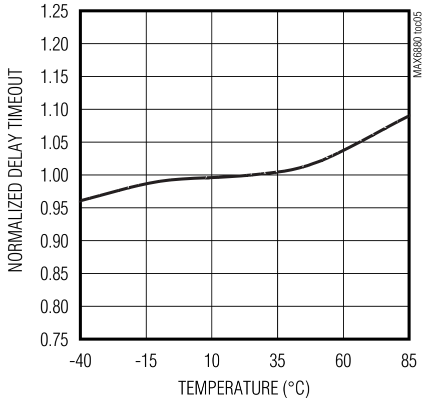
POWER-GOOD TIMEOUT vs. $C_{TIMEOUT}$



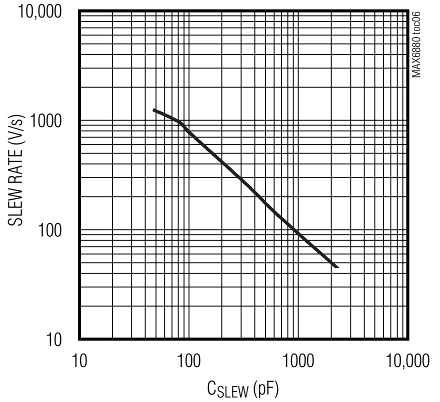
NORMALIZED SET_ THRESHOLD vs. TEMPERATURE



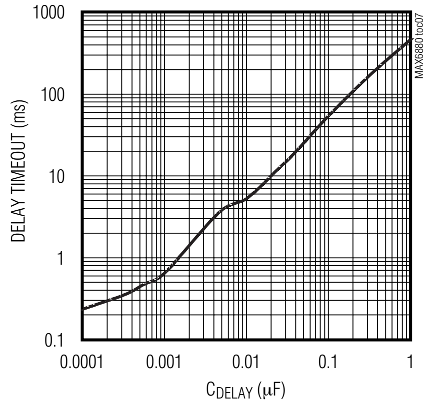
NORMALIZED DELAY TIMEOUT vs. TEMPERATURE



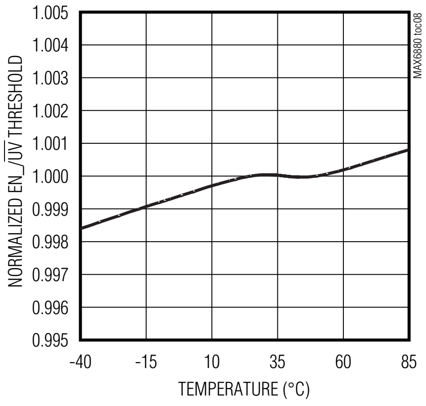
SLEW RATE vs. C_{SLEW}



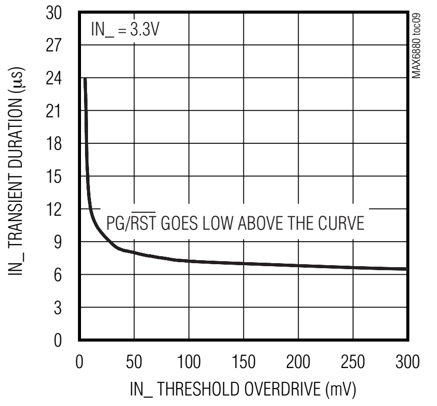
DELAY TIMEOUT vs. C_{DELAY}



NORMALIZED EN/$\overline{\text{UV}}$ THRESHOLD vs. TEMPERATURE



IN_ TRANSIENT DURATION vs. IN THRESHOLD OVERDRIVE

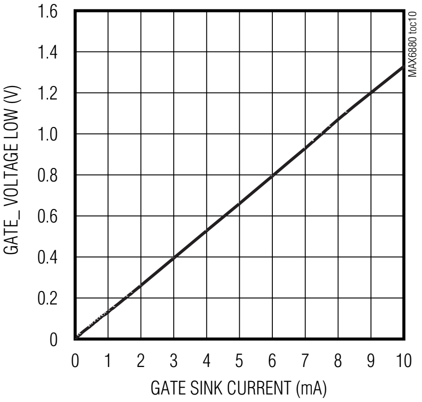


Dual-/Triple-Voltage, Power-Supply Sequencers/Supervisors

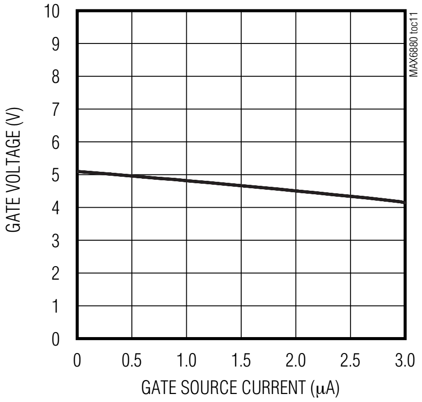
Typical Operating Characteristics (continued)

($V_{IN\_}$ = 2.7V to 5.5V, C_{SLEW} = 200pF, EN = $\overline{\text{MARGIN}}$ = ABP, T_A = +25°C, unless otherwise noted.)

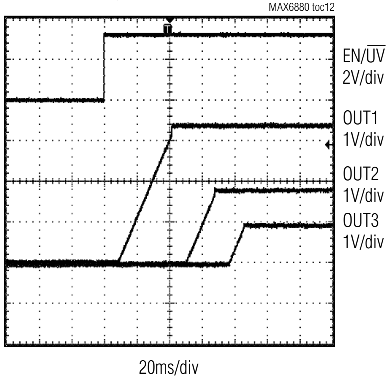
GATE_ VOLTAGE LOW vs. SINK CURRENT



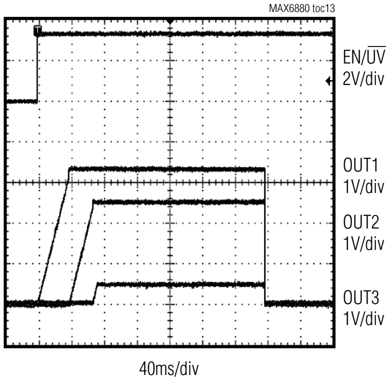
GATE_ OUTPUT VOLTAGE HIGH vs. GATE SOURCE CURRENT



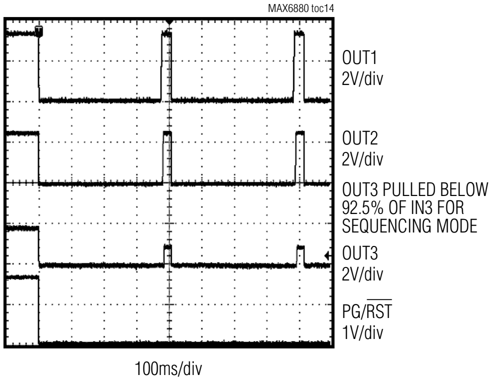
SEQUENCING MODE



FAST SHUTDOWN WITH RETRY



FAST SHUTDOWN WITH RETRY



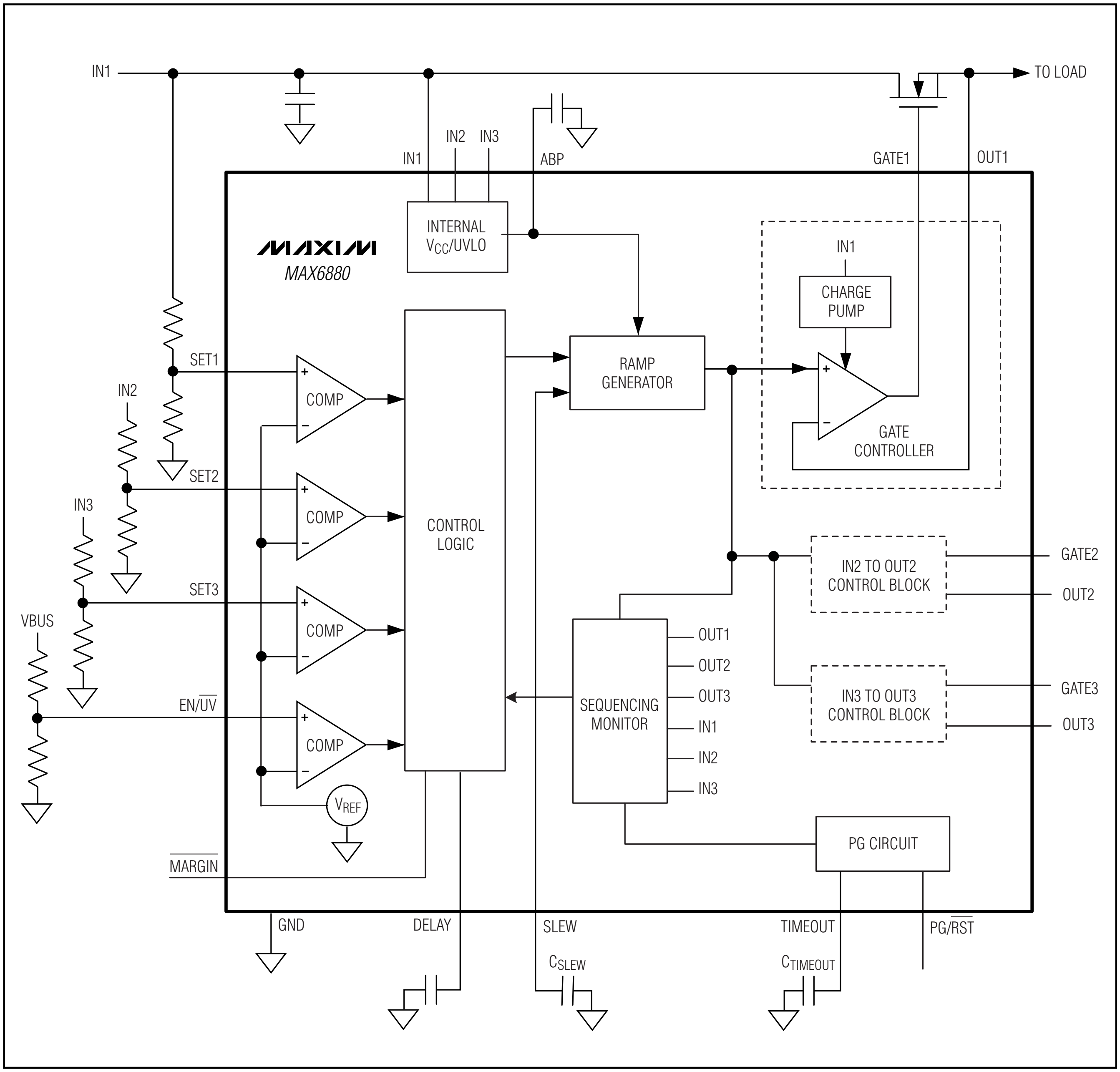
Pin Description

PIN				NAME	FUNCTION
MAX6880	**MAX6881**	**MAX6882**	**MAX6883**		
1, 11, 12, 15	—	—	1, 8, 9, 10	N.C.	No Connection. Not internally connected.
2	—	1	—	ABP	Internal Supply Bypass Input. Bypass ABP with a 1µF capacitor to GND. ABP maintains the device supply voltage during rapid power-down conditions.
3	2	—	—	SET3	Externally Adjusted IN_ Undervoltage Lockout Threshold. Connect SET_ to an external resistor-divider network to set the desired undervoltage threshold for each IN_ supply (see the *Typical Application Circuit*). All SET_ inputs must be above the internal SET_ threshold (0.5V) to enable sequencing functionality.
4	3	2	2	SET2	
5	4	3	3	SET1	
6	5	4	4	EN/$\overline{\text{UV}}$	Logic-Enable Input or Undervoltage Lockout Monitor Input. EN/$\overline{\text{UV}}$ must be high (EN/$\overline{\text{UV}}$ > V_{EN_R}) to enable voltage sequencing power-up operation. OUT_ begins tracking down when EN/$\overline{\text{UV}}$ < V_{EN_F}. Connect EN/$\overline{\text{UV}}$ to an external resistor-divider network to set the external UVLO threshold.
7	6	5	5	GND	Ground
8	7	6	6	DELAY	Sequence Delay Select Input. Connect a capacitor from DELAY to GND to select the desired delay period before sequencing is enabled (after all SET_ inputs and EN/$\overline{\text{UV}}$ are above their respective thresholds) or between supply sequences. Leave DELAY unconnected for the default 200µs delay period.
9	8	7	7	SLEW	Slew-Rate Adjustment Input. Connect a capacitor from SLEW to GND to select the desired OUT_ slew rate.
10	—	8	—	TIMEOUT	PG/$\overline{\text{RST}}$ Timeout Period Adjust Input. PG/$\overline{\text{RST}}$ asserts high after the timeout period when all OUT_ exceed their IN_ referenced threshold. Connect a capacitor from TIMEOUT to GND to set the desired timeout period. Leave TIMEOUT unconnected for the default 200µs delay period.
13	—	9	—	$\overline{\text{MARGIN}}$	Margin Input, Active-Low. Drive $\overline{\text{MARGIN}}$ low to enable margin mode (see the *Margin* section). The $\overline{\text{MARGIN}}$ functionality is disabled (returns to normal monitoring mode) after $\overline{\text{MARGIN}}$ returns high. $\overline{\text{MARGIN}}$ is internally pulled up to ABP through a 10µA current source.

Pin Description (continued)

PIN				NAME	FUNCTION
MAX6880	**MAX6881**	**MAX6882**	**MAX6883**		
14	—	10	—	PG/$\overline{RST}$	Power-Good Output, Open-Drain. PG_$\overline{RST}$ asserts high $t_{TIMEOUT}$ after all OUT_ voltages exceed the V_{TH_PG} thresholds.
16	9	—	—	OUT3	Channel 3 Monitored Output Voltage. Connect OUT3 to the source of an n-channel FET. A fault condition activates a 100Ω pulldown to ground.
17	10	—	—	GATE3	Gate Drive for External n-Channel FET. An internal charge pump boosts GATE3 to V_{IN3} + 5V to fully enhance the external n-channel FET when power-up is complete.
18	11	11	11	OUT2	Channel 2 Monitored Output Voltage. Connect OUT2 to the source of an n-channel FET. A fault condition activates a 100Ω pulldown to ground.
19	12	12	12	GATE2	Gate Drive for External n-Channel FET. An internal charge pump boosts GATE2 to V_{IN2} + 5V to fully enhance the external n-channel FET when power-up is complete.
20	13	13	13	OUT1	Channel 1 Monitored Output Voltage. Connect OUT1 to the source of an n-channel FET. A fault condition activates a 100Ω pulldown to ground.
21	14	14	14	GATE1	Gate Drive for External n-Channel FET. An internal charge pump boosts GATE1 to V_{IN1} + 5V to fully enhance the external n-channel FET when power-up is complete.
22	15	—	—	IN3	Supply Input Voltage. IN1, IN2, or IN3 must be greater than the internal undervoltage lockout (V_{ABP} = 2.7V) to enable the sequencing functionality. Each IN_ input is simultaneously monitored by SET_ inputs to ensure all supplies have stabilized before power-up is enabled. If IN_ is connected to ground or left unconnected and SET_ is above 0.5V, then no sequencing control is performed on that channel. Each IN_ is internally pulled down by a 100kΩ resistor.
23	16	15	15	IN2	
24	1	16	16	IN1	
EP	EP	EP	EP	EP	Exposed Paddle. Connect exposed paddle to ground.

Functional Diagram



Detailed Description

The MAX6880–MAX6883 multivoltage power sequencers/supervisors monitor three (MAX6880/MAX6881) and two (MAX6882/MAX6883) system voltages and provide proper power-up and power-down control for systems requiring voltage sequencing. These devices ensure the controlled voltages sequence in the proper order as system power supplies are enabled. The MAX6880–MAX6883 generate all required voltages and timing to control up to three external n-channel pass FETs for the OUT1/OUT2/OUT3 supply voltages.

The MAX6880–MAX6883 feature adjustable undervoltage thresholds for each input supply. When all of the voltages are above the adjusted thresholds these devices turn on the external n-channel MOSFETs to sequence the voltages to the system. The outputs are turned on one after the other, OUT1 first and OUT3 last.

The MAX6880–MAX6883 feature internal charge pumps to fully enhance the external FETs for low-voltage drops at highpass currents. The MAX6880/MAX6882 also feature a power-good output (PG/$\overline{RST}$) with a selectable timeout period that can be used for system reset.

The MAX6880–MAX6883 monitor up to three voltages. Devices may be configured to exclude any IN_. To disable sequencing operation of any IN_, connect the IN_ to ground (or leave unconnected) and connect SET_ to a voltage greater than 0.5V. The channel exclusion feature adds more flexibility to the device in a variety of different applications. As an example, the MAX6880 can sequence two voltages using IN1 and IN2 while IN3 is left disabled.

Powering the MAX6880–MAX6883

These devices derive power from either IN1, IN2, or IN3 voltage inputs (see the *Functional Diagram*). In order to ensure proper operation, at least one of the IN_ inputs must be at least +2.7V.

The highest input voltage on IN1/IN2/IN3 supplies power to the devices. Internal hysteresis ensures that the supply input that initially powers these devices continues to power the MAX6880–MAX6883 when multiple input voltages are within 100mV (typ) of each other.

Sequencing

The sequencing operation can be initiated after all input conditions for power-up are met $V_{EN/\overline{UV}}$ > 1.25V and all SET_ inputs are above the internal SET_ threshold (0.5V). In sequencing mode, the outputs are turned on sequentially, OUT1 first and OUT3 last. Before turning on each channel, a delay period is waited (programmable by connecting a capacitor from DELAY to ground. The power-up phase for each channel ends when its output voltage exceeds a fixed percentage (V_{TH_PG}) of the corresponding IN_ voltage. When all channels have exceeded these thresholds, PG/$\overline{RST}$ asserts high after $t_{TIMEOUT}$, indicating a successful sequence.

If there is a fault condition during the initial power-up sequence, the process is aborted.

When powering down, all outputs turn off simultaneously, tracking each other. No reverse power-down sequencing occurs.

The power-supply sequencing operation should be completed within the selected fault timeout period (t_{FAULT}) (see Figure 5). The total sequencing time is extended when the devices must vary the control slew rate to allow slow supplies to catch up. If the external FET is too small (R_{DS} is too high for the selected load current and IN_ source current), the OUT_ voltage may never reach the control ramp voltage. For a slew rate of 935V/s, a fault is signaled if all outputs have not stabilized within 22ms. For a slew rate of 93.5V/s, a fault is signaled if sequencing takes too long (more than 219ms).

The fault time period (t_{FAULT}) is set through the capacitor at SLEW (C_{SLEW}). Use the following formula to estimate the fault timeout period:

$$t_{FAULT} = 2.191 \times 10^8 \times C_{SLEW}$$

Autoretry Function

The MAX6880/MAX6881/MAX6882 feature autoretry modes to power-on again after a fault condition has been detected (see the *Typical Operating Characteristics*).

When a fault is detected, for a period of t_{RETRY}, GATE_ remains off and the 100Ω pulldowns are turned on. After the t_{RETRY} period, the device waits t_{DELAY} and retry sequencing if all power-up conditions are met (see Figure 5). These include all $V_{SET\_}$ > 0.5V, EN/$\overline{UV}$ > V_{EN_R}, and OUT_ voltages < V_{TH_PL}. The autoretry period t_{RETRY} is a function of C_{SLEW} (see Table 1).

Power-Up and Power-Down

During power-up, OUT_ is forced to follow the internal reference ramp voltage by an internal loop that controls the GATE_ of the external MOSFET. This phase must be completed within the adjustable fault timeout period (t_{FAULT}); otherwise, the part forces a shutdown on all GATE_.

Once the power-up is completed, a power-down phase can be initiated by forcing $V_{EN/\overline{UV}}$ below V_{EN_F}. The reference voltage ramp ramps down at the capacitor-adjusted slew rate. The control-loop comparators monitor each OUT_ voltage with respect to the common reference ramp voltage. During ramp down, if an OUT_ voltage is greater than the reference ramp voltage by more than V_{TRK}, the control loop dynamically stops the control ramp voltage from decreasing until the slow OUT_ voltage catches up. If an OUT_ voltage is greater or less than the reference ramp voltage by more than V_{TRK_F}, a fault is signaled and the fast-shutdown mode is initiated. In fast-shutdown mode, a 100Ω pulldown resistor is connected from OUT_ to GND to quickly discharge capacitance at OUT_, and GATE_ is pulled low with a strong I_{GDS} current (see Figure 3).

Figure 4 shows the aborted sequencing mode. When EN/$\overline{\text{UV}}$ goes low before $t_{TIMEOUT}$ expires, all the outputs go low, and the device goes into fast shutdown.

Internal Pulldown

To ensure that the OUT_ voltages are not held high by a large output capacitance after a fault has occurred, there is a 100Ω internal pulldown at OUT_. The pulldown ensures that all OUT_ voltages are below V_{TH_PL} (referenced to GND) before power-up cycling is initiated. The internal pulldown also ensures a fast discharge of the output capacitor during fast shutdown and fault modes. The pulldowns are not present during normal operation.

Stability Comment

No external compensation is required for sequencing or slew-rate control.

Inputs

IN1/IN2/IN3

The highest voltage on IN1, IN2, or IN3 supplies power to the device. The undervoltage threshold for each IN_ supply is set with an external resistor-divider from each IN_ to SET_ to ground. To disable sequencing on any IN_, connect IN_ to ground (or leave unconnected) and connect SET_ to a voltage greater than 0.5V.

Undervoltage Lockout Threshold Inputs (SET_)

The MAX6880/MAX6881 feature three and the MAX6882/MAX6883 feature two externally adjustable IN_ undervoltage lockout thresholds (SET1/SET2/SET3). The 0.5V SET_ threshold enables monitoring IN_ voltages as low as 0.5V. The undervoltage threshold for each IN_ supply is set with an external resistor-divider from each IN_ to SET_ to ground (see Figure 6). All SET_ inputs must be above the internal SET_ threshold (0.5V) to enable sequencing functionality. Use the following formula to set the UVLO threshold:

$$V_{IN\_} = V_{TH} (R1 + R2) / R2$$

where $V_{IN\_}$ is the undervoltage lockout threshold and V_{TH} is the 500mV SET threshold.

Margin Input ($\overline{\text{MARGIN}}$) (MAX6880/MAX6882)

$\overline{\text{MARGIN}}$ allows system-level testing while power supplies are below the normal ranges as adjusted by the SET_ inputs. Drive $\overline{\text{MARGIN}}$ low before varying system voltages below the adjusted thresholds to avoid signaling an error. The state of PG/$\overline{\text{RST}}$ does not change while $\overline{\text{MARGIN}}$ is low. PG/$\overline{\text{RST}}$ and all monitoring functions are disabled while MARGIN is low. $\overline{\text{MARGIN}}$ makes it possible to vary the supplies without a need to adjust the thresholds to prevent sequencer alerts. Drive $\overline{\text{MARGIN}}$ high or leave it unconnected for normal operating mode.

Slew-Rate Control Input (SLEW)

The reference ramp voltage slew rate during any controlled power-up/down phase can be programmed in the 90V/s to 950V/s range by connecting a capacitor (C_{SLEW}) from SLEW to ground. Use the following formula to calculate the typical slew rate:

$$\text{Slew Rate} = (9.35 \times 10^{-8}) / C_{SLEW}$$

where slew rate is in V/s and C_{SLEW} is in farads.

The capacitor at C_{SLEW} also sets the retry timeout period (t_{RETRY}), see Table 1.

For example, if C_{SLEW} = 100pF, we have t_{RETRY} = 350ms, t_{FAULT} = 21.91ms, slew rate = 935V/s. For example, if C_{SLEW} = 1nF, we have t_{RETRY} = 3.5s, slew rate = 93.5V/s.

C_{SLEW} is the capacitor on SLEW pad, and must be large enough so the parasitic PC board capacitance is negligible. C_{SLEW} should be in the range of 100pF < C_{SLEW} < 1nF.

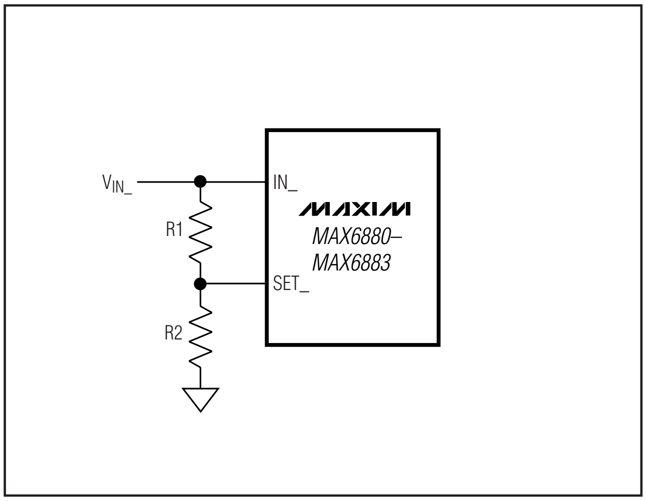


Figure 6. Setting the Undervoltage (UVLO) Thresholds

Table 1. C_{SLEW} Timing Formulas

TIME PERIOD	FORMULAS
Slew Rate	$(9.35 \times 10^{-8}) / C_{SLEW}$
t_{RETRY}	$3.506 \times 10^{9} \times C_{SLEW}$
t_{FAULT}	$2.191 \times 10^{8} \times C_{SLEW}$

Limiting Inrush Current

The capacitor (C_{SLEW}) at SLEW to ground, controls the OUT_ slew rate, thus controlling the inrush current required to charge the load capacitor at OUT_. Using the programmed slew rate, limit the inrush current by using the following formula:

$$I_{INRUSH} = C_{OUT} \times SR$$

where I_{INRUSH} is in amperes, C_{OUT} is in farads, and SR is in V/s.

Delay Time Input (DELAY)

To adjust the desired delay period (t_{DELAY}) before sequencing is enabled, connect a capacitor (C_{DELAY}) between DELAY to ground (see Figures 2 to 5). The selected delay time is also enforced when EN/$\overline{UV}$ rises from low to high when all the input voltages are present. Use the following formula to calculate the delay time:

$$t_{DELAY} = 200\mu s + (500k\Omega \times C_{DELAY})$$

where t_{DELAY} is in µs and C_{DELAY} is in farads. Leave DELAY unconnected for the default 200µs delay.

Timeout Period Input (TIMEOUT) (MAX6880/MAX6882)

These devices feature a PG/$\overline{RST}$ timeout period. Connect a capacitor ($C_{TIMEOUT}$) from TIMEOUT to ground to program the PG/$\overline{RST}$ timeout period. After all OUT_ outputs exceed their IN_ referenced thresholds (V_{TH_PG}), PG/$\overline{RST}$ remains low for the selected timeout period $t_{TIMEOUT}$ (see Figure 3).

$$t_{TIMEOUT} = 200\mu s + (500k\Omega \times C_{TIMEOUT})$$

where $t_{TIMEOUT}$ is in µs and $C_{TIMEOUT}$ is in farads. Leave TIMEOUT unconnected for the default 200µs timeout delay.

Logic-Enable Input (EN/$\overline{UV}$)

Drive logic EN/$\overline{UV}$ input above V_{EN_R} to initiate voltage sequencing during power-up operation. Drive logic EN/$\overline{UV}$ below V_{EN_F} to initiate tracking power-down operation. Connect EN/$\overline{UV}$ to an external resistor-divider network to set the external undervoltage lockout threshold.

ABP Input (MAX6880/MAX6882)

ABP powers the analog circuitry. Bypass ABP to GND with a 1µF ceramic capacitor installed as close to the device as possible. ABP takes the highest voltage of IN_. Do not use ABP to provide power to external circuitry. ABP maintains the device supply voltage during rapid power-down conditions.

OUT1/OUT2/OUT3

The MAX6880/MAX6881 monitor three OUT_ and the MAX6882/MAX6883 monitor two OUT_ outputs to control the sequencing performance. After the internal supply (ABP) exceeds the minimum voltage (2.7V) requirements, EN/$\overline{UV}$ > V_{EN_R}, and IN1/IN2/IN3 are all greater than their adjusted SET_ thresholds, OUT1/OUT2/OUT3 begin to sequence.

During fault conditions, an internal pulldown resistor (100Ω) on OUT_ is enabled to help discharge load capacitance (100Ω is connected for fast power-down control).

Outputs

*GATE_*

The MAX6880–MAX6883 feature up to three GATE_ outputs to drive up to three external n-channel FET gates. The following conditions must be met before GATE_ begins enhancing the external n-channel FET_:

1) All SET_ inputs (SET1/SET2/SET3) are above their 0.5V thresholds.
2) At least one IN_ input is above the minimum operating voltage (2.7V).
3) EN/$\overline{UV}$ > 1.25V.

At power-up mode, GATE_ voltages are enhanced by control loops so all OUT_ voltages sequence at a capacitor-adjusted slew rate. Each GATE_ is internally pulled up to 5V above its relative IN_ voltage to fully enhance the external n-channel FET when power-up is complete.

Power-Good Output (PG/$\overline{RST}$) (MAX6880/MAX6882)

The MAX6880/MAX6882 include a power-good (PG/$\overline{RST}$) output. PG/$\overline{RST}$ is an open-drain output and requires an external pullup resistor.

All the OUT_ outputs must exceed their IN_ referenced thresholds (IN_ x V_{TH_PG}) for the selected reset timeout period $t_{TIMEOUT}$ (see the *TIMEOUT Period Input* section) before PG/$\overline{RST}$ asserts high. PG/$\overline{RST}$ stays low for the selected reset timeout period ($t_{TIMEOUT}$) after all the OUT_ voltages exceed their IN_ referenced thresholds. PG/$\overline{RST}$ goes low when $V_{SET\_}$ < V_{TH} or $V_{EN/\overline{UV}}$ < V_{EN_R} (see Figure 2).

Applications Information

MOSFET Selection

The external pass MOSFET is connected in series with the sequenced power-supply source. Since the load current and the MOSFET drain-to-source impedance (R_{DS}) determine the voltage drop, the on characteristics of the MOSFET affect the load supply accuracy. The MAX6880–MAX6883 fully enhance the external MOSFET out of its linear range to ensure the lowest drain-to-source on-impedance. For highest supply accuracy/lowest voltage drop, select a MOSFET with an appropriate drain-to-source on-impedance with a gate-to-source bias of 4.5V to 6.0V.

Layout and Bypassing

For better noise immunity, bypass each of the IN_ inputs to GND with 0.1µF capacitors installed as close to the device as possible. Bypass ABP to GND with a 1µF capacitor installed as close to the device as possible. ABP is an internally generated voltage and must not be used to supply power to external circuitry.

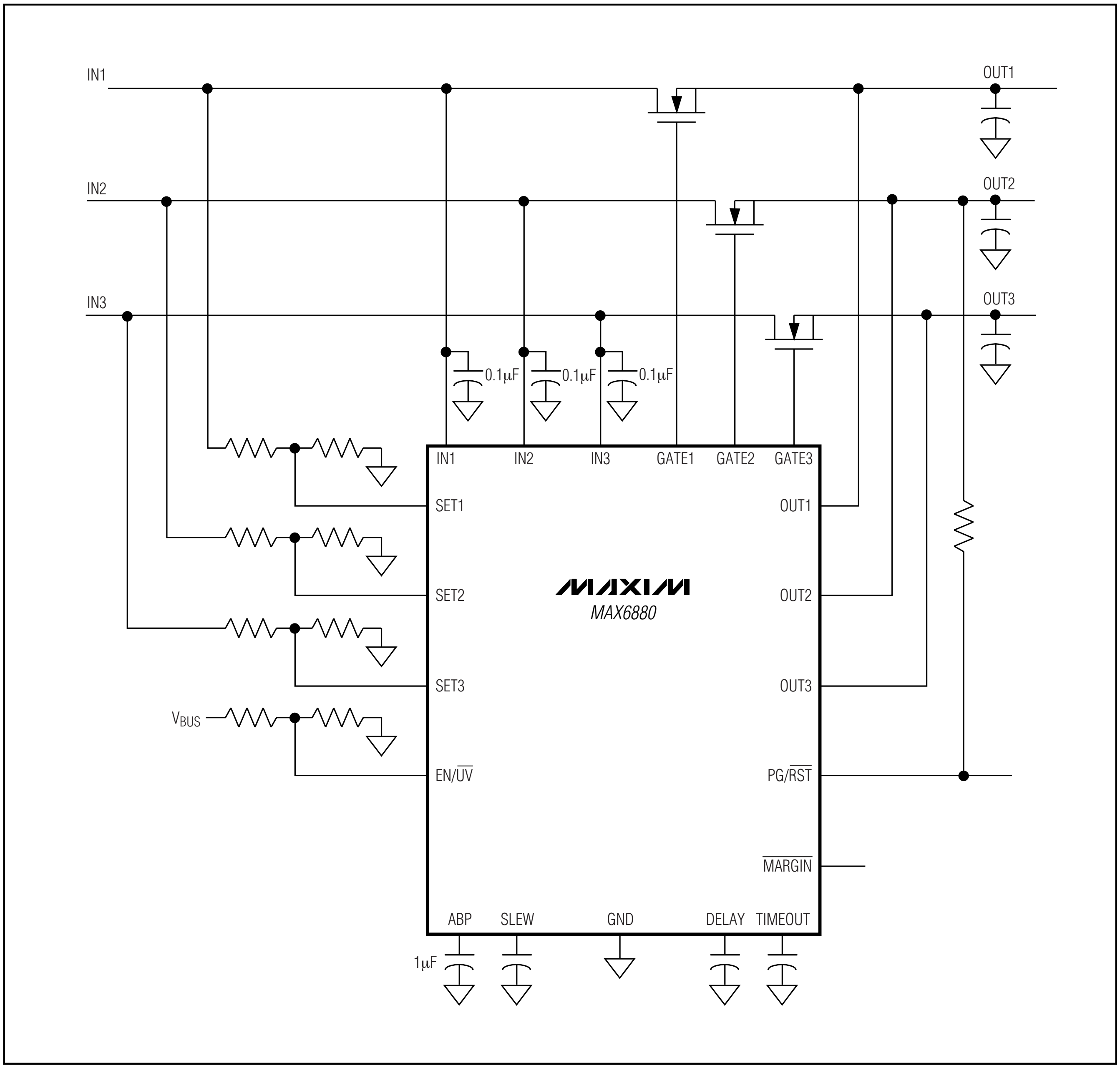
Selector Guide

PART	CHANNEL	TIMEOUT SELECTABLE	PG/$\overline{\text{RST}}$	$\overline{\text{MARGIN}}$	PG THRESHOLD VOLTAGE (%)
MAX6880	3	Yes	Yes	Yes	92.5
MAX6881	3	No	No	No	—
MAX6882	2	Yes	Yes	Yes	92.5
MAX6883	2	No	No	No	—

Chip Information

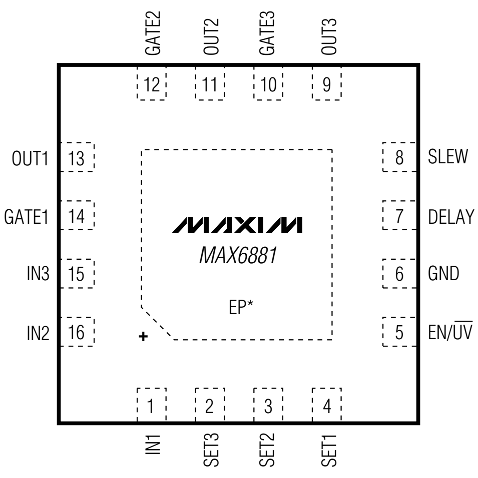
PROCESS: BiCMOS

Typical Application Circuit

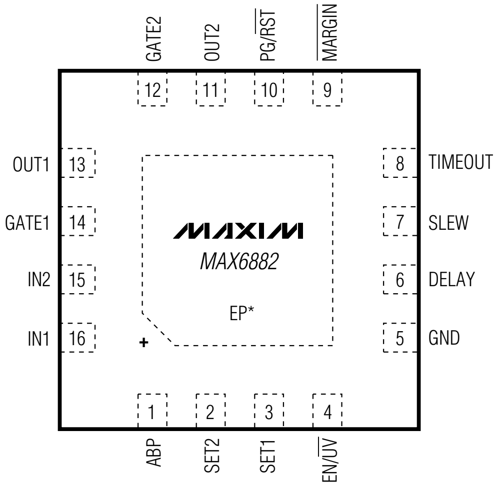


Pin Configurations (continued)

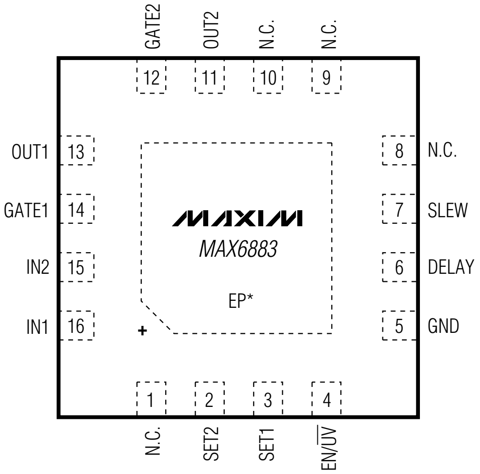
TOP VIEW



4mm x 4mm THIN QFN



4mm x 4mm THIN QFN

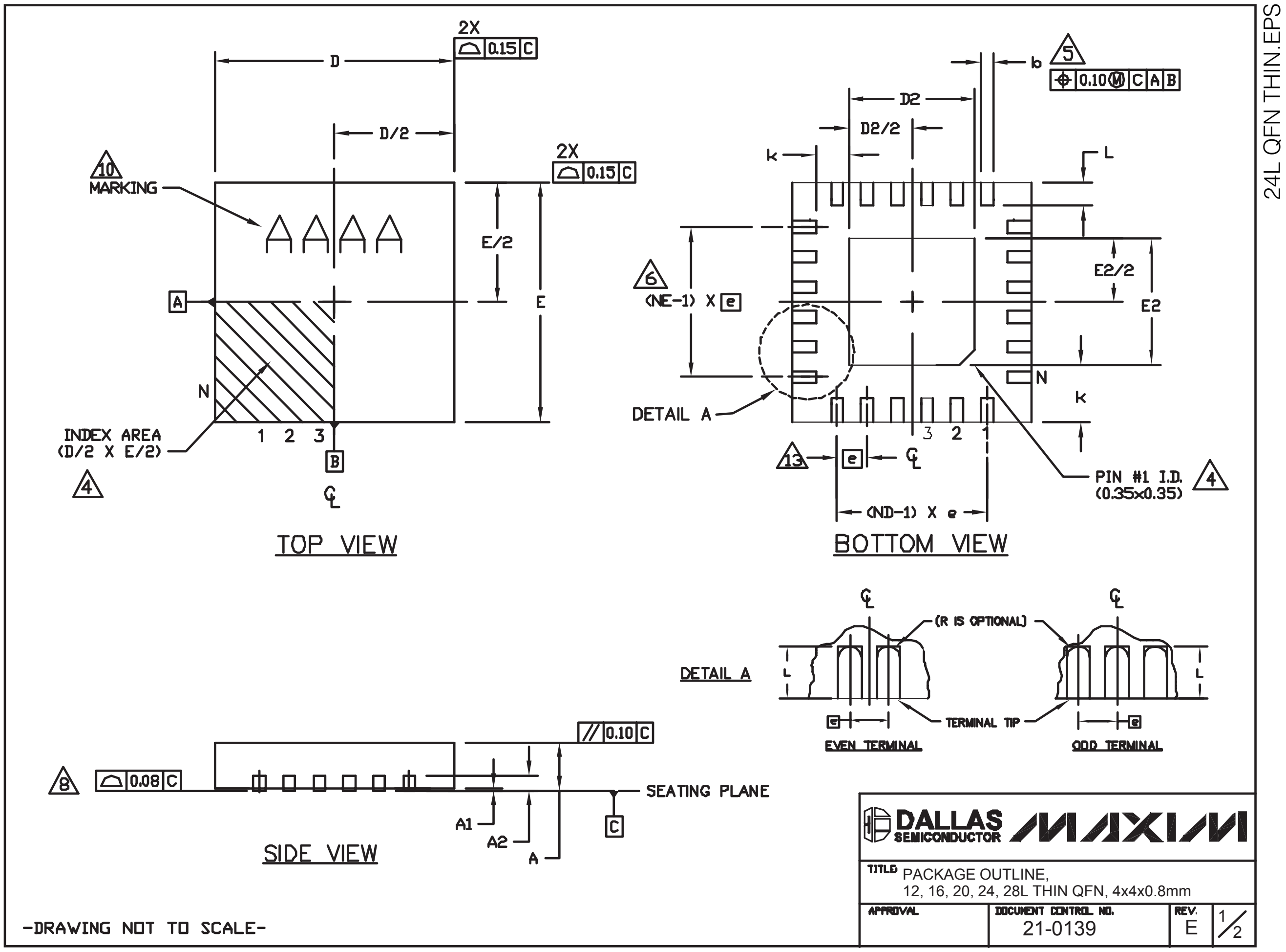


4mm x 4mm THIN QFN

*EXPOSED PADDLE CONNECTED TO GND.

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE,
12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm

APPROVAL | DOCUMENT CONTROL NO. 21-0139 | REV. E | 2/2

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