FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12533-1E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89610R Series

MB89613R/615R

■ DESCRIPTION

MB89610R series has been developed as a general-purpose version of the F²MC*-8L family of proprietary 8-bit, single-chip microcontrollers.

In addition to the F²MC-8L CPU core which can operate at low voltage but at high speed, the microcontrollers contain peripheral resources such as timers, serial interfaces, and an external interrupt.

The MB89610R series is applicable to a wide range of application from welfare products to industrial equipment, including portable devices.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- Various package options
  Three types of QFP packages (0.5-mm, 0.65-mm, 1-mm pitch)
  SDIP package
- High-speed processing at low voltages
  Minimum execution time: 0.4 µs/3.5 V and 0.8 µs/2.7 V
- F²MC-8L family CPU core

  Instruction set optimized for controllers
  - Multiplication and dividion instructions
  - 16-bit arithmetic operations
  - Test and branch instructions
  - Bit manipulation instructions, etc.

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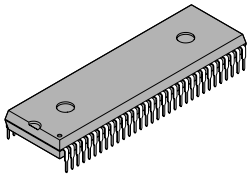
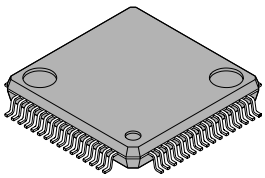
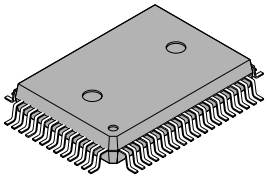
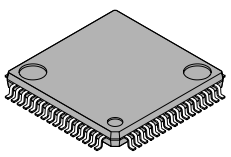
■ PACKAGES

64-pin Plastic SH-DIP	64-pin Plastic SQFP	64-pin Plastic QFP	64-pin Plastic QFP
			
(DIP-64P-M01)	(FPT-64P-M03)	(FPT-64P-M06)	(FPT-64P-M09)

(Continued)

- Four types of timers
  8-bit PWM timer (also usable a reload timer)
  8-bit pulse-width count timer (Continuous measurement capable, applicable to remote control, etc)
  16-bit timer/counter
  20-bit time-base timer
- Two serial interfaces
  Switchable transfer direction allows communication with various equipment.
- External interrupt: 4 channels
  Four channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
- Bus interface function
  Including hold and ready functions

■ PRODUCT LINEUP

Part number / Parameter	MB89613R	MB89615R	MB89P625/W625*1	MB89PV620*1
Classification	Mass production product (mask ROM products)		One-time PROM product/EPROM product	Pggyback/evaluation product (for evaluation and development)
ROM size	8 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal PROM, programming with general-purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	256 × 8 bits	512 × 8 bits		1 K × 8 bits
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.4 µs/10 MHz Interrupt processing time: 3.6 µs/10 MHz			
Ports	Input ports: 5 (4 ports also serve as peripherals) Output ports (N-ch open-drain): 8 I/O ports (N-ch open-drain): 8 (4 ports also serve as peripherals) Output ports (CMOS): 8 (All also serve as bus control pins) I/O ports (CMOS): 24 (All also serve as bus pins or peripherals) Total: 53			
8-bit PWM timer	8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 µs to 3.3 ms) 8-bit resolution PWM operation (conversion cycle: 10 µs to 839 ms)			

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Parameter \ Part number	MB89613R	MB89615R	MB89P625/W625*1	MB89PV620*1
Pulse width count timer	8-bit timer operation (overflow output capable, operating clock cycle: 0.4 µs to 12.8 µs) 8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 µs to 12.8 µs) 8-bit pulse width measurement operation (continuous measurement capable: "H" pulse width/"L" pulse width/from ↑ to ↑/from ↓ to ↓)			
16-bit timer/ counter	16-bit timer operation (operating clock cycle: 0.4 µs) 16-bit event counter operation (rising edge/falling edge/both edges selectability)			
8-bit Serial I/O 1 8-bit Serial I/O 2	8 bits LSB first/MSB first selectability One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 0.8 µs, 3.2 µs, 12.8 µs)			
External interrupt	Four independent channels (edge selection, interrupt vector, and interrupt source flag) Rising edge/falling edge selectability Used also for wake-up from stop/sleep mode (edge detection is also permitted in stop mode)			
Standby mode	Sleep mode and stop mode			
Process	CMOS			
Operating voltage*2	2.2 V to 6.0 V		2.7 V to 6.0 V	
EPROM for use	—			MBM27C256A-20CZ MBM27C256A-20TV

*1: One-time PROM product/EPROM product, and piggyback/evaluation product are applicable to the MB89620 series.

*2: Varies with conditions such as the operating frequency (See section "■ Electrical Characteristics.") In the case of the MB89PV620, the voltage varies with the restrictions the ICE or EPROM for use.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89613R MB89615R	MB89P625	MB89W625	MB89PV620
DIP-64P-M01	○	○	×	×
DIP-64C-A06	×	×	○	×
FPT-64P-M03	○	×*	×*	×*
FPT64P-M06	○	○	×	×
FPT-64P-M09	○	○	×*	×*
MDP-64C-P02	×	×	×	○
MQF-64C-P01	×	×	×	○

○ : Available × : Not available

* : Lead pitch converter sockets (manufacturer: Sun Hayato Co., Ltd.) are available.
64SD-64SQF-8L: For conversion from DIP-64P-M01 or DIP-64C-A06 to FPT-64P-M03
64SD-64QF2-8L: For conversion from DIP-64P-M01 or DIP-64C-A06 to FPT-64P-M09
Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

Notes: • For more information about each package, see section "■ Package Dimensions."
• One-time PROM product/EPROM product, and piggyback/evaluation product are applicable to the MB89620 series.

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89613R, the upper half of the register bank cannot be used.
- The stack area, etc., is set at the upper limit of the RAM.
- External area is used.

2. Current Consumption

- In the case of the MB89PV620, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than a product with a mask ROM.
- However, the current consumption in sleep/stop modes is the same. (For more information, see sections "■ Electrical Characteristics" and "■ Example Characteristics."

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section "■ Mask Options."

Take particular care on the following points:

- Pull-up resistor cannot be set for P40 to P47 on the MB89P625 and MB89W625.
- Options are fixed on the MB89PV620.

4. Differences between the MB89610 and MB89610R Series

- Memory access area
  Memory access area of both the MB89615 and MB89615R is the same.
  The access area of the MB89613 is different from that of the MB89613R when using in external bus mode. See below.

Address	Memory area	
	MB89613	MB89613R
0000_H to $007F_H$	I/O area	I/O area
0080_H to $017F_H$	RAM area	RAM area
0180_H to $027F_H$	External area	Access prohibited
0280_H to $BFFF_H$		External area
$C000_H$ to $DFFF_H$		Access prohibited
$E000_H$ to $FFFF_H$	ROM area	ROM area

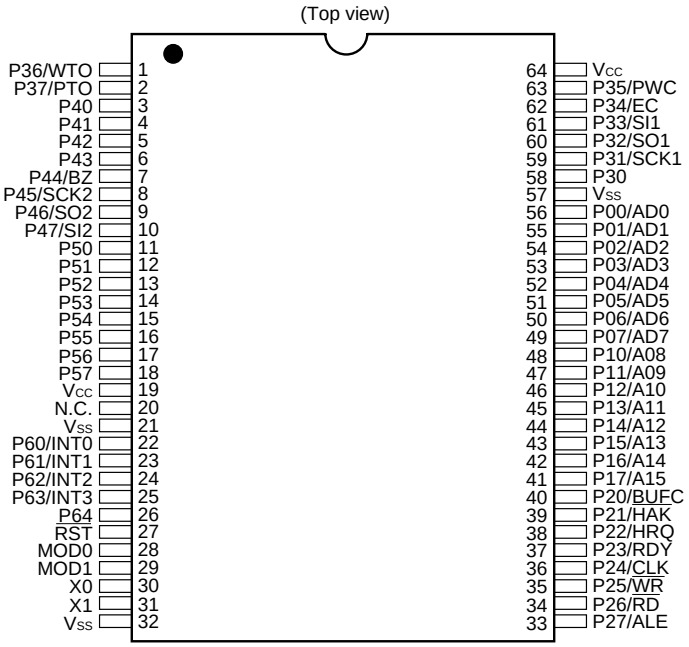
- Other specifications
  Both the MB89610 and MB89610R is the same.
- Electrical specifications/electrical characteristics
  Electrical specifications of the MB89610R series are the same with that of the MB89610 series.
  For electrical characteristics, refer to the MB89620R series data sheet.

■ CORRESPONDENCE BETWEEN THE MB89610 AND MB89610R SERIES

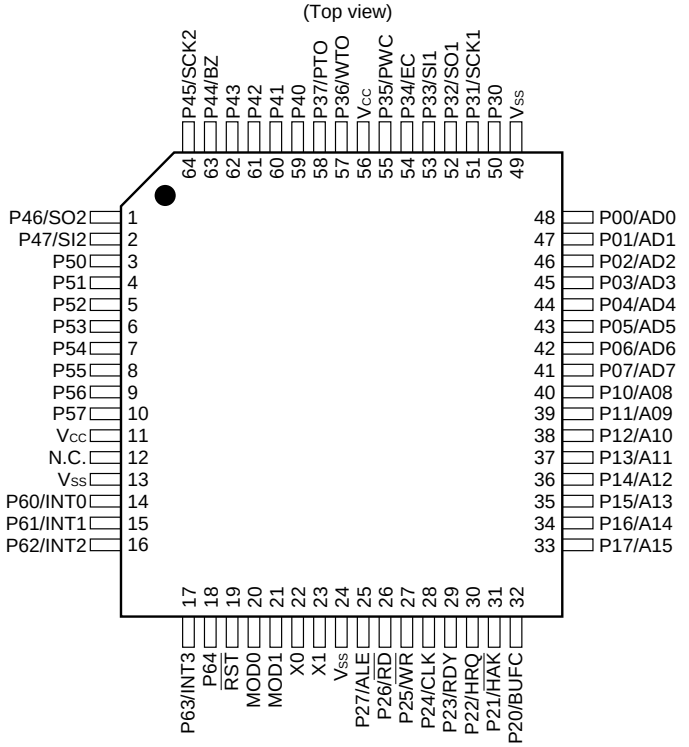
- The MB89610R series is the reduction version of the MB89610 series.
- The MB89610 and MB89610R series consist of the following products:

MB89610 series	MB89613	MB89615
MB89610R series	MB89613R	MB89615R

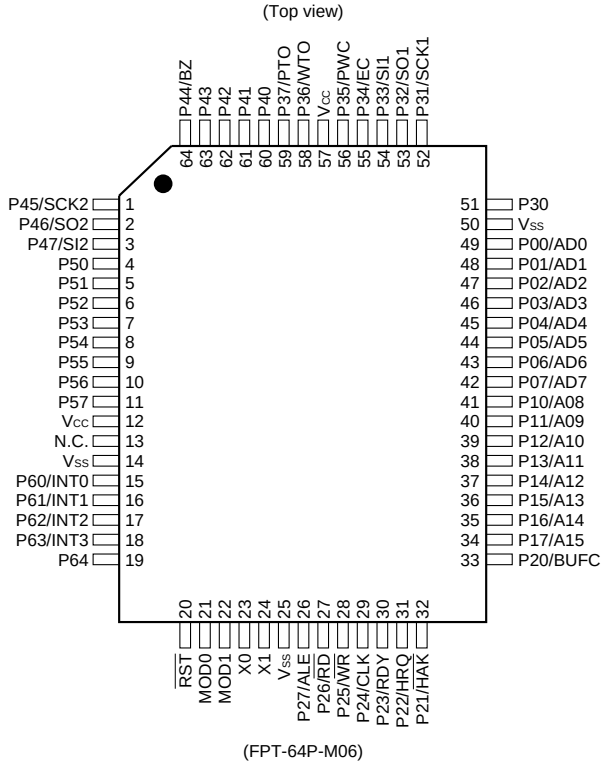
■ PIN ASSIGNMENT



(DIP-64P-M01)



(FPT-64P-M03)
(FPT-64P-M09)


(Top view)
P44/BZ 64
P43 63
P42 62
P41 61
P40 60
P37/PTO 59
P36/WTO 58
VCC 57
P35/PWC 56
P34/EC 55
P33/SI1 54
P32/SO1 53
P31/SCK1 52
P45/SCK2 1
P46/SO2 2
P47/SI2 3
P50 4
P51 5
P52 6
P53 7
P54 8
P55 9
P56 10
P57 11
VCC 12
N.C. 13
VSS 14
P60/INT0 15
P61/INT1 16
P62/INT2 17
P63/INT3 18
P64 19
51 P30
50 VSS
49 P00/AD0
48 P01/AD1
47 P02/AD2
46 P03/AD3
45 P04/AD4
44 P05/AD5
43 P06/AD6
42 P07/AD7
41 P10/A08
40 P11/A09
39 P12/A10
38 P13/A11
37 P14/A12
36 P15/A13
35 P16/A14
34 P17/A15
33 P20/BUFC
RST 20
MOD0 21
MOD1 22
X0 23
X1 24
VSS 25
P27/ALE 26
P26/RD 27
P25/WR 28
P24/CLK 29
P23/RDY 30
P22/HRQ 31
P21/HAK 32

(FPT-64P-M06)

■ PIN DESCRIPTION

Pin no.			Pin name	Circuit type	Function
SH-DIP*1, MDIP*2	QFP1*3 MQFP*4	SQFP*5 QFP2*6			
30	23	22	X0	A	Crystal oscillator pins
31	24	23	X1		
28	21	20	MOD0	B	Operating mode selection pins Connected directly to V_{CC} or V_{SS}.
29	22	21	MOD1		
27	20	19	$\overline{RST}$	C	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. “L” is output from this pin by an internal reset source. The internal circuit is initialized by the input of “L”.
56 to 49	49 to 42	48 to 41	P00/AD0 to P07/AD7	D	General-purpose I/O ports When an external bus is used, these ports function as multiplex pins of lower addresses output and data I/O.
48 to 41	41 to 34	40 to 33	P10/A08 to P17/A15	D	General-purpose I/O ports When an external bus is used, these ports function as upper addresses output.
40	33	32	P20/BUFC	F	General-purpose output-only port When an external bus is used, this port can also be used as a buffer control output by setting of BCTR.
39	32	31	P21/$\overline{HAK}$	F	General-purpose output-only port When an external bus is used, this port can also be used as a hold acknowledge output by setting of BCTR.
38	31	30	P22/HRQ	D	General-purpose output-only port When an external bus is used, this port can also be used as a hold request input by setting of BCTR.
37	30	29	P23/RDY	D	General-purpose output-only port When an external bus is used, this port functions as a ready input.
36	29	28	P24/CLK	F	General-purpose output-only port When an external bus is used, this port functions as a clock output.
35	28	27	P25/$\overline{WR}$	F	General-purpose output-only port When an external bus is used, this port functions as a write signal output.
34	27	26	P26/$\overline{RD}$	F	General-purpose output-only port When an external bus is used, this port functions as a read signal output.
33	26	25	P27/ALE	F	General-purpose output-only port When an external bus is used, this port functions as an address latch signal output.

*1: DIP-64P-M01, DIP-64C-A06
*2: MDP-64C-P02
*3: FPT-64P-M06
*4: MQP-64C-P01
*5: FPT-64P-M03
*6: FPT64P-M09

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Pin no.			Pin name	Circuit type	Function
SH-DIP*1, MDIP*2	QFP1*3 MQFP*4	SQFP*5 QFP2*6			
58	51	50	P30	E	General-purpose I/O port This port is a hysteresis input type.
59	52	51	P31/SCK1	E	General-purpose I/O port Also serves as the clock I/O for the 8-bit serial I/O 1. This port is a hysteresis input type.
60	53	52	P32/SO1	E	General-purpose I/O port Also serves as the data output for the 8-bit serial I/O 1. This port is a hysteresis input type.
61	54	53	P33/SI1	E	General-purpose I/O port Also serves as the data input for the 8-bit serial I/O 1. This port is a hysteresis input type.
62	55	54	P34/EC	E	General-purpose I/O port Also serves as the external clock input for the 16-bit timer/counter. This port is a hysteresis input type.
63	56	55	P35/PWC	E	General-purpose I/O port Also serves as the measured pulse input for the 8-bit pulse width count timer. This port is a hysteresis input type.
1	58	57	P36/WTO	E	General-purpose I/O port Also serves as the toggle output for the 8-bit pulse width count timer. This port is a hysteresis input type.
2	59	58	P37/PTO	E	General-purpose I/O port Also serves as the toggle output for the 8-bit PWM timer. This port is a hysteresis input type.
3 to 6	60 to 63	59 to 62	P40 to P43	G	N-ch open-drain I/O ports This port is a hysteresis input type.
7	64	63	P44/BZ	G	N-ch open-drain I/O port Also serves as the buzzer output. This port is a hysteresis input type.
8	1	64	P45/SCK2	G	N-ch open-drain I/O port Also serves as the clock I/O for the 8-bit serial I/O 2. This port is a hysteresis input type.
9	2	1	P46/SO2	G	N-ch open-drain I/O port Also serves as the data output for the 8-bit serial I/O 2. This port is a hysteresis input type.
10	3	2	P47/SI2	G	N-ch open-drain I/O port Also serves as the data input for the 8-bit serial I/O 2. This port is a hysteresis input type.
11 to 18	4 to 11	3 to 10	P50 to P57	H	N-ch open-drain output-only ports

*1: DIP-64P-M01, DIP-64C-A06
*2: MDP-64C-P02
*3: FPT-64P-M06
*4: MQP-64C-P01
*5: FPT-64P-M03
*6: FPT64P-M09

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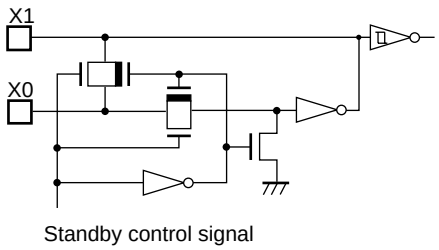
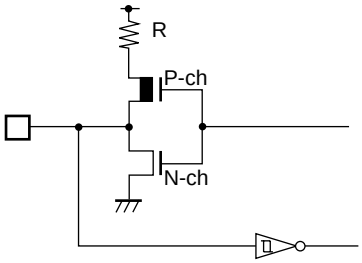
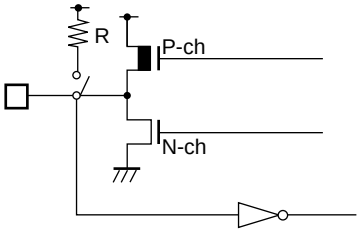
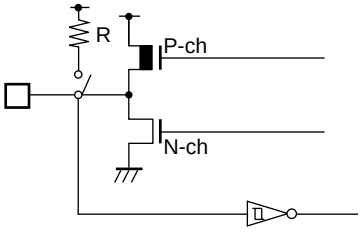
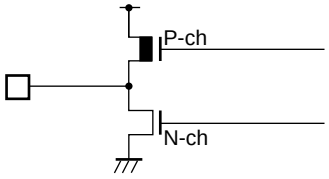
Pin no.			Pin name	Circuit type	Function
SH-DIP*1, MDIP*2	QFP1*3 MQFP*4	SQFP*5 QFP2*6			
22 to 25	15 to 18	14 to 17	P60/INT0 to P63/INT3	I	General-purpose input-only ports Also serve as external interrupt input. This port is a hysteresis input type.
26	19	18	P64	I	General-purpose input-only ports This port is a hysteresis input type.
19, 64	12, 57	11, 56	V_{CC}	—	Power supply pin
21, 32, 57	14, 25, 50	13, 24, 49	V_{SS}	—	Power supply (GND) pin
20	13	12	N.C.	—	Internally connected pin Be sure to leave it open.

*1: DIP-64P-M01, DIP-64C-A06
*2: MDP-64C-P02
*3: FPT-64P-M06
*4: MQP-64C-P01
*5: FPT-64P-M03
*6: FPT64P-M09

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• At oscillation feedback resistor of approximately 1 MΩ/5.0 V
B		
C		• At oscillation feedback resistor of approximately 50 kΩ/5.0 V • CMOS hysteresis input
D		• CMOS output • CMOS input • Pull-up resistor optional (except P22 and P23)
E		• CMOS output • Hysteresis input • Pull-up resistor optional
F		• CMOS output

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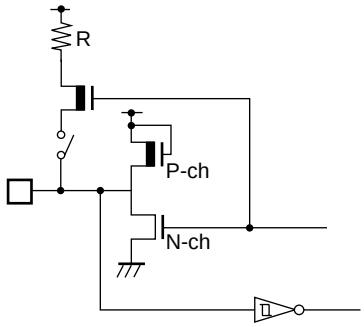
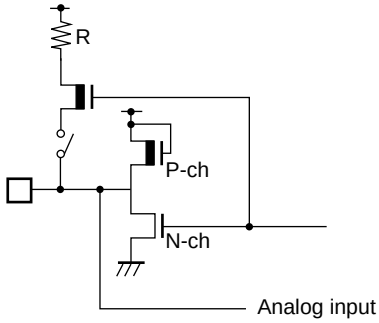
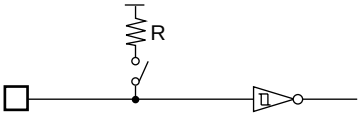
Type	Circuit	Remarks
G		• N-ch open-drain output • Hysteresis input • Pull-up resistor optional
H		• N-ch open-drain output • Pull-up resistor optional
I		• Hysteresis input • Pull-up resistor optional

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

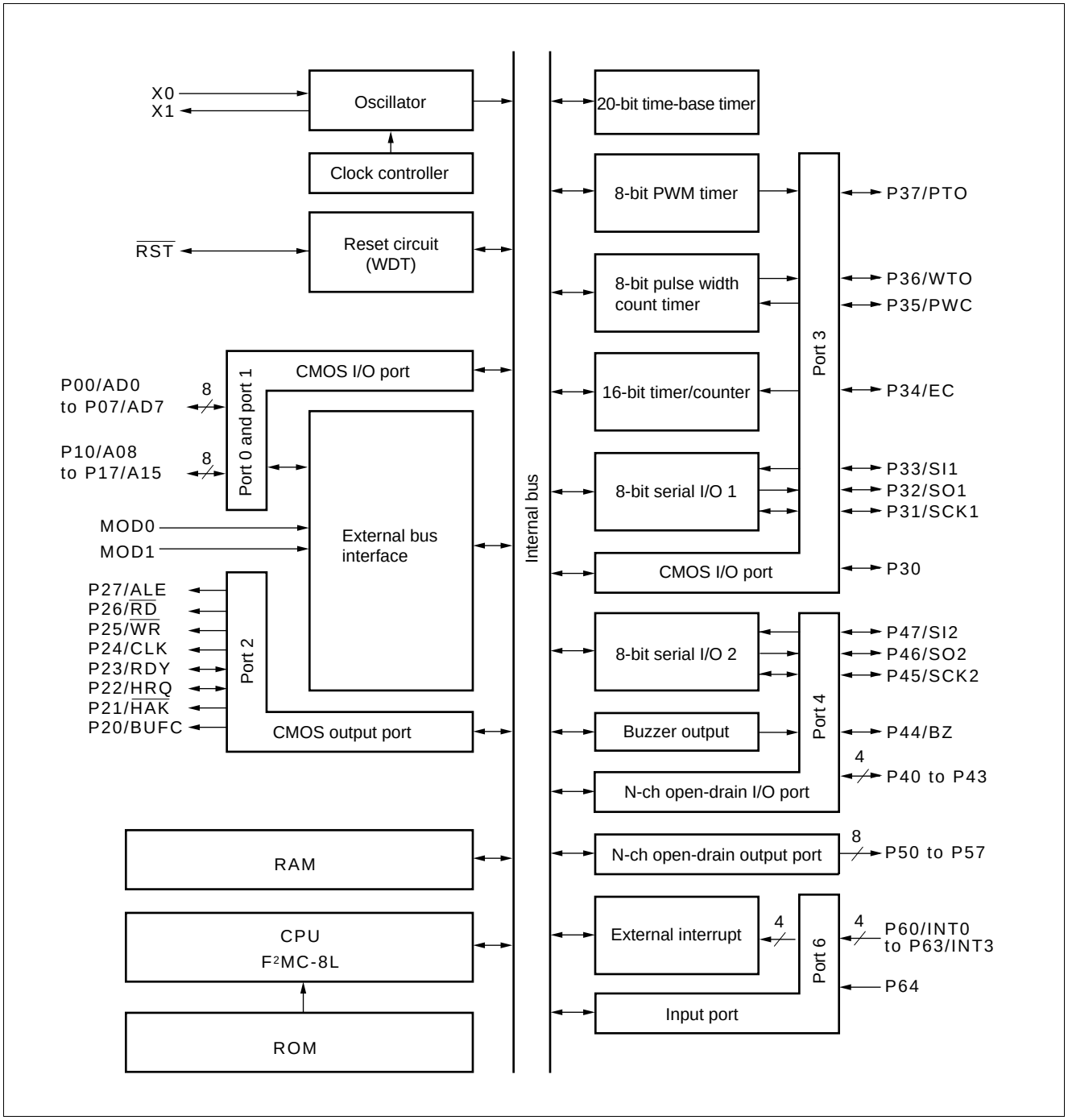
5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

■ BLOCK DIAGRAM

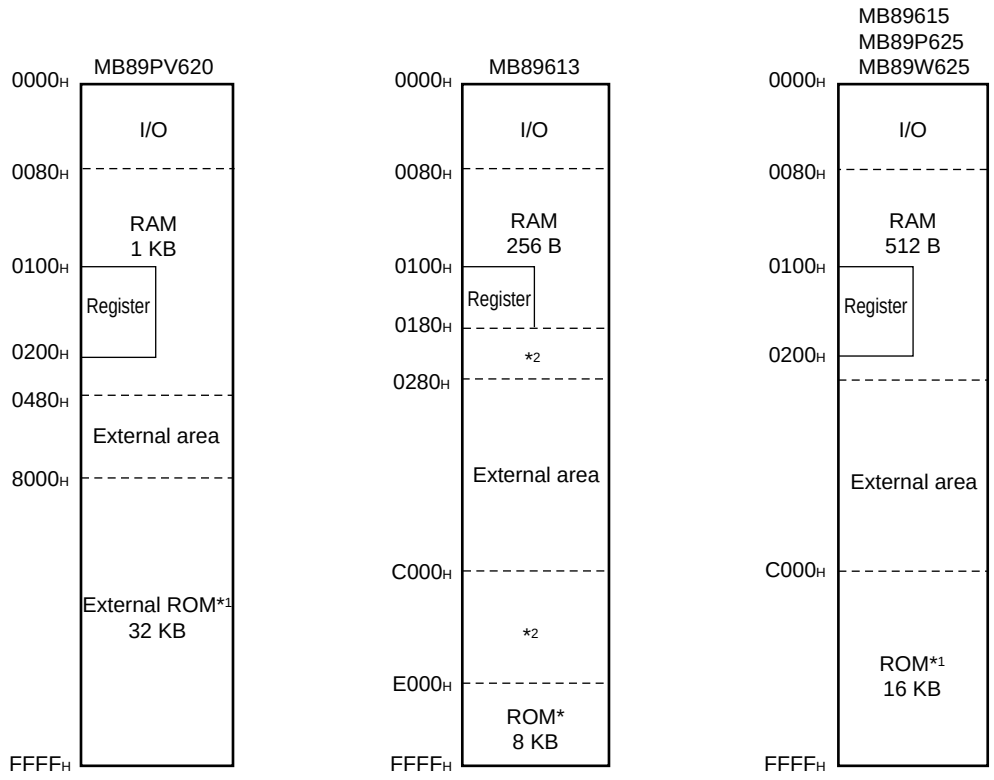


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89610 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89610 series is structured as illustrated below.

Memory Space

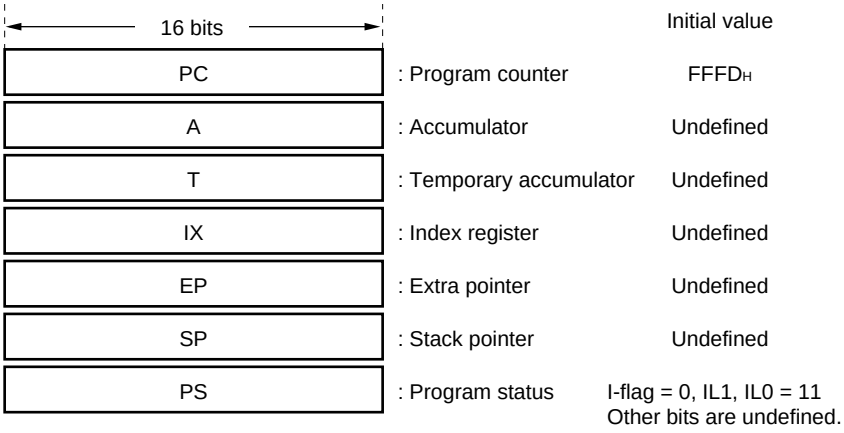


*1: The ROM area is an external area depending on the mode.
*2: Access to this area is prohibited in external bus mode.

2. Registers

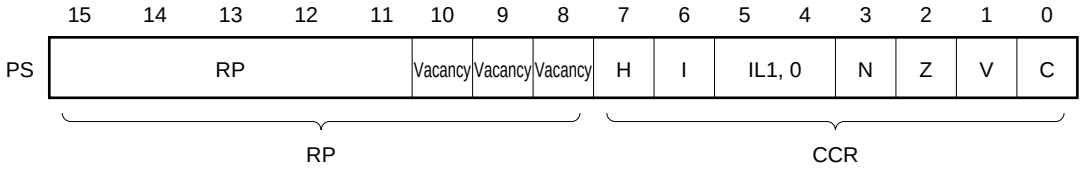
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



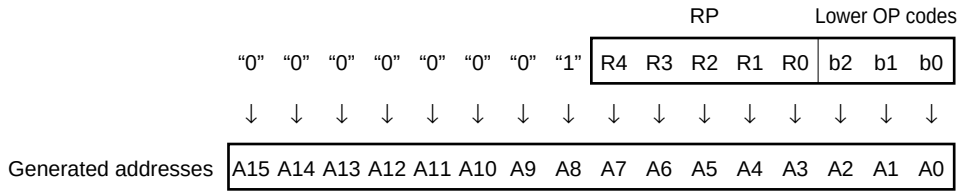
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		↕
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

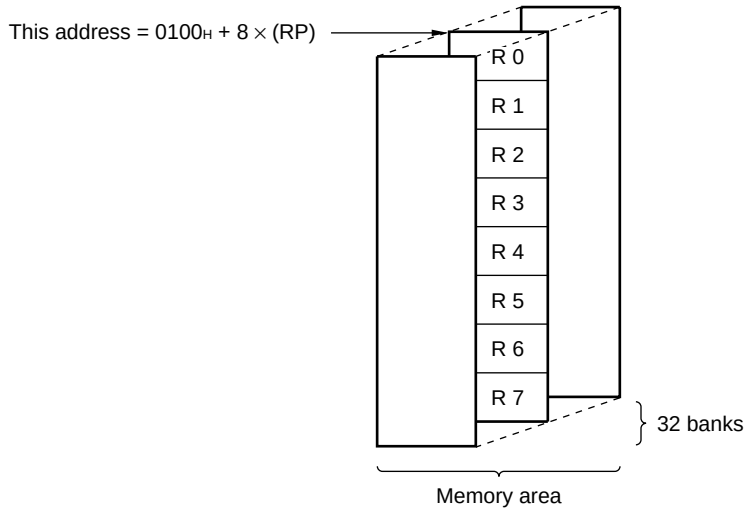
The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89610. In the MB89613, there are 16 banks in internal RAM. The remaining 16 banks can be extended externally by allocating an external RAM to addresses 0180_H to $01FF_H$ using an external circuit. The bank currently being in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size. Up to a total of 32 banks can be used on other than the MB89615.

Register Bank Configuration



■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H	(R/W)	PDR1	Port 1 data register
03H	(W)	DDR1	Port 1 data direction register
04H	(R/W)	PDR2	Port 2 data register
05H	(R/W)	BCTR	External bus control register
06H			Vacancy
07H			Vacancy
08H	(R/W)	STBC	Standby control register
09H	(R/W)	WDTC	Watchdog timer control register
0AH	(R/W)	TBTC	Time-base timer control register
0BH			Vacancy
0CH	(R/W)	PDR3	Port 3 data register
0DH	(W)	DDR3	Port 3 data direction register
0EH	(R/W)	PDR4	Port 4 data register
0FH	(R/W)	BZCR	Buzzer register
10H	(R/W)	PDR5	Port 5 data register
11H	(R)	PDR6	Port 6 data register
12H	(R/W)	CNTR	PWM control register
13H	(W)	COMR	PWM compare register
14H	(R/W)	PCR1	PWC pulse width control register 1
15H	(R/W)	PCR2	PWC pulse width control register 2
16H	(R/W)	RLBR	PWM reload buffer register
17H			Vacancy
18H	(R/W)	TMCR	16-bit timer control register
19H	(R/W)	TCHR	16-bit timer count resister (H)
1AH	(R/W)	TCLR	16-bit timer count register (L)
1BH			Vacancy
1CH	(R/W)	SMR1	Serial I/O 1 mode register
1DH	(R/W)	SDR1	Serial I/O 1 data register
1EH	(R/W)	SMR2	Serial I/O 2 mode register
1FH	(R/W)	SDR2	Serial I/O 2 data register
20H to 23H			Vacancy
21H	(R/W)	EIC1	External interrupt control register 1
25H	(R/W)	EIC2	External interrupt control register 2
26H to 7BH			Vacancy
7CH	(W)	ILR1	Interrupt level setting register 1
7DH	(W)	ILR2	Interrupt level setting register 2
7EH	(W)	ILR3	Interrupt level setting register 3
7FH			Vacancy

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P40 to P47*
	V_{I2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P40 to P47
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P40 to P47*
	V_{O2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P40 to P47
“L” level maximum output current	I_{OL}	—	20	mA	
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	40	mA	Average value (operating current × operating rate)
“H” level maximum output current	I_{OH}	—	–20	mA	
“H” level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
“H” level total maximum output current	ΣI_{OH}	—	–50	mA	
“H” level total average output current	ΣI_{OHAV}	—	–20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

* : V_I and V_O must not exceed V_{CC} + 0.3 V.

Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	2.2*	6.0*	V	Normal operation assurance range* MB89613R/615R
		1.5	6.0	V	Retains the RAM state in stop mode
Operating temperature	T_A	–40	+85	°C	

* : These values vary with the operating frequency. See Figure 1.

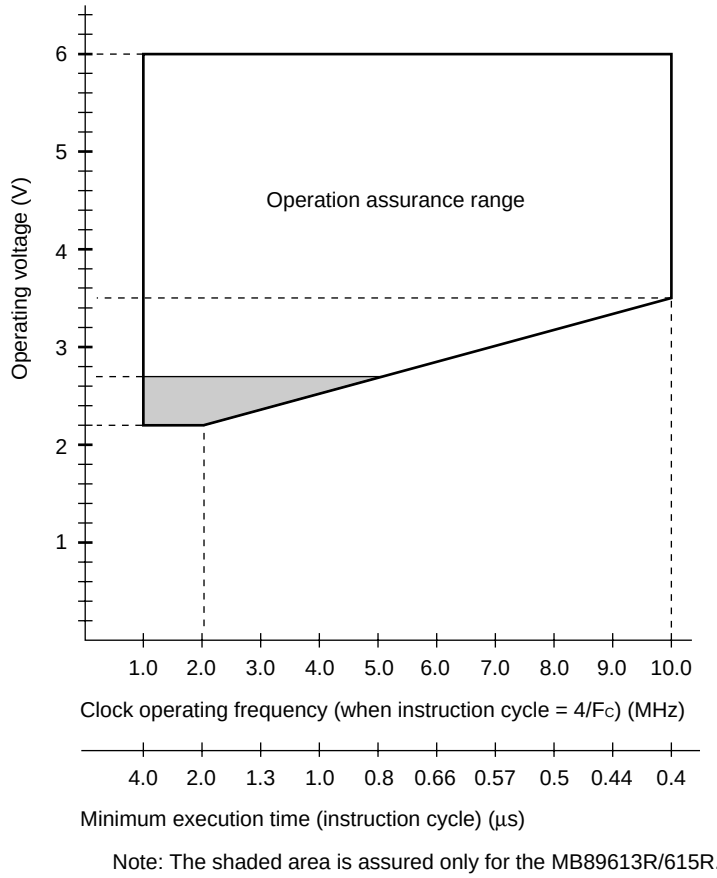


Figure 1 Operating Voltage vs. Clock Operating Frequency

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of 4/F_C.

3. DC Characteristics

(V_{CC} = +5.0 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P22, P23	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, P30 to P37, P60 to P64	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IH2}	P40 to P47	—	0.8 V_{CC}	—	V_{SS} + 6.0	V	
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P22 to P23	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, MOD0, MOD1, P30 to P37, P40 to P47, P60 to P64	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P50 to P57	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
	V_{D2}	P40 to P47	—	V_{SS} – 0.3	—	V_{SS} + 6.0	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37	I_{OH} = –2.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57	I_{OL} = +4.0 mA	—	—	0.4	V	
	V_{OL2}	$\overline{RST}$		—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P60 to P64, MOD0, MOD1	0.0 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P64, $\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	

(Continued)

(Continued)

(V_{CC} = +5.0 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply voltage*1	I_{CC}	V_{CC}	F_C = 10 MHz t_{inst}*2 = 0.4 µs Normal operation mode	—	9	15	mA	MB89613R/615R
	I_{CCS}		F_C = 10 MHz t_{inst}*2 = 0.4 µs Sleep mode	—	3	4	mA	
	I_{CCH}		T_A = +25°C Stop mode	—	—	1	µA	
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	10	—	pF	

*1: In the case of the MB89PV620, the current consumed by the connected EPROM and ICE is not included. The power supply current is measured at the external clock.

*2: For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

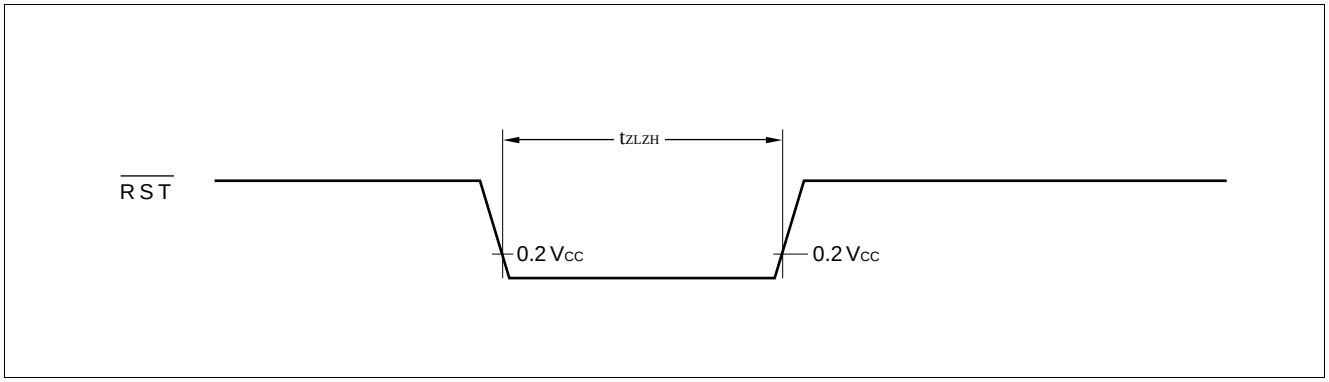
3. AC Characteristics

(1) Reset Timing

(V_{CC} = +5.0 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	16 t_{XCYL}*	—	ns	

* : t_{XCYL} is the oscillation cycle (1/F_C) to input to the X0 pin.

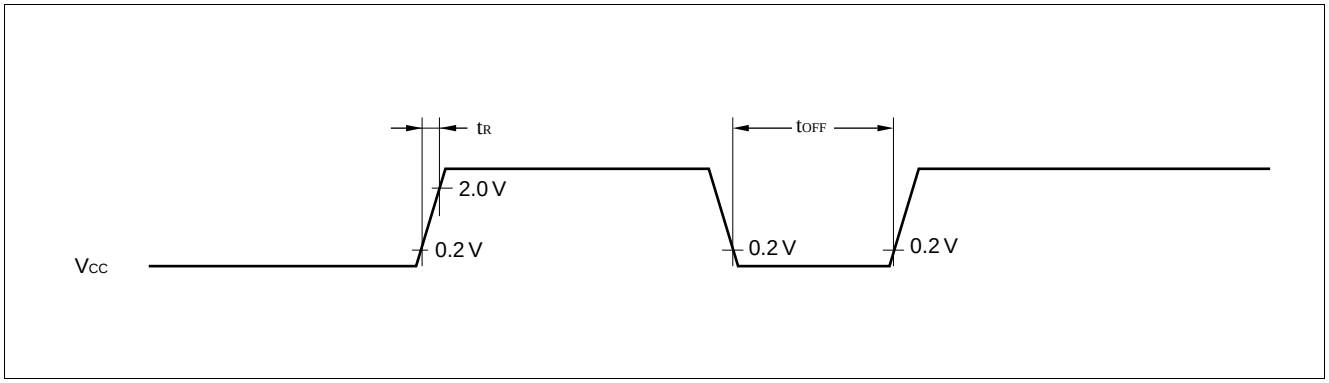


(2) Power-on Reset

(V_{CC} = +5.0 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operation

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

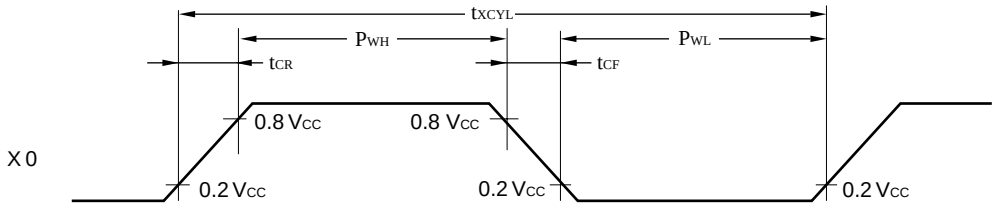


(3) Clock Timing

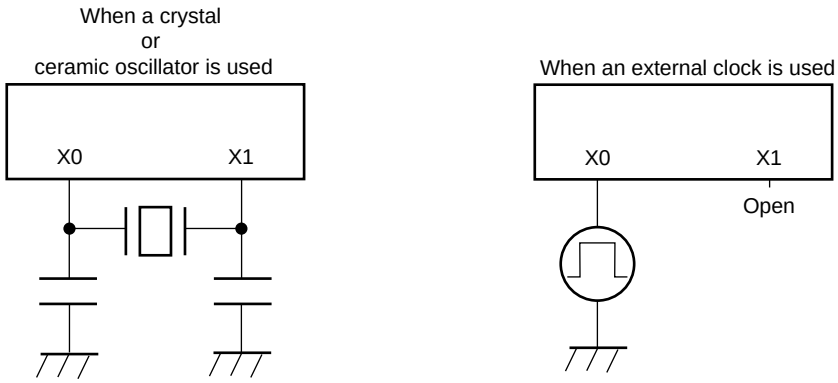
(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock frequency	F_C	X0, X1	—	1	10	MHz	
Clock cycle time	t_{XCYL}	X0, X1	—	100	1000	ns	
Input clock pulse width	P_{WH} P_{WL}	X0	—	20	—	ns	External clock
Input clock rising/falling time	t_{CR} t_{CF}	X0	—	—	10	ns	External clock

X0 and X1 Timing and Conditions



Clock Conditions



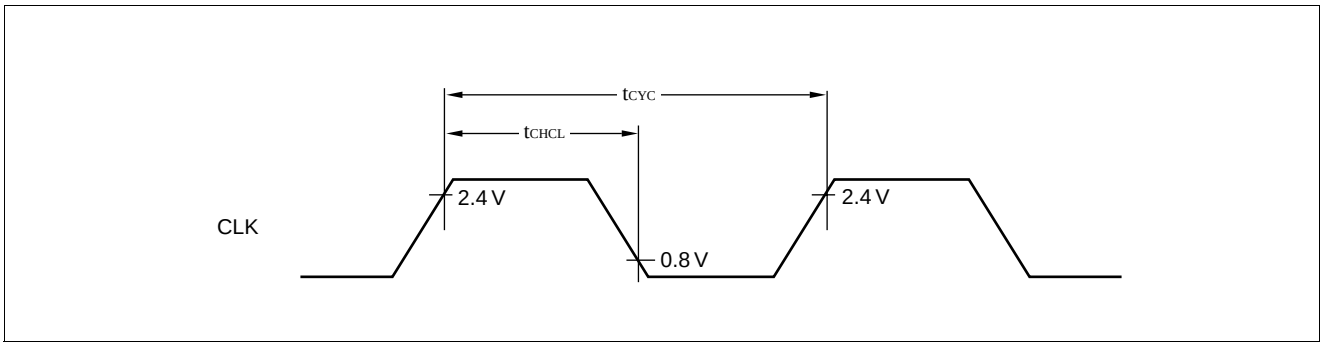
(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_C$	µs	t_{inst} = 0.4 µs when operating at F_C = 10 MHz

(5) Clock Output Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Values		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	—	200	—	ns	$t_{XCYL} \times 2$ at 10 MHz oscillation
CLK ↑ → CLK ↓	t_{CHCL}			30	100	ns	Approx. $t_{CYC}/2$ at 10 MHz oscillation

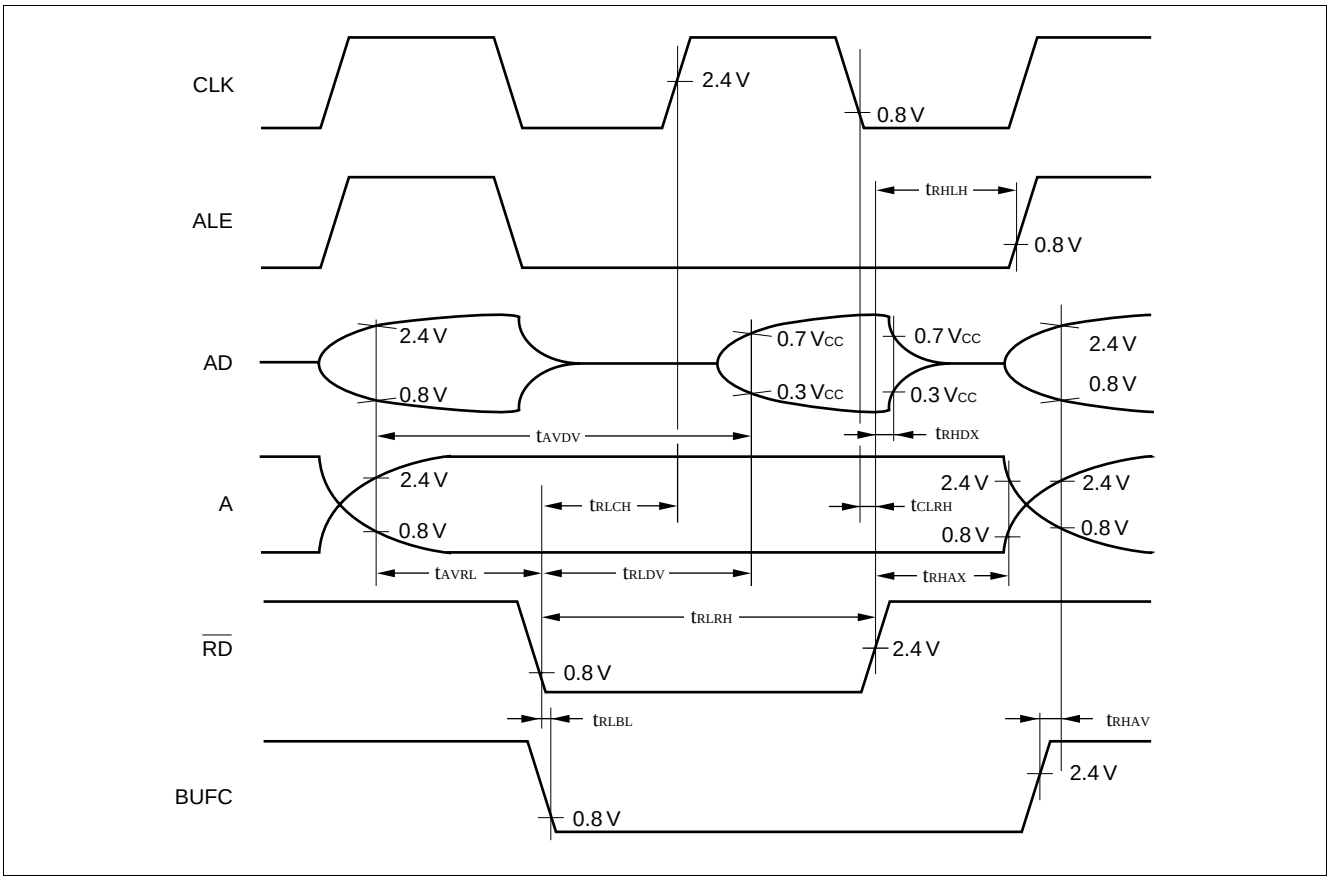


(6) Bus Read Timing

(V_{CC} = +5.0 V±10%, F_C = 10 MHz, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	$\overline{RD}$, A15 to 08 AD7 to 0	—	1/4 t_{inst}* – 64 ns	—	µs	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		1/2 t_{inst}* – 20 ns	—	µs	
Valid address → read data time	t_{AVDV}	AD7 to 0, A15 to 08		—	1/2 t_{inst}*	µs	No wait
$\overline{RD}$ ↓ → read data time	t_{RLDV}	$\overline{RD}$, AD7 to 0		—	1/2 t_{inst}* – 80 ns	µs	No wait
$\overline{RD}$ ↑ → data hold time	t_{RHDX}	AD7 to 0, $\overline{RD}$		0	—	ns	
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		1/4 t_{inst}* – 40 ns	—	µs	
$\overline{RD}$ ↑ → address invalid time	t_{RHAX}	$\overline{RD}$, A15 to 08		1/4 t_{inst}* – 40 ns	—	µs	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		1/4 t_{inst}* – 40 ns	—	µs	
CLK ↓ → $\overline{RD}$ ↑ time	t_{CLRH}			0	—	ns	
$\overline{RD}$ ↓ → BUFC ↓ time	t_{RLBL}	$\overline{RD}$, BUFC		–5	—	µs	
BUFC ↑ → valid address time	t_{BHAV}	A15 to 08, AD7 to 0, BUFC		5	—	µs	

* : For information on t_{inst}, see “(4), Instruction Cycle.”



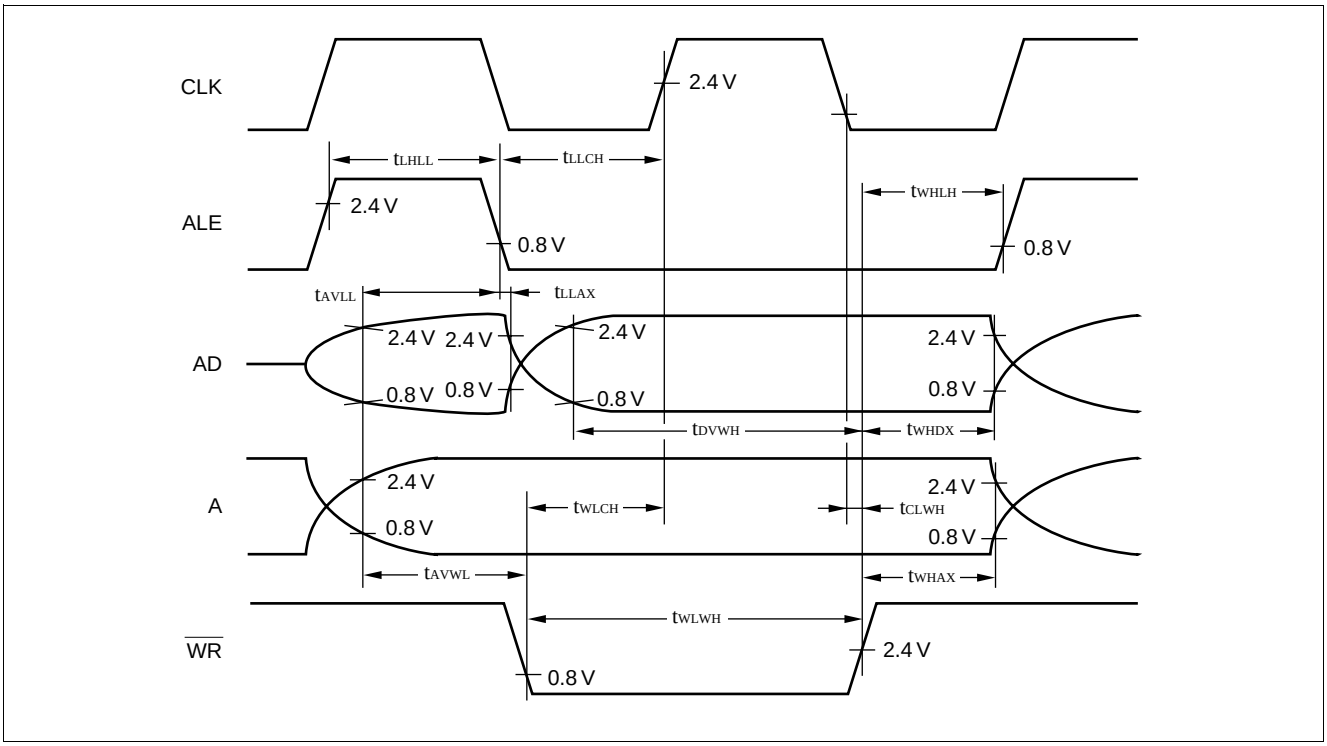
(7) Bus Write Timing

(V_{CC} = +5.0 V±10%, F_C = 10 MHz, V_{SS} = 0.0 V, T_A = –40°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid address → ALE ↓ time	t_{AVLL}	AD7 to 0, ALE, A15 to 08	—	1/4 t_{inst}* – 64 ns*2	—	µs	
ALE ↓ time → address invalid time	t_{LLAX}			5*2	—	ns	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	$\overline{WR}$, ALE		1/4 t_{inst}* – 60 ns*2	—	µs	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		1/2 t_{inst}* – 20 ns*2	—	µs	
Write data → $\overline{WR}$ ↑ time	t_{DVWH}	AD7 to 0, $\overline{WR}$		1/2 t_{inst}* – 60 ns*2	—	µs	
$\overline{WR}$ ↑ → address invalid time	t_{WHAX}	$\overline{WR}$, A15 to 08		1/4 t_{inst}* – 40 ns*2	—	µs	
$\overline{WR}$ ↑ → data hold time	t_{WHDX}	AD7 to 0, $\overline{WR}$		1/4 t_{inst}* – 40 ns*2	—	µs	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		1/4 t_{inst}* – 40 ns*2	—	µs	
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		1/4 t_{inst}* – 40 ns*2	—	µs	
CLK ↓ → $\overline{WR}$ ↑ time	t_{CLWH}	$\overline{WR}$, CLK		0	—	ns	
ALE pulse width	t_{LHLL}	ALE		1/4 t_{inst}* – 35 ns*2	—	µs	
ALE ↓ → CLK ↑ time	t_{LLCH}	ALE, CLK		1/4 t_{inst}* – 30 ns*2	—	µs	

*1: For information on t_{inst}, see “(4) Instruction Cycle.”

*2: These characteristics are also applicable to the bus read timing.

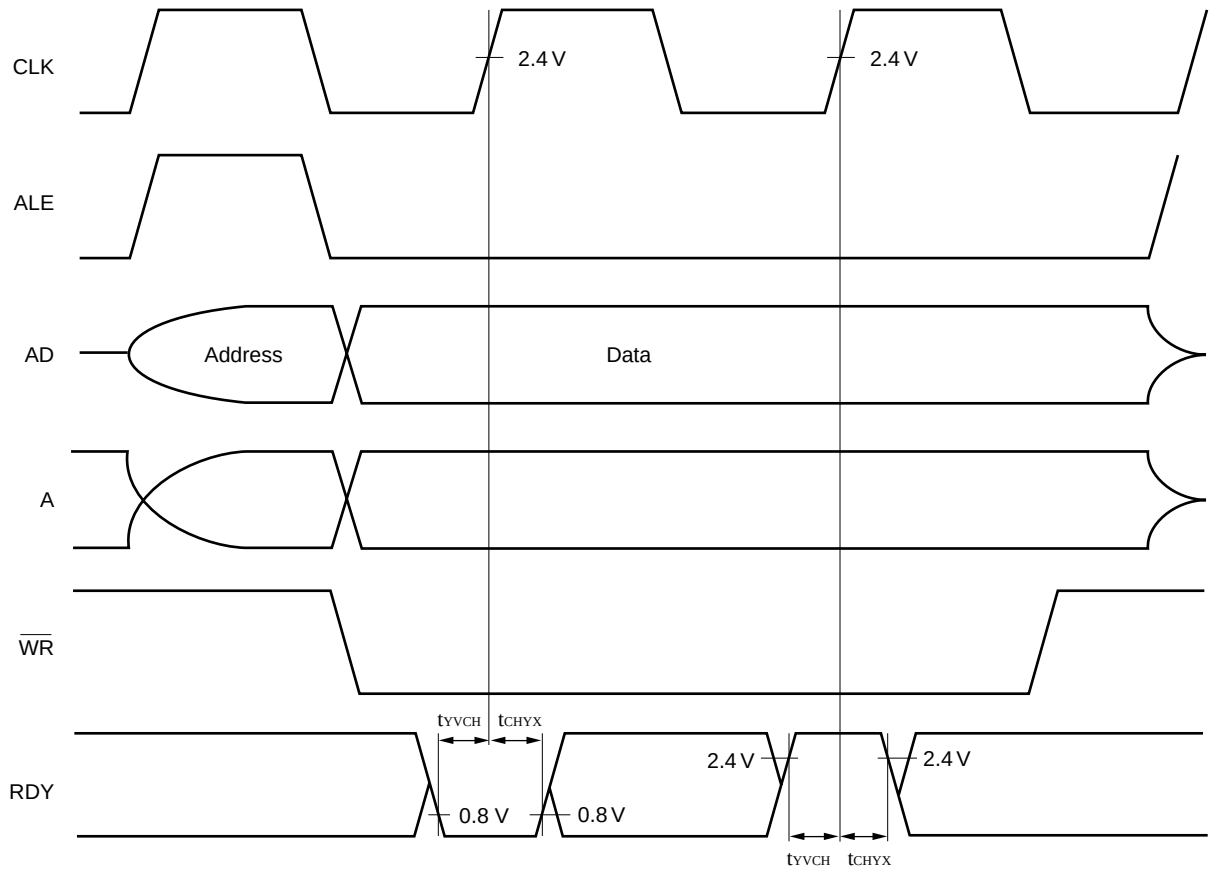


(8) Ready Input Timing

(V_{CC} = +5.0 V±10%, F_C = 10 MHz, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Values		Unit	Remarks
				Min.	Max.		
RDY valid → CLK ↑ time	t_{YVCH}	RDY, CLK	—	60	—	ns	*
CLK ↑ → RDY invalid time	t_{CHYX}			0	—	ns	*

* : These characteristics are also applicable to the read cycle.



Note: The bus cycle is also extended in the read cycle in the same manner.

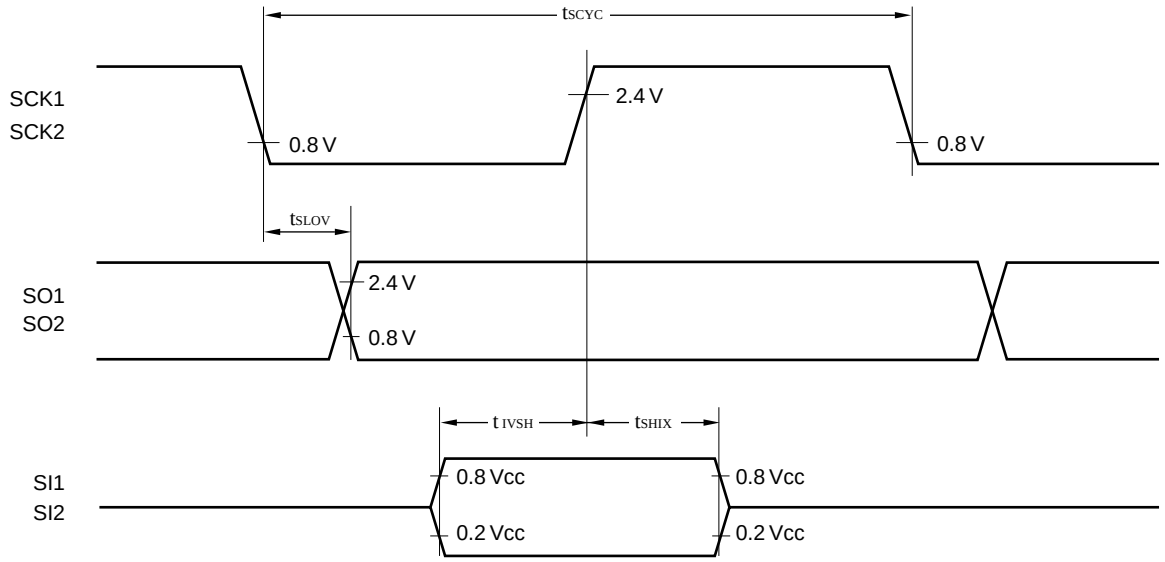
(9) Serial I/O Timing

(V_{CC} = +5.0 V±10%, F_C = 10 MHz, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

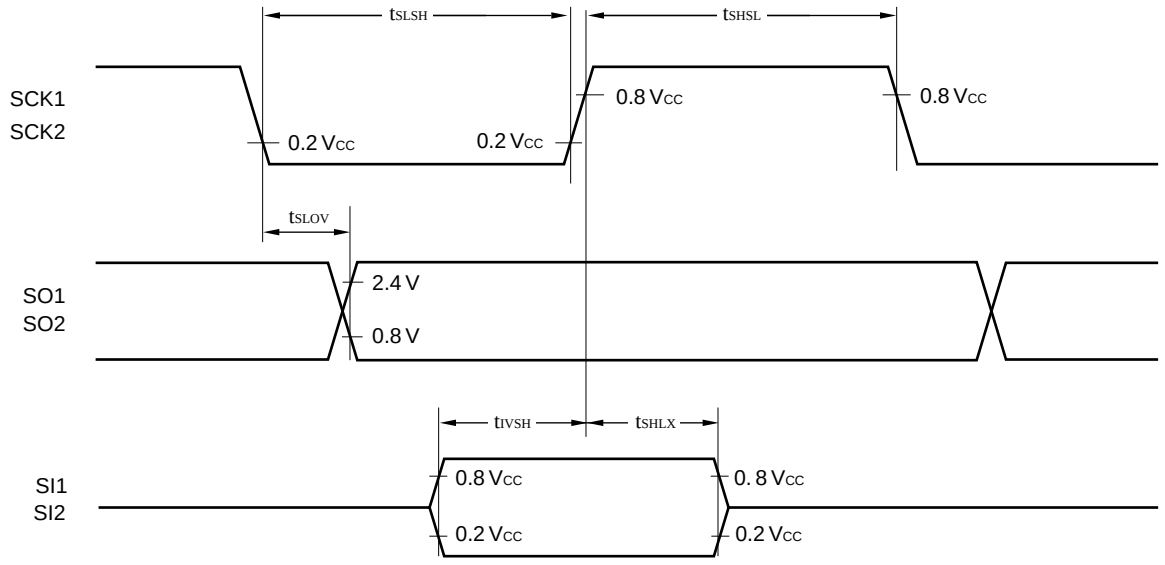
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK1, SCK2	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time SCK2 ↓ → SO2 time	t_{SLOV}	SCK1, SO1 SCK2, SO2		–200	200	ns	
SCK1 ↑ → valid SI1 hold time SCK2 ↑ → valid SI2 hold time	t_{SHIX}	SCK1, SI1 SCK2, SI2		1/2 t_{inst}*	—	µs	
Valid SI1 → SCK1 ↑ Valid SI2 → SCK2 ↑	t_{IVSH}	SI1, SCK1 SI2, SCK2		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK1, SCK2	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}*	—	µs	
SCK ↓ → SO1 time SCK2 ↓ → SO2 time	t_{SLOV}	SCK1, SO1 SCK2, SO2		0	200	ns	
SCK1 ↑ → valid SI1 hold time SCK2 ↑ → valid SI2 hold time	t_{SHIX}	SCK1, SI1 SCK2, SI2		1/2 t_{inst}*	—	µs	
Valid SI1 → SCK1 ↑ Valid SI2 → SCK2 ↑	t_{IVSH}	SI1, SCK1 SI2, SCK2		1/2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

Internal Shift Clock Mode



External Shift Clock Mode

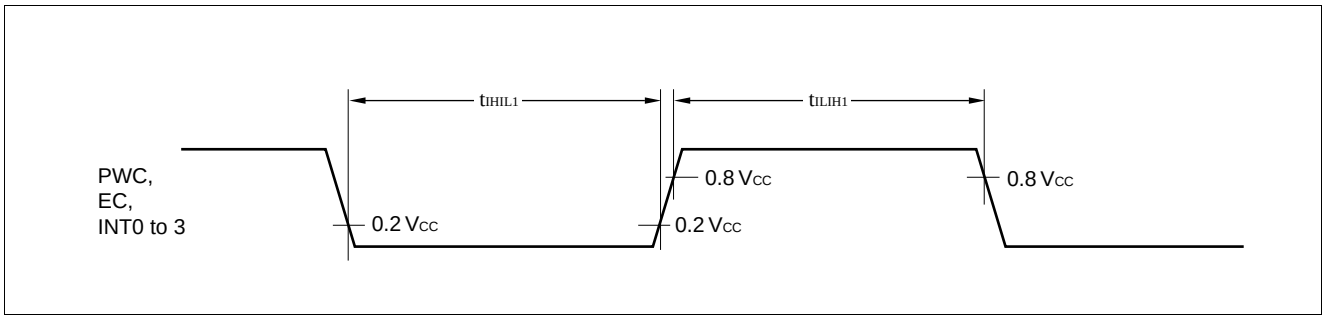


(10) Peripheral Input Timing

(V_{CC} = +5.0 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

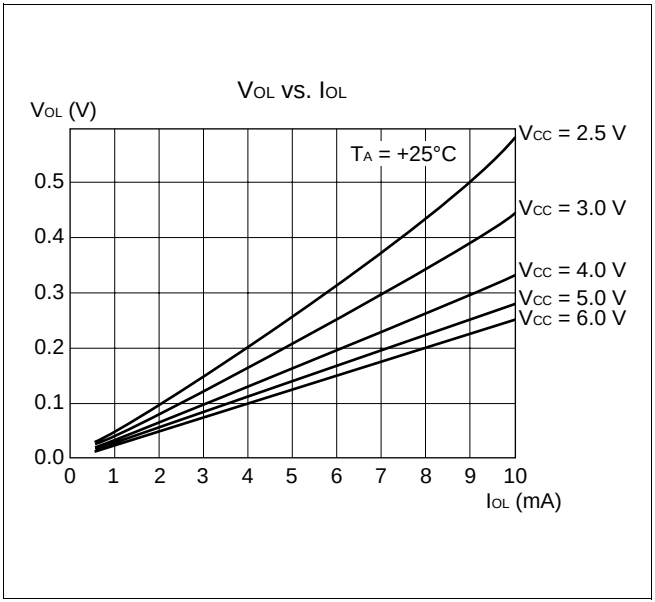
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Peripheral input “H” level pulse width 1	t_{ILIH1}	PWC, EC, INT0 to INT3	—	2 t_{inst}*	—	µs	
Peripheral input “L” level pulse width 2	t_{IHIL1}			2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

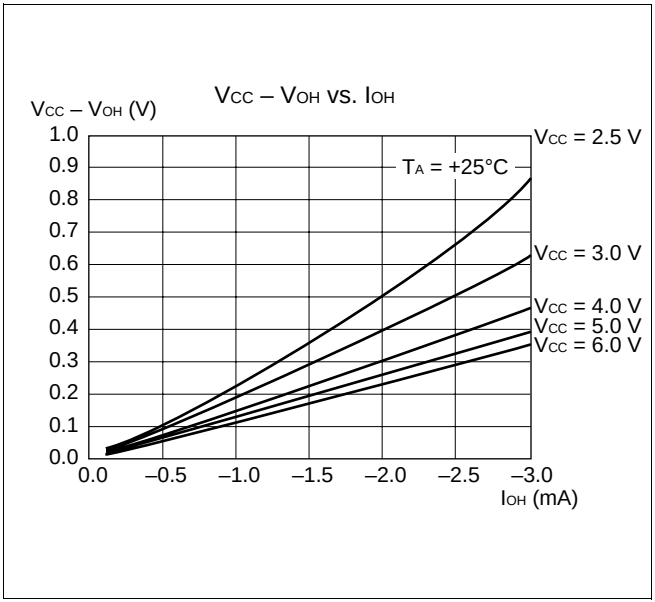


■ EXAMPLE CHARACTERISTICS

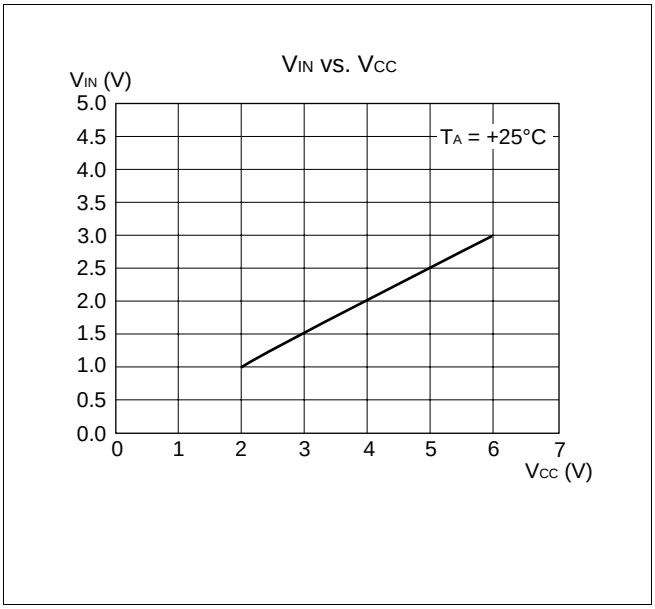
(1) “L” Level Output Voltage



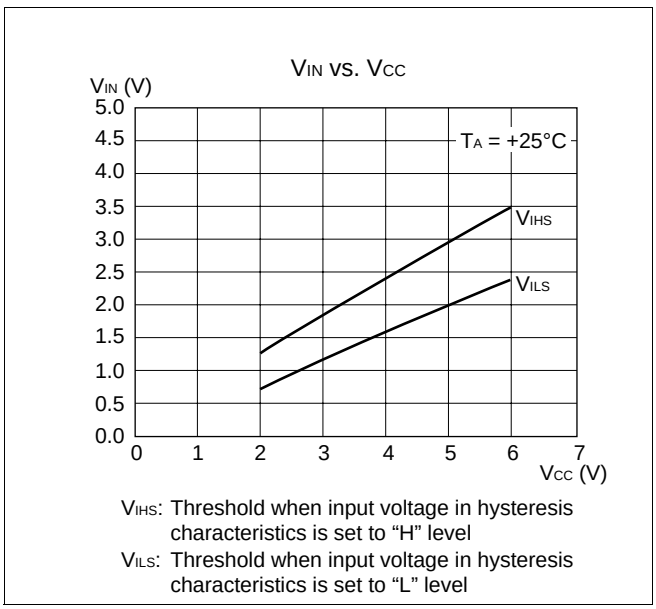
(2) “H” Level Output Voltage



(3) “H” Level Input Voltage/“L” Level Input Voltage (CMOS Input)



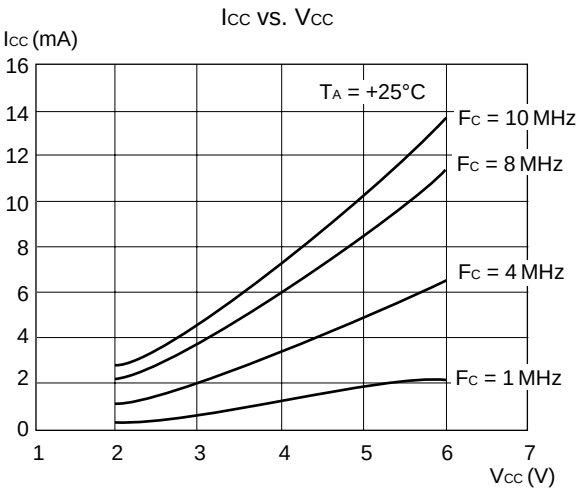
(4) “H” level Input Voltage/“L” Level Input Voltage (Hysteresis Input)

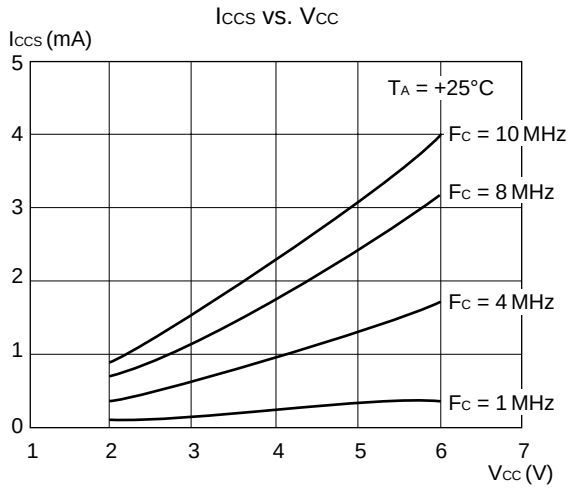


VIHS: Threshold when input voltage in hysteresis characteristics is set to “H” level

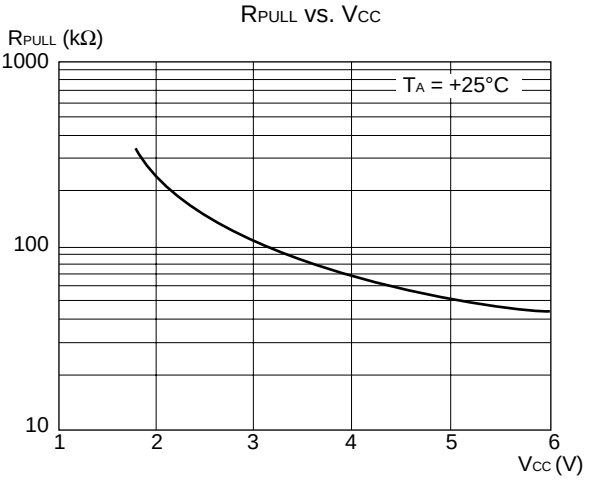
VILS: Threshold when input voltage in hysteresis characteristics is set to “L” level

(5) Power Supply Current (External Clock)





(6) Pull-up Resistance



■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A ┐	–	–	–	+ + – +	03
ROLC A	2	1	┌ C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

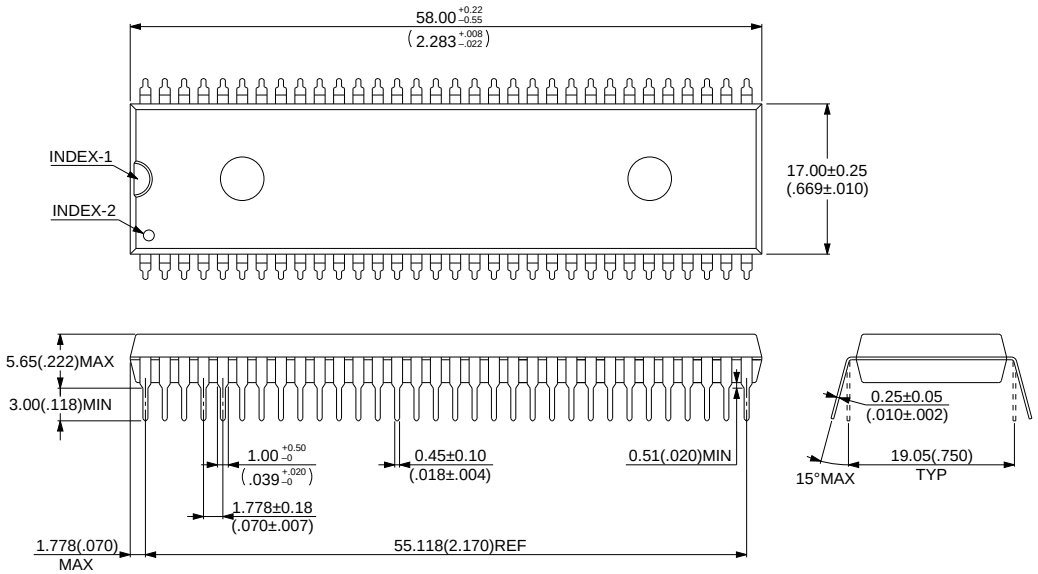
No.	Part number	MB89613R MB89615R	MB89P625 MB89W625	MB89PV620
	Specifying procedure	Specify when ordering masking	Set with EPROM programmer	Setting not possible
1	Pull-up resistors P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P64	Selectable per pin	Can be set per pin. (P40 to P47 are available only for without pull-up resistor.)	Fixed to without pull-up resistor
2	Power-on reset selection With power-on reset Without power-on reset	Selectable	Setting possible	Fixed to with power-on reset
3	Oscillation stabilization time Selection Crystal oscillator ($2^{18}/F_C$(s)) Ceramic oscillator ($2^{14}/F_C$(s))	Selectable	Setting possible	Crystal oscillator ($2^{18}/F_C$(s))
4	Reset pin output With reset output Without reset output	Selectable	Setting possible	Fixed to with reset output

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89613RP-SH MB89615RP-SH	64-pin Plastic SH-DIP (DIP-64P-M01)	
MB89613RPF MB89615RPF	64-pin Plastic QFP (FPT-64P-M06)	Lead pitch: 1.0 mm
MB89613RPFM MB89615RPFM	64-pin Plastic QFP (FPT-64P-M09)	Lead pitch: 0.65 mm
MB89613RPFV MB89615RPFV	64-pin Plastic SQFP (FPT-64P-M03)	Lead pitch: 0.5 mm

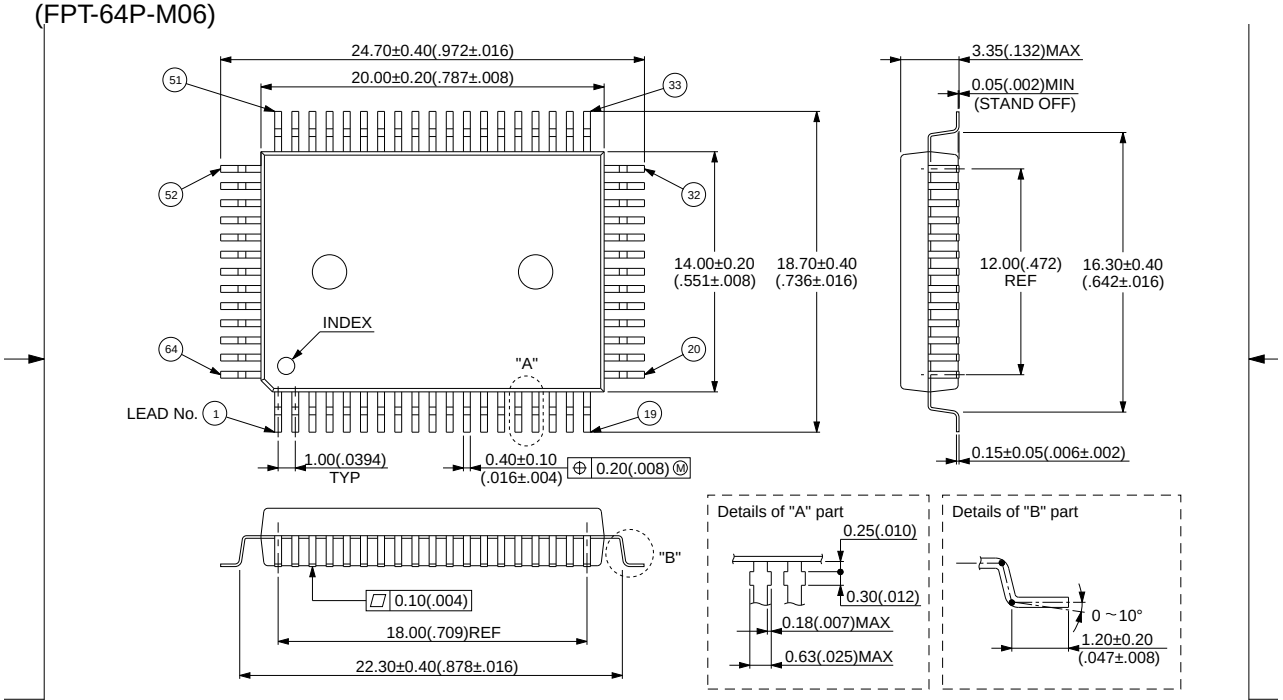
■ PACKAGE DIMENSIONS

64-pin Plastic SH-DIP
(DIP-64P-M01)



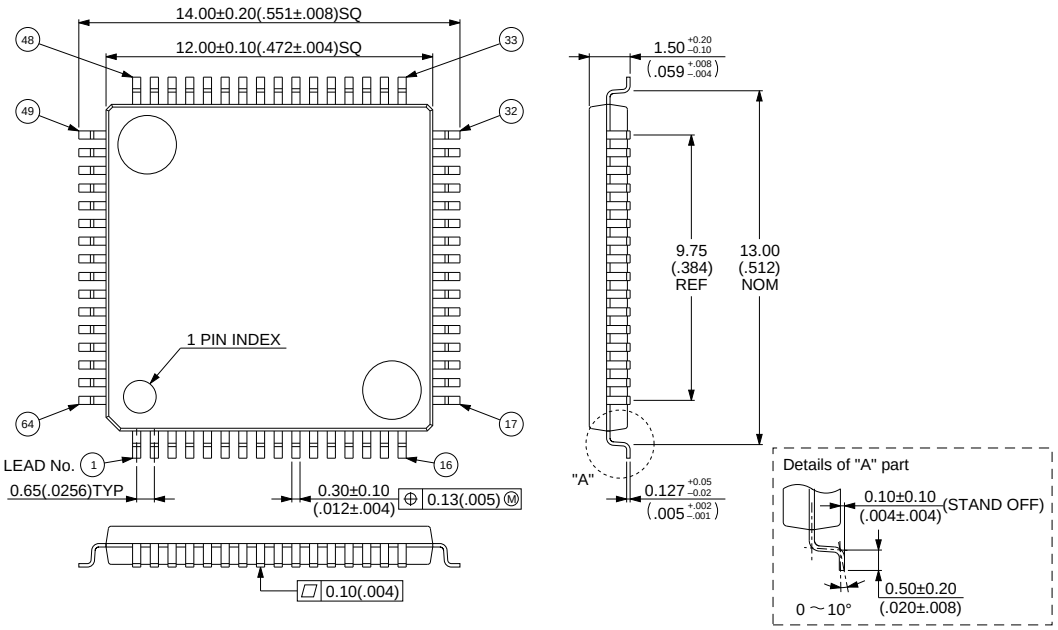
Dimensions in mm (inches)

64-pin Plastic QFP
(FPT-64P-M06)



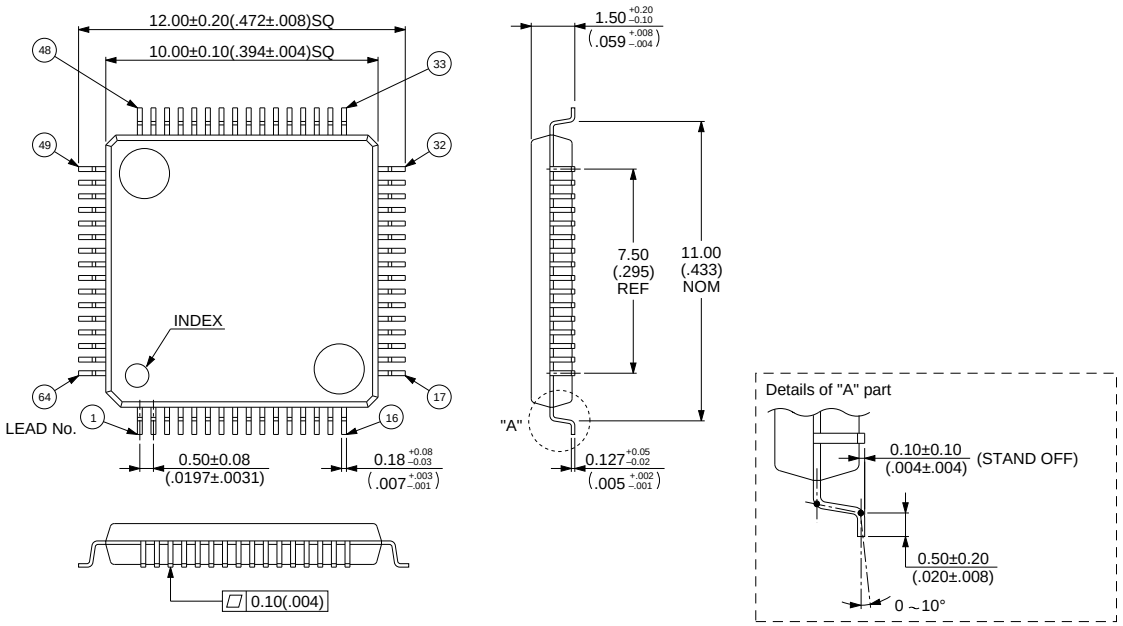
Dimensions in mm (inches)

64-pin Plastic QFP
(FPT-64P-M09)



Dimensions in mm (inches)

64-pin Plastic SQFP
(FPT-64P-M03)



Dimensions in mm (inches)

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