Application Note

USING THE CS5180 WITH MULTIPLEXED INPUTS

The CS5180 is a high-speed Delta-Sigma analog-to-digital converter capable of a 400 ksamples/second output word rate and incorporating a 4,265 tap digital filter. If signals are to be multiplexed into the A/D converter, then the digital filter will require at least 74 output words to settle to its rated accuracy. This normally requires that a microcontroller would be required to either count and discard the invalid output words or to use a programmable timer to provide the required time delay before taking the valid reading. The CS5180 has been designed with a unique feature, a SYNC input that can simplify the task of multiplexing by releiving the microcontroller of the task of counting words or time delays. This application note describes two techniques that can be used with the CS5180 to multiplex signals at up to a 5.3 kHz rate.

Figure 1 shows a typical data acquisition system that might be employed to multiplex 4 differential analog signals into one CS5180 converter. A microcontroller with several port pins and a serial port is used to sequence the 4-channel multiplexer and to read the serial data output of the CS5180. Port lines 2 and 3 are used to control the multiplexer channel select inputs, A and B, while port 1 is used to control the SYNC input to the CS5180. Serial data from the CS5180, SDO, is shifted into the microcontroller's serial port on the rising edge of the clock, SCLK, and is framed by the Frame Sync Output signal, FSO. FSO goes low at the beginning of a new word from the A/D converter and can be used to enable the input to the shift register in the microcontroller or in hardware. In normal operation, the FSO signal will go low at the start of each new output word from the CS5180 and return high after the least-significant-bit is clocked in.

When multiplexing data into the CS5180 converter, care must be taken that enough time is allowed for the digital filter to settle out to the rated accuracy of the converter after switching channels on the

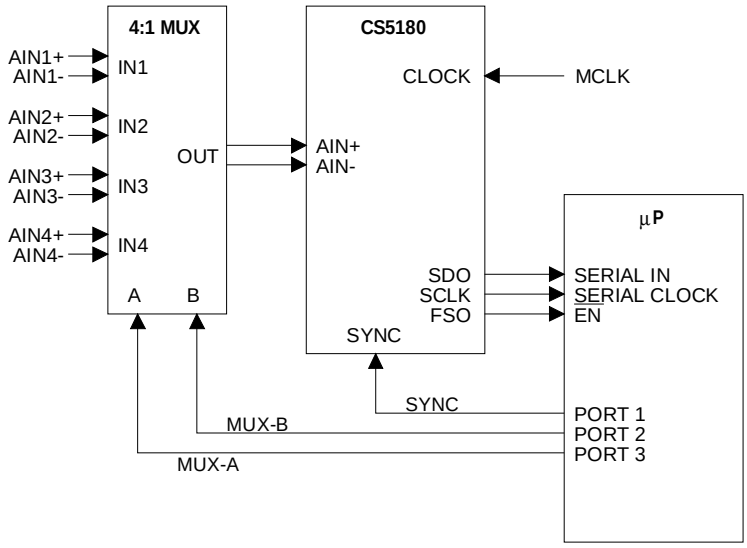

Figure 1. CS5180 Used in a Multiplexed Data Acquisition System

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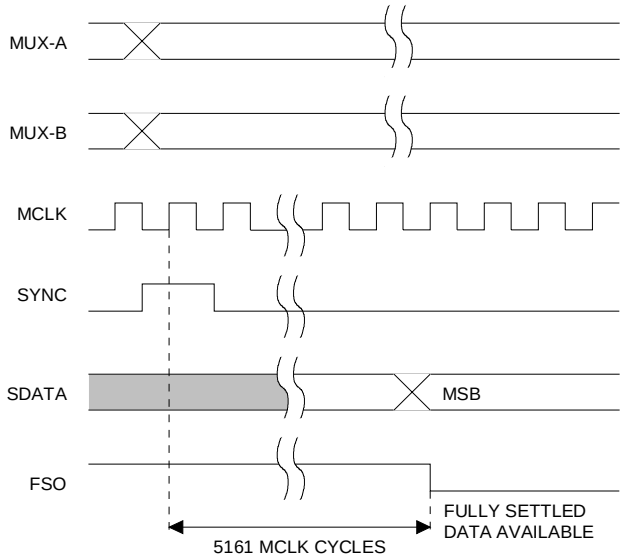
multiplexer, before taking a valid reading. In the case of the CS5180, a maximum of 4,740 clock cycles are required for the filter to settle, which translates into a delay of 185 microseconds with a 25.6 MHz master clock. Adding about 3 more microseconds for the microcontroller to acquire the serial word would bring the total time to read one multiplexed input to about 188 microseconds, or a 5.3 kHz sample rate. This assumes no filtering or active devices between the multiplexer and the converter that would require additional settling time.

If the microcontroller has a spare programmable timer and is running from an accurate oscillator, then in one implementation, after a channel is selected on the multiplexer, the user could program a delay of 185 microseconds into the timer and wait for the timer to count down before taking a valid reading on the serial port. During this time period, the converter will continue to output words that will not be useable, since the digital filter will still be settling out. In this method, the SYNC line is not needed and should be tied to ground or held at a logic low level through the port line.

Figure 2 displays the timing diagrams for a second implementation where no timer or counter is required. If the SYNC line is held high for at least one clock cycle just after switching channels on the multiplexer, the CS5180 will wait 5,161 clock cycles for the digital filter to settle before putting out a fully-settled conversion word. During this time period the FSO signal will remain high. If the FSO signal is used to gate the operation of the serial port of the microcontroller, then no time-keeping is required. Valid data will automatically be clocked into the shift register when FSO goes low. If the microcontroller has external interrupt inputs, the rising edge of FSO could be used to signal the controller that a new word has been acquired. Note that this method of multiplexing the data takes about 205 microseconds at 25.6 MHz to acquire a fully settled signal. Once the filter has settled, then valid measurements will continue to come out at 400 k samples/sec as long as the mux is not switched..

Some care should be taken in using the SYNC line when multiplexing signals. If the SYNC line is pulsed high while the CS5180 is already in the process of outputting a word, it will continue to send the word out, but the data will have been corrupted by the response to the SYNC signal. This word should be disregarded, and in either case, the first valid data word will be available 5,161 MCLK cycles after SYNC is recognized.



With a 25.6 MHz MCLK, a different channel can be read every 205 µs.

Note: If the CS5180 is in the process of outputting a word when the SYNC line is set high, it will continue until the word is finished, but that data word will not contain valid data. In either case, the first valid data will be available 5161 MCLK cycles after sync is recognized.

Figure 2. Timing Diagram for Multiplexing of Inputs Using the SYNC Input

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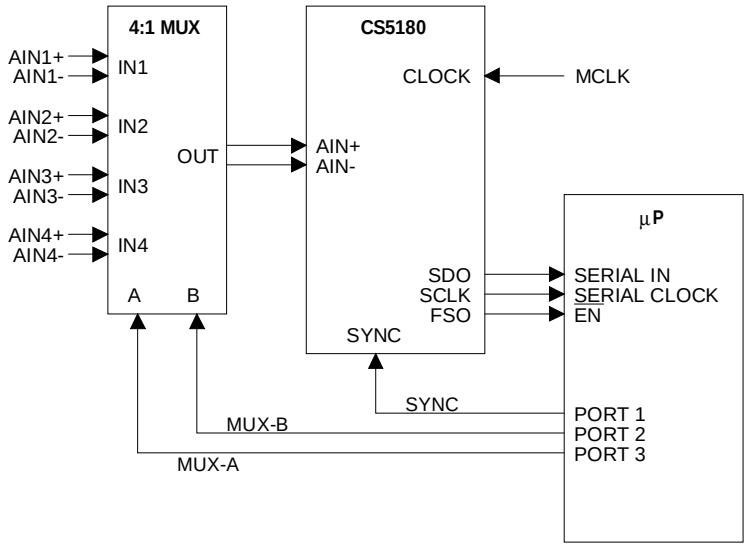

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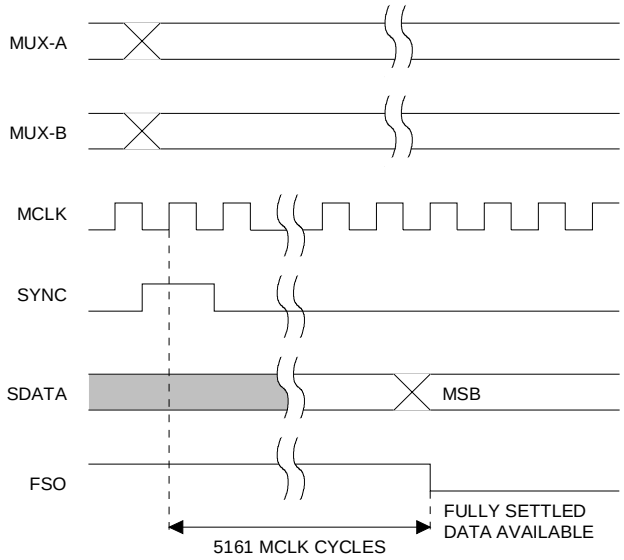

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