❑ MN103E010HRA, MN103E040HYB

Type		MN103E010HRA	MN103E040HYB
Instruction Cache		16 K-byte (4-way, set-associative)	
Data Cashe		16 K-byte (4-way, set-associative)	
SRAM Used by Both Instructions and Data		16 K-byte	
Package		BGA292-P-2727 *Lead-free	FLGA424-C-1717 *Lead-free
Minimum Instruction Execution Time		7.5 ns (at 1.8 V tolerance = ± 5%, 133 MHz)	
Interrupts		• XIRQ × 8 • NMI • Timer × 14 • DMAC × 4 • WDT • A/D • SIO × 6 • I^2C × 2 • IrDA • Softmodem • Realtime clock • Asynchronous bus error	
Timer Counter		8-bit timer × 4 (all down counters) Cascade connection possible (usable as a 16/24/32-bit timer) Timer output possible (Duty = 1:1) Internal clock source or external clock source selectable Selectable as a serial interface clock 16-bit timer × 7 (down counters) Cascade connection possible (usable as a 32-bit timer) Timer output possible (Duty = 1:1) Internal clock source or external clock source selectable Partially selectable as a serial interface clock 16-bit timer × 1 (up counter) Internal clock source or external clock source selectable Input capture function (rising edge, falling edges, or both selectable) PWM generating function (compare/capture register × 2 contained) Watchdog timer × 1	
DMA Contoroller		Number of channels: 4 Transfer unit: 1/2/4/16 byte Maximum number of bytes transferred: 1Mbyte Start factor: External request, interrupt, software Transfer mode: 2-bus cycle transfer Transfer mode: Batch transfer, intermittent transfer Addressing mode: Source/destination each fixed, increment/decrement specification possible Increment/decrement automatically executed according to the transfer unit	
Serial Interface		UART/synchronous (co-used) × 2-ch. UART (with CTS control) × 1-ch.	
I/O Pins	**I/O**	34	• Common use : 33
FPU (floating point unit)		• Data types complying with the IEEE754 standard supported • Round to the nearest mode complying with the IEEE754 standard supported • 32 single-precision floating point operation registers (FS0-FS31) These can also be referenced as 16 double-precision floating point operation registers (FD0-FD30) • Floating point operation exceptions (5 types) and floating point unload instruction exceptions complying with the IEEE754 standard supported	
Memory Management Function		32-entry full-associative TLB loaded (instructions/data separated from each other) Address conversion by paging (page size: 1 K-byte. 4 K-byte, 128 K-byte, 4 M-byte variable)	
On-chip Bus Controller		Concurrent access from three types of master devices to four types of slave devices possible	

System Bus Interface	External memory space allocation to 8 banks possible The external interface can use the built-in memory, RAM, ROM, SDRAM interfaces
Memory Bus Interface	SDRAM directly connected interface contained
Soft Modem Interface	• Interface with an external AFE (analog front end) • Output data parallel-serial conversion, input data serial-parallel conversion • Send/receive FIFO contained (16-bit width, 16 steps) • NCU control via the parallel IO port
Real-time Clock	• Clock/calendar function • Interrupt: periodic, alarm, update ended • BCD/binary accommodated • Leap year automatic correcting function • 24-hout/12-hour selectable • Daylight saving time mode accommodated
A/D Converter	• 10-bit charge re-distribution mode (error: ±4LSB) • Number of channels: 8-channel
IrDA Interface	• IrDA 1.0 SIR (–115.2 Kb/s, half-duplex) • IrDA 1.1 MIR (0.576, 1.152 Mb/s, half-duplex) • IrDA 1.1 FIR (4.0 Mbp/s, half-duplex) • UART (–1.5 Mbp/s, full-duplex) • 48 MHz clock input (baud rate generating function contained)
I^2C Interface	2 ports Master-slave interface (multi-master supported) 3.3 V interface (open drain output)

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	I_{DD18A}	VDD18 = 1.8 V ; VDD33, PVDD, AVDD, RVDD = 3.3 V fOSC = 33.33 MHz (core 133 MHz) ; FRQS[1:0] = 0.0 ; Output open	–	–	460	mA
Supply current at stopping	I_{DD18D}	VDD18 = 1.89 V ; VDD33, PVDD, AVDD, RVDD = 3.465 V fOSC = Stop ; FRQS[1:0] = 0.0 ; Output open ; Tj = 70°C	–	–	50	mA

(Ta = –20°C to +70°C)

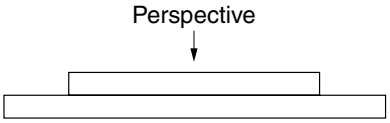
A/D conversion performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution			–	–	10	Bit
A/D conversion relative error		VREFH = 3.3 V Conversion reference clock = 4.166 MHz	–	–	±4	LSB
A/D conversion differential non-linear error			–	–	±4	LSB
A/D conversion time			2.6	–	–	µs

(Ta = –20°C to +70°C, AVDD = 3.3 V ± 0.165 V, AVSS = 0 V)

See the next page for pin assignment and support tool.

Pin Assignment



A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	
ND		XSWE1	XSCS6	XSCS2	XSCS1	SD29	SD27	VDD18	SD21	SD19	SD14	VDD18	SD6	SD1	CLK48	PIO1[3]	PIO1[1]	PIO1[0]	ND		21
		XSWE3	SD31	XSCS7	SD30	XSAS	SD23	SD22	SD17	SD16	SD9	SD8	SD3	SD4	PIO5[1]	PIO5[2]	PIO1[4]	PIO1[2]			20
RCLKI	XSCS3	XSWE0	XSWE2	XSCS0	XSCS4	SD28	SD25	SD24	SD18	VDD33	SD15	SD11	SD10	VDD33	PIO0[7]	PIO5[0]	AN1	AN3	AN7	VREFH	19
RCLKO	PIO2[0]	PWROK	ND	ND	ND	SD26	SD20	SD13	SD12	SD7	SD2	SD0	SD5	PIO0[1]	ND	ND	ND	AN5	PIO0[5]	AVSS	18
RVDD	PIO2[4]	PIO2[2]	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	AN6	AN0	AN2	17
TCPOUT	PIO2[3]	XSDK	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	PIO0[3]	XIRQ7	AN4	16
PVDD	SSZ0	XSBG	VDD33	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	XIRQ4	SBT2	PIO0[4]	AVDD	15
PVSS	SA4	SA2	XSCS5	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	SBO0	XIRQ5	XNMI	XIRQ2	14
OSCI	SA10	SA5	VDD33	ND	ND	ND	ND	VSS	VSS	VSS	VSS	VSS	ND	ND	ND	ND	SBO1	XIRQ0	PIO0[6]	PIO0[2]	13
OSCO	SA17	SA11	SA0	ND	ND	ND	ND	VSS	VSS	VSS	VSS	VSS	ND	ND	ND	ND	VDD33	XRESET	PIO0[0]	XIRQ6	12
SYSCLK	SA18	SA12	XSRE	ND	ND	ND	ND	VSS	VSS	VSS	VSS	VSS	ND	ND	ND	ND	TRCST	VDD33	XIRQ3	VDD18	11
PIO2[1]	SRXW	SSZ1	VDD33	ND	ND	ND	ND	VSS	VSS	VSS	VSS	VSS	ND	ND	ND	ND	SBI1	SBI2	SBO2	XIRQ1	10
XSBR	SA1	SA3	SA14	ND	ND	ND	ND	VSS	VSS	VSS	VSS	VSS	ND	ND	ND	ND	PIO3[2]	PIO3[3]	XRSTOUT	VDD18	09
VDD18	SA6	SA7	SA8	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	PIO3[0]	PIO3[1]	SBT0	SBT1	08
SA9	SA13	SA15	SA22	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	TRST MOD	PIO4[0]	PIO4[2]	SBI0	07
SA16	SA19	SA21	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	PIO4[1]	PIO3[4]	TCK	06
VDD18	SA23	VDD33	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND	TRCD1	PIO4[3]	TDI	05
SA27	SA26	SA24	ND	ND	ND	VDD33	VDD18	VDD33	VDD33	VDD33	VDD33	VDD18	TRCD2	TRCD7	ND	ND	ND	TRCD5	TMS	TDO	04
SA29	SA31	SA25	SA20	SA28	MA4	MA1	MA7	MA13	MA11	MA12	XMBE0	MD9	MD4	MD12	MD1	MD15	TRCD4	TRCD0	EXTRG	TRCCLK	03
ND		SA30	MA3	MA5	MA0	MA8	MA14	XMCS1	SDCKE	XMWE	XMCAS	MD6	MD10	MD11	MD2	MD14	TRCD3	TRCD6	ND		02
		NP	MA2	MA6	MA10	MA9	XMCS0	XMRAS	SDCLK	XMBE1	MDK	MD7	MD8	MD5	SDCKI	MD3	MD13	MD0			01

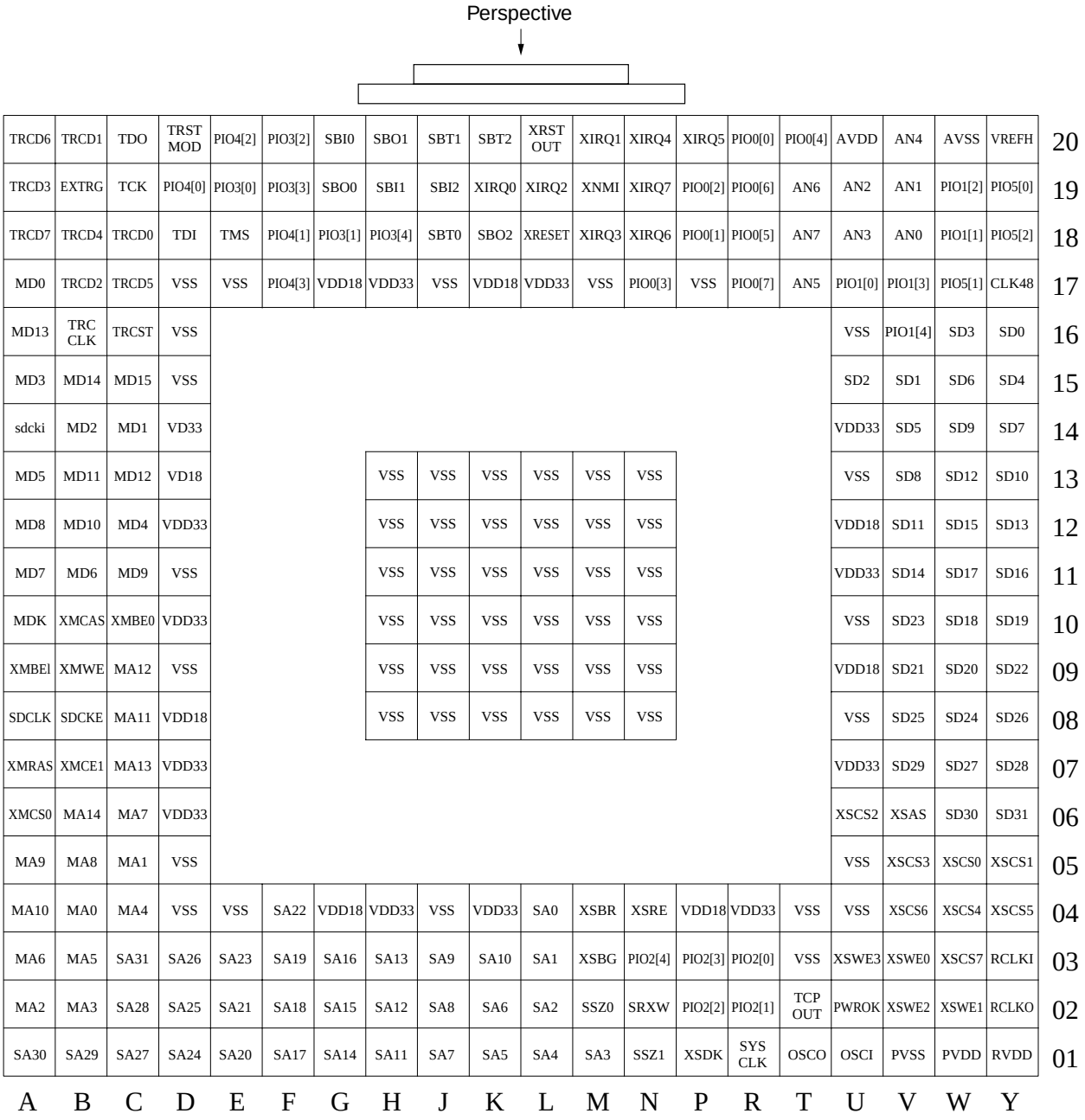
FLGA424-C-1717 *Lead-free

* ND has an electrode (pin) but N.C. is not guaranteed. Please design so as not to cause short circuit with other wiring on the user board.

* The NDs on the four corners are the lands intended for reinforcement. You are required to connect them to the PCB.

* NP (No pin.) has no electrode.

Pin Assignment(Continue)



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
20	TRCD6	TRCD1	TDO	TRST MOD	PIO4[2]	PIO3[2]	SBI0	SBO1	SBT1	SBT2	XRST OUT	XIRQ1	XIRQ4	XIRQ5	PIO0[0]	PIO0[4]	AVDD	AN4	AVSS	VREFH	20
19	TRCD3	EXTRG	TCK	PIO4[0]	PIO3[0]	PIO3[3]	SBO0	SBI1	SBI2	XIRQ0	XIRQ2	XNMI	XIRQ7	PIO0[2]	PIO0[6]	AN6	AN2	AN1	PIO1[2]	PIO5[0]	19
18	TRCD7	TRCD4	TRCD0	TDI	TMS	PIO4[1]	PIO3[1]	PIO3[4]	SBT0	SBO2	XRESET	XIRQ3	XIRQ6	PIO0[1]	PIO0[5]	AN7	AN3	AN0	PIO1[1]	PIO5[2]	18
17	MD0	TRCD2	TRCD5	VSS	VSS	PIO4[3]	VDD18	VDD33	VSS	VDD18	VDD33	VSS	PIO0[3]	VSS	PIO0[7]	AN5	PIO1[0]	PIO1[3]	PIO5[1]	CLK48	17
16	MD13	TRC CLK	TRCST	VSS													VSS	PIO1[4]	SD3	SD0	16
15	MD3	MD14	MD15	VSS													SD2	SD1	SD6	SD4	15
14	sdcki	MD2	MD1	VD33													VDD33	SD5	SD9	SD7	14
13	MD5	MD11	MD12	VD18				VSS	VSS	VSS	VSS	VSS	VSS				VSS	SD8	SD12	SD10	13
12	MD8	MD10	MD4	VDD33				VSS	VSS	VSS	VSS	VSS	VSS				VDD18	SD11	SD15	SD13	12
11	MD7	MD6	MD9	VSS				VSS	VSS	VSS	VSS	VSS	VSS				VDD33	SD14	SD17	SD16	11
10	MDK	XMCAS	XMBE0	VDD33				VSS	VSS	VSS	VSS	VSS	VSS				VSS	SD23	SD18	SD19	10
09	XMBEl	XMWE	MA12	VSS				VSS	VSS	VSS	VSS	VSS	VSS				VDD18	SD21	SD20	SD22	09
08	SDCLK	SDCKE	MA11	VDD18				VSS	VSS	VSS	VSS	VSS	VSS				VSS	SD25	SD24	SD26	08
07	XMRAS	XMCE1	MA13	VDD33													VDD33	SD29	SD27	SD28	07
06	XMCS0	MA14	MA7	VDD33													XSCS2	XSAS	SD30	SD31	06
05	MA9	MA8	MA1	VSS													VSS	XSCS3	XSCS0	XSCS1	05
04	MA10	MA0	MA4	VSS	VSS	SA22	VDD18	VDD33	VSS	VDD33	SA0	XSBR	XSRE	VDD18	VDD33	VSS	VSS	XSCS6	XSCS4	XSCS5	04
03	MA6	MA5	SA31	SA26	SA23	SA19	SA16	SA13	SA9	SA10	SA1	XSBG	PIO2[4]	PIO2[3]	PIO2[0]	VSS	XSWE3	XSWE0	XSCS7	RCLKI	03
02	MA2	MA3	SA28	SA25	SA21	SA18	SA15	SA12	SA8	SA6	SA2	SSZ0	SRXW	PIO2[2]	PIO2[1]	TCP OUT	PWROK	XSWE2	XSWE1	RCLKO	02
01	SA30	SA29	SA27	SA24	SA20	SA17	SA14	SA11	SA7	SA5	SA4	SA3	SSZ1	XSDK	SYS CLK	OSCO	OSCI	PVSS	PVDD	RVDD	01

BGA292-P-2727 *Lead-free

Support Tool

ROM Emulator	PARTNER-ETⅡ (KMC product)
On-board Development Tools	PX-ODB103E-J (On-board debug unit) PX-ODB-AMT-20 (Trace unit) PARTNER-J (KMC product)

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