The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

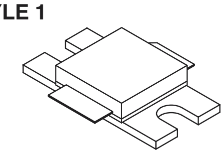
MRF18030AR3
MRF18030ASR3

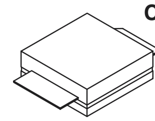
Designed for GSM and EDGE base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. Specified for GSM 1805 – 1880 MHz.

- Typical GSM Performance:
  Power Gain – 14 dB (Typ) @ 30 Watts
  Efficiency – 50% (Typ) @ 30 Watts
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 30 W Output Power
- Excellent Thermal Stability
- Available in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.

GSM/GSM EDGE 1.8 – 1.88 GHz, 30 W, 26 V LATERAL N–CHANNEL RF POWER MOSFETs

CASE 465E–03, STYLE 1
NI–400
MRF18030AR3





CASE 465F–03, STYLE 1
NI–400S
MRF18030ASR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	83.3 0.48	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	°C/W

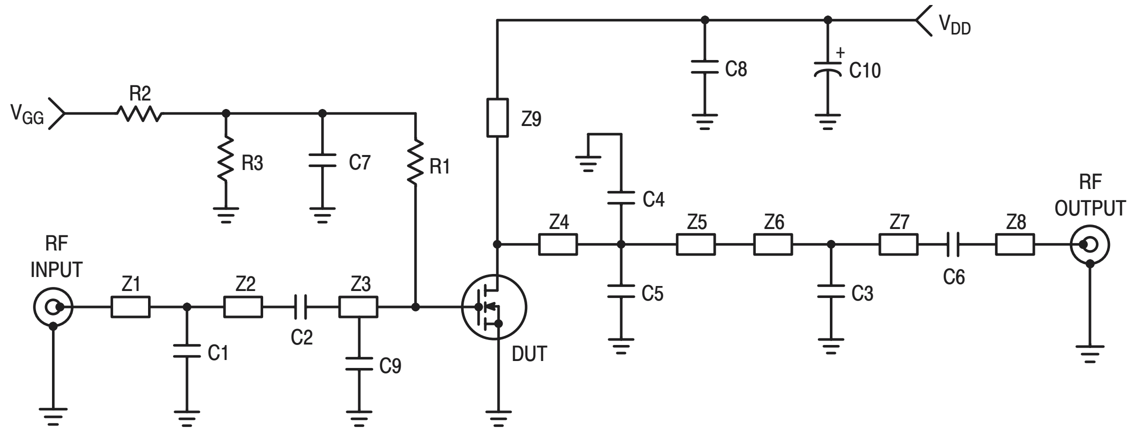
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 3

ELECTRICAL CHARACTERISTICS (T_C = 25°C, 50 ohm system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 20 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 250 mAdc)	$V_{GS(Q)}$	2	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.29	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1 Adc)	g_{fs}	—	2	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.3	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture) (2)					
Output Power, 1 dB Compression Point (V_{DD} = 26 Vdc, I_{DQ} = 250 mA, f = 1805 – 1880 MHz)	P1dB	27	30	—	Watts
Common–Source Amplifier Power Gain @ 30 W (V_{DD} = 26 Vdc, I_{DQ} = 250 mA, f = 1805 – 1880 MHz)	G_{ps}	13	14	—	dB
Drain Efficiency @ 30 W (V_{DD} = 26 Vdc, I_{DQ} = 250 mA, f = 1805 – 1880 MHz)	η	46.5	50	—	%
Input Return Loss @ 30 W (V_{DD} = 26 Vdc, I_{DQ} = 250 mA, f = 1805 – 1880 MHz)	IRL	—	–12	–9	dB
Output Mismatch Stress @ 30 W (V_{DD} = 26 Vdc, I_{DQ} = 250 mA, f1 = 1805 – 1880 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.
(2) Device specifications obtained on a Production Test Fixture.



C1	1.8 pF, 100B Chip Capacitor	Z1	0.874″ x 0.087″ Microstrip
C2	0.8 pF, 100B Chip Capacitor	Z2	1.094″ x 0.087″ Microstrip
C3	1.0 pF, 100B Chip Capacitor	Z3	0.257″ x 0.633″ Microstrip
C4, C5	1.2 pF, 100B Chip Capacitors	Z4	0.189″ x 0.394″ Microstrip
C6, C7, C8	8.2 pF, 100B Chip Capacitors	Z5	0.335″ x 0.394″ Microstrip
C9	0.3 pF, 100B Chip Capacitor	Z6	0.484″ x 0.087″ Microstrip
C10	220 μF, 63 V Electrolytic Capacitor	Z7	0.877″ x 0.087″ Microstrip
R1	1.0 kΩ, 1/8 W Chip Resistor (0805)	Z8	0.366″ x 0.087″ Microstrip
R2, R3	10 kΩ, 1/8 W Chip Resistors (0805)	Z9	≈0.600″ x 0.087″ Microstrip

Figure 1. 1805 – 1880 MHz Test Fixture Schematic

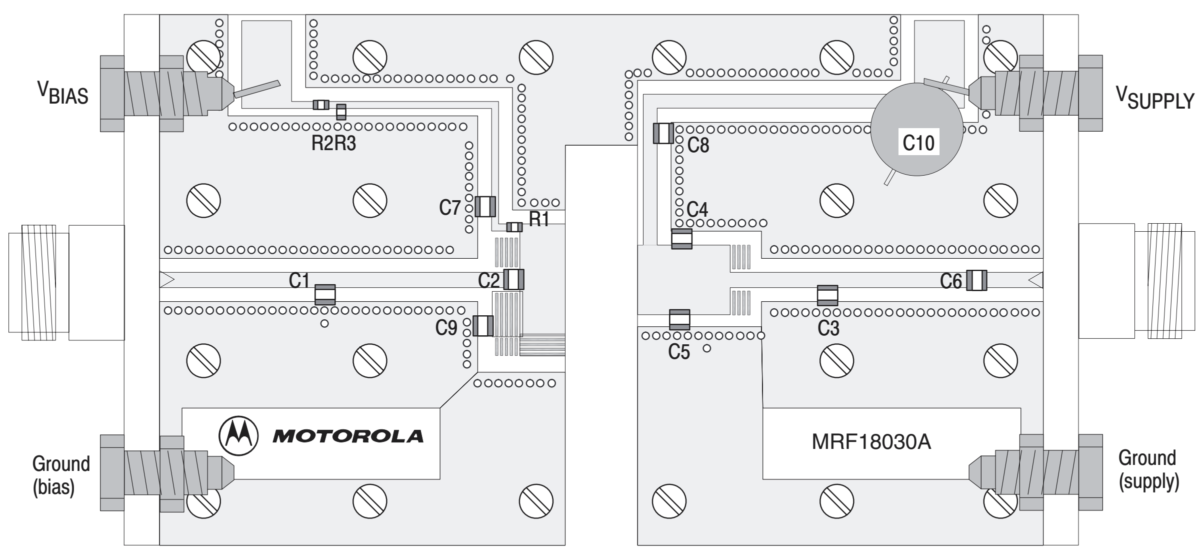


Figure 2. 1805 – 1880 MHz Test Fixture Component Layout

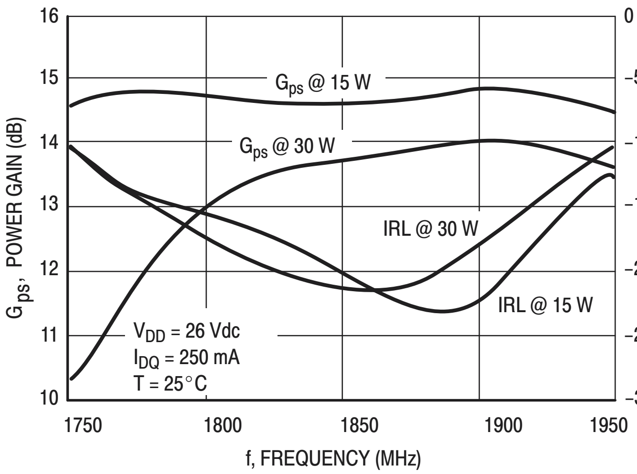


Figure 3. Wideband Gain and IRL at 30 W and 15 W Output Power

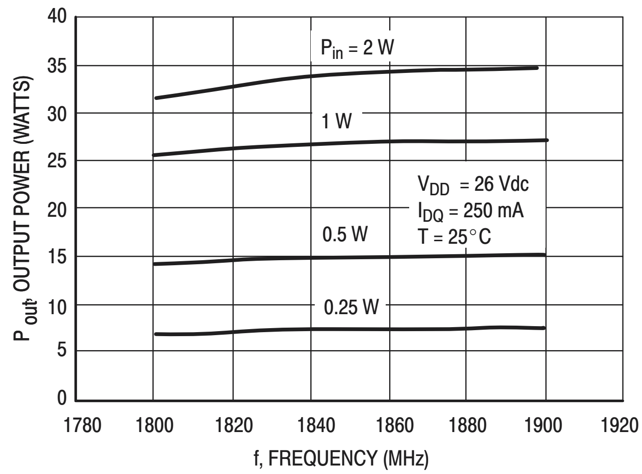


Figure 4. Output Power versus Frequency

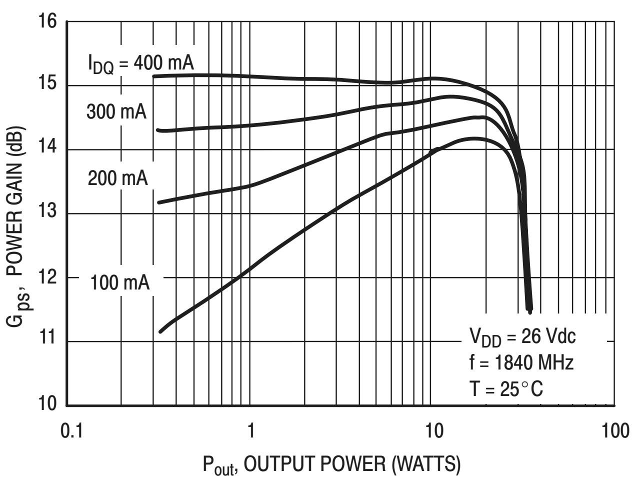


Figure 5. Power Gain versus Output Power

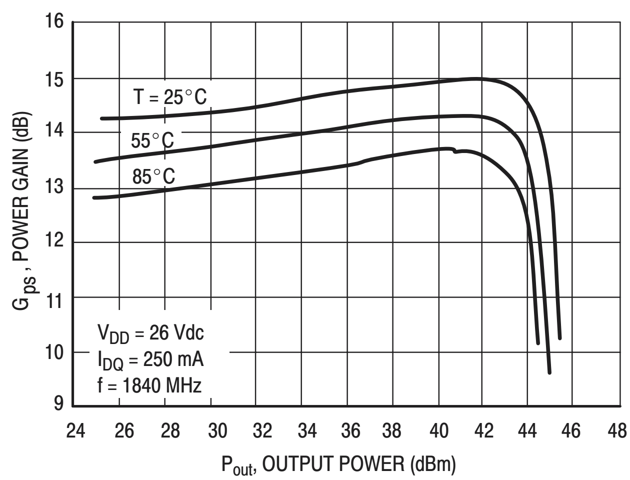


Figure 6. Power Gain versus Output Power

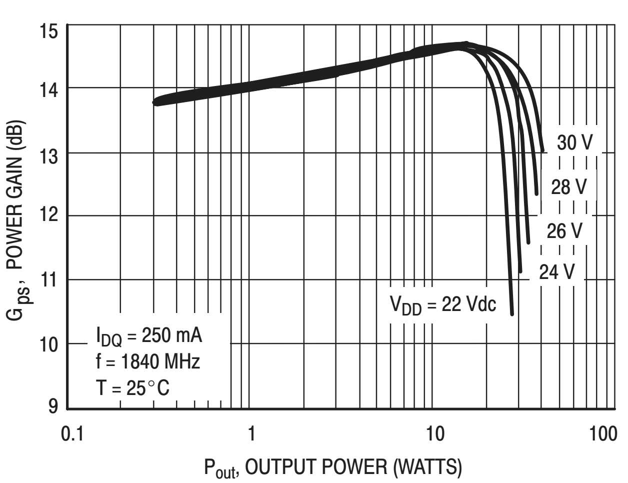


Figure 7. Power Gain versus Output Power

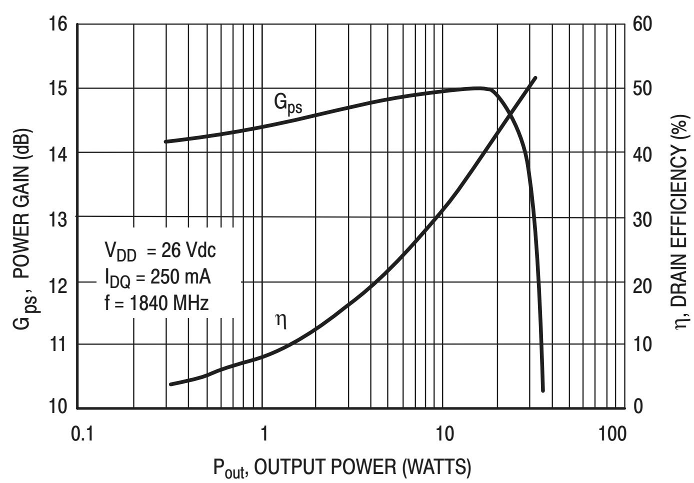
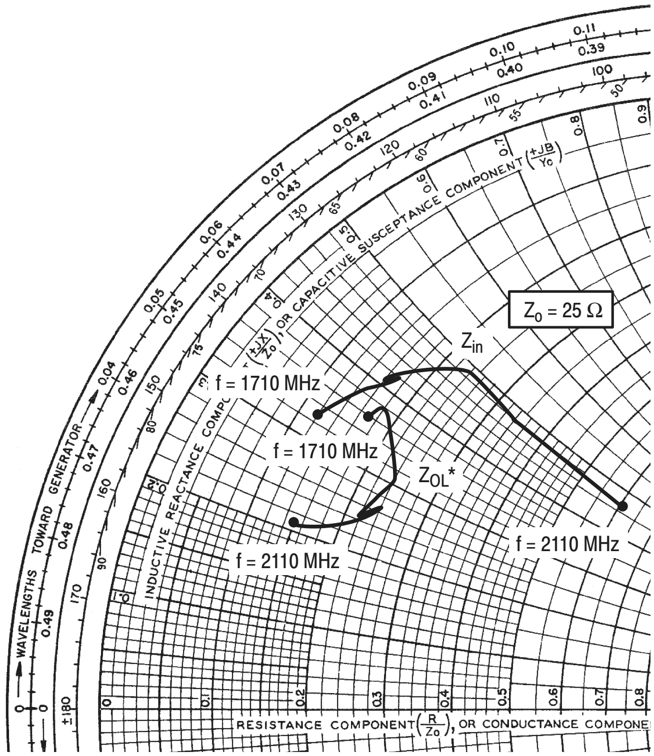


Figure 8. Power Gain and Efficiency versus Output Power



V_{DD} = 26 V, I_{DQ} = 250 mA, P_{out} = 30 W (CW)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1710	2.92 + j8.24	4.18 + j9.06
1785	3.84 + j9.75	4.59 + j9.46
1805	4.15 + j10.38	4.98 + j9.06
1840	4.04 + j10.22	6.10 + j7.63
1880	6.12 + j12.29	5.83 + j6.89
1960	6.20 + j12.29	5.55 + j6.33
1990	8.61 + j12.10	5.93 + j6.66
2110	15.19 + j11.85	3.82 + j5.33

Z_{in} = Complex conjugate of the source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given power, voltage, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, and drain efficiency.

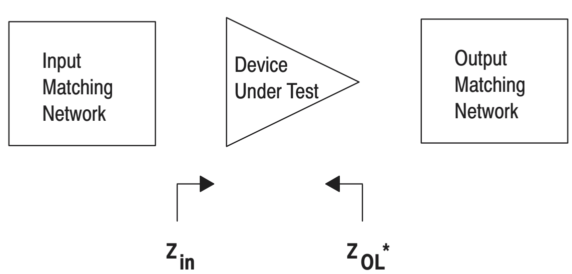
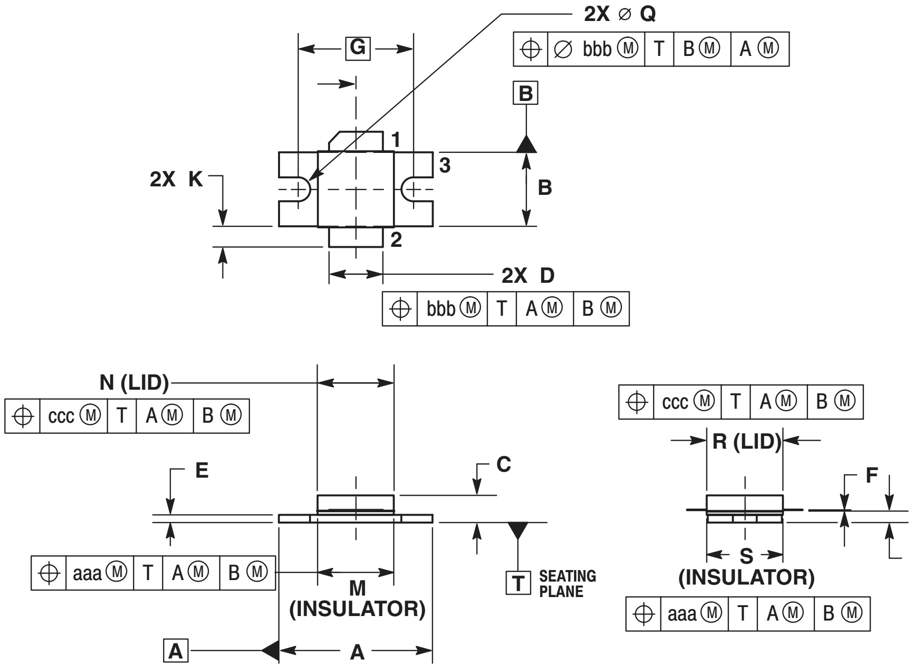


Figure 9. Series Equivalent Input and Output Impedance

NOTES

PACKAGE DIMENSIONS

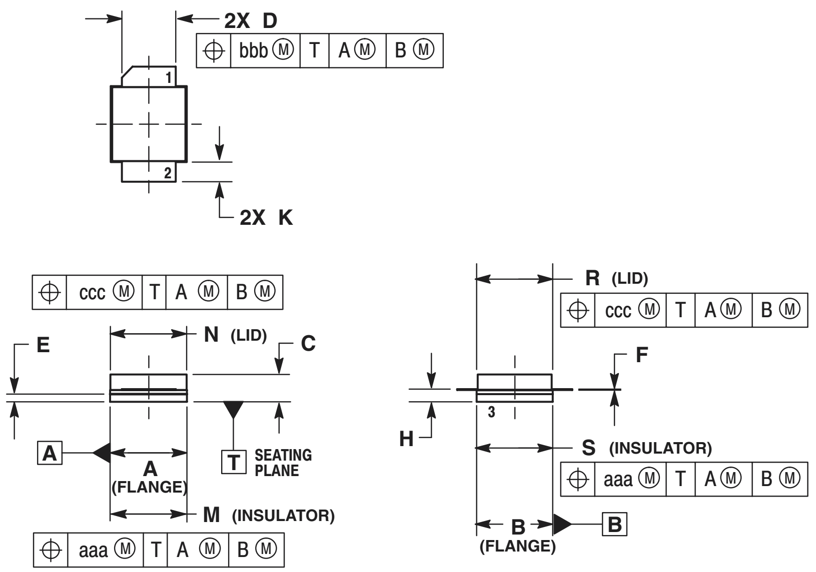


NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.795	.805	20.19	20.44
B	.380	.390	9.65	9.9
C	.125	.163	3.17	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.003	.006	0.07	0.15
G	.600 BSC		15.24 BSC	
H	.057	.067	1.45	1.7
K	.092	.122	2.33	3.1
M	.395	.405	10	10.3
N	.395	.405	10	10.3
Q	⌀ .110	⌀ .130	⌀ 2.79	⌀ 3.3
R	.395	.405	10	10.3
S	.395	.405	10	10.3
aaa	.005 BSC		0.127 BSC	
bbb	.010 BSC		0.254 BSC	
ccc	.015 BSC		0.381 BSC	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465E–03
ISSUE D
NI–400
MRF18030AR3



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	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.395	.405	10.03	10.29
B	.395	.405	10.03	10.29
C	.125	.163	3.18	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.003	.006	0.08	0.15
H	.057	.067	1.45	1.70
K	.092	.122	2.34	3.10
M	.395	.405	10.03	10.29
N	.395	.405	10.03	10.29
R	.395	.405	10.03	10.29
S	.395	.405	10.03	10.29
aaa	.005 REF		0.127 REF	
bbb	.010 REF		0.254 REF	
ccc	.015 REF		0.38 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465F–03
ISSUE B
NI–400S
MRF18030ASR3

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